700-449

NO. 1/1A ESS

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Western Electric

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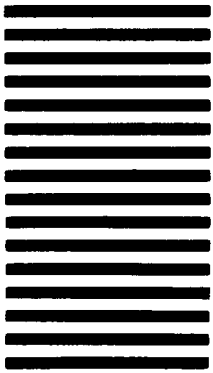

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Section 1

CENTRAL PULSE DISTRIBUTOR (CPD) (J1A034B)

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Support Documentation

SD-1A109
CD-1A109
PK-1A023 CPD Raw Data Document
TLM-1A109
ED-1A186-11
SD-1A119 Communications BUS CKT
SD-1A129 Miscellaneous CKT
PK-1A048 Peripheral Unit Bus Raw Data Document
TLM-1A119 Peripheral Unit Bus
BSP 820-230-150
TOP 231-051-001

OCTAL ORDER LAYOUT - CENTRAL PULSE DISTRIBUTOR

22 20	19 17	16 14	13 11	10	9 0
GROUP	ROW	COLUMN		HALF	

RELATED INPUT MESSAGES

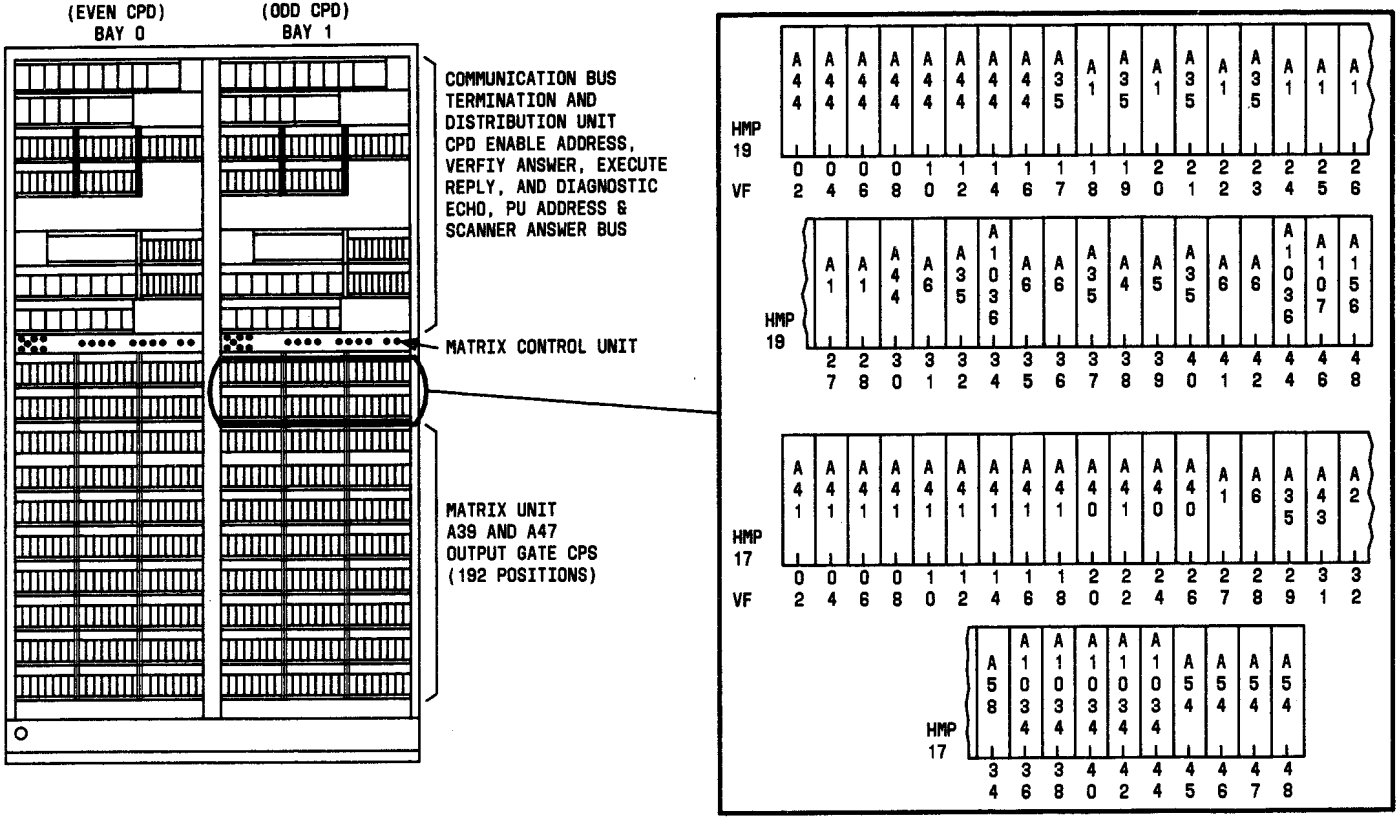
CPD-DGN- a bb.

REQUESTS DIAGNOSIS ON CENTRAL PULSE DISTRIBUTOR (CPD)

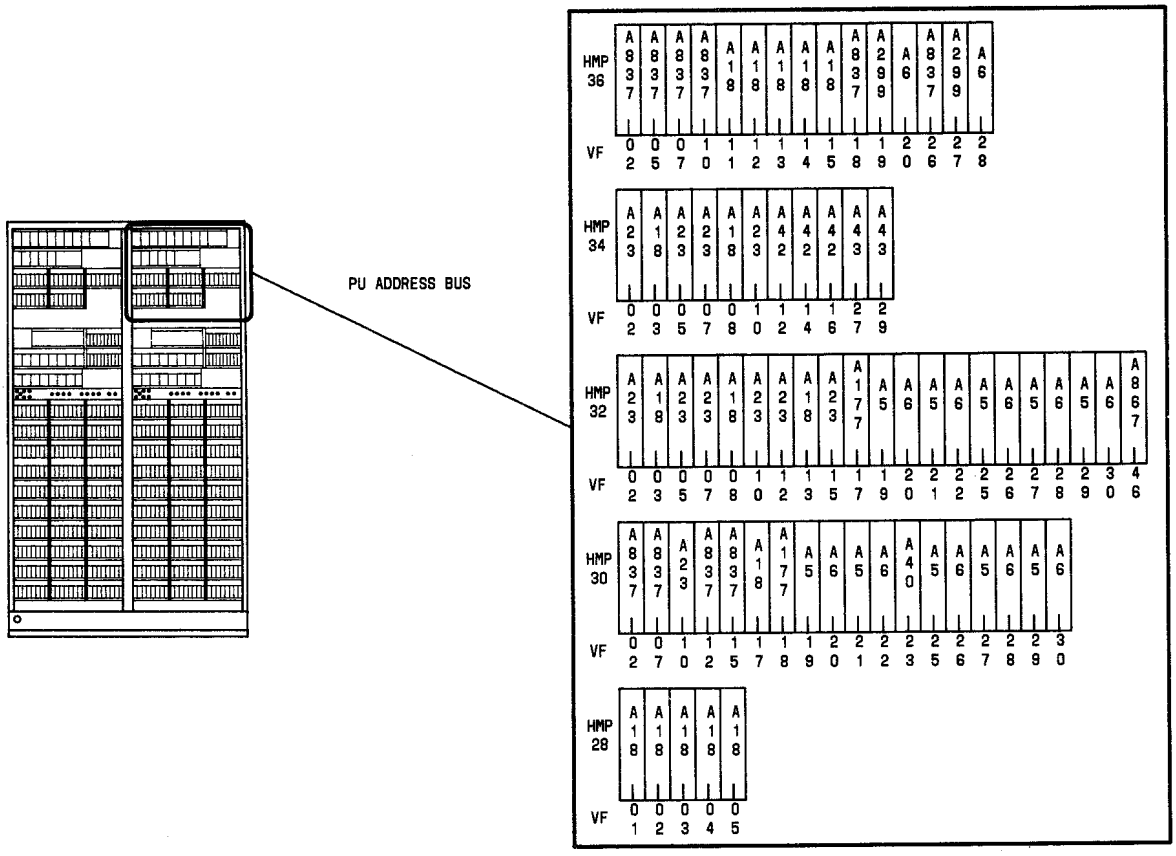
T-CPD- a bb c d e f g.

REQUESTS A PULSE OF A CPD POINT

REFERENCE: IM-6A001-01

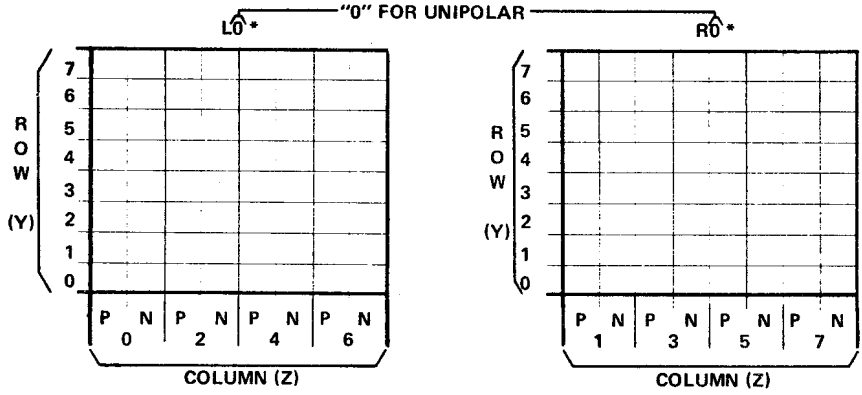


LOCATION AND TYPE OF CIRCUIT PACKS IN CPD FRAME – J1A034



LOCATION AND TYPE OF PUAB CIRCUIT PACKS IN CPD FRAME (NO. 1A ESS)

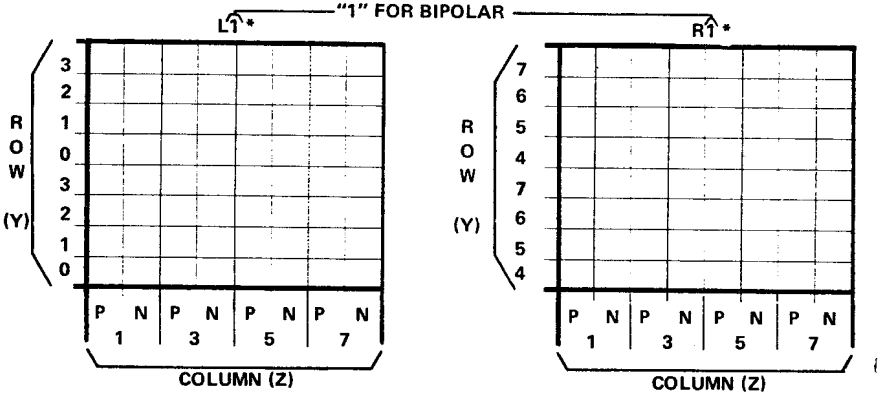
LOCATING UNIPOLAR CPD POINTS



EVEN COLUMN NUMBER–LEFT T. S.

ODD COLUMN NUMBER–RIGHT T. S.

LOCATING BIPOLAR CPD POINTS



ROWS 0 TO 3–LEFT T. S.

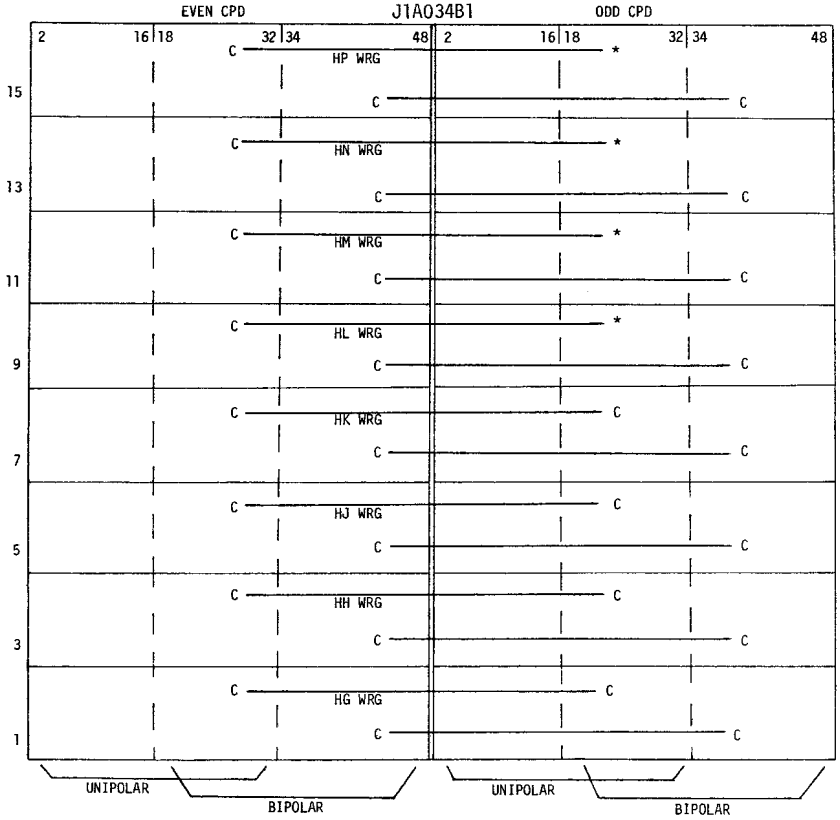
ROWS 4 TO 7– RIGHT T. S.

* THE LAST DIGIT OF THE T. S. NUMBER IS THE GROUP (X) NUMBER.

UNIPOLAR AND BIPOLAR CPD OPTIONS

SEVERAL SERVICE INTERRUPTIONS HAVE BEEN CAUSED WHEN CHANGING THE TYPES OF ASSIGNMENTS ON CPD FRAMES. THE ATTACHED SKETCH AND ASSOCIATED NOTES SHOULD HELP CLARIFY ENGINEERING NOTES 57A THRU 57D, MANUFACTURING NOTES 5 & 14, AND TABLE C ON J1A034B-1.

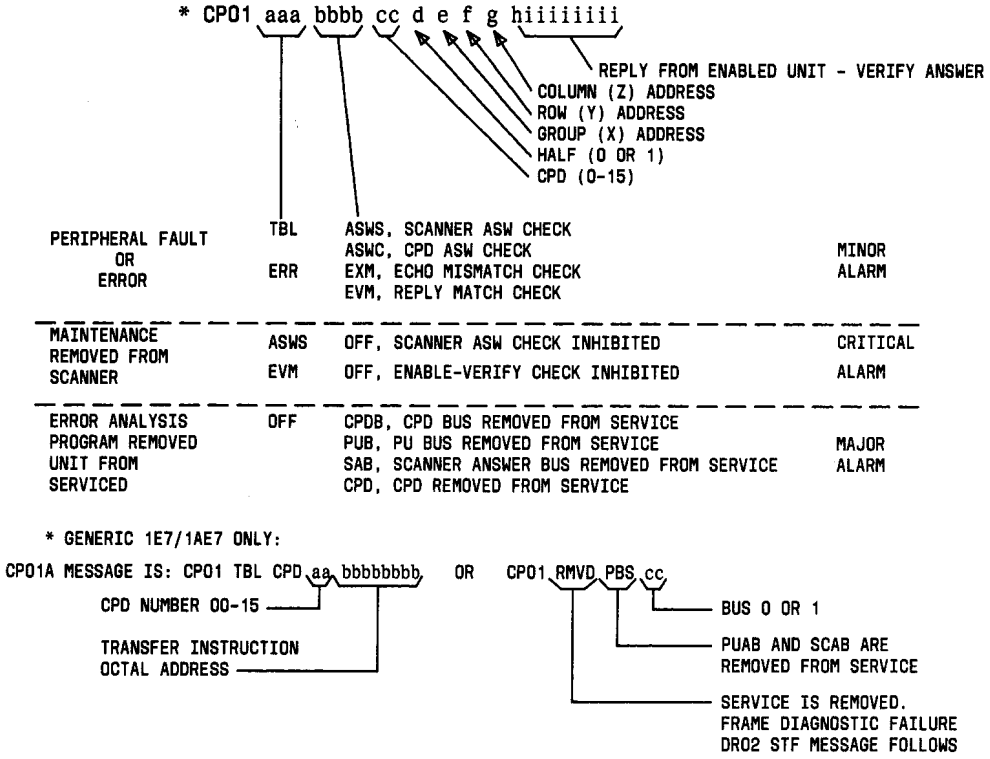
PARTICULAR ATTENTION SHOULD BE PAID TO NOTE 7 ON THE ATTACHED SKETCH. THE BULK OF THE SERVICE INTERRUPTIONS HAVE BEEN CAUSED BY INSERTING PACKS (BIPOLAR-UNIPOLAR) IN PACK POSITIONS 2-32 OF THE EVEN OR ODD CPD WHICH ARE NOT COMPATIBLE WITH THE WIRING (HG-HP) ON THE ASSOCIATED MOUNTING PLATE.



1. C - CONNECTED BY SHOP
2. * - NOT CONNECTED BY SHOP

} BIPOLAR MULTIPLE FURNISHED PER L-D (J1A034B-1)

3. HG THRU HP WRG (LOCAL CABLES) FURNISHED SEPARATELY ON OLDER FRS PER L-A.
4. CKT PACK POSITIONS 34-48 CAN ONLY BE BIPOLAR (L-2).
5. A GIVEN MTG PLATE MUST BE ALL UNIPOLAR IN CKT PACK POSITIONS 2-32 OR ALL BIPOLAR IN CKT PACK POSITIONS 18-32 (2-16 VACANT).
6. HG-HP WRG (LOCAL CABLES) SHOULD NOT BE REMOVED. THEY SHOULD ONLY BE CONNECTED (BIPOLAR) OR DISCONNECTED (UNIPOLAR) IN THE ODD CPD.
7. HG-HP WRG SHOULD BE CONNECTED OR DISCONNECTED BEFORE ASSIGNMENTS ARE WIRED AND WITH NO CKT PACKS INSERTED ON THE ASSOCIATED MTG PLATE (CKT PACK POSITIONS 2-32 MUST BE VACANT). DO NOT REMOVE PACKS FROM POS 34-48.



CP01/CP01A FAILURE MESSAGE WITH DATA FIELDS IDENTIFIED

Failing circuit pack(s), CPs, relate to raw data as follows:

- Last failing words
- Common circuit function
- Error pattern may have numerous failures in previous words

FAILURE PATTERN SENSITIVITY

* FAILURE/CHARACTERISTICS	POSSIBLE CAUSE OF FAILURE
Multiple test phases failed: Phase 1 and 2 - STF	CPD circuits failure: • Decoder X and Y address • Parity detection for group (X), row (X) and column (Z) enable address • Output gate matrix current excessive • Z-register parity checks • Control and decoder gates or timing
Single test phase • Phase 1 - STF (bus 0) • Phase 2 - STF (bus 1)	Cable driver/receiver or gate in CC to CPD bus system failed: • Enable address • Verify answer • CPD execute • CPD execute reply • CPD diagnostic echo
* Single test phase failure may result in F-level interrupt	

CPD DIAGNOSTIC TEST EVALUATION

FAILURE PATTERNS – MULTIPLE WORDS IN PHASES 1 OR 2

PHASE 1 OR 2-WORD	CIRCUIT PACK LOCATION (TYPE)		FUNCTION OR OPERATION
	BUS 0	BUS 1	
1-8	28-29(A18) 28-30(A18) 26-32(A21) 26-30(A299) 26-48(A18)	28-17(A18) 28-18(A18) 26-32(A21) 26-30(A299) 26-48(A18)	0 & 1 ASWCPD reported by CPD control and maintenance inputs and outputs; enable address EA0-7 to X-register or enable address EA8-15 to Y-register
9 & 10	28-31(A18) 28-32(A18) 26-32(A21) 26-30(A299) 26-48(A18)	28-19(A18) 28-20(A18) 26-32(A21) 26-30(A299) 26-48(A18)	0 & 1 ASWCPD, parity checks – PCA, PCB or PCC from CPD control
11-18	26-32(A21) 26-30(A299)	26-32(A21) 26-30(A299)	0 & 1 Matrix current and ASWCPD checks from CPD control
19 & 20	28-31(A21) 28-32(A18)	28-19(A21) 28-32(A18)	0 & 1 Matrix current and Z-register parity checks from CPD control
21-25	26-01(A299) 26-09(A21) 26-04(A299) 26-05(A21) 26-07(A299) 26-03(A21)	26-26(A299) 28-28(A21) 26-27(A299) 28-26(A21) 26-28(A299) 28-24(A21)	0 & 1 Verify answer checks from encoder

DECODER X- AND Y-REGISTER ADDRESSING OR ASWCPD FAIURES

WORD *	BIT *	CP LOCATION A40	CP LOCATION A41	CP LOCATION A40	GROUP X	GROUP EA	ROW Y	ROW EA
1	8	17-02	17-18	17-24	0	0	0	8
	9	17-04	17-18	17-24	1	1	0	8
	10	17-06	17-18	17-24	2	2	0	8
	11	17-08	17-18	17-24	3	3	0	8
	12	17-10	17-18	17-26	4	4	0	8
	13	17-12	17-18	17-26	5	5	0	8
	14	17-14	17-18	17-26	6	6	0	8
	15	17-16	17-18	17-26	7	7	0	8
2	8	17-02	17-18	17-24	0	0	1	9
	9	17-04	17-18	17-24	1	1	1	9
	10	17-06	17-18	17-24	2	2	1	9
	11	17-08	17-18	17-24	3	3	1	9
	12	17-10	17-18	17-26	4	4	1	9
	13	17-12	17-18	17-26	5	5	1	9
	14	17-14	17-18	17-26	6	6	1	9
	15	17-16	17-18	17-26	7	7	1	9
3	8	17-02	17-18	17-24	0	0	2	10
	9	17-04	17-18	17-24	1	1	2	10
	10	17-06	17-18	17-24	2	2	2	10
	11	17-08	17-18	17-24	3	3	2	10
	12	17-10	17-18	17-26	4	4	2	10
	13	17-12	17-18	17-26	5	5	2	10
	14	17-14	17-18	17-26	6	6	2	10
	15	17-16	17-18	17-26	7	7	2	10
4	8	17-02	17-18	17-24	0	0	3	11
	9	17-04	17-18	17-24	1	1	3	11
	10	17-06	17-18	17-24	2	2	3	11
	11	17-08	17-18	17-24	3	3	3	11
	12	17-10	17-18	17-26	4	4	3	11
	13	17-12	17-18	17-26	5	5	3	11
	14	17-14	17-18	17-26	6	6	3	11
	15	17-16	17-18	17-26	7	7	3	11
5	8	17-02	17-20	17-24	0	0	4	12
	9	17-04	17-20	17-24	1	1	4	12
	10	17-06	17-20	17-24	2	2	4	12
	11	17-08	17-20	17-24	3	3	4	12
	12	17-10	17-20	17-26	4	4	4	12
	13	17-12	17-20	17-26	5	5	4	12
	14	17-14	17-20	17-26	6	6	4	12
	15	17-16	17-20	17-26	7	7	4	12
6	8	17-02	17-20	17-24	0	0	5	13
	9	17-04	17-20	17-24	1	1	5	13
	10	17-06	17-20	17-24	2	2	5	13
	11	17-08	17-20	17-24	3	3	5	13
	12	17-10	17-20	17-26	4	4	5	13
	13	17-12	17-20	17-26	5	5	5	13
	14	17-14	17-20	17-26	6	6	5	13
	15	17-16	17-20	17-26	7	7	5	13
7	8	17-02	17-20	17-24	0	0	6	14
	9	17-04	17-20	17-24	1	1	6	14
	10	17-06	17-20	17-24	2	2	6	14
	11	17-08	17-20	17-24	3	3	6	14
	12	17-10	17-20	17-26	4	4	6	14
	13	17-12	17-20	17-26	5	5	6	14
	14	17-14	17-20	17-26	6	6	6	14
	15	17-16	17-20	17-26	7	7	6	14
8	8	17-02	17-20	17-24	0	0	7	15
	9	17-04	17-20	17-24	1	1	7	15
	10	17-06	17-20	17-24	2	2	7	15
	11	17-08	17-20	17-24	3	3	7	15
	12	17-10	17-20	17-26	4	4	7	15
	13	17-12	17-20	17-26	5	5	7	15
	14	17-14	17-20	17-26	6	6	7	15
	15	17-16	17-20	17-26	7	7	7	15

* Failures in multiple words and bits indicate faulty 17-22(A41) or 17-27(A1) CP

ASWCPD, EXM, MCE, PCA, PCB OR PCC FAILURES

WORD & BIT	CP LOCATION (TYPE)	FUNCTION
9 or 10, Bit 16	17-31(A43), 17-28(A6), 19-45(A107), 19-44(A1035), and 19-42(A6)	ASWCPD – All seems well CPD
9 or 10, Bit 17	19-44(A43), 19-49(A156), 19-42(A6), and 17-28(A6)	MCE – Matrix current excessive
9 or 10, Bit 18	19-35(A6), 19-36(A6), 19-38(A4), 19-39(A5), 17-24(A40), 17-26(A40), and 17-27(A1)	PCA – Parity check X-register
9 or 10, Bit 19	19-35(A6), 19-36(A6), 19-38(A4), 19-39(A5), 17-18(A40), 17-20(A40), and 17-27'A1)	PCB – Parity check Y-register
9 or 10, Bit 20	19-48(A156), 19-44(A1036), 19-36(A6), 19-38(A4), 19-39(A5), 26-24(A40), 26-22(A40), 26-20(A40), 26-18(A40), and 17-44(A40)	PCC – Parity check Z-register
9 or 10, Bit 21	19-46(A107), 19-44(A1036), 19-41(A6), and 19-38(A4)	EXM – Execute pulse complemented

TABLE D — OUTPUT GATING — MCE AND ASWCPD FAILURES

WORD	BIT	CP LOCATION		GROUP		ROW		FAILURE		WORD	BIT	CP LOCATION		GROUP		ROW		FAILURE	
		A39	A47	X	EA	Y	EA	MCE	ASWCPD			A39	A47	X	EA	Y	EA	MCE	ASWCPD
11	0	15-34	15-02,15-18	0	0	0	8		x	13	0	15-38	15-06,15-22	0	0	2	10		x
	1	15-34	15-02,15-18	0	0	0	8	x			1	15-38	15-06,15-22	0	0	2	10	x	
	2	13-34	13-02,13-18	1	1	0	8		x		2	13-38	13-06,13-22	1	1	2	10		x
	3	13-34	13-02,13-18	1	1	0	8	x			3	13-38	13-06,13-22	1	1	2	10	x	
	4	11-34	11-02,11-18	2	2	0	8		x		4	11-38	11-06,11-22	2	2	2	10		x
	5	11-34	11-02,11-18	2	2	0	8	x			5	11-38	11-06,11-22	2	2	2	10	x	
	6	09-34	09-02,09-18	3	3	0	8		x		6	09-38	09-06,09-22	3	3	2	10		x
	7	09-34	09-02,09-18	3	3	0	8	x			7	09-38	09-06,09-22	3	3	2	10	x	
	8	07-34	07-02,07-18	4	4	0	8		x		8	07-38	07-06,07-22	4	4	2	10		x
	9	07-34	07-02,07-18	4	4	0	8	x			9	07-38	07-06,07-22	4	4	2	10	x	
	10	05-34	05-02,05-18	5	5	0	8		x		10	05-38	05-06,05-22	5	5	2	10		x
	11	05-34	05-02,05-18	5	5	0	8	x			11	05-38	05-06,05-22	5	5	2	10	x	
	12	03-34	03-02,03-18	6	6	0	8		x		12	03-38	03-06,03-22	6	6	2	10		x
	13	03-34	03-02,03-18	6	6	0	8	x			13	03-38	03-06,03-22	6	6	2	10	x	
	14	01-34	01-02,01-18	7	7	0	8		x		14	01-38	01-06,01-22	7	7	2	10		x
	15	01-34	01-02,01-18	7	7	0	8	x			15	01-38	01-06,01-22	7	7	2	10	x	
12	0	15-36	15-04,15-20	0	0	1	9		x	14	0	15-40	15-08,15-24	0	0	3	11		x
	1	15-36	15-04,15-20	0	0	1	9	x			1	15-40	15-08,15-24	0	0	3	11	x	
	2	13-36	13-04,13-20	1	1	1	9		x		2	13-40	13-08,13-24	1	1	3	11		x
	3	13-36	13-04,13-20	1	1	1	9	x			3	13-40	13-08,13-24	1	1	3	11	x	
	4	11-36	11-04,11-20	2	2	1	9		x		4	11-40	11-08,11-24	2	2	3	11		x
	5	11-36	11-04,11-20	2	2	1	9	x			5	11-40	11-08,11-24	2	2	3	11	x	
	6	09-36	09-04,09-20	3	3	1	9		x		6	09-40	09-08,09-24	3	3	3	11		x
	7	09-36	09-04,09-20	3	3	1	9				7	09-40	09-08,09-24	3	3	3	11	x	
	8	07-36	07-04,07-20	4	4	1	9		x		8	07-40	07-08,07-24	4	4	3	11		x
	9	07-36	07-04,07-20	4	4	1	9	x			9	07-40	07-08,07-24	4	4	3	11	x	
	10	05-36	05-04,05-20	5	5	1	9		x		10	05-40	05-08,05-24	5	5	3	11		x
	11	05-36	05-04,05-20	5	5	1	9	x			11	05-40	05-08,05-24	5	5	3	11	x	
	12	03-36	03-04,03-20	6	6	1	9		x		12	03-40	03-08,03-24	6	6	3	11		x
	13	03-36	03-04,03-20	6	6	1	9	x			13	03-40	03-08,03-24	6	6	3	11	x	
	14	01-36	01-04,01-20	7	7	1	9		x		14	01-40	01-08,01-24	7	7	3	11		x
	15	01-36	01-04,01-20	7	7	1	9	x			15	01-40	01-08,01-24	7	7	3	11	x	

TABLE D – OUTPUT GATING – MCE AND ASWCPD FAILURES (Contd)

WORD	BIT	CP LOCATION		GROUP		ROW		FAILURE		WORD	BIT	CP LOCATION		GROUP		ROW		FAILURE	
		A39	A47	X	EA	Y	EA	MCE	ASWCPD			A39	A47	X	EA	Y	EA	MCE	ASWCPD
15	0	15-42	15-10,15-26	0	0	4	12		x	17	0	15-46	15-14,15-30	0	0	6	14		x
	1	15-42	15-10,15-26	0	0	4	12	x			1	15-46	15-14,15-30	0	0	6	14	x	
	2	13-42	13-10,13-26	1	1	4	12		x		2	13-46	13-14,13-30	1	1	6	14		x
	3	13-42	13-10,13-26	1	1	4	12	x			3	13-46	13-14,13-30	1	1	6	14	x	
	4	11-42	11-10,11-26	2	2	4	12		x		4	11-46	11-14,11-30	2	2	6	14		x
	5	11-42	11-10,11-26	2	2	4	12	x			5	11-46	11-14,11-30	2	2	6	14	x	
	6	09-42	09-10,09-26	3	3	4	12		x		6	09-46	09-14,09-30	3	3	6	14		x
	7	09-42	09-10,09-26	3	3	4	12	x			7	09-46	09-14,09-30	3	3	6	14	x	
	8	07-42	07-10,07-26	4	4	4	12		x		8	07-46	07-14,07-30	4	4	6	14		x
	9	07-42	07-10,07-26	4	4	4	12	x			9	07-46	07-14,07-30	4	4	6	14	x	
	10	05-42	05-10,05-26	5	5	4	12		x		10	05-46	05-14,05-30	5	5	6	14		x
	11	05-42	05-10,05-26	5	5	4	12	x			11	05-46	05-14,05-30	5	5	6	14	x	
	12	03-42	03-10,03-26	6	6	4	12		x		12	03-46	03-14,03-30	6	6	6	14		x
	13	03-42	03-10,03-26	6	6	4	12	x			13	03-46	03-14,03-30	6	6	6	14	x	
	14	01-42	01-10,01-26	7	7	4	12		x		14	01-46	01-14,01-30	7	7	6	14		x
	15	01-42	01-10,01-26	7	7	4	12	x			15	01-46	01-14,01-30	7	7	6	14	x	
16	0	15-44	15-12,15-28	0	0	5	13		x	18	0	15-48	15-16,15-32	0	0	7	15		x
	1	15-44	15-12,15-28	0	0	5	13	x			1	15-48	15-16,15-32	0	0	7	15	x	
	2	13-44	13-12,13-28	1	1	5	13		x		2	13-48	13-16,13-32	1	1	7	15		x
	3	13-44	13-12,13-28	1	1	5	13	x			3	13-48	13-16,13-32	1	1	7	15	x	
	4	11-44	11-12,11-28	2	2	5	13		x		4	11-48	11-16,11-32	2	2	7	15		x
	5	11-44	11-12,11-28	2	2	5	13	x			5	11-48	11-16,11-32	2	2	7	15	x	
	6	09-44	09-12,09-28	3	3	5	13		x		6	09-48	09-16,09-32	3	3	7	15		x
	7	09-44	09-12,09-28	3	3	5	13	x			7	09-48	09-16,09-32	3	3	7	15	x	
	8	07-44	07-12,07-28	4	4	5	13		x		8	07-48	07-16,07-32	4	4	7	15		x
	9	07-44	07-12,07-28	4	4	5	13	x			9	07-48	07-16,07-32	4	4	7	15	x	
	10	05-44	05-12,05-28	5	5	5	13		x		10	05-48	05-16,05-32	5	5	7	15		x
	11	05-44	05-12,05-28	5	5	5	13	x			11	05-48	05-16,05-32	5	5	7	15	x	
	12	03-44	03-12,03-28	6	6	5	13		x		12	03-48	03-16,03-32	6	6	7	15		x
	13	03-44	03-12,03-28	6	6	5	13	x			13	03-48	03-16,03-32	6	6	7	15	x	
	14	01-44	01-12,01-28	7	7	5	13		x		14	01-48	01-16,01-32	7	7	7	15		x
	15	01-44	01-12,01-28	7	7	5	13	x			15	01-48	01-16,01-32	7	7	7	15	x	

Z-REGISTER – MCE AND PCC FAILURES

*WORD	*BIT	CP LOCATION			COLUMN		MCE	PCC	*WORD	*BIT	CP LOCATION			COLUMN		MCE	PCC
		A40	A58	A1034	Z	EA					A40	A58	A1034	Z	EA		
19	3			17-36	0	16	X		20	3			17-40	8	24	X	
	4	26-24	17-34	17-36	0	16		X		4	26-20	17-34	17-40	8	24		X
	5			17-36	1	17	X			5			17-40	9	25	X	
	6	26-24	17-34	17-36	1	17		X		6	26-20	17-34	17-40	9	25		X
	7			17-36	2	18	X			7			17-40	10	26	X	
	8	26-24	17-34	17-36	2	18		X		8	26-20	17-34	17-40	10	26		X
	9			17-36	3	19	X			9			17-40	11	27	X	
	10	26-24	17-34	17-36	3	19		X		10	26-20	17-34	17-40	11	27		X
	11			17-38	4	20	X			11			17-42	12	28	X	
	12	26-22	17-34	17-38	4	20		X		12	26-18	17-34	17-42	12	28		X
	13			17-38	5	21	X			13			17-42	13	29	X	
	14	26-22	17-34	17-38	5	21		X		14	26-18	17-34	17-42	13	29		X
	15			17-38	6	22	X			15			17-42	14	30	X	
	16	26-22	17-34	17-38	6	22		X		16	26-18	17-34	17-42	14	30		X
	17			17-38	7	23	X			17			17-42	15	31	X	
	18	26-22	17-34	17-38	7	23		X		18	26-18	17-34	17-42	15	31		X

* Failure in multiple words and bits indicate faulty A54 CP (17-45, 17-46, 17-47, or 17-48) or 17-44 (A40)

CPD VERIFY ANSWER VA00 THROUGH 15 FAILURES

WORD & BIT	CIRCUIT PACK LOCATIONS (TYPE)				WORD & BIT	CIRCUIT PACK LOCATIONS (TYPE			
	ENCODER	OUTPUT GATES (TYPE A47)	SIGNAL GROUP	GROUP-ROW		ENCODER	OUTPUT GATES (TYPE A47)	SIGNAL GROUP	GROUP-ROW
Word 21 or 24 Bit 0	19-18 (A1), 19-02 (A44)	15-02, 15-18 15-04, 15-20 15-06, 15-22 15-08, 15-24 15-10, 15-26 15-12, 15-28 15-14, 15-30 15-16, 15-32	XYV00 XYV01 XYV02 XYV03 XYV04 XYV05 XYV06 XYV07	X0-Group 0	Word 21 or 24 Bit 4	19-22 (A1), 19-10 (A44)	07-02, 07-18 07-04, 07-20 07-06, 07-22 07-08, 07-24 07-10, 07-26 07-12, 07-28 07-14, 07-30 07-16, 07-32	XYV40 XYV41 XYV42 XYV43 XYV44 XYV45 XYV46 XYV47	X4-Group 4
Word 21 or 24 Bit 1	19-18 (A1), 19-04 (A44)	13-02, 13-18 13-04, 13-20 13-06, 13-22 13-08, 13-24 13-10, 13-26 13-12, 13-28 13-14, 13-30 13-16, 13-32	XYV10 XYV11 XYV12 XYV13 XYV14 XYV15 XYV16 XYV17	X1-Group 1	Word 21 or 24 Bit 5	19-22 (A1), 19-12 (A44)	05-02, 05-18 05-04, 05-20 05-06, 05-22 05-08, 05-24 05-10, 05-26 05-12, 05-28 05-14, 05-30 05-16, 05-32	XYV50 XYV51 XYV52 XYV53 XYV54 XYV55 XYV56 XYV57	X5-Group 5
Word 21 or 24 Bit 2	19-20 (A1), 19-06 (A44)	11-02, 11-18 11-04, 11-20 11-06, 11-22 11-08, 11-24 11-10, 11-26 11-12, 11-28 11-14, 11-30 11-16, 11-32	XYV20 XYV21 XYV22 XYV23 XYV24 XYV25 XYV26 XYV27	X2-Group 2	Word 21 or 24 Bit 6	19-24 (A1), 19-14 (A44)	03-02, 03-18 03-04, 03-20 03-06, 03-22 03-08, 03-24 03-10, 03-26 03-12, 03-28 03-14, 03-30 03-16, 03-32	XYV60 XYV61 XYV62 XYV63 XYV64 XYV65 XYV66 XYV67	X6-Group 6
Word 21 or 24 Bit 3	19-20 (A1), 19-08 (A44)	09-02, 09-18 09-04, 09-20 09-06, 09-22 09-08, 09-24 09-10, 09-26 09-12, 09-28 09-14, 09-30 09-16, 09-32	XYV30 XYV31 XYV32 XYV33 XYV34 XYV35 XYV36 XYV37	X3-Group 3	Word 21 or 24 Bit 7	19-24 (A1), 19-16 (A44)	01-02, 01-18 01-04, 01-20 01-06, 01-22 01-08, 01-24 01-10, 01-26 01-12, 01-28 01-14, 01-30 01-16, 01-32	XYV70 XYV71 XYV72 XYV73 XYV74 XYV75 XYV76 XYV77	X7-Group 7

CPD VERIFY ANSWER VA00 THROUGH 15 FAILURES (Contd)

WORD & BIT	CIRCUIT PACK LOCATIONS (TYPE)				WORD & BIT	CIRCUIT PACK LOCATIONS (TYPE)			
	ENCODER	OUTPUT GATES (TYPE A47)	SIGNAL GROUP	GROUP-ROW		ENCODER	OUTPUT GATES (TYPE A47)	SIGNAL GROUP	GROUP-ROW
Word 21 or 24 Bit 8	19-25, 19-02 19-04 19-06 19-08 19-10 19-12 19-14 19-16	15-02, 15-18 13-02, 13-18 11-02, 11-18 09-02, 09-18 07-02, 07-18 05-02, 05-18 03-02, 03-18 01-02, 01-18	XYV00 XYV10 XYV20 XYV30 XYV40 XYV50 XYV60 XYV70	Y0-Row 0	Word 21 or 24 Bit 12	19-27, 19-02 19-04 19-06 19-08 19-10 19-12 19-14 19-16	15-10, 15-26 13-10, 13-26 11-10, 11-26 09-10, 09-26 07-10, 07-26 05-10, 05-26 03-10, 03-26 01-10, 01-26	XYV04 XYV14 XYV24 XYV34 XYV44 XYV54 XYV64 XYV74	Y4-Row 4
Word 21 or 24 Bit 9	19-25, 19-02 19-04 19-06 19-08 19-10 19-12 19-14 19-16	15-04, 15-20 13-04, 13-20 11-04, 11-20 09-04, 09-20 07-04, 07-20 05-04, 05-20 03-04, 03-20 01-04, 01-20	XYV01 XYV11 XYV21 XYV31 XYV41 XYV51 XYV61 XYV71	Y1-Row 1	Word 21 or 24 Bit 13	19-27, 19-02 19-04 19-06 19-08 19-10 19-12 19-14 19-16	15-12, 15-28 13-12, 13-28 11-12, 11-28 09-12, 09-28 07-12, 07-28 05-12, 05-28 03-12, 03-28 01-12, 01-28	XYV05 XYV15 XYV25 XYV35 XYV45 XYV55 XYV65 XYV75	Y5-Row 5
Word 21 or 24 Bit 10	19-26, 19-02 19-04 19-06 19-08 19-10 19-12 19-14 19-16	15-06, 15-22 13-06, 13-22 11-06, 11-22 09-06, 09-22 07-06, 07-22 05-06, 05-22 03-06, 03-22 01-06, 01-22	XYV02 XYV12 XYV22 XYV32 XYV42 XYV52 XYV62 XYV72	Y2-Row 2	Word 21 or 24 Bit 14	19-28, 19-02 19-04 19-06 19-08 19-10 19-12 19-14 19-16	15-14, 15-30 13-14, 13-30 11-14, 11-30 09-14, 09-30 07-14, 07-30 05-14, 05-30 03-14, 03-30 01-14, 01-30	XYV06 XYV16 XYV26 XYV36 XYV46 XYV56 XYV66 XYV76	Y6-Row 6
Word 21 or 24 Bit 11	19-26, 19-02 19-04 19-06 19-08 19-10 19-12 19-14 19-16	15-08, 15-24 13-08, 13-24 11-08, 11-24 09-08, 09-24 07-08, 07-24 05-08, 05-24 03-08, 03-24 01-08, 01-24	XYV03 XYV13 XYV23 XYV33 XYV43 XYV53 XYV63 XYV73	Y3-Row 3	Word 21 or 24 Bit 15	19-29, 19-02 19-04 19-06 19-08 19-10 19-12 19-14 19-16	15-16, 15-32 13-16, 13-32 11-16, 11-32 09-16, 09-32 07-16, 07-32 05-16, 05-32 03-16, 03-32 01-16, 01-32	XYV07 XYV17 XYV27 XYV37 XYV47 XYV57 XYV67 XYV77	Y7-Row 7

CPD VERIFY ANSWER VA16 THROUGH 23 FAILURES

WORD & BIT	OUTPUT GATES CP (A47) GRP 0-7							
	0	1	2	3	4	5	6	7
21 or 24, Bit 16	15-02	13-02	11-02	09-02	07-02	05-02	03-02	01-02
21 or 24, Bit 17	15-20	13-20	11-20	09-20	07-20	05-20	03-20	01-20
21 or 24, Bit 18	15-06	13-06	11-06	09-06	07-06	05-06	03-06	01-06
21 or 24, Bit 19	15-24	13-24	11-24	09-24	07-24	05-24	03-24	01-24
21 or 24, Bit 20	15-10	13-10	11-10	09-10	07-10	05-10	03-10	01-10
21 or 24, Bit 21	15-28	13-28	11-28	09-28	07-28	05-28	03-28	01-28
21 or 24, Bit 22	15-14	13-14	11-14	09-14	07-14	05-14	03-14	01-14
21 or 24, Bit 23	15-32	13-32	11-32	09-32	07-32	05-32	03-32	01-32

INHIBIT AND NORMAL ERROR REPORT FAILURES

WORD & BITS	CIRCUIT PACK LOCATION (TYPE)	FUNCTION
Word 22 Bit 17	19-42(A46), 19-46(A156), 19-44(A43), 19-38(A4), 17-32(A2), 19-39(A5)	Matrix current excessive (MCE)
Word 22 Bit 19	26-24(A40), 26-22(A40) 26-20(A40), 26-18(A40), 17-34(A58), 17-36(A1034), 17-38(A1034), 17-40(A1034) 17-42(A1034)	Z-register parity check (PCC)
Word 23 Bit 16	17-31(A43), 17-28(A6), 19-46(A107), 19-44(A1036), 19-42(A6)	(All seems well CPD)
Word 23 Bit 17	19-44(A43), 19-48(A156), 19-42(A6), 17-28(A6)	Matrix current excessive (MCE)
Word 23 Bit 21	19-31(A6), 19-30(A44)	Verify answer (VA23)
Word 25 Bits 2, 4, 6, 8	17-24(A40), 19-39(A5), 19-36(A6), 19-38(A4), 26-30(A299), 26-32(A21)	X-register parity check
Word 25 Bits 10, 12, 14, 16	17-24(A40), 19-39(A5), 19-36(A6), 19-38(A4), 26-30(A299), 26-32(A21)	X-register parity
Word 25 Bits 3, 5, 7, 9	17-18(A40), 19-39(A5), 19-36(A6), 19-38(A4), 26-30(A299), 26-32(A21)	Y-register parity check
Word 25 Bits 11, 13, 15, 17	17-20(A40), 19-39(A5) 19-36(A6), 19-38(A4), 26-30(A299), 26-32(A21)	Y-register parity check

FAILURE PATTERN SENSITIVITY

FAILURE CHARACTERISTIC	POSSIBLE CAUSE OF FAILURE
Test phase 1 – STF	PU address bus 0 or scanner answer bus 0
Test phase 2 – STF	PU address bus 1 or scanner answer bus 1
Word(s) 1, 3, 6, or 8 – Bit(s) 0-14 Even	PU address fanout circuits for AD00-37: • Northeast fanout • Southwest fanout or scanner answer fan-in circuits for AN00-15 and scanner ASW
Word(s) 2, 4, 5 or 7 – Bit(s) 1-15 Odd	
Word(s) 9 or 11 Bit(s) 1 or 3	
Word(s) 10 or 12 Bit(s) 0 or 2	
Word(s) 13 or 15 Bit(s) 4 or 5	
Word(s) 14 or 15 Bit(s) 4 or 5	
Word(s) 1-8 Bit 18 or 19	PU parity check circuits – PUP feature generics 1E6/1AE6 and later
Any word with all bits set in preceding combinations	Enable address and gating circuit to address maintenance bus
Words 16-18 Bit 22	• WRMI A & B • WRMI C & D

PU ADDRESS BUS 0 (TEST PHASE 1) AND BUS 1 (TEST PHASE 2)

WORD	CPD ENABLE*	PU ADDRESS LEADS TESTED	FAN-OUT	SCANNER ANSWER BUS†	OCTAL TEST ORDER
1	C1A	Even – AD00-14	North-East	AN00-15,18&19	52525
2	C1A	Odd – AD01-15	North-East	AN00-15,18&19	125252
3	C2A	Even – AD00-14	South-West	AN00-15,18&19	52525
4	C2A	Odd – AD01-15	South-West	AN00-15,18&19	125252
5	C3A	Odd – AD17-31	North-East	AN00-15,18&19	125252
6	C3A	Even – AD16-30	North-East	AN00-15,18&19	52525
7	C4A	Odd – AD17-31	South-West	AN00-15,18&19	125252
8	C4A	Even – AD16-30	South-West	AN00-15,18&19	52525
9	C5A	Odd – AD33 & 35	North-East	AN00-03	12
10	C5A	Even – AD32 & 34	North-East	AN00-03	5
11	C6A	Odd – AD33 & 35	South-West	AN00-03	12
12	C6A	Even – AD32 & 34	South-West	AN00-03	5
13	C5A & C6A	AD36 & 37	North-East	AN04 & 05	60
14	C5A & C6A	AD36 & 37	South-West	AN04 & 05	60
15	C5A & C6A	AD36 & 37	North-East & South-West	AN04 & 05	60
16	C5A & C6A	AD00-31	WRMI A & B	AN16 (ASWS)	CPD enable address
17	C5A & C6A	AD00-31	WRMI C & D	AN16 (ASWS)	CPD enable address
18	C5A & C6A	AD00-31	WRMI A & B or WRMI C & D	AN16 (ASWS)	CPD enable address

* CPD group, row and column addresses are: C1A-056(0) & 057(1), C2A-060(0) & 061(1), C3A-062(0) & 063(1), C4A-064(0) & 065(1), C5A-066(1) & 067(1), and C6A-070(0) & 071(1)

† Bits 18 and 19 are dedicated to test PUPCK and PUP circuits for peripheral unit parity feature – generic 1AE6/1E6 and later

ADDRESS BUS FAN-OUT AND SCANNER ANSWER FAN-IN TEST – EVEN AND ODD CPD FRAME

REPLY WORD	FAILING BITS*	SUSPECTED FAULTY CIRCUIT PACK LOCATION (TYPE) IN REPLACEMENT ORDER	FUNCTION
1 and 2	0-3	36-02(A837), 34-02(A23), 34-03(A18), 32-20(A6), 32-19(A5), 28-01(A18), 36-18(A837), 36-19(A299), 36-20(A6)	Exercises northeast fanout and scanner answer fan-in circuits using alternate 101 and 010 patterns for address bits AD0-15
	4-7	36-05(A837), 34-05(A23), 34-03(A18), 32-20(A6), 32-19(A5), 28-01(A18), 36-18(A837), 36-19(A299), 36-20(A6)	
	8-11	36-07(A837), 34-07(A23), 34-08(A18), 32-22 (A6), 32-21(A5), 28-02(A18), 36-26(A837), 37-27(A299), 36-28(A6)	
	12-15	36-10(A837), 34-10(A23), 34-08(A18), 32-22(A6), 32-21(A5), 28-02(A18), 36-26(A837), 37-27(A299), 36-28(A6)	
	18 or 19	30-21(A837 or A21), 30-19(A177), 32-46(A867), 30-17(A18)	Tests parity check request (bit 18) and parity (bit 19) circuits of peripheral unit parity (PUP) feature – generic 1AE6 or 1E6 and later
3 and 4	0-3	30-20(A6), 30-19(A5), 36-11(A18), 36-02(A837)	Exercises southwest fanout and scanner answer fan-in circuits using alternate 101 and 010 patterns for address bits AD0-15
	4-7	30-20(A6), 30-19(A5), 36-11(A18), 36-05(A837)	
	8-11	30-22(A6), 30-21(A5), 36-12(A18), 36-07(A837)	
	12-15	30-22(A6), 30-21(A5), 36-12(A18), 36-10(A837)	
	18 or 19	30-21(A837 or A21), 30-19(A177), 32-46(A867), 30-17(A18)	Tests parity check request (Bit 18) and parity (bit 19) circuits of peripheral unit parity (PUP) feature – generic 1AE6 or 1E6 and later

See footnote at end of table

ADDRESS BUS FAN-OUT AND SCANNER ANSWER FAN-IN TEST – EVEN AND ODD CPD FRAME (Contd)

REPLY WORD	FAILING BITS*	SUSPECTED FAULTY CIRCUIT PACK LOCATION (TYPE) IN REPLACEMENT ORDER	FUNCTION
5 and 6	0-3	30-02(A837), 32-02(A23), 32-03(A18), 32-26(A6), 32-25(A5), 28-03(A18)	Exercises northeast fanout and scanner answer fan-in circuits using alternate 101 and 010 patterns for address bits AD16-31
	4-7	36-05(A837), 32-05(A23), 32-03(A18), 32-26(A6), 32-25(A5), 28-03(A18)	
	8-11	30-10(A837), 32-10(A23), 32-08(A18), 32-28(A6), 32-27(A5), 28-04(A18)	
	12-15	30-07(A837), 32-07(A23), 32-08(A18), 32-28 (A6), 32-27(A5), 28-04(A18)	
	18 or 19	30-21(A837 or A21), 30-19(A177), 32-46(A867), 30-17(A18)	Tests parity check request (bit 18) and parity (bit 19) circuits of peripheral unit parity (PUP) feature – generic 1AE6 or 1E6 and later
7 and 8	0-3	30-26(A6), 30-25(A5), 36-13(A18), 30-02(A837)	Exercises southwest fanout and scanner answer fan-in circuits using alternate 101 and 010 patterns for address bits AD16-31
	4-7	30-26(A6), 30-25(A5), 36-13(A18), 36-05(A837)	
	8-11	30-28(A6), 30-27(A5), 36-14(A18), 30-10(A837)	
	12-15	30-28(A6), 30-27(A5), 36-14(A18), 30-07(A837)	
	18 or 19	30-21(A837 or A21), 30-19(A177), 32-46(A867), 30-17(A18)	Tests parity check request (bit 18) and parity (bit 19) circuits of peripheral unit parity (PUP) feature – generic 1AE6 or 1E6 and later

See footnote at end of table

ADDRESS BUS FAN-OUT AND SCANNER ANSWER FAN-IN TEST – EVEN AND ODD CPD FRAME (Contd)

REPLY WORD	FAILING BITS*	SUSPECTED FAULTY CIRCUIT PACK LOCATION (TYPE) IN REPLACEMENT ORDER	FUNCTION
9 and 10	0-3	30-12(A837), 32-12(A23), 32-13(A18), 32-30(A6), 32-29(A5), 28-05(A18)	Exercises northeast fanout and scanner answer fan-in circuits using alternate 1010 and 0101 patterns for address bits AD32-35
11 and 12	0-3	30-30(A6), 30-29(A5), 36-15(A18), 30-12(A837)	Exercises southwest fanout and scanner answer fan-in circuits using alternate 1010 and 0101 patterns for address bits AD32-35
13, 14, and 15	4 and 5	30-30(A6), 30-29(A5), 36-15(A18), 30-15 (A837), 32-15(A23), 32-13(A18)	Exercises fanout and scanner answer fan-in circuits using alternate 1 and 0 patterns for address bit AD36: (A) northeast (words 13 and 15) (B) southwest (words 14 and 15)
16 17 18	AN16 (ASWS)	30-17 (A18), 30-23 (A40), 30-18 (A177) 30-25 (A837)	Exercises we-really-mean-it (WRMI) fanout circuits and scanner answer AN16 (ASWS) circuits: (A) Word 16 – WRMI A & B (B) Word 17 – WRMI C & D (C) Word 18 – WRMI A & B or WRMI C & D

* Bit 16 of all reply words, except 13, 14, and 15, indicates status of 0/1 CPD all seems well (ASWCPD) and denotes, when set, failure of PU bus to operate at specified enable address

0 OR 1 CPD ENABLING PULSE C1A THROUGH C6A STROBE OPERATIONAL TEST

REPLY WORD	FAILING BITS	SUSPECTED FAULTY CIRCUIT PACK LOCATION (TYPE) IN REPLACEMENT ORDER	FUNCTION
1 2	0,2,4,6 and/or 8,10,12, 14, 1,3,5,7 and/or 9,11,13,15	32-17(A177), 34-12(A42) 32-20(A6) – Bits 0-7 32-22(A6) – Bits 8-15	Checks C1A enable pulse from 0/1 CPD at GRC* addresses 056(0) and 057(1) for scanner answer bits AN0-15
3 4	0,2,4,6 and/or 8,10,12,14 1,3,5,7, and/or 9,11,13,15	32-17(A177), 34-14(A42) 30-20(A6) – Bits 0-7 30-22(A6) – Bits 8-15	Checks C2A enable pulse from 0/1 CPD at GRC* addresses 060(0) and 061(1) for scanner answer bits AN0-15
5 6	1,3,5,7, and/or 9,11,13,15 0,2,4,6, and/or 8,10,12,14	32-17(A177), 34-12(A42) 32-26(A6) – Bits 0-7 32-28(A6) – Bits 8-15	Checks C3A enable pulse from 0/1 CPD at GRC* addresses 062(0) and 063(1) for scanner answer bits AN0-15
7 8	1,3,5,7, and/or 9,11,13,15 0,2,4,6, and/or 8,10,12,14	32-17(A177), 34-14(A42) 30-26(A6) – Bits 0-7 30-28(A6) – Bits 8-15	Checks C4A enable pulse from 0/1 CPD at GRC* addresses 064(0) and 065(1) for scanner answer bits AN0-15
9 10	1 and 3 0 and 2	32-17(A177), 32-30(A6), 34-16(A42), 34-29(A43), 30-30(A6)	Checks C5A enable pulse from 0/1 CPD at GRC* addresses 066(0) and 067(1) for scanner answer bits AN0-3
11 12	1 and 3 0 and 2	32-17(A177), 32-30(A6), 34-16(A42), 34-27(A43), 30-30(A6)	Checks C6A enable pulse from 0/1 CPD at GRC* addresses 070(0) and 071(1) for scanner answer bits AN0-3
13 14 or 15	4 and 5	32-17(A177), 32-30(A6), 34-16(A42), 34-27(A43)	Checks 0/1 CPD enable pulse C5A and C6A to gate address bit AD36 to scanner answer bits AN4 and AN5 fan-in circuits

* GRC address is group, row, and column address of output gate terminal strip located in 0 or 1 CPD

PROBABLE FAILURE PATTERNS – TEST PHASES 1 AND 2

WORD, BIT	FAILURE OF FUNCTION OR TROUBLE CONDITION	PATTERN NO.
Words 1-8 Bits 8-15	ASWCPD for test (T) – lead in conjunction with all 64 X- and Y-decoder addresses: 1. Single failure-any word: Decoder XY-address 2. All bits failing-any word: Y-address 3. Single bit failing -all words: X-address 4. All words and bits: control operations, input gate at decoder and Z-register or ouput gate	1
Words 9,10 Bits 16-21	1. Parity checks for X- and Y-registers in decoder and Z-register: control, decoder or output gate 2. Maintenance input and output data transfers	2
Words 11-18 Bits 0-15	Matrix current of output gates and ASWCPD for all X- and Y-addresses during control inhibit mode: checks for shorted diodes in output gates	3
Words 19,20 Bits 3-18	Matrix current of output gates and parity check of Z-register for each Z-register driver using 16 valid addresses during the inhibited state	4
Words 21,24 Bits 0-22	Z-register test lead in inhibit mode – (word 20) and normal terminated CPD address – (word 23) indicate failure of encoder or verify answer bus	5
Word 22 Bits 17,19 & 21	Matrix current and parity check PCC indicate Z-register and encoder failures	6
Word 23 Bits 17,19 & 21	Shorted CPD address has matrix current and ASWCPD checked. CPD operates in normal mode. Failure indicates control error	6
Word 25 Bits 2-17	Parity checks for X- and Y-addresses detect failure of control and detector	6

FAILURE PATTERN SENSITIVITY

FAILURE CHARACTERISTIC	POSSIBLE CAUSE OF FAILURE	NUMBER
Test phase 1 – STF	PU address bus 0 or scanner answer bus 0	1
Test phase 2 – STF	PU address bus 1 or scanner answer bus 1	2
Word(s) 1, 3, 6, or 8 – Bit(s) 0-14 even	PU address fanout circuits for ADOO-37: • Northeast fanout • Southwest fanout or scanner answer fan-in circuits for ANOO-15 and scanner ASW	3
Word(s) 2, 4, 5 or 7 – Bit(s) 1-15 odd		
Word(s) 9 or 11 Bit(s) 1 or 3		
Word(s) 10 or 12 Bit(s) 0 or 2		
Word(s) 13 or 15 Bit(s) 4 or 5		
Word(s) 14 or 15 Bit(s) 4 or 5		
Any word with all bits set in preceding combinations	Enable address and gating circuit to address maintenance bus	4
Word(s) 1-8 Bit 18 or 19	PU parity check circuits – PUP feature generics 1E6/1AE6 and later	5
Words 16-18 Bit 22	• WRMI A & B • WRMI C & D	6

Section 2

COMBINED MISCELLANEOUS TRUNK (CMT) (J1A088C)

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Supporting Documentation

MASTER SCANNER (MS), UNIT TYPE 5
SD-1A209
J1A043B
CD-1A209
PK-1A027 Scanner Raw Data Document
TLM-1A209
ED-1A207-11

SUPPLEMENTARY SIGNAL DISTRIBUTOR (SSD), UNIT TYPE 21

SD-1A401 Basic SSD
SD-A402 Optional SSD
CD-1A401
CD-1A402
TLM-1A401
TLM-1A402
ED-1A355-12

SD-1A403 Matrix
SD-1A404 TIC (Trunk Interconnect CKT)
SD-1A405 Power and Miscellaneous
SD-1A452 960 Point Matrix
PK-1A028 Remreed NTWK Raw Data DOC
BSP 820-232-150 MS
BSP 820-031-153 CMT
TOP 231-050-002 2-Wire MT Frame

F, S, AND T POINT LAYOUT - MASTER SCANNER

	CONTROLLER SCAN POINTS			
	F	S	T	CONDITION
0	0	0	0	POWER ON (OLD)
1	0	0	1	
2	0	1	0	
3	0	1	1	POWER ON (NEW)
4	1	0	0	
5	1	0	1	
6	1	1	0	
7	1	1	1	POWER OFF

OCTAL ORDER LAYOUT - MASTER SCANNER

22 10	9 7	6 4	3 0
	MST SIG ROW	LST SIG ROW	

LAYOUT TO DISPLAY SCAN POINTS AT MASTER CONTROL CENTER

MASTER SCANNER ROW CODE = 000

22 21	20 18	17 16	15 10	9 4	3 0
	CODE		FRAME NUMBER	ROW	SCAN POINT

F, S, AND T POINT LAYOUT - SUPPLEMENTARY SIGNAL DISTRIBUTOR

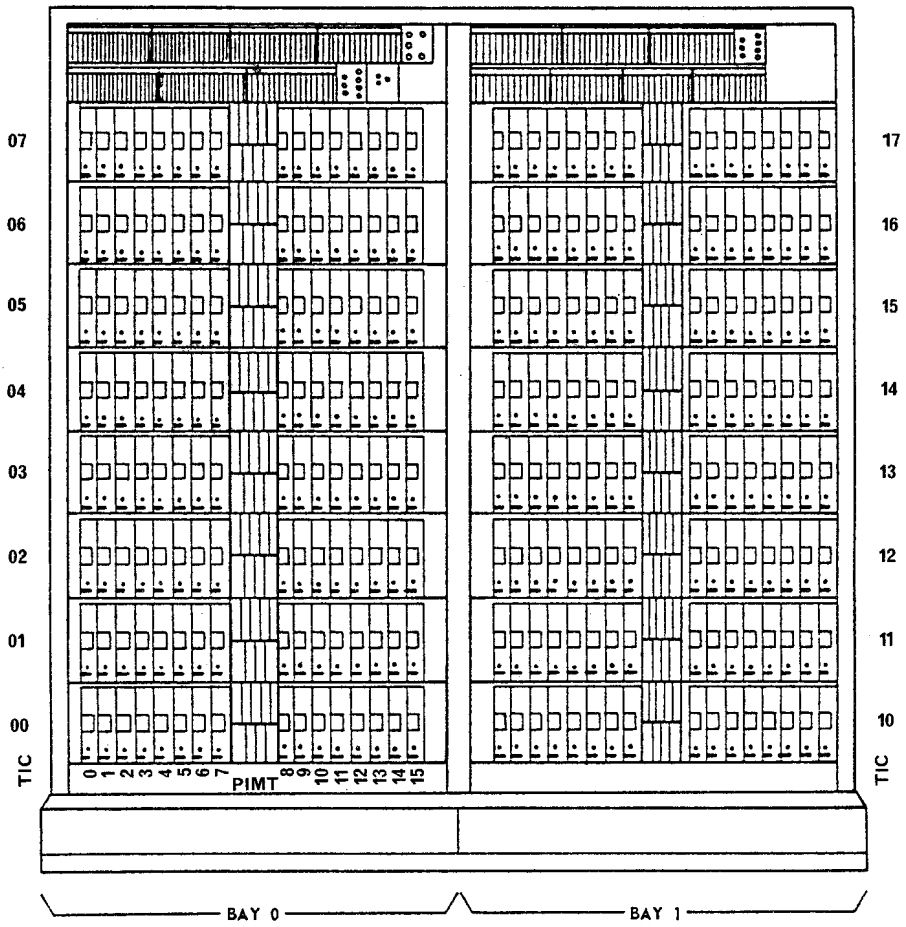
	CONTROLLER SCAN POINTS			
	F	S	T	CONDITION
0	0	0	0	IDLE
1	0	0	1	QUAR
2	0	1	0	
3	0	1	1	TPAQ
4	1	0	0	ENABLED
5	1	0	1	
6	1	1	0	TPA
7	1	1	1	POWER OFF

OCTAL ORDER LAYOUT - SUPPLEMENTARY SIGNAL DISTRIBUTOR

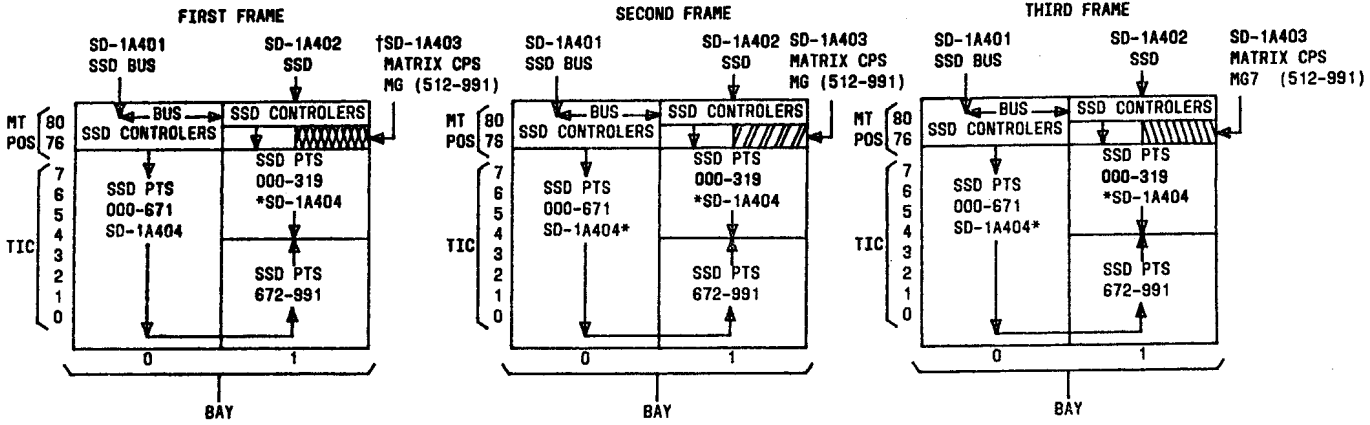
22 11	10	9	8 7	6 2	1 0
	OPR	HALF	QUAD	ROW	FIELD

OPR = 0 OPERATE
= 1 RELEASE

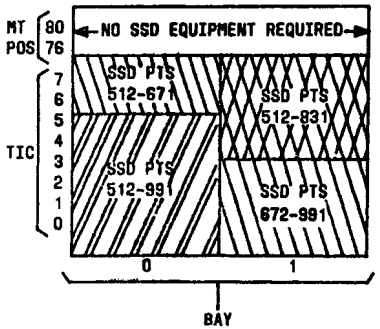
CMT FRAME, J1A088C



TYPE A CMT FRAME



‡FOURTH FRAME



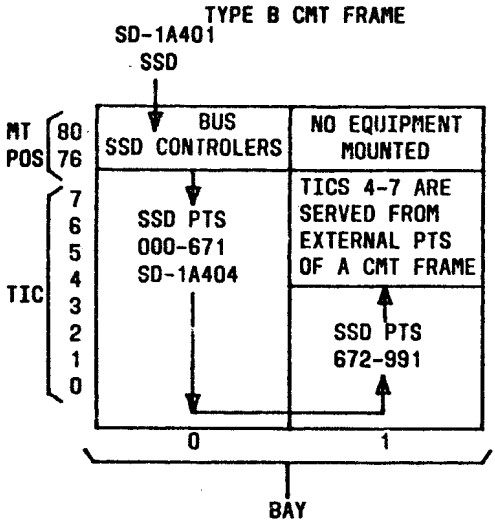
EACH CMT FRAME CAN CONTAIN 256 PIMTS:
(A) 16 VF(S) X 8 TIC(S) = 128 PIMTS PER BAY
(B) 128 X 2 BAYS = 256 PIMTS PER CMT FRAME

"A" TYPE CMT FRAME (J1A088A)

THIS FRAME ACCEPTS ONY TWO TYPES OF PLUG IN MISCELLANEOUS TRUNKS PIMTS.
A. 2-WAY TRK MF4-W (TOLL) SD-1A236-05
B. 2-WAY TRK DP4-W (TOLL) SD-1A237-05

ALL TRUNK INTERCONNECT CIRCUITS WILL BE J1A088EC PER SD-1A404.

*SD-1A404 CONTAINS THE MATRIX CPS MG7
†SD-1A403 CONTAINS THE MATRIX CPS (MG7) FOR THE SD-1A402 SSD AND CABLED TO FOURTH FRAME
‡FOURTH FRAME TICS ARE IN SD-1A404 (OPTION W;NO MATRIX CPS)



TYPE "B" CMT FRAME (J1A088B)

THIS FRAME ACCEPTS ONLY 5 TYPES OF PIMTS.

A. 2-WAY TRK MF4-W (LOCAL) SD-1A236-05

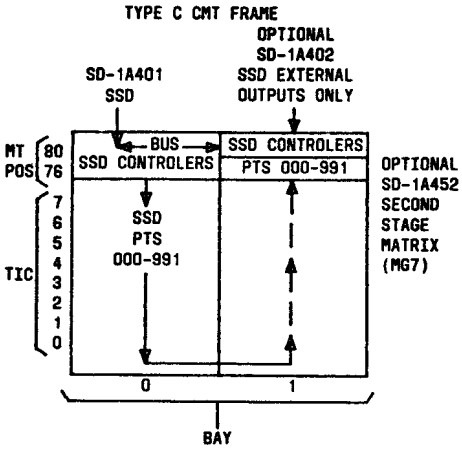
B. 2-WAY TRK DP4-W (LOCAL) SD-1A237-05

C. LONG HAUL FX TRK SD-1A415-05

D. FX TRK SD-1A416-05

E. 2-WAY TRK DP SD-1A163-05

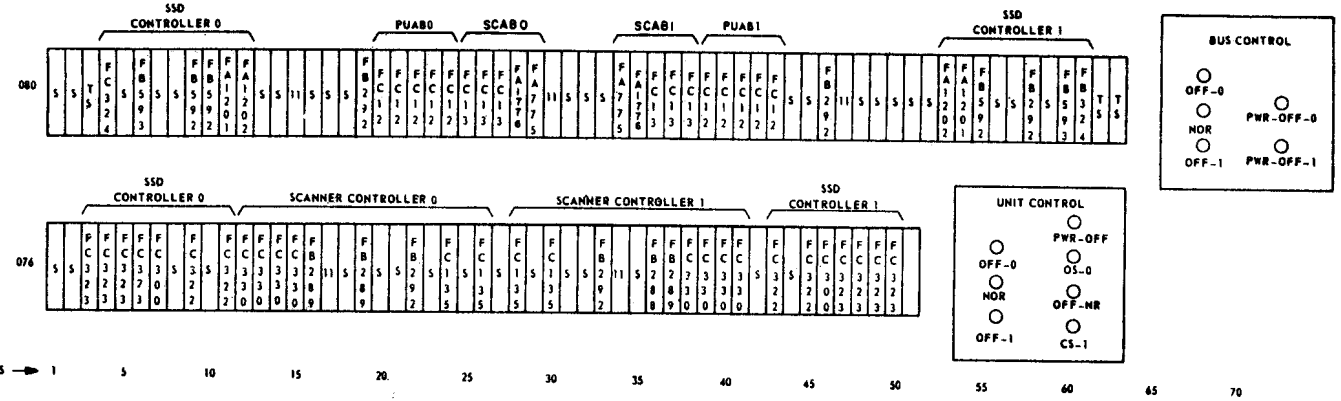
ALL TICS WILL BE J1A088EC PER SD-1A404.



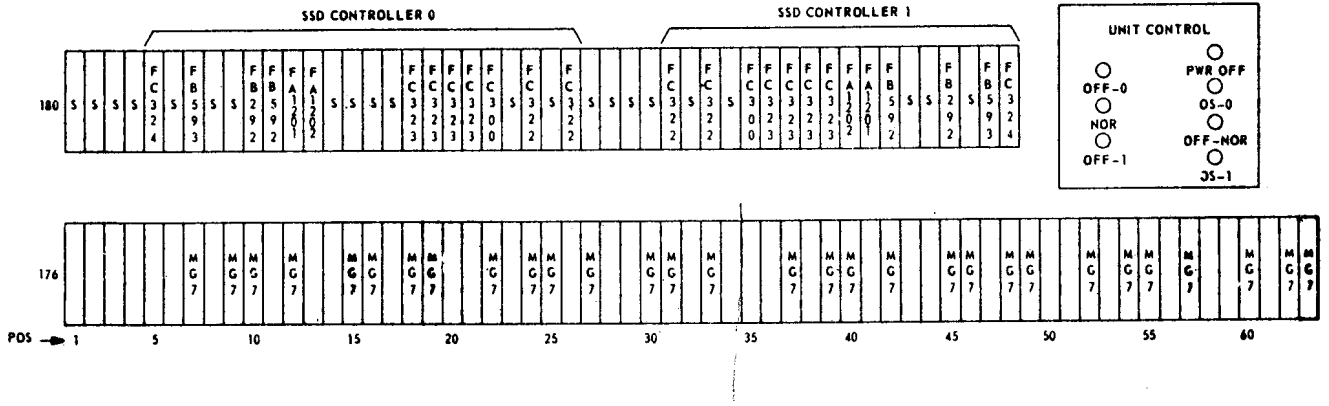
TYPE "C" CMT FRAME (J1A088C)

THIS FRAME IS MANUFACTURED PER JOB REQUIREMENTS FOR ANY TYPE OF PIMT.

SD NO.	PIMT	TIC "J" NO.	TIC SD NO.
SD-1A236-05	2-WAY TRK MF4-W (TOLL OR LOCAL)	J1A088EC	SD-1A404
237-05	2-WAY TRK DP4-W (TOLL OR LOCAL)		
163-05	2-WAY TRK DP		
415-05	LONG HAUL FX TRK		
416-05	2-WAY TRK DP		
SD-1A172-05	CDPR	J1A088EK	SD-1A407
SD-1A311-05	CAMA INC TRK SXS	J1A088EL	SD-1A408
SD-1A168-05	RING 1 AND 2 PRY	J1A088EM	SD-1A409
SD-1A245-05	ATND TRK 2-W	J1A088EP	SD-1A410
248-05	ATND TRK 4-W		
283-05	ATND LOOP		
SD-1A284-05	3 PORT CONF	J1A088ER	SD-1A411
SD-1A177-05	VERIF REQ AND INCPT	J1A088ES	SD-1A412
239-05	DP RPTR		
319-05	LINE ACCESS TRK		
SD-1A169-05	OGT 3CL SWBD (DIST BLDG)	J1A088EN	SD-1A413
221-05	AUD. RING & REC ANN		
222-05	PS-PARTIAL DIAL HOLD		
223-05	OGT TRK TO 3C/3CL SWBD		
224-05	INC TRK FROM 3C/3CL SWBD		
SD-1A220-05	INC SXS TRK	J1A088ET	SD-1A414
321-05	INC TRK FROM TRAFFIC SVC POS #1		
SD-1C650-01	TT DET	J99338C	SD-1C650



CMT SSD AND SCANNER CONTROLLERS



CMT OPTIONAL SSD

CIRCUIT PACK FUNCTION, TYPE AND LOCATION

TYPE	CIRCUIT PACK FUNCTION	FS	BASIC CMT CKT 0	BASIC CMT CKT 1	OPTIONAL CMT CKT 0	OPTIONAL CMT CKT 1
FA775 (CONT)	Controller, Register and Translator	6	06-29	06-34		
FA1776 (SA)	Scanner Answer Bus Register	1	06-28	06-35		
FA1201	Enable, Buffer Reg, TRNSL and DISCR	1	06-11	06-54	02-12	02-41
FA1202	Buffer Reg, MTCE and Diagnostic CKT	1	06-12	06-53	02-13	02-40
FB288 (ICD)	Interrogate Current Drivers	6	02-19	02-36		
FB289B (TB)	Scanner Timing	6	02-16	02-37		
FB592	Timing and Differentiating CKT	2	06-10	06-55	02-11	02-42
FB593	Pulse and Detector CKT	3	06-06	06-60	02-07	02-47
FC12 (CR0)	Cable Receiver - PU Address Bits 0 - 7	1	06-20	06-39	From Basic CMT	
FC12 (CR1)	Cable Receiver - PU Address Bits 8 - 15	1	06-21	06-40	From Basic CMT	
FC12 (CR2)	Cable Receiver - PU Address Bits 16 - 23	1	06-22	06-41	From Basic CMT	
FC12 (CR3)	Cable Receiver - PU Address Bits 24 - 27, 36	1	06-23	06-42	From Basic CMT	
FC12 (CR4)	Cable Receiver - PU Enable from CPD	1	06-24	06-43	From Basic CMT	
FC13 (CD0)	Cable Driver - PU Enable Verify to CPD	1	06-25	06-36	To Basic CMT	
FC13 (CD1)	Cable Driver - Scanner Answer	1	06-26	06-37		
FC13 (CD2)	Cable Driver - Scanner Answer	1	06-27	06-38		

Note: Only basic CMT is provided with miniaturized scanner and has ferrod matrix available using terminal strip.

COMBINED MINIATURIZED TRUNK FRAME

SD 1A401 - Basic SSD
SD 1A402 - Optional SSD

CIRCUIT PACK FUNCTION, TYPE AND LOCATION

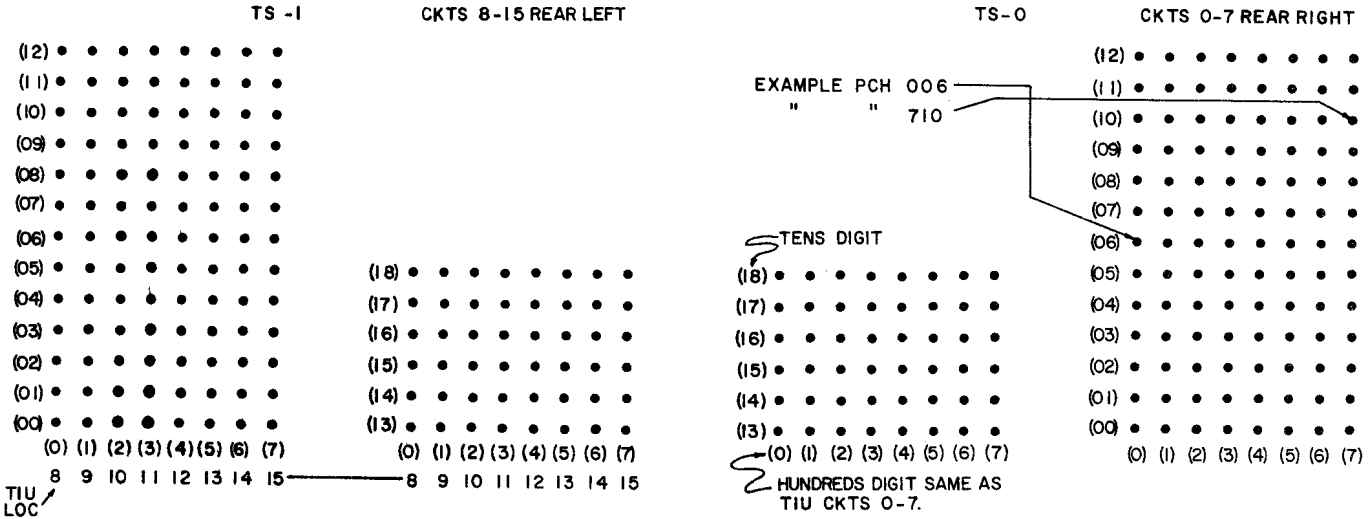
TYPE	CIRCUIT PACK FUNCTION	FS	BASIC CMT CKT 0	BASIC CMT CKT 1	OPTIONAL CMT CKT 0	OPTIONAL CMT CKT 1
FC135 (SDO)	Scanner Detector	7	02-24	02-26		
FC135 (SD1)	Scanner Detector	7	02-28	02-30		
FC300	Interface CKT	4	02-07	02-46	02-22	02-35
FC322	TRIAC Selection CKT - Normal (NTSEL)	4	02-09	02-45	02-24	02-31
FC322	TRIAC Selection CKT - Quarantine (QTSEL)	4	02-11	02-43	02-26	02-33
FC323	First Stage TRIAC CKT - Normal (NOFST)	5	02-03	02-50	02-18	02-39
FC323	First Stage TRIAC CKT - Quarantine (QOFST)	5	02-05	02-48	02-20	02-37
FC323	First Stage TRIAC CKT - Normal (N1FST)	5	02-04	02-49	02-19	02-38
FC323	First Stage TRIAC CKT - Quarantine (Q1FST)	5	02-06	02-47	02-21	02-36
FC324	Miscellaneous Circuit	3	06-04	06-61	02-05	02-48
FC330 (IM0)	Interrogate Matrix	6	02-12	02-38		
FC330 (IM1)	Interrogate Matrix	6	02-13	02-39		
FC330 (IM2)	Interrogate Matrix	6	02-14	02-40		
FC330 (IM3)	Interrogate Matrix	6	02-15	02-41		

COMBINED MINIATURIZED TRUNK FRAME

SD 1A401 - Basic SSD
SD 1A402 - Optional SSD

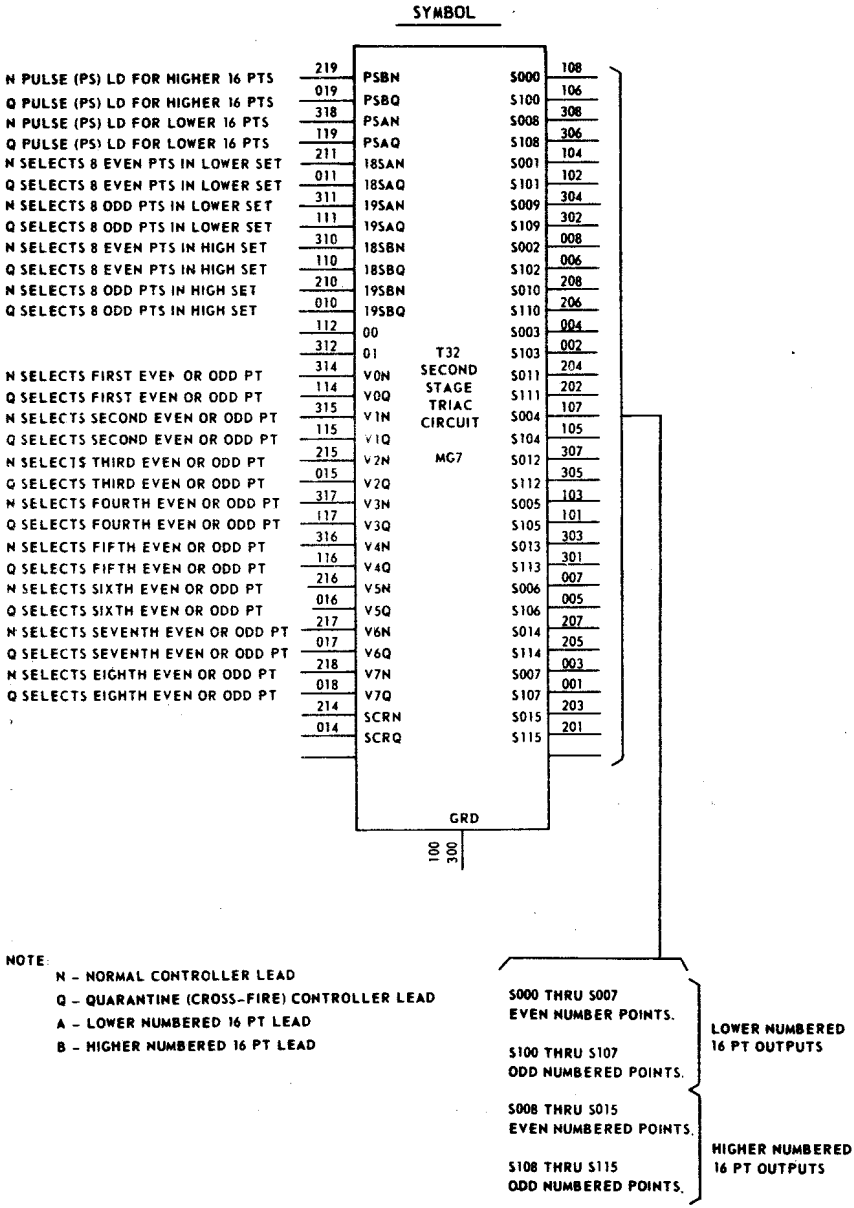
TIU TS

LEAD ASSIGNMENTS ON REAR OF CMT																				
TRUNK	SD-1AXXX-05	J-1A088-	PCH ON REAR OF TIU																	
			0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
RING 1&2 PTY	168	DB-1	R	T	R(A)	T(A)															
CDPR	172	DC-1	R	T	R (TT)	T (TT)															
VERIF REQ† INCPT	177	BB-1	R	T	RI	TI								+130							
INC SXS	220	AB-1	R	T	R	T	RI	TI	RI	TI	N	G	N	G							
AUD RING & REC ANN	221	DT-1	R2	T2	R5	T5	S	TO	RO	TI	RI	DA 11	DA 12	DA 10	DA 20	T3	R3	T4	R4	F	FG
2 WY TRK DP 4W	237	CC-1	R	T	RI	TI	R2	T2	E	SG	M	SB									
3 PORT CONF	284	JG-1	R	T	RI	TI	R2	T2													



BACKPLANE TS - TIU

MG7 CIRCUIT PACK
SYMBOL, TERMINALS, AND TERMINAL DESIGNATIONS



NOTE:

N – NORMAL CONTROLLER LEAD

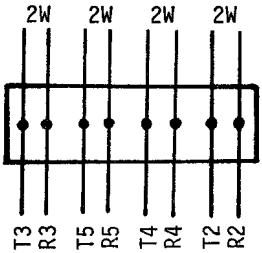
Q – QUARANTINE (CROSS-FIRE) CONTROLLER LEAD

A – LOWER NUMBERED 16 PT LEAD

B – HIGHER NUMBERED 16 PT LEAD

CMT MDF WIRING

CROSS-CONNECTIONS TO CIRCUITS



LEAD DESIG	TRK TERM MOD	TRK DWG	DESTINATION
( ) R2 ( ) T2	R (RA1) T (RA1)	T1A221-15 T1A222-15	TO TONE CIRCUIT OR RECORDED ANN CKT
( ) R2 ( ) T2	GB G	T1A224-15	TO GROUP BUSY LAMP, TONE AND REG CKT
( ) R4 ( ) T4	R (RA0) T (RA0)	T1A221-15 T1A222-15	TO TONE CIRCUIT OR RECORDED ANN CKT
( ) R4 ( ) T4	RT TT	T1A223-15 T1A224-15	TO TRUNK, JACK LAMP AND KEY CIRCUIT
( ) R4 ( ) T4	R T	T1A169-15	TO TRANSMISSION AND SIGNALLING FACILITIES
( ) R5 ( ) T5	R (AR0) T (AR0)	T1A221-15	TO TONE CIRCUIT (TONE DISTRIBUTION)
( ) R5	LR	T1A223-15	TO MULT LAMP RELAY CKT
( ) R5 ( ) T5	LS LG	T1A224-15	TO IDLE INDICATING LAMP CIRCUIT
( ) R3 ( ) T3	R (AR1) T (AR1)	T1A221-15	TO TONE CIRCUIT (TONE DISTRIBUTION)

REFERENCE - T1A413

PERIPHERAL BUS
CONNECTORIZED CABLE LOCATION

COMBINED MINIATURIZED TRUNK FRAME

ANSWER BUS CABLES	BUS 0	
BITS	IN	OUT
00-07	80-26-310	80-26-110
08-15	80-27-310	80-27-110
ASW	80-18-310	80-18-110

ANSWER BUS CABLES	BUS 1	
BITS	IN	OUT
00-07	80-37-310	80-37-110
08-15	80-38-310	80-38-110
ASW	80-45-310	80-45-110

ADDRESS BUS CABLES	BUS 0	
BITS	IN	OUT
00-07	80-20-310	80-20-110
08-15	80-21-310	80-21-110
16-23	80-22-310	80-22-110
24-31	80-17-310	80-17-110
32-37	80-17-100	80-17-300

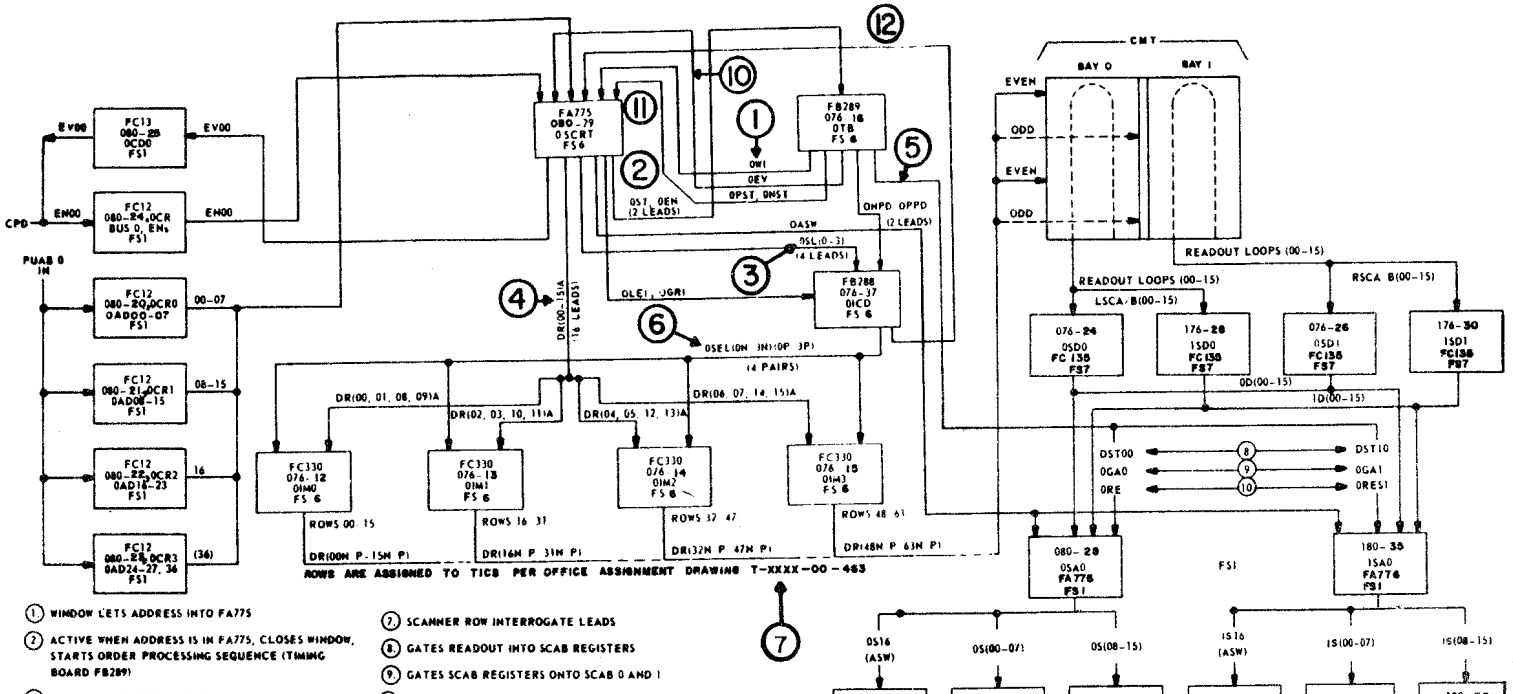
ADDRESS BUS CABLES	BUS 1	
BITS	IN	OUT
00-07	80-39-310	80-39-110
08-15	80-40-310	80-40-110
16-23	80-41-310	80-41-110
24-31	80-44-310	80-44-110
32-37	80-44-100	80-44-300

COMBINED MISCELLANEOUS TRUNK FRAME
ENABLE LEAD INPUT LOCATION
SYNC POINT LOCATION

ENABLE	INPUT PIN	COLOR	SYNC POINT	CKT	CPD
00P	80-24-311	BL1W	80-24-308	SC	0
00N	-211	BL2W		SC	0
10P	-312	BL1W	-307	SC	1
10N	-212	BL2W		SC	1
00P	-313	OR1W	-306	RIGHT	0
00N	-213	OR2W		SSD	0
10P	-314	OR1W	-305	BAY 1	1
10N	-214	OR2W		BAY 1	1
00P	-315	GR1W	-304	LEFT	0
00N	-215	GR2W		SSD	0
10P	-316	GR1W	-303	BAY 0	1
10N	-216	GR2W		BAY 0	1
-	-317	BR1W	-302	-	-
-	-217	BR2W		-	-
-	-318	BR1W	-301	-	-
-	-218	BR2W		-	-

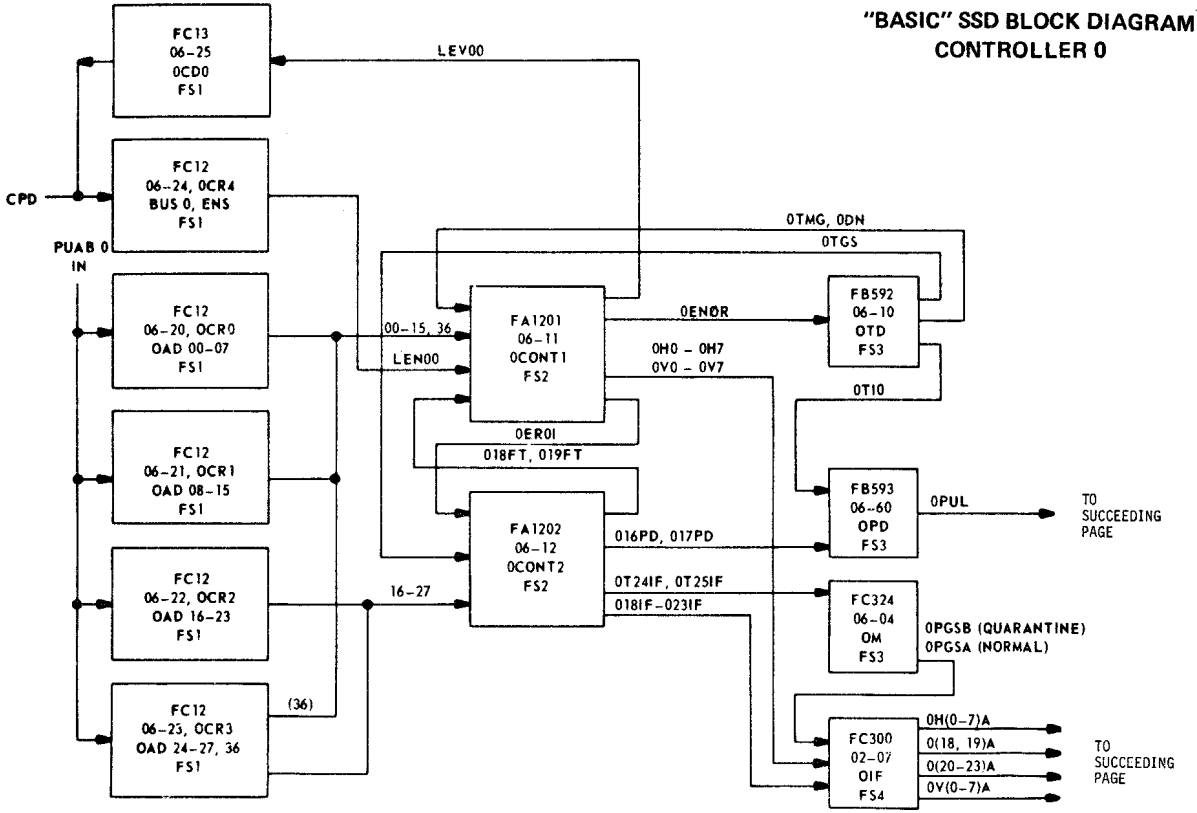
ENABLE	INPUT PIN	COLOR	SYNC POINT	CKT	CPD
01P	80-43-311	BL1W	80-43-308	SC	1
01N	-211	BL2W		SC	1
11P	-312	BL1W	-307	SC	0
11N	-212	BL2W		SC	0
01P	-313	OR1W	-306	RIGHT	1
01N	-213	OR2W		SSD	1
11P	-314	OR1W	-305	BAY 1	0
11N	-214	OR2W		BAY 1	0
01P	-315	GR1W	-304	LEFT	1
01N	-215	GR2W		SSD	1
11P	-316	GR1W	-303	BAY 0	0
11N	-216	GR2W		BAY 0	0
-	-317	BR1W	-302	-	-
-	-217	BR2W		-	-
-	-318	BR1W	-301	-	-
-	-218	BR2W		-	-

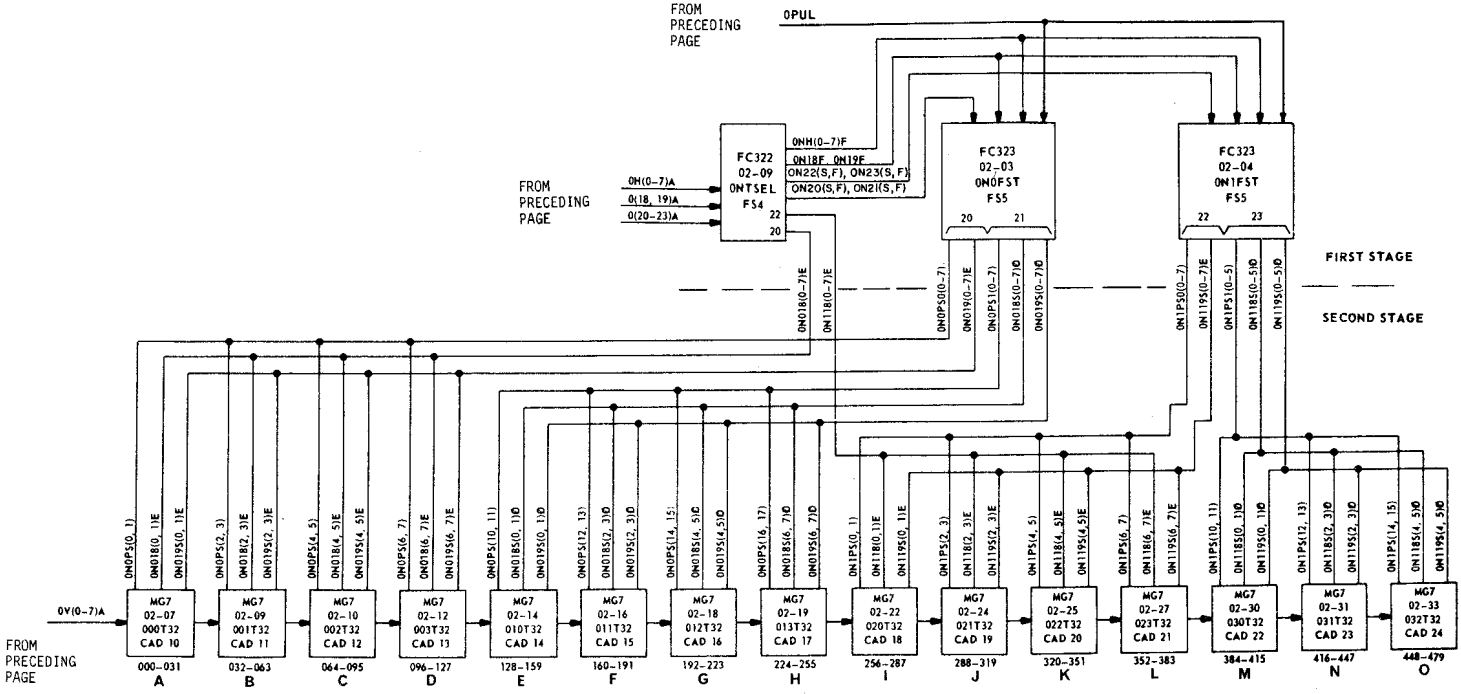
	CMT				MUT				SSD - JCT SSD
	IN	OUT			IN	OUT	IN	OUT	
	080-03	080-62	080-63	180-03	080-11	080-12	180-12	180-11	MISC
AR	201	201			216	216	216	216	050
ARM	001	001			215	215	215	215	060
BR	202	202			214	214	214	214	051
BRM	002	002			213	213	213	213	061
DR	203	203			212	212	212	212	052
DRM	003	003			211	211	211	211	062
DF	205	205			206	206	206	206	054
DFM	005	005			205	205	205	205	064
AP	204	204			208	208	208	208	053
APM	004	004			207	207	207	207	063
FO	206/212			206	204			204	032
FOM	006/012			006	203			203	042
SO	207			207	202			202	033
SOM	007			007	201			201	043
TO	208			208	018			018	034
TOM	008			008	017			017	044
F1	/213			201	016			016	035
F1M	/013			001	015			015	045
S1				202	014			014	036
S1M				002	013			013	046
T1				203	012			012	037
T1M				003	011			011	047
SC003		006			217				
SC013		007							
SC00		206			218				
SC10		207							
		FOR 355A TS				FOR 355A TS			FOR 288 MISC TS



1. WINDOW LETS ADDRESS INTO FA775
2. ACTIVE WHEN ADDRESS IS IN FA775, CLOSES WINDOW, STARTS ORDER PROCESSING SEQUENCE (TIMING BOARD FB289)
3. 1:4 SELECT FOR SCANNER ROW
4. 1:16 SELECT FOR SCANNER ROW
5. ACTIVATES AND TIMES THE NEGATIVE (RESET) AND POSITIVE (INTERROGATE) DRIVES IN FB288
6. NEGATIVE AND POSITIVE DRIVE LEADS TO FC330
7. SCANNER ROW INTERROGATE LEADS
8. GATES READOUT INTO SCAB REGISTERS
9. GATES SCAB REGISTERS ONTO SCAB 0 AND 1
10. RESETS SCAB REGISTERS AND CONTROLLER CP FA775
11. STROBES OR GATES FOR LESS-THAN AND GREATER-THAN FAILURES
12. LESS-THAN AND GREATER-THAN INDICATION LEADS

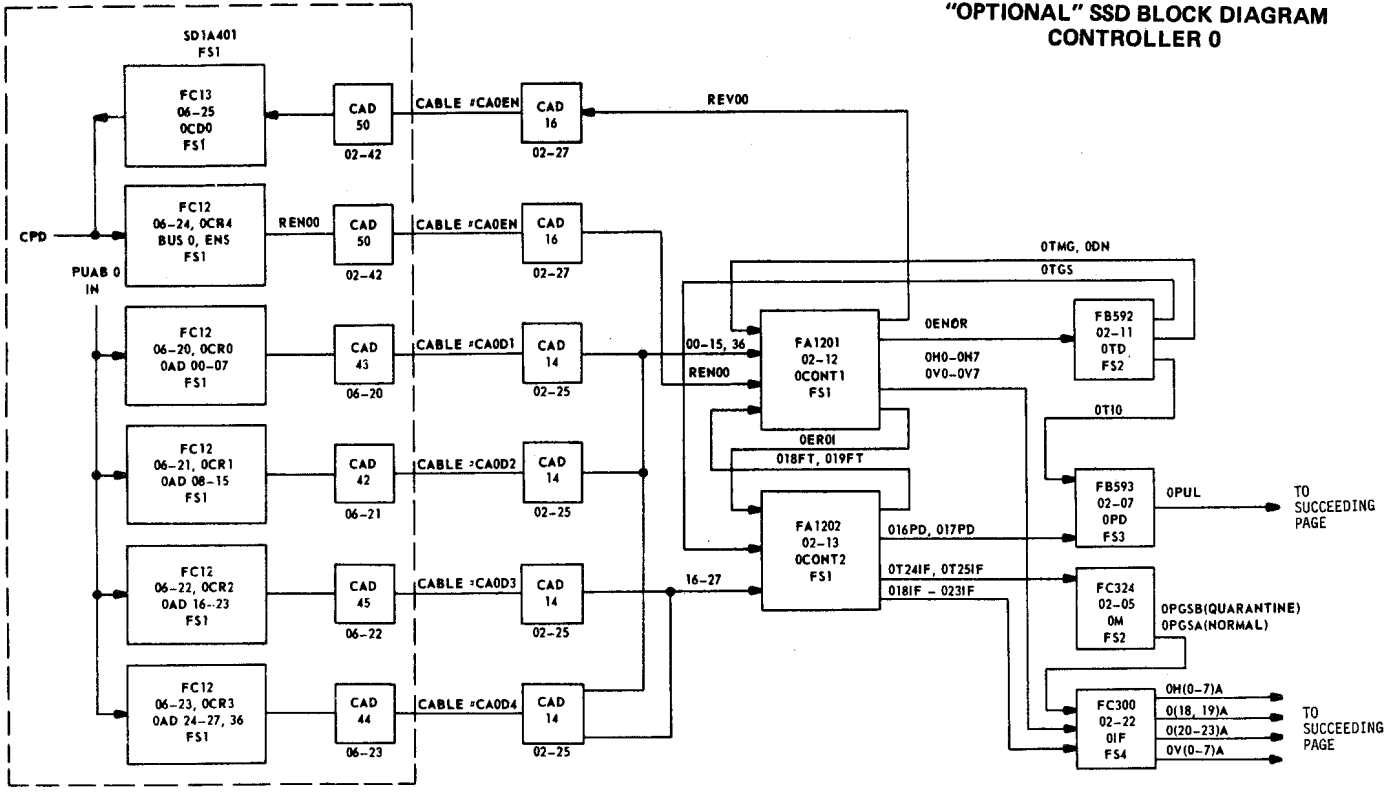
SCANNER BLOCK DIAGRAM (CONTR 0) CMT

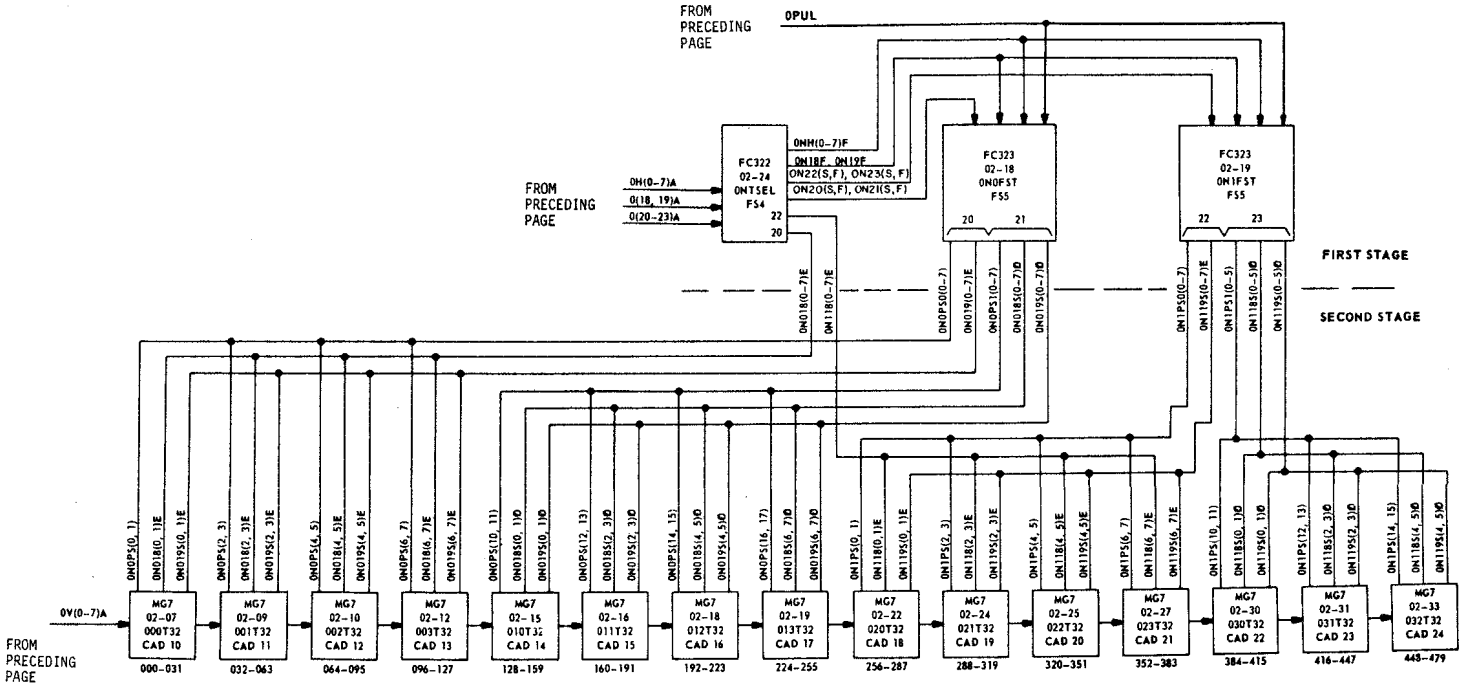

"BASIC" SSD BLOCK DIAGRAM
CONTROLLER 0
FC13
06-25
0CD0
FS1
LEV00
FC12
06-24, 0CR4
BUS 0, ENS
FS1
CPD
PUAB 0
IN
FC12
06-20, 0CR0
OAD 00-07
FS1
FC12
06-21, 0CR1
OAD 08-15
FS1
FC12
06-22, 0CR2
OAD 16-23
FS1
FC12
06-23, 0CR3
OAD 24-27, 36
FS1
(36)
00-15, 36
LEN00
16-27
FA1201
06-11
0CONT1
FS2
FA1202
06-12
0CONT2
FS2
0TMG, 0DN
0TGS
0ENOR
0H0 - 0H7
0V0 - 0V7
0ER0I
018FT, 019FT
016PD, 017PD
0T24IF, 0T25IF
018IF-023IF
FB592
06-10
OTD
FS3
0T10
FB593
06-60
OPD
FS3
0PUL
TO
SUCCEEDING
PAGE
FC324
06-04
OM
FS3
0PGSB (QUARANTINE)
0PGSA (NORMAL)
FC300
02-07
OIF
FS4
0H(0-7)A
0(18, 19)A
0(20-23)A
0V(0-7)A
TO
SUCCEEDING
PAGE



BASIC SSD, FIRST AND SECOND STAGE TRIAC

"OPTIONAL" SSD BLOCK DIAGRAM CONTROLLER 0



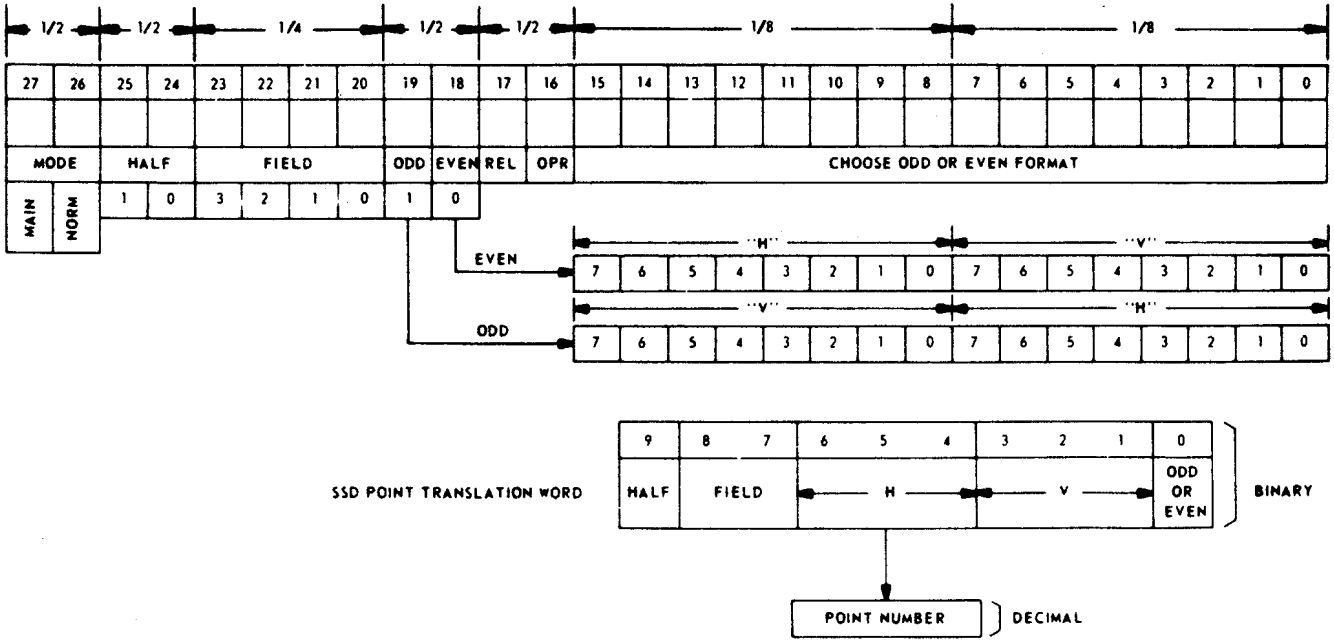


OPTIONAL SSD, FIRST AND SECOND STAGE TRIAC

LOCATION OF CMT SSD POINTS

CONTROLLER 0			CONTROLLER 1		
SD LOC	PHY LOC	PTS	SD LOC	PHY LOC	PTS
02-07	176-07	000-031	02-37	176-37	512-543
09	09	032-063	39	-39	544-575
10	10	064-095	40	-40	576-607
12	12	096-127	42	-42	608-639
15	15	128-159	45	-45	640-671
16	16	160-191	46	-46	672-703
18	18	192-223	48	-48	704-735
19	19	224-255	49	-49	736-767
22	22	256-287	52	-52	768-799
24	24	288-319	54	-54	500-831
25	25	320-351	55	-55	832-863
27	27	352-383	57	-57	864-875
30	30	384-415	60	-60	896-927
31	31	416-447	61	-61	928-959
02-33	176-33	448-479	02-63	176-63	960-991

PUAB TO SSD POINT NUMBER



TRIAC SSD POINT NUMBERS, CMT, MUT

HALF 0

FIELD	QUADRANT	ROW 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
0	0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
	1	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
	2	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
	3	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127
1	0	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159
	1	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191
	2	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223
	3	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255
2	0	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287
	1	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319
	2	320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351
	3	352	353	354	355	356	357	358	359	360	361	362	363	364	365	366	367	368	369	370	371	372	373	374	375	376	377	378	379	380	381	382	383
3	0	384	385	386	387	388	389	390	391	392	393	394	395	396	397	398	399	400	401	402	403	404	405	406	407	408	409	410	411	412	413	414	415
	1	416	417	418	419	420	421	422	423	424	425	426	427	428	429	430	431	432	433	434	435	436	437	438	439	440	441	442	443	444	445	446	447
	2	448	449	450	451	452	453	454	455	456	457	458	459	460	461	462	463	464	465	466	467	468	469	470	471	472	473	474	475	476	477	478	479
	3	480	481	482	483	484	485	486	487	488	489	490	491	492	493	494	495	496	497	498	499	500	501	502	503	504	505	506	507	508	509	510	511

HALF	FIELD	QUADRANT	ROW	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
1	0	0		512	513	514	515	516	517	518	519	520	521	522	523	524	525	526	527	528	529	530	531	532	533	534	535	536	537	538	539	540	541	542	543
		1		544	545	546	547	548	549	550	551	552	553	554	555	556	557	558	559	560	561	562	563	564	565	566	567	568	569	570	571	572	573	574	575
		2		576	577	578	579	580	581	582	583	584	585	586	587	588	589	590	591	592	593	594	595	596	597	598	599	600	601	602	603	604	605	606	607
		3		608	609	610	611	612	613	614	615	616	617	618	619	620	621	622	623	624	625	626	627	628	629	630	631	632	633	634	635	636	637	638	639
	1	0		640	641	642	643	644	645	646	647	648	649	650	651	652	653	654	655	656	657	658	659	660	661	662	663	664	665	666	667	668	669	670	671
		1		672	673	674	675	676	677	678	679	680	681	682	683	684	685	686	687	688	689	690	691	692	693	694	695	696	697	698	699	700	701	702	703
		2		704	705	706	707	708	709	710	711	712	713	714	715	716	717	718	719	720	721	722	723	724	725	726	727	728	729	730	731	732	733	734	735
		3		736	737	738	739	740	741	742	743	744	745	746	747	748	749	750	751	752	753	754	755	756	757	758	759	760	761	762	763	764	765	766	767
	2	0		768	769	770	771	772	773	774	775	776	777	778	779	780	781	782	783	784	785	786	787	788	789	790	791	792	793	794	795	796	797	798	799
		1		800	801	802	803	804	805	806	807	808	809	810	811	812	813	814	815	816	817	818	819	820	821	822	823	824	825	826	827	828	829	830	831
		2		832	833	834	835	836	837	838	839	840	841	842	843	844	845	846	847	848	849	850	851	852	853	854	855	856	857	858	859	860	861	862	863
		3		864	865	866	867	868	869	870	871	872	873	874	875	876	877	878	879	880	881	882	883	884	885	886	887	888	889	890	891	892	893	894	895
	3	0		896	897	898	899	900	901	902	903	904	905	906	907	908	909	910	911	912	913	914	915	916	917	918	919	920	921	922	923	924	925	926	927
		1		928	929	930	931	932	933	934	935	936	937	938	939	940	941	942	943	944	945	946	947	948	949	950	951	952	953	954	955	956	957	958	959
		2		960	961	962	963	964	965	966	967	968	969	970	971	972	973	974	975	976	977	978	979	980	981	982	983	984	985	986	987	988	989	990	991
		3		992	993	994	995	996	997	998	999	1000	1001	1002	1003	1004	1005	1006	1007	1008	1009	1010	1011	1012	1013	1014	1015	1016	1017	1018	1019	1020	1021	1022	1023

TRIAC SSD POINT NUMBERS, CMT, MUT

HALF	FIELD	"H" SELECT	EVEN "H" SELECT — "V" SELECT *								ODD "H" SELECT — "V" SELECT *							
			0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	0, 1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
		2, 3	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
		4, 5	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
		6, 7	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127
	1	0, 1	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159
		2, 3	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191
		4, 5	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223
		6, 7	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255
	2	0, 1	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287
		2, 3	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319
		4, 5	320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351
		6, 7	352	353	354	355	356	357	358	359	360	361	362	363	364	365	366	367	368	369	370	371	372	373	374	375	376	377	378	379	380	381	382	383
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		2, 3	416	417	418	419	420	421	422	423	424	425	426	427	428	429	430	431	432	433	434	435	436	437	438	439	440	441	442	443	444	445	446	447
		4, 5	448	449	450	451	452	453	454	455	456	457	458	459	460	461	462	463	464	465	466	467	468	469	470	471	472	473	474	475	476	477	478	479
		6, 7																															510	511

TEST MLR PTS

1	0	0, 1	512	513	514	515	516	517	518	519	520	521	522	523	524	525	526	527	528	529	530	531	532	533	534	535	536	537	538	539	540	541	542	543
		2, 3	544	545	546	547	548	549	550	551	552	553	554	555	556	557	558	559	560	561	562	563	564	565	566	567	568	569	570	571	572	573	574	575
		4, 5	576	577	578	579	580	581	582	583	584	585	586	587	588	589	590	591	592	593	594	595	596	597	598	599	600	601	602	603	604	605	606	607
		6, 7	608	609	610	611	612	613	614	615	616	617	618	619	620	621	622	623	624	625	626	627	628	629	630	631	632	633	634	635	636	637	638	639
	1	0, 1	640	641	642	643	644	645	646	647	648	649	650	651	652	653	654	655	656	657	658	659	660	661	662	663	664	665	666	667	668	669	670	671
		2, 3	672	673	674	675	676	677	678	679	680	681	682	683	684	685	686	687	688	689	690	691	692	693	694	695	696	697	698	699	700	701	702	703
		4, 5	704	705	706	707	708	709	710	711	712	713	714	715	716	717	718	719	720	721	722	723	724	725	726	727	728	729	730	731	732	733	734	735
		6, 7	736	737	738	739	740	741	742	743	744	745	746	747	748	749	750	751	752	753	754	755	756	757	758	759	760	761	762	763	764	765	766	767
	2	0, 1	768	769	770	771	772	773	774	775	776	777	778	779	780	781	782	783	784	785	786	787	788	789	790	791	792	793	794	795	796	797	798	799
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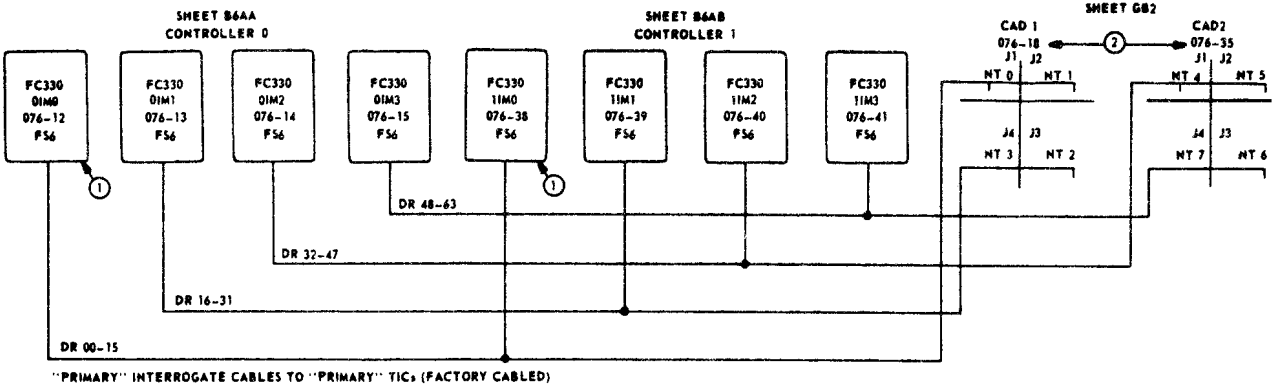
		4, 5	832	833	834	835	836	837	838	839	840	841	842	843	844	845	846	847	848	849	850	851	852	853	854	855	856	857	858	859	860	861	862	863
		6, 7	864	865	866	867	868	869	870	871	872	873	874	875	876	877	878	879	880	881	882	883	884	885	886	887	888	889	890	891	892	893	894	895
	3	0, 1	896	897	898	899	900	901	902	903	904	905	906	907	908	909	910	911	912	913	914	915	916	917	918	919	920	921	922	923	924	925	926	927
		2, 3	928	929	930	931	932	933	934	935	936	937	938	939	940	941	942	943	944	945	946	947	948	949	950	951	952	953	954	955	956	957	958	959
		4, 5	960	961	962	963	964	965	966	967	968	969	970	971	972	973	974	975	976	977	978	979	980	981	982	983	984	985	986	987	988	989	990	991
		6 7																															1022	1023

TEST MLR PTS

* EACH "V" SELECT CHOOSES AN ODD AND EVEN NUMBERED POINT.
BIT 18 = 1 CHOOSE EVEN POINT NUMBER
BIT 19 = 1 CHOOSE ODD POINT NUMBER

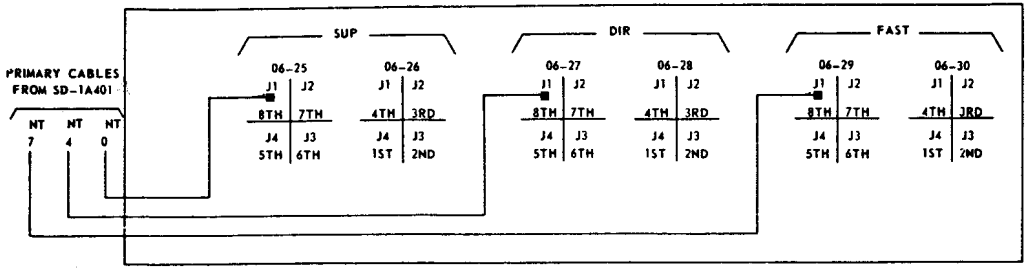


For a group of 8 unassigned scanner rows, 942E connector replaces "NT x" cable.

(1) (2) SD location given as unit location (e.g., 02-12, 02-35).

(3) Primary cable plugged into TIC assigned highest row number for that cable (e.g., 7, 15, 23, etc.).

CONTROLLER INTERROGATE WIRING
SD 1A401 - Basic SSD



CONNECTORS FOR PARTIALLY UNASSIGNED ROWS

942AH	1 UNASGND ROW(S)
AJ	2
AK	3
AL	4
AM	5
AN	6
AP	7

PRIMARY TIC INTERROGATE LOOP EXAMPLE

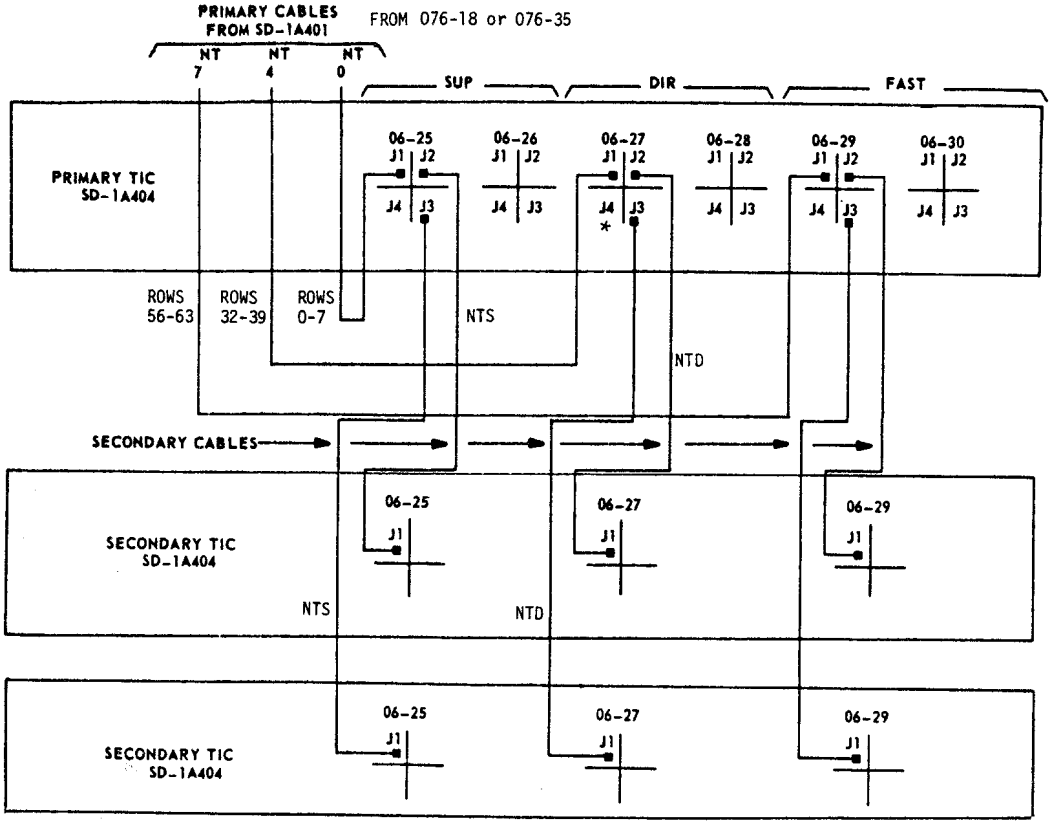
The primary TIC shows the NT 4 cable plugged into connector 06-27, J1. Since NT 4 cable is Rows 32-39, the connectors would be as follows:

Quadrant to row number is as follows:

8TH ROW	7TH ROW	4TH ROW	3RD ROW
7TH	6TH	3RD	2ND
6TH	5TH	2ND	1ST
5TH	4TH	1ST	
4TH	3RD		
3RD	2ND		
J1 2ND	1ST J2	J1	J2
310 1ST	110	310	110
5TH ROW	6TH ROW	1ST ROW	2ND ROW
4TH	5TH		1ST
3RD	4TH		
2ND	3RD		
1ST	2ND		
J4	1ST J3	J4	J3
300	100	300	100

ROW 39	ROW 38	ROW 35	ROW 34
38	37	34	33
37	36	33	32
36	35	32	
35	34		
34	33		
33	32		
32			
ROW 36	ROW 37	ROW 32	ROW 33
35	36		32
34	35		
33	34		
32	33		
	32		

PRIMARY/SECONDARY TIC INTERROGATE LOOP EXAMPLE



TIC LOCATIONS, CABLING	
TIC 7(17)	72(172)-25 TO 30
6(16)	64(164)
5(15)	56(156)
4(14)	48(148)
3(13)	40(140)
2(12)	32(132)
1(11)	24(124)
0(10)	16(116)

CA NTS FROM 06-25, J2 TO 06-25, J1; 7TH ROW ASSIGNED
NTS FROM 06-25, J3 TO 06-25, J1; 1ST TO 6TH ASSIGNED

CA NTD FROM 06-27, J2 TO 06-27, J1; 7TH ROW ASSIGNED
NTD FROM 06-27, J3 TO 06-27, J1; 6TH ROW ASSIGNED
*942AM CONNECTOR ON J4 ; 1ST TO 5TH ROW UNASSIGNED

COMBINED MISCELLANEOUS TRUNK FRAME

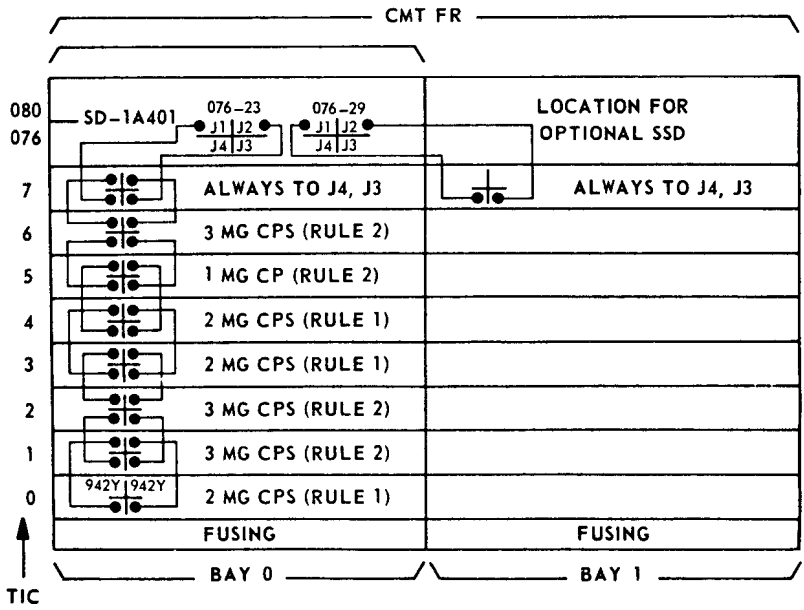
SD 1A401 - Basic SSD
SD 1A402 - Optional SSD

READOUT LOOP CABLE RULES

1. If the number of rows (MG CP's) is even on a TIC, the paddleboard is plugged into the other quadrant from where the cable is started.

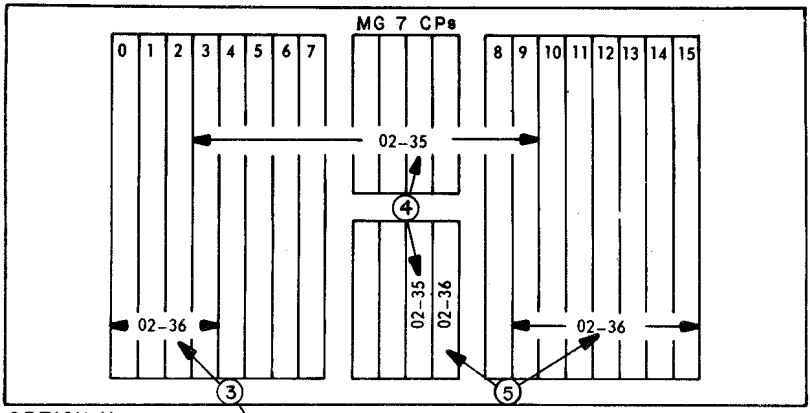
2. If there is an odd number of rows (MG CP's) on a TIC, the paddleboard is plugged into the same quadrant from where the cable is started.

EXAMPLE OF READOUT LOOP CABLING

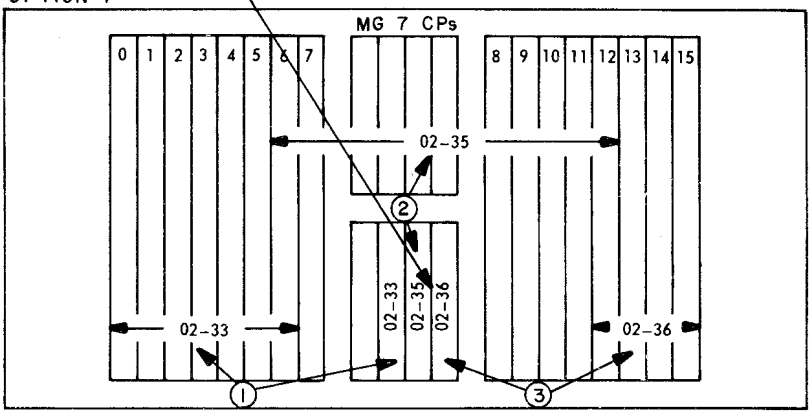


TIC VERTICAL FILES

OPTION X



OPTION Y



Each VF requires 5 points (5 MLRs).
16 VFs in TIC = 80 pts.
Each MG7 CP provides 32 pts.

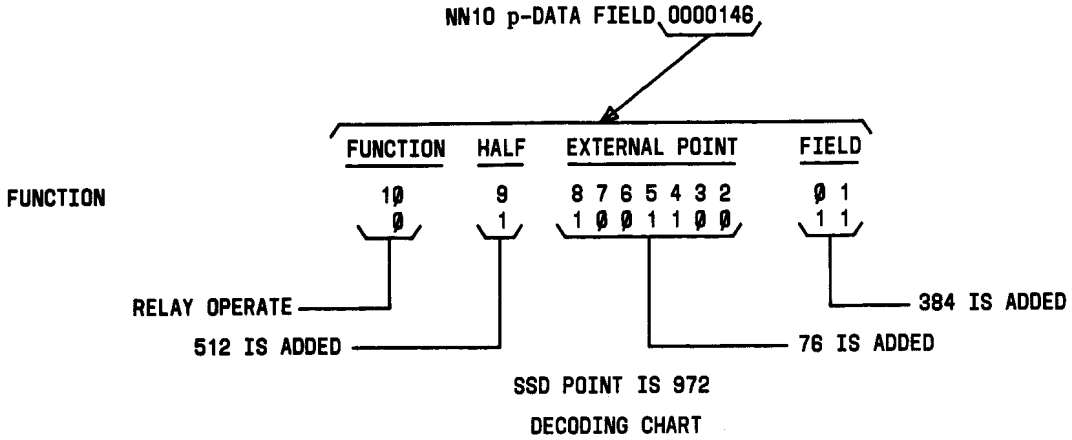
Examples of VF to MG7 CP association:

Option Y

1. 02-33 (32 pts.) services VF00-05 plus 2 pts. in VF06.
2. 02-35 (32 pts.) services 3 pts. in VF06, VF07-11, 4 pts. in VF12.
3. 02-36 (32 pts.) services 1 pt. in VF12, VF13-15, and donates 16 pts. to next TIC-VF00-02 and 1 pt. in VF03.

Option X

3. Preceding TIC MG7 at 02-36 services VF00-02 plus 1 pt. in VF03.
4. 02-35 (32 pts.) services 4 pts. in VF03, VF04-08, plus 3 pts. in VF09.
5. 02-06 (32 pts.) services 2 pts. in VF09 and VF10-15.



FIELD

1 : 00

2 : 01

3 : 10

4 : 11

EXTERNAL POINT

0 : 000-511

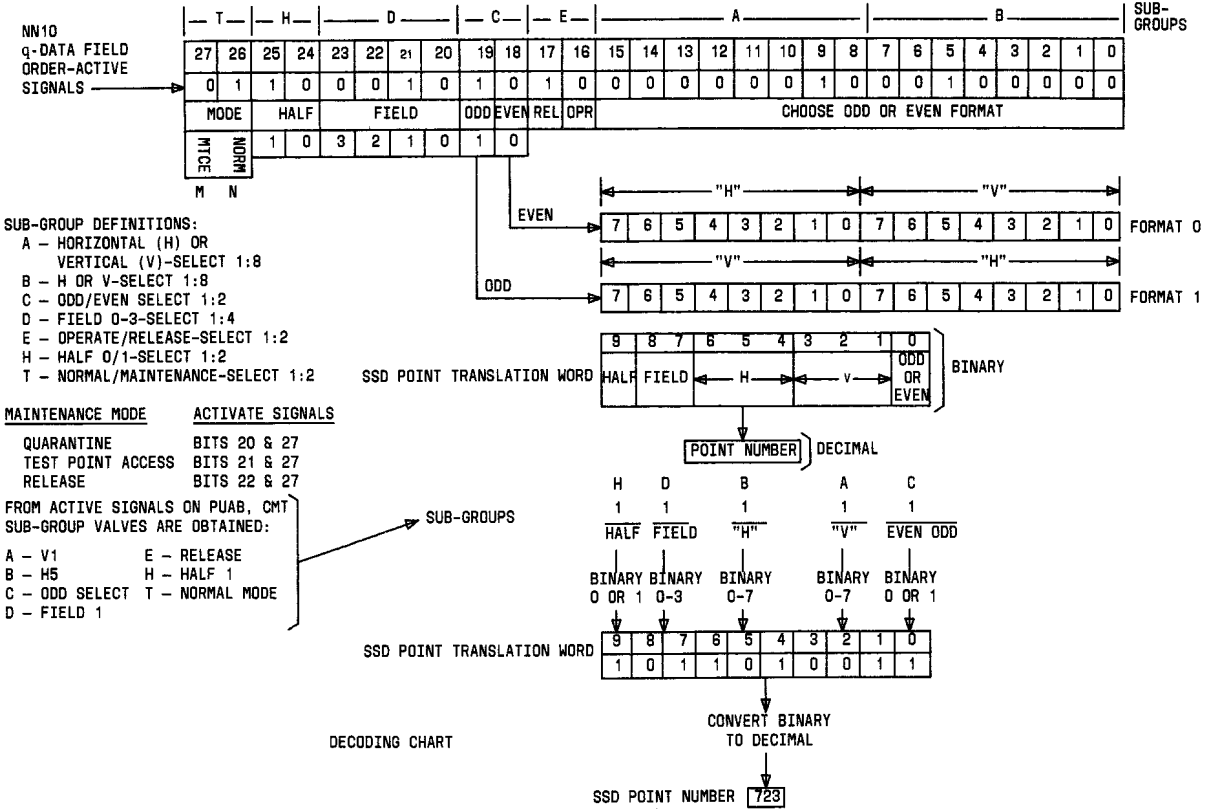
1 : 512-1024

FUNCTION

0 : RELAY OPERATE

1 : RELAY RELEASE

DETERMINING SD OR SSD POINT FROM p-DATA FIELD



EXAMPLE OF DETERMINING FAILING SIGNAL DISTRIBUTOR POINT USING q-DATA FIELD OF NN10 MESSAGE

ERROR PATTERN SENSITIVITY – SD CONTROLLER 081

TROUBLE CONDITIONS	SUSPECTED FAULTY CIRCUIT PACK TYPE IN REPLACEMENT ORDER
Multiple SD point failures in all Trunk Interconnect (TIC) Units in Bay 0 or 1	FC300, FC322, FC323
Multiple SD point failures in single TIC unit	MG7, FC322, FC323
One SD controller (may have diagnostic response DR02 printed)	FC300, FA1201, FA1202
Single SD point failure in one TIC	MG7

SD POINT TO TRIAC SELECT CIRCUIT PACKS

SD POINT	INTERFACE CKT-FC300	TRIAC SELECT CKT – FC322	FIRST STAGE CKT – FC323
000 – 127	(0) 02-07	(0) 02-09	(0) 02-03
128 – 255	(0) 02-07	(0) 02-09	(0) 02-03
256 – 383	(0) 02-07	(0) 02-09	(0) 02-04
384 – 479	(0) 02-07	(0) 02-09	(0) 02-04
512 – 639	(1) 02-46	(1) 02-45	(1) 02-50
640 – 767	(1) 02-46	(1) 02-45	(1) 02-50
768 – 895	(1) 02-46	(1) 02-45	(1) 02-49
896 – 991	(1) 02-46	(1) 02-45	(1) 02-49

SSD POINT TO TRIAC SELECT CIRCUIT PACKS

SSD POINT	INTERFACE CKT-FC300	TRIAC SELECT CKT – FC322	FIRST STAGE CKT – FC323
000 – 127	(0) 02-22	(0) 02-24	(0) 02-18
128 – 255	(0) 02-22	(0) 02-24	(0) 02-18
256 – 383	(0) 02-22	(0) 02-24	(0) 02-19
384 – 479	(0) 02-22	(0) 02-24	(0) 02-19
512 – 639	(1) 02-35	(1) 02-31	(1) 02-39
640 – 767	(1) 02-35	(1) 02-31	(1) 02-39
768 – 895	(1) 02-35	(1) 02-31	(1) 02-38
896 – 991	(1) 02-35	(1) 02-31	(1) 02-38

TIC SECOND STAGE TRIAC CIRCUIT (MG7) – SD POINTS AND LOCATION

TIC SD*	SD POINTS	MG7	SD OPTION(S)	TIC SD*	SD POINTS	MG7	SD OPTION(S)
SD-1A404	000 - 031	02 - 33P	Y	SD-1A412	000 - 031	02 - 33P	Z
	032 - 063	02 - 35	X and Y		032 - 063	02 - 35	Z
	064 - 095	02 - 36P	X and Y		064 - 095	02 - 36P	Z
SD-1A407	000 - 031	02 - 33P	Y	SD-1A413	000 - 031	02 - 33P	Z
	032 - 063	02 - 35	Y and Z		032 - 063	02 - 35	Z
	064 - 095	02 - 36P	Y and Z		064 - 095	02 - 36P	Z
SD-1A408	000 - 031	02 - 33P	Z	SD-1A414	000 - 031	02 - 33P	Z
	032 - 063	02 - 35	Z		032 - 063	02 - 35	Z
	064 - 095	02 - 36P	Z		064 - 095	02 - 36P	Z
	096 - 127	02 - 38	Z	SD-1A464	000 - 031	02 - 33P	Z
SD-1A409	000 - 031	02 - 35	Z		032 - 063	02 - 35	Z
	032 - 063	02 - 36P	Z		064 - 095	02 - 36P	Z
SD-1A410†	000 - 095	–	–	SD-1A489	096 - 127	02 - 38	Z
SD-1A411	000 - 031	02 - 33P	Z		000 - 031	02 - 35	Y
	032 - 063	02 - 35	Z		032 - 063	02 - 36P	W and Y
	064 - 095	02 - 36P	Z	SD-1A610	000 - 031	02 - 33P	Y
	096 - 127	02 - 38	Z		032 - 063	02 - 35	Y
	128 - 159	06 - 33P	Z		064 - 095	02 - 36P	Y

*All Trunk interconnection circuits (TIC's) have optional wiring arrangements where part or all SSD points are assigned to MG7 circuit pack(s) external to associated TIC
†SD points 000-095 are assigned from MG7 circuit packs external to TIC

MATRIX CKT – MG7 LOCATION*

SSD POINT	2ND STG TRIAC-MG7	SSD POINT	2ND STG TRIAC-MG7
000-031	02-07P	512-543	02-37P
032-063	02-09P	544-576	02-39
064-095	02-10P	576-607	02-40P
096-127	02-12	608-639	02-42
128-159	02-15	640-671	02-45
160-191	02-16P	672-703	02-46P
192-223	02-18	704-735	02-48
224-255	02-19P	736-767	02-49P
256-287	02-22P	768-799	02-52P
288-319	02-24	800-831	02-54
320-351	02-25P	832-863	02-55P
352-383	02-27	864-895	02-57
384-415	02-30	896-927	02-60
416-447	02-31P	928-959	02-61P
448-479	02-33	960-991	02-63

* SD-1A452 – 960 SSD Points

MATRIX CKT – MG7 LOCATION*

SSD POINT	2ND STG TRIAC-MG7	SSD POINT	2ND STG TRIAC-MG7
512-543	02-37P	768-799	02-52P
544-576	02-39	800-831	02-54
576-607	02-40P	832-863	02-55P
608-639	02-42	864-895	02-57
640-671	02-45	896-927	02-60
672-703	02-46P	928-959	02-61P
704-735	02-48	960-991	02-63
736-767	02-49P	–	–

* SD-1A403 – 480 SSD Points

CP TYPE REPLACEMENTS

CP TYPE	CORRESPONDING* REPLACEMENT TYPE
FA1202	FA1810
FB593	FB698
FC300	FC661
FC322	FC664
FC323	FC665
FC324	FC666
MG7	MG7B

* Generics 1E7/1AE7 and later, with improved diagnostic test (IMD)

CMT SIGNAL DISTRIBUTORS

SCAN POINT	SD-1A401		SD-1A402*		CP TYPE
	CKT 0	CKT 1	CKT 0	CKT 1	
DF	80-06	80-06	80-07	80-47	FB698
	80-12	80-53	80-13	80-40	FA1810
	80-04	80-61	80-05	80-48	FC666
	80-10	80-55	80-11	80-42	FB592
FS0	76-09	76-45	80-24	80-31	FC664
	76-03	76-50	80-18	80-39	FC664
	76-04	76-49	80-19	80-38	FC665
FS1	76-07	76-46	80-22	80-35	FC661
	80-04	80-61	80-05	80-48	FC666
	80-12	80-53	80-13	80-40	FA1810
PD0	76-09	76-45	80-24	80-31	FC664
	76-03	76-50	80-18	80-39	FC665
	80-06	80-60	80-07	80-47	FB698
	76-07	76-46	80-22	80-35	FC661
PD1	80-04	80-61	80-05	80-48	FC666
	80-06	80-60	80-07	80-47	FB698
	76-03	76-50	80-18	80-39	FC665
	76-09	76-45	80-24	80-31	FC664
	76-04	76-49	80-19	80-38	FC665

* Supplementary signal distributor (SSD) located in Bay 1

TIC SCANNER MATRIX - FERROD SENSOR LOCATION (TYPE)

TIC/TPC SD	OPTION	CKT 1*	CKT 2*	CKT 3*	CKT 4*
SD 1A404	U	06-35(MG4)	06-36P(MG5)	06-38(MG5)	–
	V	06-35(MG6)	06-36P(MG6)	06-30(MG5)	–
	Z	06-35(MG4)	06-36P(MG5)	06-38(MG5)	–
SD 1A407	–	06-35(MG5)	06-36P(MG5)	06-38(MG5)	–
SD 1A408	–	06-33(MG4)	06-35(MG5)	06-36P(MG4)	06-38(MG5)
SD 1A409	–	06-35(MG5)	06-36P(MG5)	06-38(MG5)	–
SD 1A410	–	06-33(MG8)	06-35(MG5)	06-36P(MG5)	06-38(MG5)
SD 1A411	–	06-35(MG5)	06-36P(MG5)	06-38(MG5)	–
SD 1A412	–	06-33(MG4)	06-35(MG4)	–	–
SD 1A413	–	06-33(MG9)	06-35(MG9)	06-36P(MG9)	06-38(MG9)
SD 1A414	V	06-33(MG4)	06-35(MG8)	06-36P(MG4)	06-38(MG8)
	W	06-33(MG4)	06-35(MG5)	06-36P(MG4)	06-38(MG5)
SD 1A464	–	06-33(MG1)	06-35(MG1)	06-36P(MG2)	06-38(MG3)
SD 1A465	Y	06-33(MG5)	06-35(MG5)	06-36P(MG5)	06-38(MG5)
	Z	02-33P(MG5)	02-35(MG5)	–	–
SD 1A489	–	02-33P(MG5)	02-38(MG5)	–	–

* Each circuit pack provides ferrod readouts for 16 scan points which are assigned per SD-1A272

MATRIX CIRCUIT (SD-1A403) – 256 SCAN POINTS MATRIX†

FERROD SENSORS – EVEN ROWS			FERROD SENSORS – ODD ROWS	
LOCATION	OPTION Y*	OPTION Z*	LOCATION	OPTION Y & Z*
02 -07P	MG4	MG5	02 -09	MG5
02 -10P	MG4	MG5	02 -12	MG5
02 -15	MG4	MG5	02 -16P	MG5
02 -18	MG4	MG5	02 -19P	MG5
02 -22P	MG4	MG5	02 -24	MG5
02 -25P	MG4	MG5	02 -27	MG5
02 -30P	MG4	MG5	02 -31P	MG5
02 -33P	MG4	MG5	02 -34P	MG5

* Options are: MG4 Ferrod Battery & Ground
MG5 Looped Ferrods

† Each circuit pack provides ferrod readouts for 16 Scan points which are assigned per SD-1A272

Section 3

MISCELLANEOUS TRUNK (MT)/UNIVERSAL TRUNK (UT) (J1A033C/J1A032A)

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Supporting Documentation

MISCELLANEOUS TRUNK

SD-1A129
CD-1A129
ED-1A217-13
or
J1A033F
SD-1A129
CD-1A129
ED-1A217-13
ED-1A217-14
or
J1A033E
SD-1A247
CD-1A247
TLM-1A247
ED-1A217-12
SD-1A119 Pheripheral Unit BUS
SD-1A129 Miscellaneous CKT
TLM-1A119 Pheripheral Unit BUS
PK-1A028 Remreed NTWK Raw Data Doc
or
J1A033G
SD-1A301
PK-1A059 AIOD CKT Raw Data
TLM-1A301
ED-1A217-15
CD-1A301
or
J1A033R ED-1A217-23
or
J1A033S ED-1A217-24
or
J1A033T ED-1A217-25
or
J1A033U ED-1A217-30
or
J1A033V ED-1A217-31
or
J1A033W ED-1A217-26
or
J1A033X ED-1A217-27
or

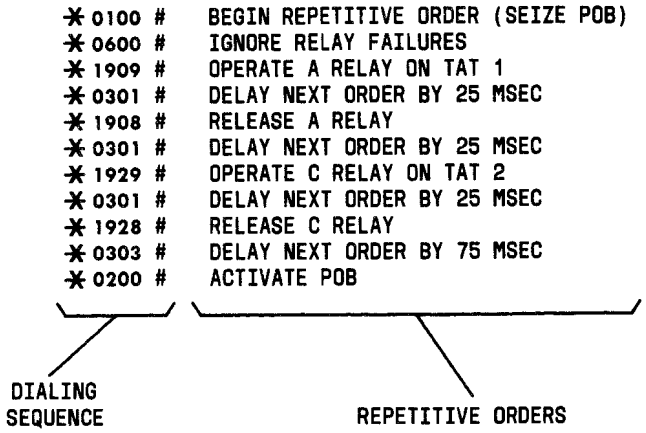
MISCELLANEOUS TRUNK (Contd)

J1A033H ED-1A217-16
or
J1A033J ED-1A217-17
or
J1A033K ED-1A217-18
or
J1A033L ED-1A217-19
or
J1A033M ED-1A217-20
or
J1A033N ED-1A217-21
or
J1A033P ED-1A217-22
or
J1A033Y ED-1A217-28
or
J1A033Z ED-1A217-29

UNIVERSAL TRUNK

PD-1A028
PK-1A028
TLM-1A216
CD-1A216
SD-1A216
CD-1A247
SD-1A247
CD-1A113
SD-1A113
CD-1A127
SD-1A127
CD-1A128
SD-1A128
PF-1A028
TOP-231-051-001

Following documents are for MT and UT:
SD-1A341 Miscellaneous Circuit
CD-1A341 Miscellaneous Circuit
BSP-820-031-150



CODE EXPLANATIONS

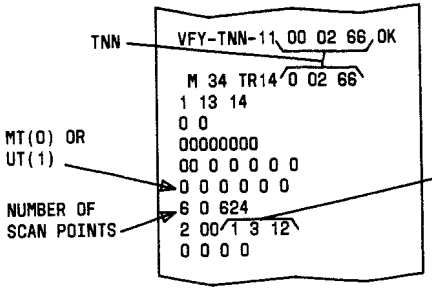
CODE	FUNCTION	ACTIVITY/COMMAND
0100	BEGIN	SAVE DATA UP TO ACTIVATE CODE FOR USE IN REPETITIVE ORDER SEQUENCE
0200	ACTIVATE	USE DATA SAVED AND ACT UPON IT REPETITIVELY
03AA	SPECIFIES NUMBER OF 25 MSEC DELAY INTERVALS PER ORDER PERIODS	AA = NUMBER OF 25-MSEC DELAYS
0500	STOP	DEACTIVATE PERIPHERAL ORDER BUFFER (POB) ACCESS
*0600	IGNORE RELAY FAILURES	WHEN RELAY FAILURE OCCURS DURING POB ORDER, DO NOT STOP REPETITIVE ACTIONS

* THIS CODE MUST BE KEYED BETWEEN BEGIN AND ACTIVATE CODES OR REPETITIVE ORDER SEQUENCING WILL BE TERMINATED

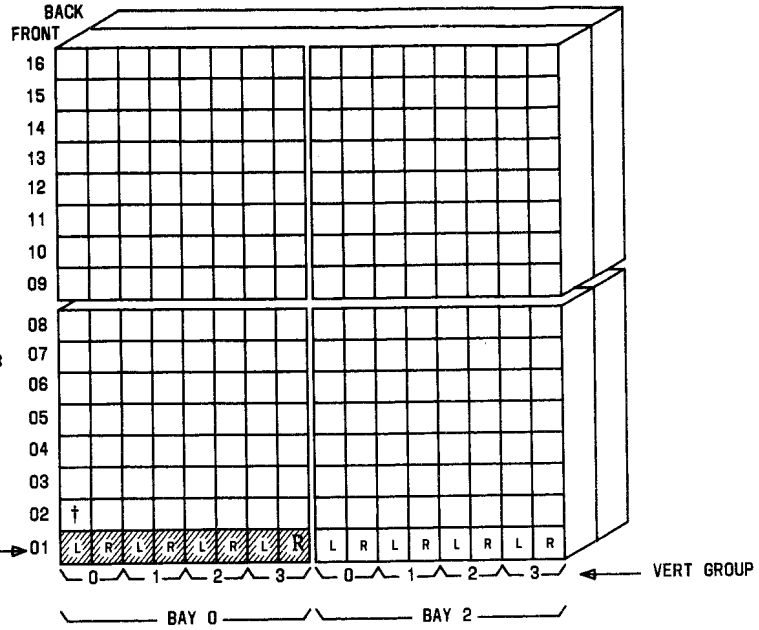
EXAMPLE OF REPETITIVE ORDERS TO OPERATE AND RELEASE A AND C RELAYS ON TAT 1 GENERIC 1E6/1AE6

SIGNAL DISTRIBUTOR (SD) ERROR PATTERNS

FAILURE CHARACTERISTICS	POSSIBLE CAUSE OF FAILURE
Phase 1 STF	• MAC timed out resulting in invalid test • Maintenance interrupt or fuse alarm problem • Mate or test controller not in normal mode or cannot be placed in test point access mode
Phases 2 and 3 – STF (SD Controller 0) Phases 4 and 5 – STF (SD Controller 1)	Diagnostic bus scan points report SD controller fault as follows: 1. States of PU address buffer registers group checks: Scan points • AR — Horizontal Select • BR — Vertical Select • DR — Relay Select • AP — Apex Pulser path 2. Controller Modes: Scan points • F, S, T — Test point access, quarantine, test, normal or power off • DF — Idle or busy condition
Phases 2 and 4 – STF * (PU Address Bus 0) Phases 3 and 5 – STF * (PU Address Bus 1)	PU address bus order fails to enable SD controller or enable verify is not received at CPD enable address: • Cable driver(s), cable receiver(s) or bus transformer
Phase 6 STF	• Live order or test vertical tests not performed but all other tests passed • PU address bus problem not clear • SD controller mate out of service
* Multiple frames failing on same bus fanout indicates PU address bus trouble	



A – TR14 MESSAGE



* 8 SHADED PAIRS OF FERRODS ARE SCANNED SIMULTANEOUSLY

† L = TYPE IC R= TYPE ID

	H/M	(0,2) BAY	(01-16) HOR ROW		(0-3) VERT GRP	FRONT (0) OR BACK (1)	LEFT (L) OR RIGHT (R)
FERROD DESIGNATION							

B – SD-1A215 UTSC FERROD DESIGNATION

EXAMPLE OF IDENTIFYING MISCELLANEOUS TRUNK (MT) OR UNIVERSAL TRUNK (UT) SCAN POINT

SCANNER ERROR PATTERNS

FAILURE CHARACTERISTICS	POSSIBLE CAUSE OF FAILURE
Phases 1 & 3 – STF	Scanner controller 0
Phases 2 & 4 – STF	Scanner controller 1
Phases 1 & 4 – STF	• PU address bus 0 • Scanner bus 0
Phases 2 & 3 – STF	• PU address bus 1 • Scanner bus 1
Phases 1 through 4 – STF	Open ferrod sensor interrogate winding
*Scanner answer reply AN00-15, or scanner ASW, AN16	• Faulty secondary winding of test scanner transformer • Open ferrod readout loop • Faulty detector – amplifier • Faulty cable driver – output circuit
*Multiple failures in AN00-15 & ASW-S	• Delay and pulse shaper • Maintenance circuits • No continuity through primary windings of scanner test transformer
* This failure may be reported by F-level interrupt TTY message	

TEST 1, SCANNER ANSWER BUS
ACTIVE STATE WITH MAINTENANCE BIT AD16 SET TO 1

PHASE & WORD	CP LOCATION (TYPE)	ANSWER BUS*
Phase 1 Word 1	34-40 (A147), 32-06 (A49), 34-30 (A1038), 32-14 (A1051), 34-36 (A1036), 34-28 (A146)	32-07 (A51) 32-08 (A51)
Phase 2 Word 1	34-42 (A147), 32-12 (A49), 34-34, (A1038), 32-16 (A1051), 34-38 (A1035), 34-32 (A146)	32-09 (A51) 32-10 (A51)
Phase 3 Word 1	34-40 (A147), 32-06 (A49), 34-30 (A1038) 32-14 (A1051), 34-36, (A1035), 34-29 (A146)	32-09 (A51) 32-10 (A51)
Phase 4	34-42 (A147), 32-12 (A49), 34-34 (A1038), 32-16 (A1051), 34-38 (A1035), 34-32 (A146)	32-07 (A51) 32-08 (A51)

* Failure Scanner ASW results in F-Level Interrupt TTY message. All scanner answer AN00-15 are set to 1

TEST 2A, SCANNER ANSWER BUS
QUIENSCENT STATE WITH INVALID ADDRESS

PHASE, WORD	CP LOCATION (TYPE)	COMMENTS
Phase 1 or 3 Word 2	34-36 (A1035), 34-30 (A1038), 34-40 (A147), 32-18 (A48), 30-18 (A56), 32-14 (A1051)	Check of scanner to recognize invalid address or inhibit output to answer bus
Phase 2 or 4 Word 2	34-38 (A1035), 34-34 (A1038), 34-42 (A147), 32-26 (A48), 30-40 (A56), 32-16 (A1051)	Check of scanner to recognize invalid address or inhibit output to answer bus

TEST 2B, SCANNER ENABLE/ENABLE VERIFY
OPERATION WORD 2, BIT 22

PHASE, WORD	LOCATION (TYPE)	COMMENTS
Phase 1 or 3	34-36 (A1035), 34-10 (A21)	Check of scanner to recognize enable signal and to verify by replying to CPD
Phase 2 or 4	34-38 (A1035), 34-16 (A21)	Check of scanner to recognize enable signal and to verify by replying to CPD

TEST 3, SCANNER ADDRESS PARITY OPERATIONS USING INVALID ADDRESSES

PHASE, WORD	* BITS	CP LOCATION (TYPE)	EXPLANATIONS
Phase 1 or 3 Word 2	17-21	34-30 (A1038), 34-28 (A146), 34-10 (A21)	Check of scanner to verify correct parity and inhibit ASWS answer to CC when parity is incorrect
Phase 2 or 4 Word 2	17-21	34-34 (A1038), 34-32 (A146), 34-16 (A21)	Check of scanner to verify correct parity and inhibit ASWS answer to CC when parity is incorrect

* Addresses are as follows:
Bit 17 – 8 & 1, 8 & 0 Bit 19 – 8 & 1, 8 & 2 Bit 21 – 8 & 2, 8 & 1
Bit 18 – 8 & 1, 8 & 1 Bit 20 – 8 & 0, 8 & 1

TEST 4, SCANNER ROW READOUT AND ANSWER OPERATIONS – PHASES 1 THROUGH 4*

REPLY WORD/ BIT	ROW	ACCESS CIRCUIT – CP (A048)		†CORE MATRIX – CP (A037)		ASWS TRANSFORMER CP (A052)	PU ADDRESS
		CIRCUIT 0	CIRCUIT 1	CORE 0	CORE 1		
3/0	0	32-22, 32-18	32-30, 32-26	30-22	30-24	30-42	AD0 & 8
3/1	8	32-22, 32-18	32-30, 32-26	30-22	30-24	30-42	AD0 & 9
3/2	16	32-22, 32-18	32-30, 32-26	30-21	30-23	32-42	AD0 & 10
3/3	24	32-22, 32-18	32-30, 32-26	30-21	30-23	32-42	AD0 & 11
3/4	32	32-24, 32-18	32-32, 32-26	30-30	30-32	32-44	AD0 & 12
3/5	40	32-24, 32-18	32-32, 32-26	30-30	30-32	32-44	AD0 & 13
3/6	48	32-24, 32-18	32-32, 32-26	30-29	30-31	30-44	AD0 & 14
3/7	56	32-24, 32-18	32-32, 32-26	30-29	30-31	30-44	AD0 & 15
3/8	1	32-22, 32-20	32-30, 32-28	30-26	30-28	30-46	AD1 & 8
3/9	9	32-22, 32-20	32-30, 32-28	30-26	30-28	30-46	AD1 & 9
3/10	17	32-22, 32-20	32-30, 32-28	30-25	30-27	32-46	AD1 & 10

See footnotes at end of table

TEST 4, SCANNER ROW READOUT AND ANSWER OPERATIONS – PHASES 1 THROUGH 4* (Contd)

REPLY WORD/ BIT	ROW	ACCESS CIRCUIT – CP (A048)		†CORE MATRIX – CP (A037)		ASWS TRANSFORMER CP (A052)	PU ADDRESS
		CIRCUIT 0	CIRCUIT 1	CORE 0	CORE 1		
3/11	25	32-22, 32-20	32-30, 32-28	30-25	30-27	32-46	AD1 & 11
3/12	33	32-24, 32-20	32-32, 32-28	30-34	30-36	32-48	AD1 & 12
3/13	41	32-24, 32-20	32-32, 32-28	30-34	30-36	32-48	AD1 & 13
3/14	49	32-24, 32-20	32-32, 32-28	30-33	30-35	30-48	AD1 & 14
3/15	57	32-24, 32-20	32-32, 32-28	30-33	30-35	30-48	AD1 & 15
4/0	2	32-22, 32-18	32-30, 32-26	30-22	30-24	30-42	AD2 & 8
4/1	10	32-22, 32-18	32-30, 32-26	30-22	30-24	30-42	AD2 & 9
4/2	18	32-22, 32-18	32-30, 32-26	30-21	30-23	32-42	AD2 & 10
4/3	26	32-22, 32-18	32-30, 32-26	30-21	30-23	32-42	AD2 & 11
4/4	34	32-24, 32-18	32-32, 32-26	30-30	30-32	32-44	AD2 & 12
4/5	42	32-24, 32-18	32-32, 32-26	30-30	30-32	32-44	AD2 & 13
4/6	50	32-24, 32-18	32-32, 32-26	30-29	30-31	30-44	AD2 & 14
4/7	58	32-24, 32-18	32-32, 32-26	30-29	30-31	30-44	AD2 & 15
4/8	3	32-22, 32-20	32-30, 32-28	30-26	30-28	30-46	AD3 & 8
4/9	11	32-22, 32-20	32-30, 32-28	30-26	30-28	30-46	AD3 & 9
4/10	19	32-22, 32-20	32-30, 32-28	30-25	30-27	32-46	AD3 & 10
4/11	27	32-22, 32-20	32-30, 32-28	30-25	30-27	32-46	AD3 & 11
4/12	35	32-24, 32-20	32-32, 32-28	30-34	30-36	32-48	AD3 & 12
4/13	43	32-24, 32-20	32-32, 32-28	30-34	30-36	32-48	AD3 & 13
4/14	51	32-24, 32-20	32-32, 32-28	30-33	30-35	30-48	AD3 & 14
4/15	59	32-24, 32-20	32-32, 32-28	30-33	30-35	30-48	AD3 & 15
5/0	4	32-22, 32-18	32-30, 32-26	30-22	30-24	33-42	AD4 & 8

See footnotes at end of table

TEST 4, SCANNER ROW READOUT AND ANSWER OPERATIONS – PHASES 1 THROUGH 4* (Contd)

REPLY WORD/ BIT	ROW	ACCESS CIRCUIT – CP (A048)		†CORE MATRIX – CP (A037)		ASWS TRANSFORMER CP (A052)	PU ADDRESS
		CIRCUIT 0	CIRCUIT 1	CORE 0	CORE 1		
5/1	12	32-22, 32-18	32-30, 32-26	30-22	30-24	30-42	AD4 & 9
5/2	20	32-22, 32-18	32-30, 32-26	30-21	30-23	32-42	AD4 & 10
5/3	28	32-22, 32-18	32-30, 32-26	30-21	30-23	32-42	AD4 & 11
5/4	36	32-24, 32-18	32-32, 32-26	30-30	30-32	32-44	AD4 & 12
5/5	44	32-24, 32-18	32-32, 32-26	30-30	30-32	32-44	AD4 & 13
5/6	52	32-24, 32-18	32-32, 32-26	30-29	30-31	30-44	AD4 & 14
5/7	60	32-24, 32-18	32-32, 32-26	30-29	30-31	30-44	AD4 & 15
5/8	5	32-22, 32-20	32-30, 32-28	30-26	30-28	30-46	AD5 & 8
5/9	13	32-22, 32-20	32-30, 32-28	30-26	30-28	30-46	AD5 & 9
5/10	21	32-22, 32-20	32-30, 32-28	30-25	30-27	32-46	AD5 & 10
5/11	29	32-22, 32-20	32-30, 32-28	30-25	30-27	32-46	AD5 & 11
5/12	37	32-24, 32-20	32-32, 32-28	30-34	30-36	32-48	AD5 & 12
5/13	45	32-24, 32-20	32-32, 32-28	30-34	30-36	32-48	AD5 & 13
5/14	53	32-24, 32-20	32-32, 32-28	30-33	30-35	30-48	AD5 & 14
5/15	61	32-24, 32-20	32-32, 32-28	30-33	30-35	30-48	AD5 & 15
6/0	6	32-22, 32-18	32-30, 32-26	30-22	30-24	30-42	AD6 & 8
6/1	14	32-22, 32-18	32-30, 32-26	30-22	30-24	30-42	AD6 & 9
6/2	22	32-22, 32-18	32-30, 32-26	30-21	30-23	32-42	AD6 & 10
6/3	30	32-22, 32-18	32-30, 32-26	30-21	30-23	32-42	AD6 & 11
6/4	38	32-24, 32-18	32-32, 32-26	30-30	30-32	32-44	AD6 & 12
6/5	46	32-24, 32-18	32-32, 32-26	30-30	30-32	32-44	AD6 & 13
6/6	54	32-24, 32-18	32-32, 32-26	30-29	30-31	30-44	AD6 & 14

See footnotes at end of table

TEST 4, SCANNER ROW READOUT AND ANSWER OPERATIONS – PHASES 1 THROUGH 4* (Contd)

REPLY WORD/ BIT	ROW	ACCESS CIRCUIT – CP (A048)		†CORE MATRIX – CP (A037)		ASWS TRANSFORMER CP (A052)	PU ADDRESS
		CIRCUIT 0	CIRCUIT 1	CORE 0	CORE 1		
6/7	62	32-24, 32-18	32-32, 32-26	30-29	30-31	30-44	AD6 & 15
6/8	7	32-22, 32-20	32-30, 32-28	30-26	30-28	30-46	AD7 & 8
6/9	15	32-22, 32-20	32-30, 32-28	30-26	30-28	30-46	AD7 & 9
6/10	23	32-22, 32-20	32-30, 32-28	30-25	30-27	32-46	AD7 & 10
6/11	31	32-22, 32-20	32-30, 32-28	30-25	30-27	32-46	AD7 & 11
6/12	39	32-24, 32-20	32-32, 32-28	30-34	30-36	32-48	AD7 & 12
6/13	47	32-24, 32-20	32-32, 32-28	30-34	30-36	32-48	AD7 & 13
6/14	55	32-24, 32-20	32-32, 32-28	30-33	30-35	30-48	AD7 & 14
6/15	63	32-24, 32-20	32-32, 32-28	30-33	30-35	30-48	AD7 & 15

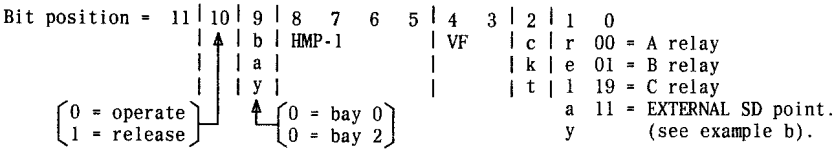
* Scanner answer AN00-15 failure is associated with detector amplifier (A1350), output cable driver (A51), and test transformer (A49) as follows:

AN00-03,	(0)	30-02 (A1350)	AN00-07,	(0)	32-07 (A51)	32-06 (A49)
	(1)	30-10 (A1350)		(1)	32-09 (A51)	
AN04-07,	(0)	30-04 (A1350)				
	(1)	30-12 (A1350)				
AN08-11,	(0)	30-06 (A1350)	AN08-15,	(0)	32-08 (A51)	32-12 (A49)
	(1)	30-14 (A1350)		(1)	32-10 (A51)	
AN12-15,	(0)	30-08 (A1350)				
	(1)	30-16 (A1350)				

† 30-18 & 30-40 (A56) must be operational

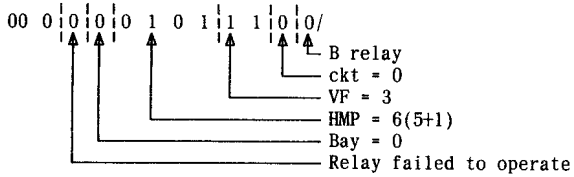
Analyze ppppppp as follows: for 2-wire No. 1 ESS

Note: If bit position 0 and 1 = 11, then it is an EXTERNAL SD point (MT) (see example b).

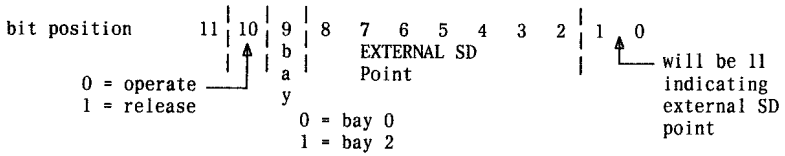


(a) EXAMPLE : Internal SD point

ppppppp = 000271



(b) EXTERNAL SD point



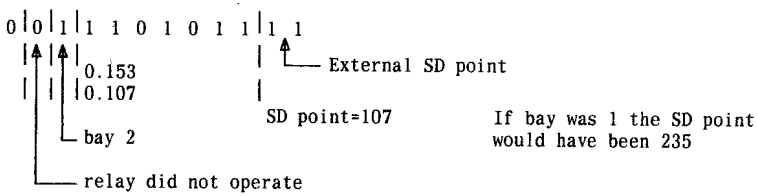
To determine SD point: convert binary bits 2 through 8 to octal, convert octal to decimal for SD point for bay "0", if bay is 1, add 128 to decimal number for SD point. SD points 000 through 127 appear on bay 0 and SD points 128 through 255 appear on bay 2.

Use the 1201 form (MT Frame Assignments) to locate the TNN. Use office base T drawing to locate signal distributor points.

(c) EXAMPLE:

EXTERNAL SD point

ppppppp = 1657



ADDRESS REGISTER RELAYS	GROUP	ADRS BITS	FUNCTION
L/R 08-15	A	8 – 15	OPR R/LX0-7 FOR X SELECTION
L/R 00-07	B	0 – 7	OPR R/LY0-7 FOR Y SELECTION
L/R 20-23	D	20 – 23	OPR LW0-3 FOR W SELECTION, IF BIT 27 =1 SELECT MTC RELAYS
L/R 18-19	C	18 (UPPER) – (LOWER) 19	SELECT QUARTERS OF MATRIX FIELD 19 | 18 | 1/4'S 0 | 1 | UPPER 1 | 0 | LOWER
L/R 16-17	E	16 (OPR) – (RLS) 17	SELECT OPR OR RLS FOR ML RELAYS 17 | 16 | 1 | 0 | RLS 0 | 1 | OPR
L/R 24-25	H	24 (LH) – (RH) 25	SELECT CONTROLLER 25 | 24 | 0 | 1 | LEFT 1 | 0 | RIGHT
L/R 26-27	T	26 (NORM) – (MAINT) 27	TYPE 27 26 ORDER 0 1 NORM 1 0 MTC

CONTACT MATRIX RELAYS	SLAVES OF	MULTIPLE CONTACTS FOR
LX0-7	L08-15	X SELECTION
LY0-7	L00-07	Y SELECTION
LW0-2	L20-22	W SELECTION OR SELECT MTC RELAY LW LW LW 27 | 2 | 1 | 0 | SELECT 1 | 0 | 0 | 1 | RQ 1 | 0 | 1 | 0 | RTA 1 | 1 | 0 | 0 | R2B

APEX RELAYS	FUNCTION
R/LC0	LIMITS TIME + 24V RLS PULSE. PREVENTS OPRN OF ML ON RLS PULSE
R/LS0	BY THEIR OPR TIMES, PREVENT DETECTOR CKT FROM OPR ON NOISE IN EARLY PART OF CYCLE
R/LSR	

MAINTENANCE RELAYS	FUNCTION
LTA	TEST POINT ACCESS MODE
L2B	RLS MTC RELAYS, RETURN LEFT CONTROLLER TO NORMAL MODE
LQ	QUARATINE MODE
LCPO	GIVES CONTROL OF LW, LX & LY RELAYS TO RIGHT CONT.
LCPI	COMBINE CONTACT MATRIX TO RIGHT CONT. FOLLOWS LQ RELAY

CONTROLLER RESET RELAYS	FUNCTION
RPN	OPR WHEN LEFT CONT. MTC RELAY OPRN SENSED. RESETS RIGHT CONTROL
L2B	OPR AFTER SUCCESSFUL ML RELAY ACTION. RESETS LEFT CONTROLLER
LPW	OPR WHEN POWER IN LEFT CONTROLLER

SELECTION		MTCE		HALF		W				QTR.		OPER.		X								Y							
GROUP		T		H		D				C		E		A								B							
ADDRESS		27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONTROLLER 0	L REL	MTC 27	NOR 26																										
	APEX NM	L27	L26	–	NORM	LW3/LW3A	LW2	RW1	LW0	LEAD LLP	LEAD LUP	RLS	OPR	LX7	LX6	LX5	LX4	LX3	LX2	LX1	LX0	LY7	LY6	LY5	LY4	LY3	LY2	LY1	LY0
	APEX DUP	L27	L26	COMB	–	LW3/LW3A	RW2	RW1	RW0	LLS	LUS	RLS	OPR	RX7	RX6	RX5	RX4	RX3	RX2	RX1	RX0	RY7	RY6	RY5	RY4	RY3	RY2	RY1	RY0
CONTROLLER 1	R REL	MTC 27	NOR 26																										
	APEX NM	R27	R26	NORM	–	LW3/LW3A	RW2	RW1	RW0	RLP	RUP	RLS	OPR	RX7	RX6	RX5	RX4	RX3	RX2	RX1	RX0	RY7	RY6	RY5	RY4	RY3	RY2	RY1	RY0
	APEX DUP	R27	R26	–	COMB	LW3/LW3A	LW2	LW1	LW0	RLS	RUS	RLS	OPR	LX7	LX6	LX5	LX4	LX3	LX2	LX1	LX0	LY7	LY6	LY5	LY4	LY3	LY2	LY1	LY0

	RW2	RW1	RW0	LW2	LW1	LW0		EXT MATRIX		
RL LP	J	H	G	C	B	F	LEAD	N	R	LW3
RL	M	L	K	F	E	D		P	S	LW3A

SIGNAL DISTRIBUTION LEAD SELECTION CHART

UNIVERSAL CIRCUIT NUMBER	EQUIPMENT LOCATION			UNIVERSAL CIRCUIT NUMBER	EQUIPMENT LOCATION			UNIVERSAL CIRCUIT NUMBER	EQUIPMENT LOCATION			UNIVERSAL CIRCUIT NUMBER	EQUIPMENT LOCATION		
	HORIZONTAL MTG. PLT.	VERTICAL FILE	CIRCUIT		HORIZONTAL MTG. PLT.	VERTICAL FILE	CIRCUIT		HORIZONTAL MTG. PLT.	VERTICAL FILE	CIRCUIT		HORIZONTAL MTG. PLT.	VERTICAL FILE	CIRCUIT
21 23	25 26	27	28	21 23	25 26	27	28	21 23	25 26	27	28	21 23	25 26	27	28
000	01	0	0	032	05	0	0	064	09	0	0	096	13	0	0
001	01	0	1	033	05	0	1	065	09	0	1	097	13	0	1
002	01	1	0	034	05	1	0	066	09	1	0	098	13	1	0
003	01	1	1	035	05	1	1	067	09	1	1	099	13	1	1
004	01	2	0	036	05	2	0	068	09	2	0	100	13	2	0
005	01	2	1	037	05	2	1	069	09	2	1	101	13	2	1
006	01	3	0	038	05	3	0	070	09	3	0	102	13	3	0
007	01	3	1	039	05	3	1	071	09	3	1	103	13	3	1
008	02	0	0	040	06	0	0	072	10	0	0	104	14	0	0
009	02	0	1	041	06	0	1	073	10	0	1	105	14	0	1
010	02	1	0	042	06	1	0	074	10	1	0	106	14	1	0
011	02	1	1	043	06	1	1	075	10	1	1	107	14	1	1
012	02	2	0	044	06	2	0	076	10	2	0	108	14	2	0
013	02	2	1	045	06	2	1	077	10	2	1	109	14	2	1
014	02	3	0	046	06	3	0	078	10	3	0	110	14	3	0
015	02	3	1	047	06	3	1	079	10	3	1	111	14	3	1
016	03	0	0	048	07	0	0	080	11	0	0	112	15	0	0
017	03	0	1	049	07	0	1	081	11	0	1	113	15	0	1
018	03	1	0	050	07	1	0	082	11	1	0	114	15	1	0
019	03	1	1	051	07	1	1	083	11	1	1	115	15	1	1
020	03	2	0	052	07	2	0	084	11	2	0	116	15	2	0
021	03	2	1	053	07	2	1	085	11	2	1	117	15	2	1
022	03	3	0	054	07	3	0	086	11	3	0	118	15	3	0
023	03	3	1	055	07	3	1	087	11	3	1	119	15	3	1
024	04	0	0	056	08	0	0	088	12	0	0	120	16	0	0
025	04	0	1	057	08	0	1	089	12	0	1	121	16	0	1
026	04	1	0	058	08	1	0	090	12	1	0	122	16	1	0
027	04	1	1	059	08	1	1	091	12	1	1	123	16	1	1
028	04	2	0	060	08	2	0	092	12	2	0	124	16	2	0
029	04	2	1	061	08	2	1	093	12	2	1	125	16	2	1
030	04	3	0	062	08	3	0	094	12	3	0	126	16	3	0
031	04	3	1	063	08	3	1	095	12	3	1	127	16	3	1

Section 4

MASTER SCANNER (MS)
(J1A043B)

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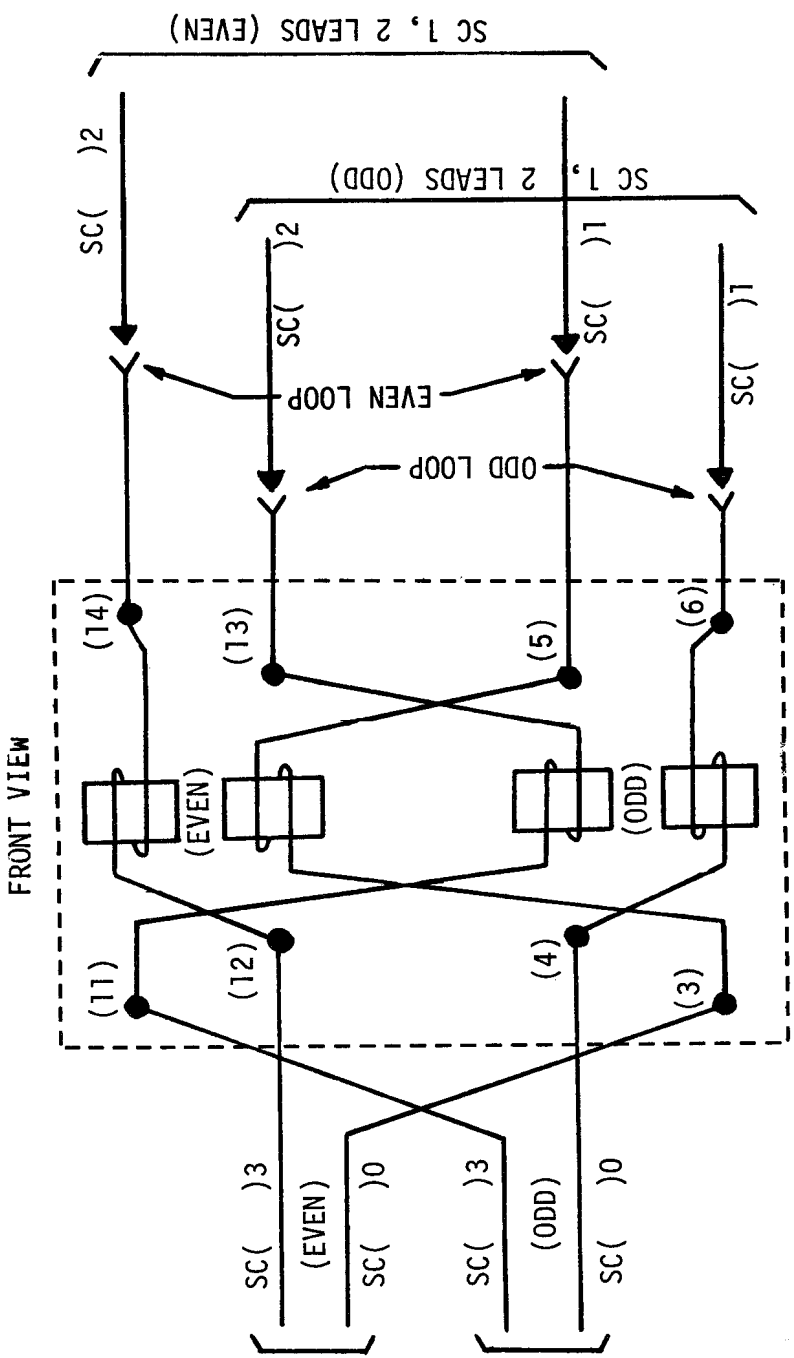
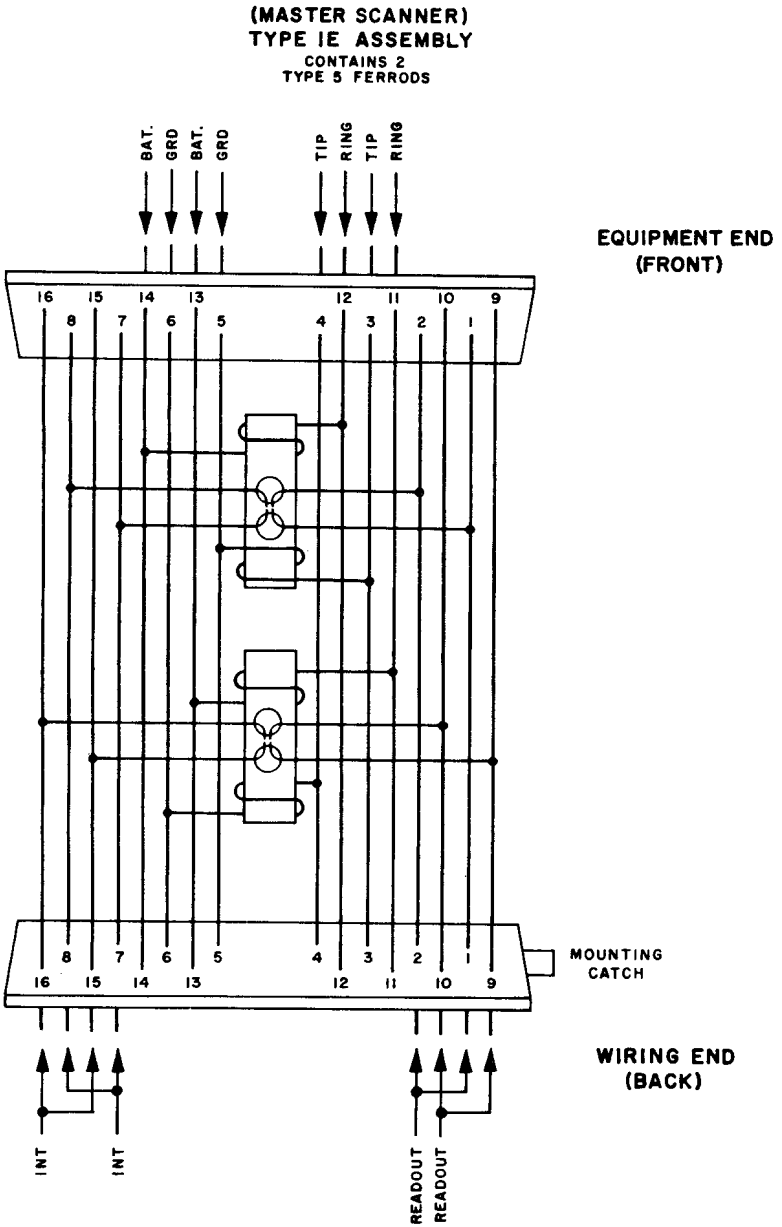
Supporting Documentation

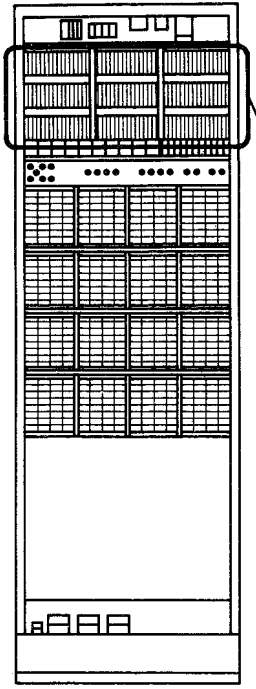
SD-1A209
CD-1A209
PK-1A207 Scanner Raw Data Document
TLM-1A209
ED-1A207-11
BSP 820-232-150
TOP 231-051-001



MASTER SCANNER FERRODS



Wiring Arrangements of Type 1E Ferrod Sensor Assembly



| | | |

SCANNER ERROR PATTERNS

FAILURE CHARACTERISTICS	POSSIBLE CAUSE OF FAILURE
Phases 1 & 3 – STF	Scanner controller 0
Phases 2 & 4 – STF	Scanner controller 1
Phases 1 & 4 – STF	• PU address bus 0 • Scanner bus 0
Phases 2 & 3 – STF	• PU address bus 1 • Scanner bus 1
Phases 1 through 4 – STF	Open ferrod sensor interrogate winding
*Scanner answer reply AN00-15, or scanner ASW, AN16	• Faulty secondary winding of test scanner transformer • Open ferrod readout loop • Faulty detector – amplifier • Faulty cable driver – output circuit
*Multiple failures in AN00-15 & ASW-S	• Delay and pulse shaper • Maintenance circuits • No continuity through primary windings of scanner test transformer

* This failure may be reported by F-level interrupt TTY message

TEST 1, SCANNER ANSWER BUS
ACTIVE STATE WITH MAINTENANCE BIT AD16 SET TO 1

PHASE & WORD	CP LOCATION (TYPE)	ANSWER BUS*
Phase 1 Word 1	34-40 (A147), 32-06 (A49), 34-30 (A1038), 32-14 (A1051), 34-36 (A1036), 34-28 (A146)	32-07 (A51) 32-09 (A51)
Phase 2 Word 1	34-42 (A147), 32-12 (A49), 34-34, (A1038), 32-16 (A1051), 34-38 (A1035), 34-32 (A146)	32-09 (A51) 32-10 (A51)
Phase 3 Word 1	34-40 (A147), 32-06 (A49), 34-30 (A1038) 32-14 (A1051), 34-36, (A1035), 34-29 (A146)	32-09 (A51) 32-10 (A51)
Phase 4	34-42 (A147), 32-12 (A49), 34-34 (A1038), 32-16 (A1051), 34-38 (A1035), 34-32 (A146)	32-07 (A51) 32-08 (A51)

* Failure Scanner ASW results in F-Level Interrupt TTY message. All scanner answer AN00-15 are set to 1

TEST 2A, SCANNER ANSWER BUS
QUIENSCENT STATE WITH INVALID ADDRESS

PHASE, WORD	CP LOCATION (TYPE)	COMMENTS
Phase 1 or 3 Word 2	34-36 (A1035), 34-30 (A1038), 34-40 (A147), 32-18 (A48), 30-18 (A56), 32-14 (A1051)	Check of scanner to recognize invalid address or inhibit output to answer bus
Phase 2 or 4 Word 2	34-38 (A1035), 34-34 (A1038), 34-42 (A147), 32-26 (A48), 30-40 (A56), 32-16 (A1051)	Check of scanner to recognize invalid address or inhibit output to answer bus

TEST 2B, SCANNER ENABLE/ENABLE VERIFY
OPERATION WORD 2, BIT 22

PHASE, WORD	LOCATION (TYPE)	COMMENTS
Phase 1 or 3	34-36 (A1035), 34-10 (A21)	Check of scanner to recognize enable signal and to verify by replying to CPD
Phase 2 or 4	34-38 (A1035), 34-16 (A21)	Check of scanner to recognize enable signal and to verify by replying to CPD

TEST 3, SCANNER ADDRESS PARITY OPERATIONS USING INVALID ADDRESSES

PHASE, WORD	* BITS	CP LOCATION (TYPE)	EXPLANATIONS
Phase 1 or 3 Word 2	17-21	34-30 (A1038), 34-28 (A146), 34-10 (A21)	Check of scanner to verify correct parity and inhibit ASWS answer to CC when parity is incorrect
Phase 2 or 4 Word 2	17-21	34-34 (A1038), 34-32 (A146), 34-16 (A21)	Check of scanner to verify correct parity and inhibit ASWS answer to CC when parity is incorrect

* Addresses are as follows:

Bit 17 – 8 & 1, 8 & 0
Bit 18 – 8 & 1, 8 & 1
Bit 19 – 8 & 1, 8 & 2
Bit 20 – 8 & 0, 8 & 1
Bit 21 – 8 & 2, 8 & 1

TEST 4, SCANNER ROW READOUT AND ANSWER OPERATIONS – PHASES 1 THROUGH 4*

REPLY WORD/ BIT	ROW	ACCESS CIRCUIT – CP (A048)		†CORE MATRIX – CP (A037)		ASWS TRANSFORMER CP (A052)	PU ADDRESS
		CIRCUIT 0	CIRCUIT 1	CORE 0	CORE 1		
3/0	0	32-22, 32-18	32-30, 32-26	30-22	30-24	30-42	AD0 & 8
3/1	8	32-22, 32-18	32-30, 32-26	30-22	30-24	30-44	AD0 & 9
3/2	16	32-22, 32-18	32-30, 32-26	30-21	30-23	30-46	AD0 & 10
3/3	24	32-22, 32-18	32-30, 32-26	30-21	30-23	30-48	AD0 & 11
3/4	32	32-24, 32-18	32-32, 32-26	30-30	30-32	30-42	AD0 & 12
3/5	40	32-24, 32-18	32-32, 32-26	30-30	30-32	30-44	AD0 & 13
3/6	48	32-24, 32-18	32-32, 32-26	30-29	30-31	30-46	AD0 & 14
3/7	56	32-24, 32-18	32-32, 32-26	30-29	30-31	30-48	AD0 & 15
3/8	1	32-22, 32-18	32-30, 32-26	30-22	30-24	30-42	AD1 & 8
3/9	9	32-22, 32-18	32-30, 32-26	30-22	30-24	30-44	AD1 & 9
3/10	17	32-22, 32-18	32-30, 32-26	30-21	30-23	30-46	AD1 & 10

* See footnotes at end of table

TEST 4, SCANNER ROW READOUT AND ANSWER OPERATIONS – PHASES 1 THROUGH 4* (Contd)

REPLY WORD/ BIT	ROW	ACCESS CIRCUIT – CP (A048)		†CORE MATRIX – CP (A037)		ASWS TRANSFORMER CP (A052)	PU ADDRESS
		CIRCUIT 0	CIRCUIT 1	CORE 0	CORE 1		
3/11	25	32-22, 32-18	32-30, 32-26	30-21	30-23	30-48	AD1 & 11
3/12	33	32-24, 32-18	32-32, 32-26	30-30	30-32	30-42	AD1 & 12
3/13	41	32-24, 32-18	32-32, 32-26	30-30	30-32	30-44	AD1 & 13
3/14	49	32-24, 32-18	32-32, 32-26	30-29	30-31	30-46	AD1 & 14
3/15	57	32-24, 32-18	32-32, 32-26	30-29	30-31	30-48	AD1 & 15
4/0	2	32-22, 32-18	32-30, 32-26	30-22	30-24	30-42	AD2 & 8
4/1	10	32-22, 32-18	32-30, 32-26	30-22	30-24	30-44	AD2 & 9
4/2	18	32-22, 32-18	32-30, 32-26	30-21	30-23	30-46	AD2 & 10
4/3	26	32-22, 32-18	32-30, 32-26	30-21	30-23	30-48	AD2 & 11
4/4	34	32-24, 32-18	32-32, 32-26	30-30	30-32	30-42	AD2 & 12
4/5	42	32-24, 32-18	32-32, 32-26	30-30	30-32	30-44	AD2 & 13
4/6	50	32-24, 32-18	32-32, 32-26	30-29	30-31	30-46	AD2 & 14
4/7	58	32-24, 32-18	32-32, 32-26	30-29	30-31	30-48	AD2 & 15
4/8	3	32-22, 32-18	32-30, 32-26	30-22	30-24	30-42	AD3 & 8
4/9	11	32-22, 32-18	32-30, 32-26	30-22	30-24	30-44	AD3 & 9
4/10	19	32-22, 32-18	32-30, 32-26	30-21	30-23	30-46	AD3 & 10
4/11	27	32-22, 32-18	32-30, 32-26	30-21	30-23	30-48	AD3 & 11
4/12	35	32-24, 32-18	32-32, 32-26	30-30	30-32	30-42	AD3 & 12
4/13	43	32-24, 32-18	32-32, 32-26	30-30	30-32	30-44	AD3 & 13
4/14	51	32-24, 32-18	32-32, 32-26	30-29	30-31	30-46	AD3 & 14
4/15	59	32-24, 32-18	32-32, 32-26	30-29	30-31	30-48	AD3 & 15
5/0	4	32-22, 32-20	32-30, 32-28	30-26	30-28	30-42	AD4 & 8

See footnotes at end of table

TEST 4, SCANNER ROW READOUT AND ANSWER OPERATIONS – PHASES 1 THROUGH 4* (Contd)

REPLY WORD/ BIT	ROW	ACCESS CIRCUIT – CP (A048)		†CORE MATRIX – CP (A037)		ASWS TRANSFORMER CP (A052)	PU ADDRESS
		CIRCUIT 0	CIRCUIT 1	CORE 0	CORE 1		
5/1	12	32-22, 32-20	32-30, 32-28	30-26	30-28	30-44	AD4 & 9
5/2	20	32-22, 32-20	32-30, 32-28	30-25	30-27	30-46	AD4 & 10
5/3	28	32-22, 32-20	32-30, 32-28	30-25	30-27	30-48	AD4 & 11
5/4	36	32-24, 32-20	32-32, 32-28	30-34	30-36	32-42	AD4 & 12
5/5	44	32-24, 32-20	32-32, 32-28	30-34	30-36	32-44	AD4 & 13
5/6	52	32-24, 32-20	32-32, 32-28	30-33	30-35	32-46	AD4 & 14
5/7	60	32-24, 32-20	32-32, 32-28	30-33	30-35	32-48	AD4 & 15
5/8	5	32-22, 32-20	32-30, 32-28	30-26	30-28	30-42	AD5 & 8
5/9	13	32-22, 32-20	32-30, 32-28	30-26	30-28	30-44	AD5 & 9
5/10	21	32-22, 32-20	32-30, 32-28	30-25	30-27	30-46	AD5 & 10
5/11	29	32-22, 32-20	32-30, 32-28	30-25	30-27	30-48	AD5 & 11
5/12	37	32-24, 32-20	32-32, 32-28	30-34	30-36	32-42	AD5 & 12
5/13	45	32-24, 32-20	32-32, 32-28	30-34	30-36	32-44	AD5 & 13
5/14	53	32-24, 32-20	32-32, 32-28	30-33	30-35	32-46	AD5 & 14
5/15	61	32-24, 32-20	32-32, 32-28	30-33	30-35	32-48	AD5 & 15
6/0	6	32-22, 32-20	32-30, 32-28	30-26	30-28	30-42	AD6 & 8
6/1	14	32-22, 32-20	32-30, 32-28	30-26	30-28	30-44	AD6 & 9
6/2	22	32-22, 32-20	32-30, 32-28	30-25	30-27	30-46	AD6 & 10
6/3	30	32-22, 32-20	32-30, 32-28	30-25	30-27	30-48	AD6 & 11
6/4	38	32-24, 32-20	32-32, 32-28	30-34	30-36	32-42	AD6 & 12
6/5	46	32-24, 32-20	32-32, 32-28	30-34	30-36	32-44	AD6 & 13
6/6	54	32-24, 32-20	32-32, 32-28	30-33	30-35	32-46	AD6 & 14

See footnotes at end of table

TEST 4, SCANNER ROW READOUT AND ANSWER OPERATIONS – PHASES 1 THROUGH 4* (Contd)

REPLY WORD/ BIT	ROW	ACCESS CIRCUIT – CP (A048)		†CORE MATRIX – CP (A037)		ASWS TRANSFORMER CP (A052)	PU ADDRESS
		CIRCUIT 0	CIRCUIT 1	CORE 0	CORE 1		
6/7	62	32-24, 32-20	32-32, 32-28	30-33	30-35	32-48	AD6 & 15
6/8	7	32-22, 32-20	32-30, 32-28	30-26	30-28	30-42	AD7 & 8
6/9	15	32-22, 32-20	32-30, 32-28	30-26	30-28	30-44	AD7 & 9
6/10	23	32-22, 32-20	32-30, 32-28	30-25	30-27	30-46	AD7 & 10
6/11	31	32-22, 32-20	32-30, 32-28	30-25	30-27	30-48	AD7 & 11
6/12	39	32-24, 32-20	32-32, 32-28	30-34	30-36	32-42	AD7 & 12
6/13	47	32-24, 32-20	32-32, 32-28	30-34	30-36	32-44	AD7 & 13
6/14	55	32-24, 32-20	32-32, 32-28	30-33	30-35	32-46	AD7 & 14
6/15	63	32-24, 32-20	32-32, 32-28	30-33	30-35	32-48	AD7 & 15

* Scanner answer AN00-15 failure is associated with detector amplifier (A1350), output cable driver (A51), and test transformer (A49) as follows:

AN00-03,	(0)	30-02 (A1350)	AN00-07,	(0)	32-07 (A51)	32-06 (A49)
	(1)	30-10 (A1350)		(1)	32-09 (A51)	
AN04-07,	(0)	30-04 (A1350)				
	(1)	30-12 (A1350)				
AN08-11,	(0)	30-06 (A1350)	AN08-15,	(0)	32-08 (A51)	32-12 (A49)
	(1)	30-14 (A1350)		(1)	32-10 (A51)	
AN12-15,	(0)	30-08 (A1350)				
	(1)	30-16 (A1350)				

† 30-18 & 40 (A56) must be operational

```
*
A 00 REPT: F-LEVEL @05341407 MFNUM=00020275 MICON=00000023    COMPLETED!
     LVDATA=0040 SRDATA=40000002 FRDATA=00002400

     SCFR REPLY MATCH SWITCHED MS 1 CPD 0

     F-LEVEL
     00301540  00000000  05341370  00000016  00177377  00160723
     00177777  04172717  00000016  05341407  00000440  05341405
     00177777  05341412  60001055  00000041  07633730  00000003
     04651402  34000000  00000043  00000002  57600001  20000401
     00301540  00000440  14600000  00177377  00000043  00000041
     57600001  20000000  00301540  34000000  00000043  00000041
     60001055  07633730  00177377  00000004  00000040  22040004
     00000000  00000000  00000000  00000000  00000000

A 00 DR01 TBL NOS CPD 0
     CELL NOS
     ATP

     #496
```

ACTION LINE REPORTS TYPE
OF FAILURE AS REPLY MATCH
OF MASTER SCANNER

REGISTERS TO EXAMINE - CPD ENABLED

CSC - CC AND PU COMMUNICATIONS CONTROL
DE - DIAGNOSTIC ECHO
ER - ENABLE
L - LOGIC (SCANNER ANSWER)
PES - PERIPHERAL ERROR SUMMARY
RR - REPLY (CPD VERIFY ANSWER)

* SUPPLEMENTARY INFORMATION HAD BEEN INHIBITED FROM BEING PRINTED AS FOLLOWS:
(1) CONTENTS OF STACK (10 WORDS)
(2) PERIPHERAL MAC CONTROL BLOCK (3 WORDS)
(3) CPD AND BUS TEST RESULTS AND CONFIGURATION (5 WORDS)
(4) CONTENTS OF POB (70 WORDS)

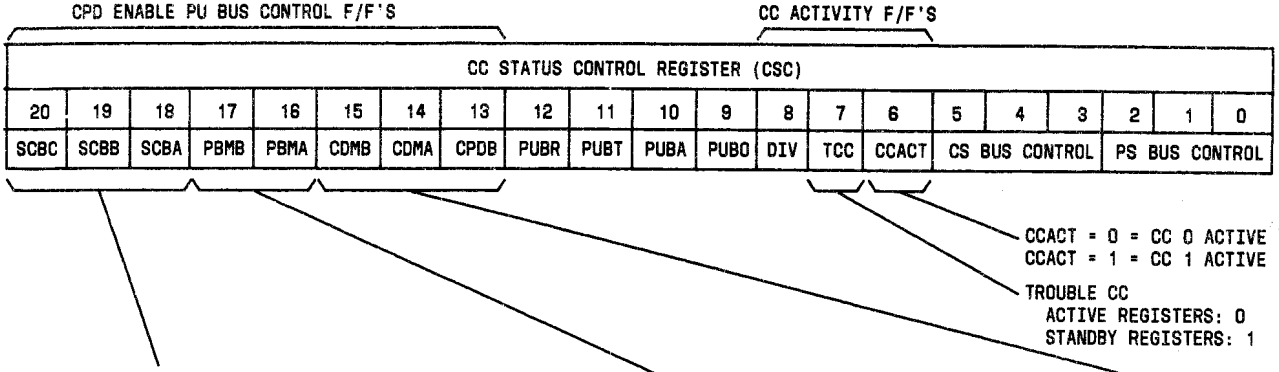
† DATA FIELDS

AC1FR	AC1GR	AC1JR	AC1KR	AC1LR	AC1XR
AC1YR	AC1ZR	IN1BR	IN1CAR	AC1ILA	AC1SCA
AC1SDA	AC1SPA	AC1CSC	AC1INS	AC1INH	AC1SC
AC1SR	AC1INJ	AC1PES	AC1PSC	AC1DE	AC1RR
AC1ER	AC1PRM	AC1PRL	ST1LR	ST1PES	ST1PSC
ST1DE	ST1RR	ST1ER	ST1PRM	ST1PRL	ST1INS
ST1CSC	ST1INH	IB1ULR	IB1RFLC00	IB1RFLC01	IB1RFLC02
IB1RFLC03	IB1RFLC04	IB1RFLC05	IB1RFLC06	IB1RFLC07	

† ACTIVE CC REGISTERS ARE PREFIXED WITH 'AC1'
STANDBY CC REGISTERS ARE PREFIXED WITH 'ST1'

EXAMPLE OF MS REPLY MATCH WITH ASSOCIATED REGISTERS IDENTIFIED

COMPONENTS OF CC AND PU COMMUNICATIONS CONTROL (CSC) REGISTER



PU REPLY BUS

CSC BIT			PU REPLY BUS (PUR)	
20	19	18		
SCBC	SCBB	SCBA	ACT CC	STBY CC
0	0	0	0	1
0	1	0	0	0
0	0	1	1	0
0	1	1	1	1
1	X	X	0 & 1	0 & 1

PU WRITE BUS

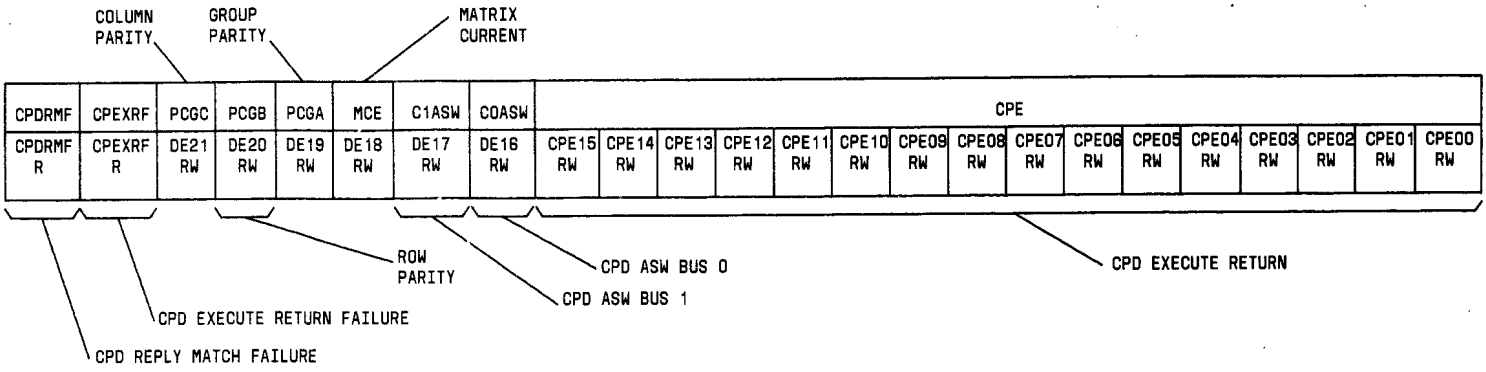
CSC BIT		ER BIT	PU WRITE BUS (PUW)	
17	16	14		
PBMB	PBMA		ACT CC	STBY CC
0	0	0	0	X
0	0	1	1	X
1	0	0	0	1
1	0	1	1	0
0	1	0	1	X
0	1	1	0	X
1	1	0	X	0
1	1	1	X	1

REPLY BUS (CPR)

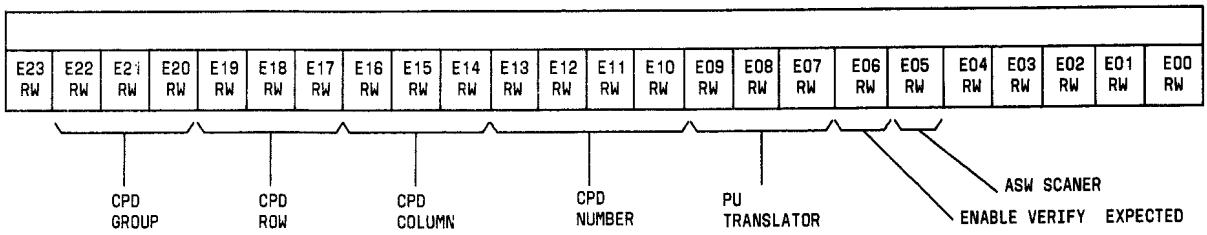
CSC BIT			CPD REPLY BUS (CPR)	
CDMB	CDMA	CPDB	ACT CC	STBY CC
15	14	13		
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	1	1
1	0	0	0	0
1	0	1	1	1
1	1	0	0	0
1	1	1	1	1

ERROR PATTERN IN REPT: F-LEVEL MESSAGE

DIAGNOSTIC ECHO (DE) REGISTER



ENABLE REGISTER (ER)



COMPONENTS OF DIAGNOSTIC ECHO (DE) AND ENABLE (ER) REGISTERS

PERIPHERAL ERROR SUMMARY (PES) REGISTER

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RMEPU	RMEGCP	ISCU	INHAP	INHASW	PWP2	PWP1	CPDKC	APUT	APUB	APEPU	ASWEPU	RMFCPD	ASWECPD	AP1PU	APOPU	ASW1PU	ASWOPU
RMEPU R	RMEGCP R	ISCU RW	INHAP R	INHASW R	PWP2 R	PWP1 R	CPDKC RW	APUT RW	APUB RW	APEPU RW	ASWEPU RW	RMFCPD RW	ASWECPD RW	AP1PU RW	APOPU RW	ASW1PU RW	ASWOPU RW

ENABLE ORDER JUST EXECUTED
0 - CPD 1 - CODED

PU PARITY ERROR

ASW ERROR PU

REPLY MATCH FAILURE CPD

ASW ERROR OR EXECUTE
RETURN FAILURE FROM CPD

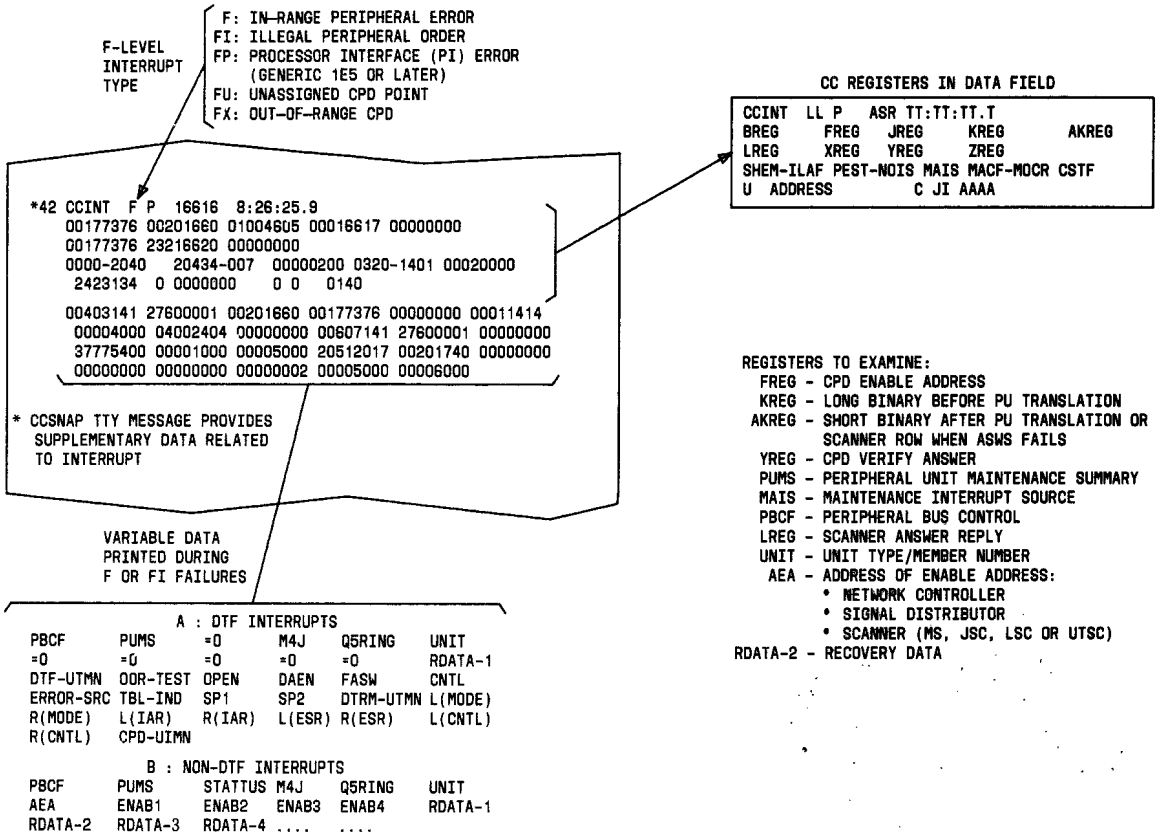
ASW FROM PU
REPLY BUS 1

ASW FROM PU REPLY BUS 0

REPLY REGISTER (RR)

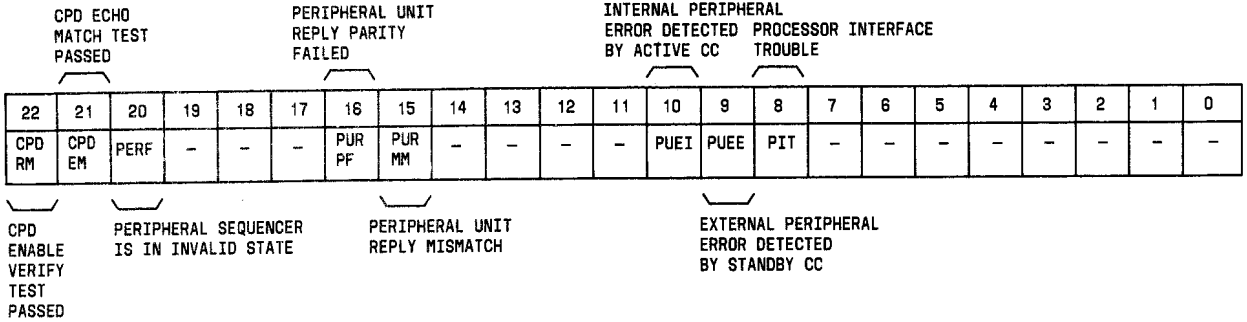
R23 RW	R22 RW	R21 RW	R20 RW	R19 RW	R18 RW	R17 RW	R16 RW	R15 RW	R14 RW	R13 RW	R12 RW	R11 RW	R10 RW	R09 RW	R08 RW	R07 RW	R06 RW	R05 RW	R04 RW	R03 RW	R02 RW	R01 RW	R00 RW
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
CPD COLUMN								CPD ROW								CPD GROUP							

COMPONENTS OF PERIPHERAL ERROR SUMMARY (PES) AND REPLY (RR) REGISTERS

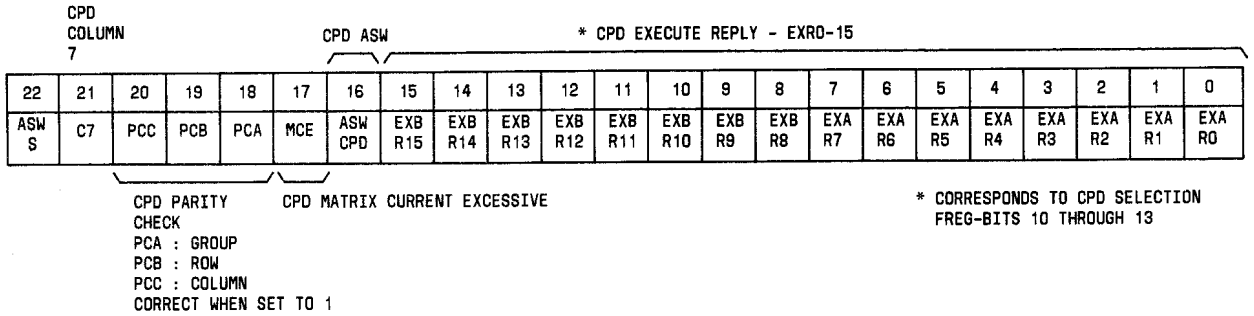


CCINT TTY MESSAGE INDICATING PERIPHERAL UNIT (PU) FAILURE – DATA FIELD IDENTIFICATION

MAINTENANCE INTERRUPT SOURCE (MAIS) REGISTER



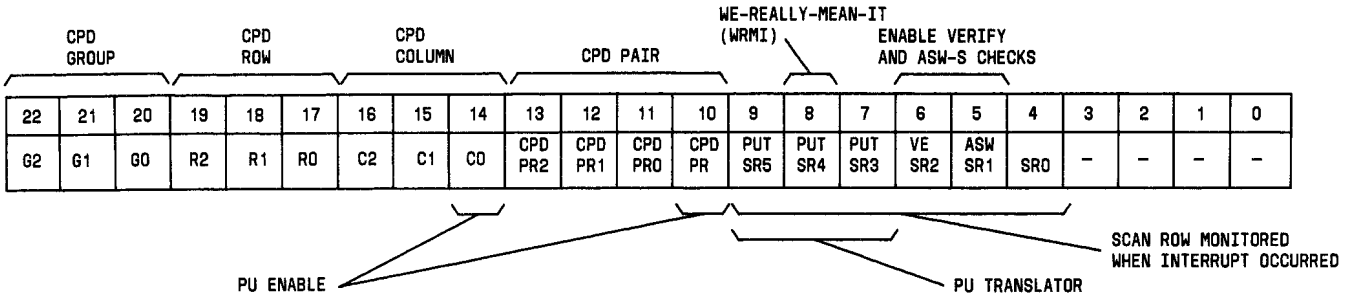
PERIPHERAL UNIT MAINTENANCE SUMMARY (PUMS) REGISTER



ERROR PATTERN IN CCINT F-LEVEL MESSAGE
COMPONENTS OF MAIS AND PUMS REGISTERS

CCINT TTY MESSAGE – INDICATOR FLIP-FLOP(S), PU FAILURE SOURCE, AND TROUBLE CONDITION INDICATED

REGISTER	FLIP-FLOP / BIT	PU FAILURE SOURCE	TROUBLE CONDITION INDICATED
PUMS	ASWCPD/16 MCE/17, PCA/18, PCB/19 or PCC/20	All-seems-well (ASW) CPD	Maintenance circuits in CPD detect incorrect enable address or amplitude of access current. ASW-CPD signal is not returned to CC when bit 16 is reset to 0
PUMS	ASWS/22	ASW – scanner (S)	Maintenance circuits in scanner detect more than one row of ferrod selected and interrogate current exceeds nominal value. Failure is indicated when bit 22 is reset to 0
MAIS	CPDEM/21	CPD execute reply match	CPD returns execute pulse to CC in PUMS register bits 0 through 15. CC then compares CPD selection made by translation of F register bits 10 through 13 to CPD echo in PUMS. Failure is indicated when bit 21 is reset to 0
MAIS	CPDRM/22	CPD verify answer match	CPD enable sent to PU does not match address on verify answer bus as received by CC. Y register contents is compared to translation F register bits 14 through 22. Failure is indicated when bit 22 is reset to 0
MAIS	PERF/20	Peripheral sequencer	Peripheral sequencer enters an invalid state when internal CC checks are make. Failure is indicated when bit 20 is reset to 0
MAIS	PIT/8	Processor interface (PI)	In office equipped with PI features – generic 1E5 or later: failure of internal PT checks and source [illegible] in 3ACC processor produce report of trouble condition. When it is determined at fault by program, PIINT/PISNAP TTY message is printed; otherwise, CCINT FP TTY message contains data reporting failure
MAIS	PURMM/15 or PURPF/16	Peripheral unit parity (PUP) reply	In office equipped with peripheral unit controller (PUC) – generic 1E6 or later: Failure develops as short in scanner control to readout winding. Failure is reported that undetected false ones are received in L register on peripheral orders where scanner response is expected. Peripheral unit parity (PUP) and PUP check (PUPCHK) responses from PUC are also detected by CC for proper match on all PU responses. PUP, PUPCK, RAWPCK and IPURPF flip-flops are located in FBCF register



BIT STATE		CONTR	BUS	ENABLE
14	10			
0	0	0	0	EN00
1	0	1	1	EN11
0	1	1	0	EN10
1	1	0	1	EN01

BIT STATE			TRANSLATOR SELECTED
9	8	7	
0	0	0	PU SHORT BINARY
0	0	1	PU LONG BINARY
0	1	0	4:1 LSF
0	1	1	2:1 LSF
1	0	0	TSF OR JSF
1	0	1	CPD LONG BINARY
1	1	0	SIGNAL DISTRIBUTOR
1	1	1	SCANNER

COMPONENTS OF F-REGISTER (FREG) ASSOCIATED WITH CPD ENABLE ADDRESS

22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	AN15	AN14	AN13	AN12	AN11	AN10	AN9	AN8	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0

L-REGISTER (LREG) CONTAINING SCANNER ANSWER REPLY

CPD COLUMN 0-6 | CPD ROW 0-7 | CPD GROUP 0-7

22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C6	C5	C4	C3	C2	C1	C0	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0

Y-REGISTER (YREG) CONTAINING CPD ECHO – GROUP, ROW AND COLUMN

22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	–	–	–	AN35	AN34	AN33	AN32	AN31	AN30	AN29	AN28	AN27	AN26	AN25	AN24	AN23

K-REGISTER (KREG) - LONG BINARY TRANSLATOR

SCAN ROW OF PU DURING INTERRUPT

22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AN22	AN21	AN20	AN19	AN18	AN17	AN16	AN15	AN14	AN13	AN12	AN11	AN10	AN9	AN8	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0

ADDEND K-REGISTER (AKREG) - PU ORDER AFTER TRANSLATION

F-LEVEL
INTERRUPT
TYPE

P: IN-RANGE PERIPHERAL ERROR
PI: ILLEGAL PERIPHERAL ORDER
PU: UNASSIGNED CPD POINT
PX: OUT-OF-RANGE CPD
PM: PU PARITY (PUP) ERROR (GENERIC 1E6 OR LATER)
PF: PUP ERROR AT PU FRAME (GENERIC 1E6 OR LATER)

```
26 SPINT    P   QEXC   8:26:25.9
     16616 23216620    16620 00177376 00201660 01004605
  00016617 00177376 00201660 00177777 23216620 00000000
  00011414 00004000 04002404 00000000 00000000    16616
  0000-2040   20434-007   00000200   0320-1401   00020000
   2423134  0 0000000     0 0   0140

 00403141 27600001 00201660 00177376 00000000 00011414
  00004000 04002404 00000000 00607141 27600001 00000000
  37775400 00001000 00005000 20512017 00201740 00000000
  00000000 00000000 00000002 00005000 00006000
```

†

SP REGISTERS IN DATA FIELD

```
SPINT      II   JJJJ     TT:TT:TT.T
     SP-ASR   SP-IREG   SP-AREG   SP-BREG   SP-FREG   SP-JREG
     SP-KREG  SP-LREG   SP-PREG   SP-QREG   SP-XREG   SP-YREG
     SP-ESG   SP-SCG1   SP-SCG2   SP-SCG3   SP-CCDR   SP-CAR

     SHEM-ILAF PEST-NOIS MAIS     MACF-MOCR CSTF
     CC-ASR  U  ADDRESS    C JI   AAAA
```

REGISTERS TO EXAMINE:
- DER: CPD DIAGNOSTIC ECHO AND EXECUTE REPLY
- FREG: CPD ENABLE ADDRESS
- YREG: CPD VERIFY ANSWER
- LREG: SCANNER ANSWER RESPONSE
- PREG: SHORT BINARY TRANSLATOR DATA ON PUAB
- KREG: LONG BINARY TRANSLATOR DATA ON PUAB
- ESG: ERROR SUMMARY GROUP
- UNIT: UNIT TYPE/MEMBER NUMBER
- AEA: ADDRESS OF ENABLE ADDRESS:
  - NETWORK CONTROLLER
  - SIGNAL DISTRIBUTOR
  - SCANNER (JSC, LSC, MSC OR UTSC)

RDATA: 2: RECOVERY DATA

VARIABLE DATA PRINTED DURING
P, PF, PI OR PM FAILURES:
GENERICS 1E5 AND LATER

STBY-PBC*	STBY-DER*	STBY-FREG*	STBY-LREG*	STBY-YREG*	STBY-ESG*
STBY-SCG1*	STBY-SCG2*	STBY-SCG3*	ACT-PBC	ACT-DER	STATUS
M4J	Q5RING	UNIT	AEA	ENABL1	ENABL2
ENABL3	ENABL4	RDATA-1	RDATA-2	RDATA-4	.....

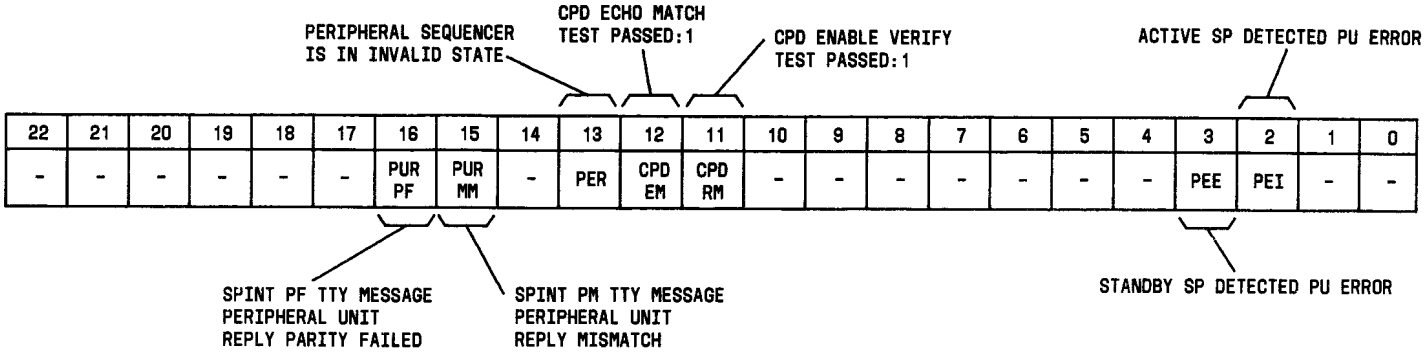
VARIABLE DATA PRINTED
DURING P OR PI FAILURES:
GENERICS 1E5 AND LATER

PBC	DER	STATUS	M4J	Q5RING	UNIT
AEA	ENABL1	ENABL2	ENABL3	ENABL4	RDATA-1
RDATA-2	RDATA-3	RDATA-4	....	....	

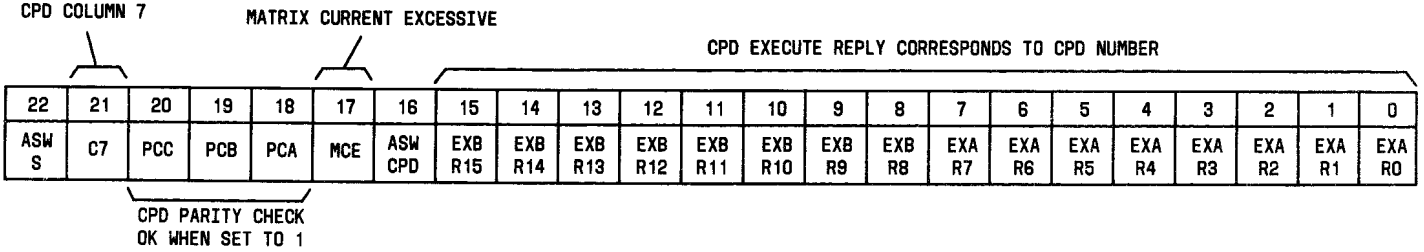
* WHEN STANDBY (STBY) SP IS OUT-OF-SERVICE, STBY REGISTERS ARE SET TO ZERO

† SPSNAP TTY MESSAGE PROVIDES SUPPLEMENTARY DATA RELATED TO INTERRUPT

ERROR PATTERN IN SPINT F-LEVEL MESSAGE



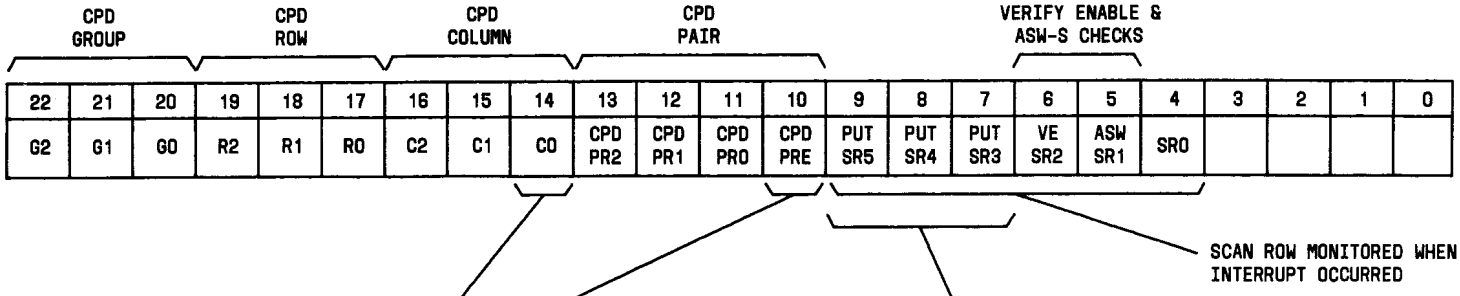
ERROR SUMMARY GROUP (ESG) REGISTER



DIAGNOSTIC ECHO REGISTER (DER)

SPINT TTY MESSAGE – INDICATOR FLIP-FLOPS, PU FAILURE SOURCE AND TROUBLE CONDITION INDICATED

REGISTER	FLIP-FLOP/BIT	PU FAILURE SOURCE	TROUBLE CONDITION INDICATED
DER	ASW-CPD/16, MCE/17,/PCA/18, PCB/19, or PCC/20	All-seems-well (ASW) – CPD	Maintenance circuits in CPD detect incorrect enable address or amplitude of access current. ASW – CPD signal is not returned to CC when bit is reset to 0 MCE: Matrix current excessive (0) PCB: Parity check row (0) PCA: Parity check group (0) PCB: Parity check column (0)
DER	ASW-S/22	ASW – scanner	Maintenance circuits in Scanner detect more than one row of ferrods selected and interrogate current exceeds nominal value. Failure is indicated when bit 22 is reset to zero
ESG	CPD RM/11	CPD verify answer match	CPD enable address sent to PU does not match address on verify answer bus as received by SP. Y register contents are compared to translation of F register bits 14 through 22. Failure is indicated when bit 11 is reset to zero
ESG	CPD EM/12	CPD execute reply match	CPD returns execute pulse to SP DER register bits 0 through 15. SP then compares CPD selection made by translation of F register bits 10 through 13. Failure is indicated when bit 12 is reset to zero
ESG	PER/13	Peripheral sequencer	Peripheral sequencer enters an invalid state when internal SP checks are made. Failure is indicated when 13 is reset to zero
ESG	PURMM/15 or PURPF/16	Peripheral unit parity (PUP) reply	In office equipped with peripheral unit controller (PUC) – generic 1E6 or later: failure develops as short in scanner control to readout winding. Failure is reported that undetected false ones are received in L register on peripheral orders where scanner response is expected. Peripheral unit (PU) parity (PUP) and PUP check (PUPCHK) responses from PUC are also detected by SP for proper match on all PU responses. PUP, PUPCHK, RAWPCK and IPURF flip-flops are located in special control group (SCG) 3



PU ENABLE

BIT STATE		CONTR	BUS	ENABLE
*14	10			
0	0	0	0	EN00
1	0	1	1	EN11
0	1	1	0	EN10
1	1	0	1	EN01

* BIPOLAR POINTS: POLARITY OF PULSE - 0 : RESET
1 : SET

PU TRANSLATOR

BIT STATE			TRANSLATOR SELECTED
9	8	7	
0	0	0	PU SHORT BINARY
0	0	1	PU LONG BINARY
0	1	0	4:1 LSF
0	1	1	2:1 LSF
1	0	0	TSF OR JSF
1	0	1	CPD LONG BINARY
1	1	0	SIGNAL DISTRIBUTOR
1	1	1	SCANNER

COMPONENTS OF F-REGISTER (FREG) ASSOCIATED WITH CPD ENABLE ADDRESS

22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	AN15	AN14	AN13	AN12	AN11	AN10	AN9	AN8	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0

L-REGISTER (LREG) CONTAINING SCANNER ANSWER RESPONSE

CPD COLUMN 0-6 | CPD ROW 0-7 | CPD GROUP 0-7

22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C6	C5	C4	C3	C2	C1	C0	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0

Y-REGISTER (YREG) CONTAINING CPD ECHO – GROUP, ROW, and COLUMN

22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	AD35	AD35	AD33	AD32	AD31	AD30	AD29	AD28	AD27	AD26	AD25	AD24	AD23

K-REGISTER (KREG) – LONG BINARY TRANSLATOR

SCAN ROW AT POINT OF INTERRUPT

22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AD22	AD21	AD20	AD19	AD18	AD17	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

P-REGISTER (PREG) – SHORT BINARY TRANSLATOR

```
A 23 REPT: F-LEVEL @04127235 MFNUM=00000025 MICON=00000023   COMPLETED
     LVDATA=0040 SRDATA=40000000 FRDATA=00000200

     PFLR SOFT ERROR MCC 0

     DATA: F-LEVEL
     14022227 00000000 04126674 00035000 00000000 00000000
     00000000 00000000 00000000 24127235 00000040 04127233
     00754000 04127240 62005648 00000040 07410037 00000003
     04122640 34000000 00016104 00000007 57600001 10000401
     00755540 00000000 00000000 00000000 00002007 00000000
     60600000 00000000 00000000 00000000 00000000 00000000
     00025646 77637777 00000000 00172004 00000004 00000000
     00000000 00000000 00004000 00000000 00000004

     DATA: CONTENTS OF STACK
     04576740 04200072 04421274 04122640 04433121 04424722
     04425460 04424757 04425270 00000000 00000000 00000000

     DATA: PERIPHERAL MAC CONTROL BLOCK
     10040131 00000057 05264112
     00/00/00  00:23:06
     #041
```

ACTION LINE REPORTS TYPE OF FAILURE AND PU TYPE AS FOLLOWS:

- PPI/MCC
- IOU

*DATA FIELDS

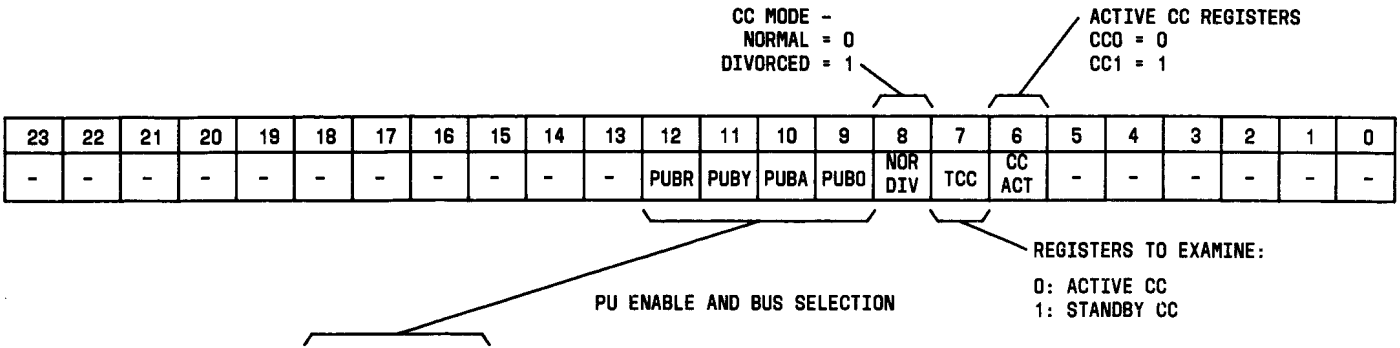
AC1FR	AC1GR	AC1JR	AC1KR	AC1LR	AC1XR
AC1YR	AC1ZR	IN1BR	IN1CAR	AC1ILA	AC1SCA
AC1SDA	AC1SPA	AC1CSC	AC1INS	AC1INH	AC1SC
AC1SR	AC1INJ	AC1PES	AC1PSC	AC1DE	AC1RR
AC1ER	AC1PRM	AC1PRL	ST1LR	ST1PES	ST1PSC
ST1DE	ST1RR	ST1ER	ST1PRM	ST1PRL	ST1INS
ST1CSC	ST1INH	IB1ULR	IB1RFLC00	IB1RFLC01	IB1RFLC02
IB1RFLC03	IB1RFLC04	IB1RFLC05	IB1RFLC06	IB1RFLC07	

* ACTIVE CC REGISTERS ARE PREFIXED WITH 'AC1'
  STANDBY CC REGISTERS ARE PREFIXED WITH 'ST1'

CROSS HATCHED RECOVERY DATA IS CONTAINED IN REGISTERS IB1RFLC00 THROUGH IB1RFLC05 AND IB1RLC07

REGISTERS TO EXAMINE – CODED ENABLE:
CSC – CC AND PU COMMUNICATION CONTROL
PES – PERIPHERAL ERROR SUMMARY
  E – PU ENABLE
PRM – P-REGISTER MOST SIGNIFICANT ADDRESS

ERROR PATTERN IN REPT:F-LEVEL
CODED ENABLE MESSAGE



BUS SELECTION				PU ENABLE		PU WRITE		PU REPLY	
12	11	10	9	ACT	STBY	ACT	STBY	ACT	STBY
0	0	0	0	0	1	0	1	0	1
0	0	1	0	1	0	1	0	1	0
0	1	0	0	0	*	0	*	0	0
0	1	1	0	1	*	1	*	1	1
0	0	0	1	0&1	*	0&1	*	0	1
0	0	1	1	0&1	*	0&1	*	1	0
0	1	0	1	0&1	*	0&1	*	0	0
0	1	1	1	0&1	*	0&1	*	1	1
1	–	–	–	0&1	*	0&1	*	0&1	0&1
* NOT USED									

COMPONENTS OF CC AND PU COMMUNICATION CONTROL (CSC) REGISTER

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	APE PU	REM CGP	REM EPU	-	-	-	-	-	-	-	APE PU	ASW EPU	-	-	AP1 PU	APO PU	ASW 1PU	ASW 0PU

PARITY ERROR

ASW ERROR

17	16	15	PARITY ERROR
1	0	0	FAILURE OCCURRED
0	0	1	NORMAL PU ORDER
0	1	0	GCP ORDER

3	2	FAILURE
0	1	BUS 0
1	0	BUS 1

1	0	CONTR
0	1	0
1	0	1

PERIPHERAL ERROR SUMMARY (PES) REGISTER

UNIT TYPE

MEMBER NUMBER

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	UTY 4	UTY 3	UTY 2	UTY 1	UTY 0	MEM N6	MEM N5	MEM N4	MEM N3	MEM N2	MEM N1	MEM N0	-	-	-	-	-	-	-	-	-	-

K-CODE

BITS	OCTAL	PU SELECTED
21-10	121	PPI
21-10	117	I/O UNIT SELECTOR

ENABLE (E) REGISTER

IB1RFLC01 REGISTER – PU STATUS

BIT	INDICATION WHEN SET TO 1
0	Maintenance access
1	Receive on bus 0 or 1
2	Send on bus 0
3	Send on bus 1
7	Diagnostic requested
8	Removed from service via TTY
12	Unit out-of-service
16	Cannot receive on bus 0
17	Cannot send on bus 0
18	Cannot receive on bus 1
19	Cannot send on bus 1
20-23	Maintenance state

IB1RFLC01 REGISTER – PU MAINTENANCE STATE

23	22	21	20	CONDITION REPORTED
0	0	0	0	Normal
0	0	0	1	Diagnostic state
0	0	1	0	Exercise state
0	0	1	1	Fault recognition – error analysis
0	1	0	0	Controller removed – listen state
0	1	0	1	Controller OS – unequipped
0	1	1	0	Seized for diagnostic
0	1	1	1	Controller OS – growth
1	0	0	1	Diagnostic failed
1	1	0	0	Unit not restored in a phase
1	1	1	0	Unit failed to be restored

IB1RFLC05 REGISTER – PU ERROR SOURCE

BIT	INDICATION WHEN SET TO 1
0	CC-0
1	CC-1
2	Controller 0
3	Controller 1
4	PU bus 0
5	PU bus 1
6	Bus 0 at unit
7	Bus 1 at unit
8	Unit removed; diagnostic requested
9	Unit removed; no diagnostic request
10	Fault recognition could not find fault
11	Software error
12	Transient error

Section 5
MINITURIZED UNIVERSAL TRUNK (MUT)
(J1A084A)

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Supporting Documentation

SD-1A338
CD-1A338
TLM-1A338
ED-1A342-11
PK-1A027 Scanner Raw Data Doc
PK-1A028 Remreed NTWK Raw Data Doc
BSP 820-120-151
TOP 231-050-002

F, S, AND T POINT LAYOUT - UNIVERSAL SIGNAL DISTRIBUTOR

	CONTROLLER SCAN POINTS			
	F	S	T	CONDITION
0	0	0	0	IDLE
1	0	0	1	QUAR
2	0	1	0	
3	0	1	1	TPAQ
4	1	0	0	ENABLED
5	1	0	1	
6	1	1	0	TPA
7	1	1	1	POWER OFF

OCTAL ORDER LAYOUT - UNIVERSAL SIGNAL DISTRIBUTOR

22 11	10	9	8 5	4 3	2	1 0
	OPR	BAY	HMP-1	VF	CKT	RELAY

OPR = 0 OPERATE
= 1 RELEASE

F, S, AND T POINT LAYOUT - UNIVERSAL TRUNK SCANNER

	CONTROLLER SCAN POINTS			
	F	S	T	CONDITION
0	0	0	0	POWER ON (OLD)
1	0	0	1	
2	0	1	0	
3	0	1	1	POWER ON (NEW)
4	1	0	0	
5	1	0	1	
6	1	1	0	
7	1	1	1	POWER OFF

OCTAL ORDER LAYOUT - UNIVERSAL TRUNK SCANNER

22 10	9 7	6 4	3 0
	MST SIG ROW	LST SIG ROW	

LAYOUT TO DISPLAY SCAN POINTS AT MASTER CONTROL CENTER

UNIVERSAL TRUNK SCANNER ROW CODE = 001

22 21	20 18	17 16	15 10	9	8 5	4 3	2	1	0
	CODE		FRAME NUMBER	BAY	HMP-1	VF	CKT	PORT	

MINIATURIZED UNIVERSAL TRUNK FRAME
SD 1A338-02

CIRCUIT PACK FUNCTION, TYPE AND LOCATION

TYPE	CIRCUIT PACK FUNCTION	FS	CIRCUIT 0	CIRCUIT 1
FA775 (CONT)	Controller, Register and Translator	13	076-29	176-29
FA776 or FA1776	Scanner Answer Bus Register (SA)	1	080-40	180-40
FA1201	Enable, Buffer Reg, TRNSL and DISCR	2	*80-17	*80-20
FA1202	Buffer Reg, MTCE, and Diagnostic Circuit	2	*80-18	*80-19
FB288	Interrogate Current Drivers	13	076-37	176-37
FB289B (TB)	Scanner Timing	13	076-35	176-35
FB591	Miscellaneous Circuit	3	*76-09	*76-21
FB592	Timing and Differentiating Circuit	3	*80-16	*80-21
FB593	Pulse and Detector Circuit	3	*76-08	*76-23
FC12 (CR0)	Cable Receiver - PU Bits 0 - 7	1	080-34	180-34
FC12 (CR1)	Cable Receiver - PU Bits 8 - 15	1	080-35	180-35
FC12 (CR2)	Cable Receiver - PU Bits 16 - 23	1	080-36	180-36
FC12 (CR3)	Cable Receiver - PU Bits 24 - 27, 36	1	080-38	180-38
FC12 (CR4)	Cable Receiver - PU Enable from CPD	1	080-39	180-39
FC13 (CD0)	Cable Driver - PU Enable Verify to CPD	1	080-41	180-41
FC13 (CD1)	Cable Driver - Scanner Answer	1	080-42	180-42
FC13 (CD2)	Cable Driver - Scanner Answer	1	080-43	180-43
FC135 (SD0)	Scanner Detector	15	076-41	176-41
FC135 (SD1)	Scanner Detector	15	076-39	176-39
FC300	Interface Ckt	4	*76-14	*76-16
FC301	TRIAC Selection Circuit	5	*76-13	*76-18
FC302	First Stage TRIAC CKT - Normal (NFST)	5	*76-10	*76-20
FC302	First Stage TRIAC CKT - Quarantine (QFST)	5	*76-11	*76-19
FC330 (IM0)	Interrogate Matrix	13	076-34	176-34
FC330 (IM1)	Interrogate Matrix	13	076-33	176-33
FC330 (IM2)	Interrogate Matrix	13	076-32	176-32
FC330 (IM3)	Interrogate Matrix	13	076-31	176-31

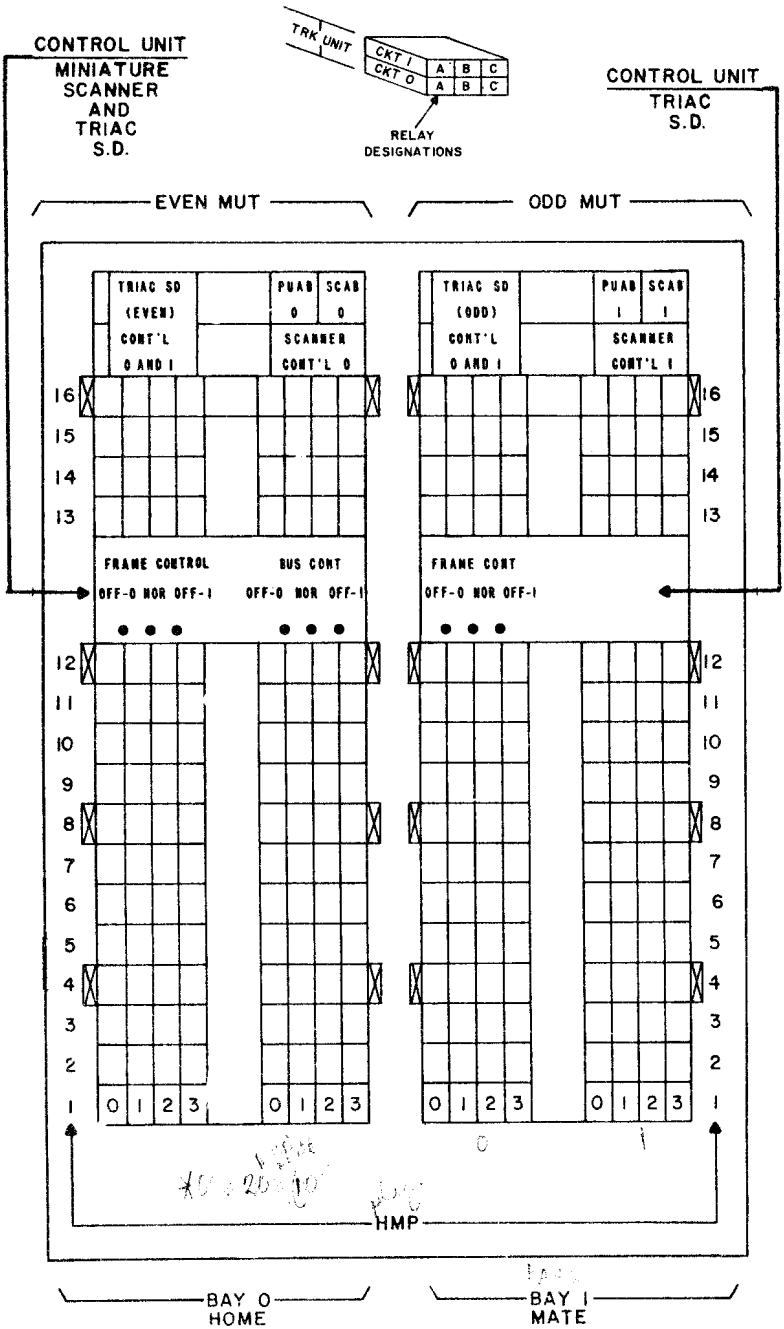
* - Bay 0 and 1

CIRCUIT PACK FUNCTION, TYPE AND LOCATION

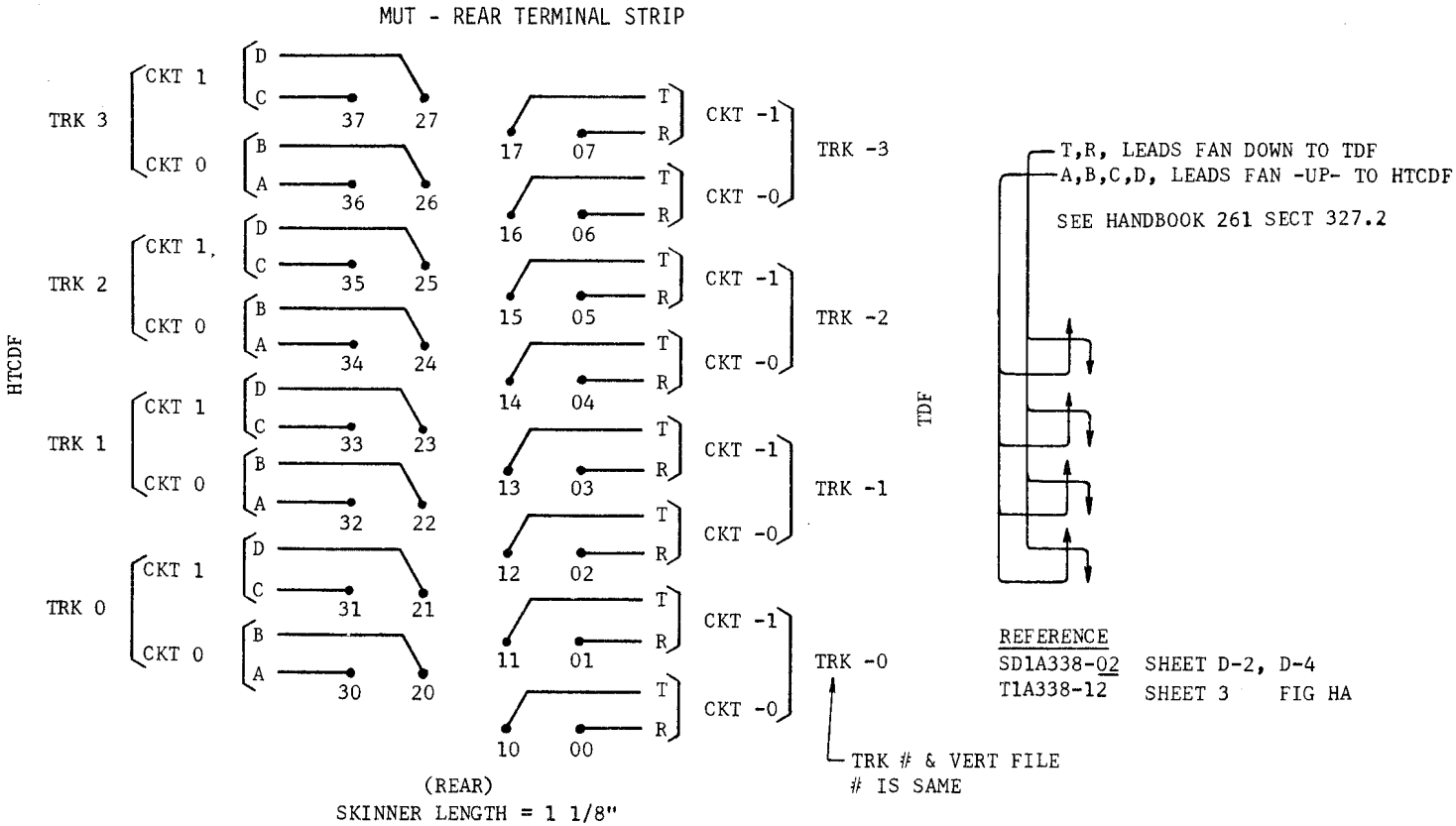
TYPE	CIRCUIT PACK FUNCTION	FS	CIRCUIT 0	CIRCUIT 1
MG002	Second Stage TRIAC SEL & TRIAC CKT (0T24)	6	*14-17A	*14-27C
MG002	Second Stage TRIAC SEL & TRIAC CKT (1T24)	6	*22-17A	*22-27C
MG002	Second Stage TRIAC SEL & TRIAC CKT (2T24)	6	*30-17A	*30-27C
MG002	Second Stage TRIAC SEL & TRIAC CKT (3T24)	6	*38-17A	*38-27C
MG002	Second Stage TRIAC SEL & TRIAC CKT (4T24)	6	*46-17A	*46-27C
MG002	Second Stage TRIAC SEL & TRIAC CKT (5T24)	6	*54-17A	*54-27C
MG002	Second Stage TRIAC SEL & TRIAC CKT (6T24)	6	*64-17A	*64-27C
MG002	Second Stage TRIAC SEL & TRIAC CKT (7T24)	6	*72-17A	*72-27C
MG003	Second Stage TRIAC CKT (0T40)	6	*10-17A	*10-27C
MG003	Second Stage TRIAC CKT (1T40)	6	*18-17A	*18-27C
MG003	Second Stage TRIAC CKT (2T40)	6	*26-17A	*26-27C
MG003	Second Stage TRIAC CKT (3T40)	6	*34-17A	*34-27C
MG003	Second Stage TRIAC CKT (4T40)	6	*42-17A	*42-27C
MG003	Second Stage TRIAC CKT (5T40)	6	*50-17A	*50-27C
MG003	Second Stage TRIAC CKT (6T40)	6	*60-17A	*60-27C
MG003	Second Stage TRIAC CKT (7T40)	6	*68-17A	*68-27C

* - Bay 0 and 1

MUT FRAME J1A084A



⊠ = EXTERNAL POINT TERMINAL STRIP (32 EXT. PTS. EACH)


MUT - REAR TERMINAL STRIP
HTCDF
TRK 3
CKT 1
CKT 0
TRK 2
CKT 1
CKT 0
TRK 1
CKT 1
CKT 0
TRK 0
CKT 1
CKT 0
D
C
B
A
37
27
36
26
35
25
34
24
33
23
32
22
31
21
30
20
T
R
17
07
16
06
15
05
14
04
13
03
12
02
11
01
10
00
CKT -1
CKT -0
TRK -3
TRK -2
TRK -1
TRK -0
TDF
T,R, LEADS FAN DOWN TO TDF
A,B,C,D, LEADS FAN -UP- TO HTCDF
SEE HANDBOOK 261 SECT 327.2
REFERENCE
SD1A338-02 SHEET D-2, D-4
T1A338-12 SHEET 3 FIG HA
TRK # & VERT FILE
IS SAME
(REAR)
SKINNER LENGTH = 1 1/8"

PERIPHERAL BUS
CONNECTORIZED CABLE LOCATION

MINIATURIZED UNIVERSAL TRUNK FRAME

BAY 0

ANSWER BUS CABLES		BUS 0
BITS	IN	OUT
00-07	080-42-310	080-42-110
08-15	080-43-310	080-43-110
ASW	080-44-310	080-44-110

BAY 1

ANSWER BUS CABLES		BUS 1
BITS	IN	OUT
00-07	180-42-310	180-42-110
08-15	180-43-310	180-43-110
ASW	180-44-310	180-44-110

BAY 0

ADDRESS BUS CABLES		BUS 0
BITS	IN	OUT
00-07	080-34-310	080-34-110
08-15	080-35-310	080-35-110
16-23	080-36-310	080-36-110
24-31	080-31-310	080-31-110
32-37	080-31-300	080-31-100

BAY 1

ADDRESS BUS CABLES		BUS 1
BITS	IN	OUT
00-07	180-34-310	180-34-110
08-15	180-35-310	180-35-110
16-23	180-36-310	180-36-110
24-31	180-31-310	180-31-110
32-37	180-31-300	180-31-100

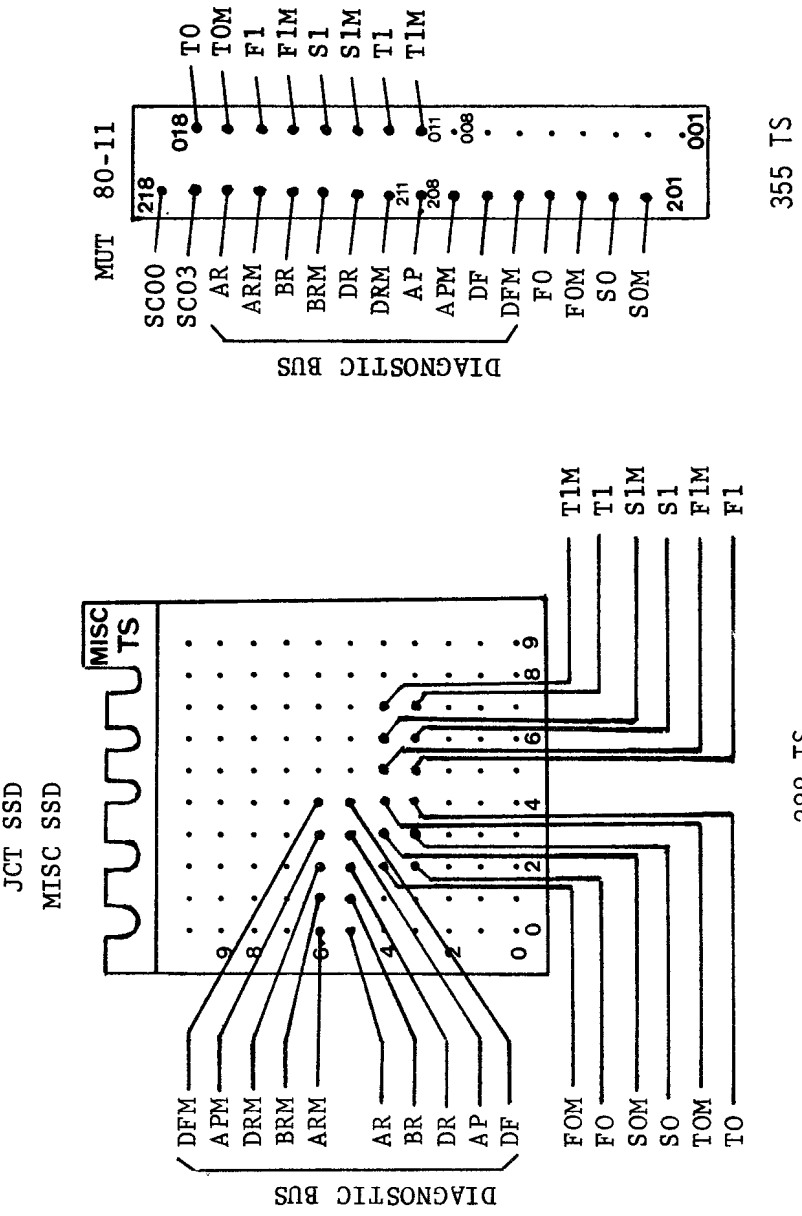
ENABLE AND SYNC POINT LOCATION

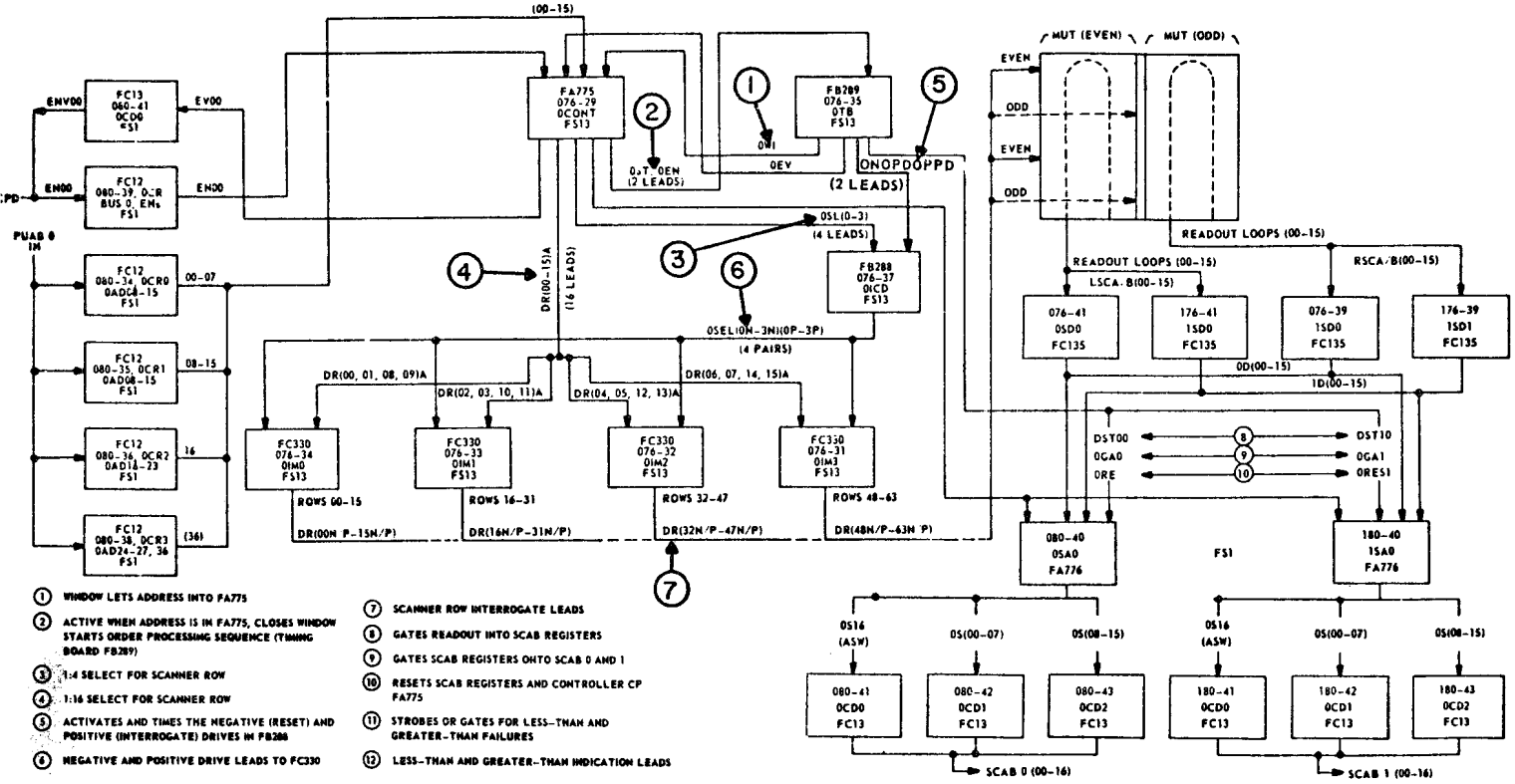
ENABLE	INPUT PIN	COLOR	SYNC POINT	CKT	CPD
00P	080-41-101	BL1W	080-39-308	SC	0
00N	-001	BL2W		SC	0
11P	-102	OR1W	180-39-307	SC	0
11N	-002	OR2W		SC	0
00P	-103	GR1W	080-39-306	RSD	0
00N	-003	GR2W		RSD	0
11P	-104	BR1W	180-39-305	RSD	0
11N	-004	BR2W		RSD	0
00P	-105	SL1W	080-39-304	LSD	0
00N	-005	SL2W		LSD	0
11P	-106	BL1R	180-39-303	LSD	0
11N	-006	BL2R		LSD	0
00P					
00N					
11P					
11N					

ENABLE	INPUT PIN	COLOR	SYNC POINT	CKT	CPD
01P	180-41-101	BL1W	180-39-308	SC	1
01N	-001	BL2W		SC	1
10P	-102	OR1W	080-39-307	SC	1
10N	-002	OR2W		SC	1
01P	-103	GR1W	180-39-306	RSD	1
01N	-003	GR2W		RSD	1
10P	-104	BR1W	080-39-305	RSD	1
10N	-004	BR2W		RSD	1
01P	-105	SL1W	180-39-304	LSD	1
01N	-005	SL2W		LSD	1
10P	-106	BL1R	080-39-303	LSD	1
10N	-006	BL2R		LSD	1

	MUT				SSD - JCT SSD	CMT			
	IN	OUT	IN	OUT		IN	OUT		
	080-11	080-12	180-12	180-11	MISC	080-03	080-62	080-63	180-03
AR	216	216	216	216	050	201	201		
ARM	215	215	215	215	060	001	001		
BR	214	214	214	214	051	202	202		
BRM	213	213	213	213	061	002	002		
DR	212	212	212	212	052	203	203		
DRM	211	211	211	211	062	003	003		
DF	206	206	206	206	054	205	205		
DFM	205	205	205	205	064	005	005		
AP	208	208	208	208	053	204	204		
APM	207	207	207	207	063	004	004		
FO	204			204	032	206/212			206
FOM	203			203	042	006/012			006
SO	202			202	033	207			207
SOM	201			201	043	007			007
TO	018			018	034	208			208
TOM	017			017	044	008			008
F1	016			016	035	/213			201
F1M	015			015	045	/013			001
S1	014			014	036				202
S1M	013			013	046				002
T1	012			012	037				203
T1M	011			011	047				003
SC003	217						006		
SC013							007		
SC00	218						206		
SC10							207		
	FOR 355A TS				FOR 288 MISC TS	FOR 355A TS			

SIGNAL DISTRIBUTOR DIAGNOSTIC BUS FST POINTS, MISC POINTS

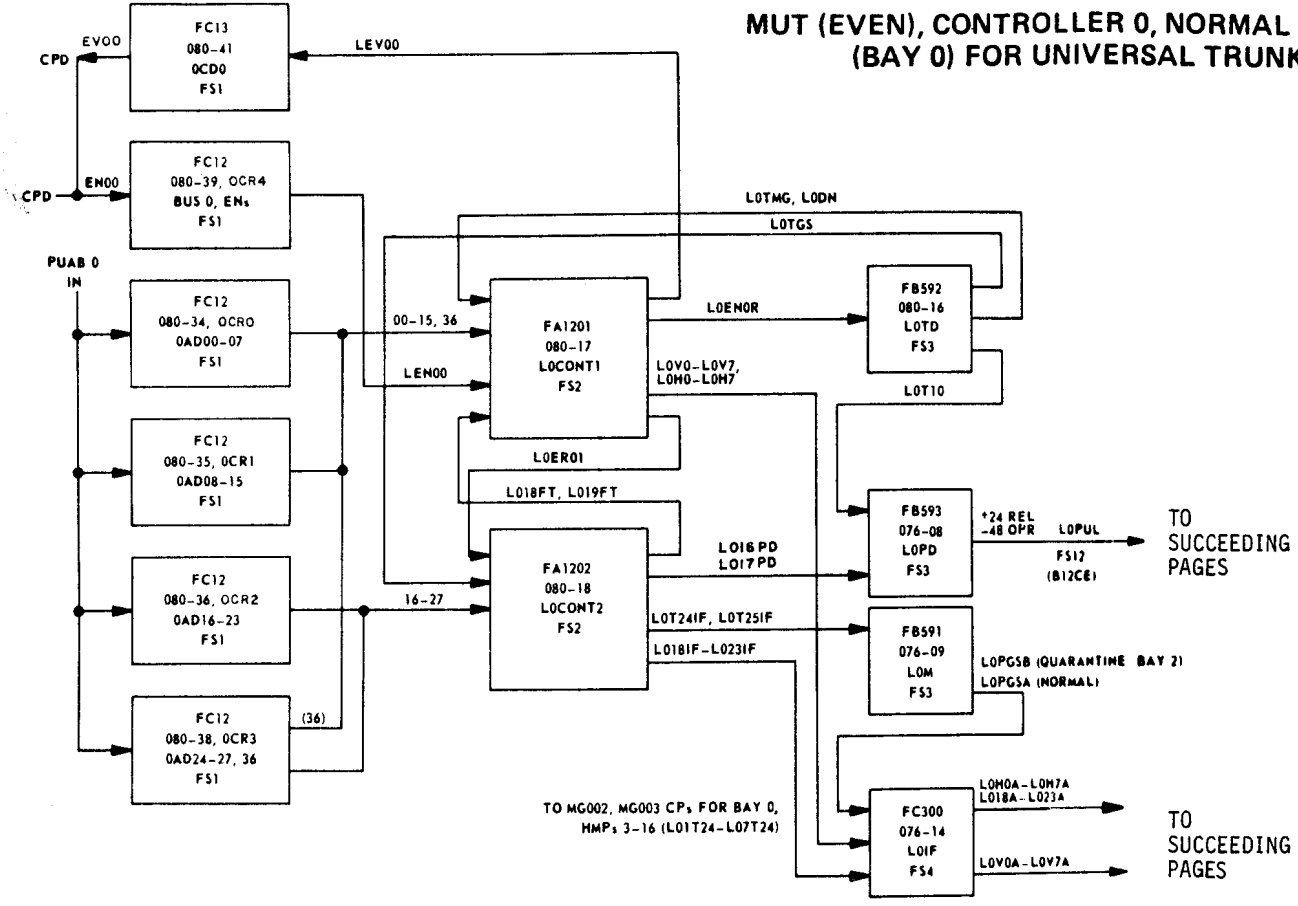


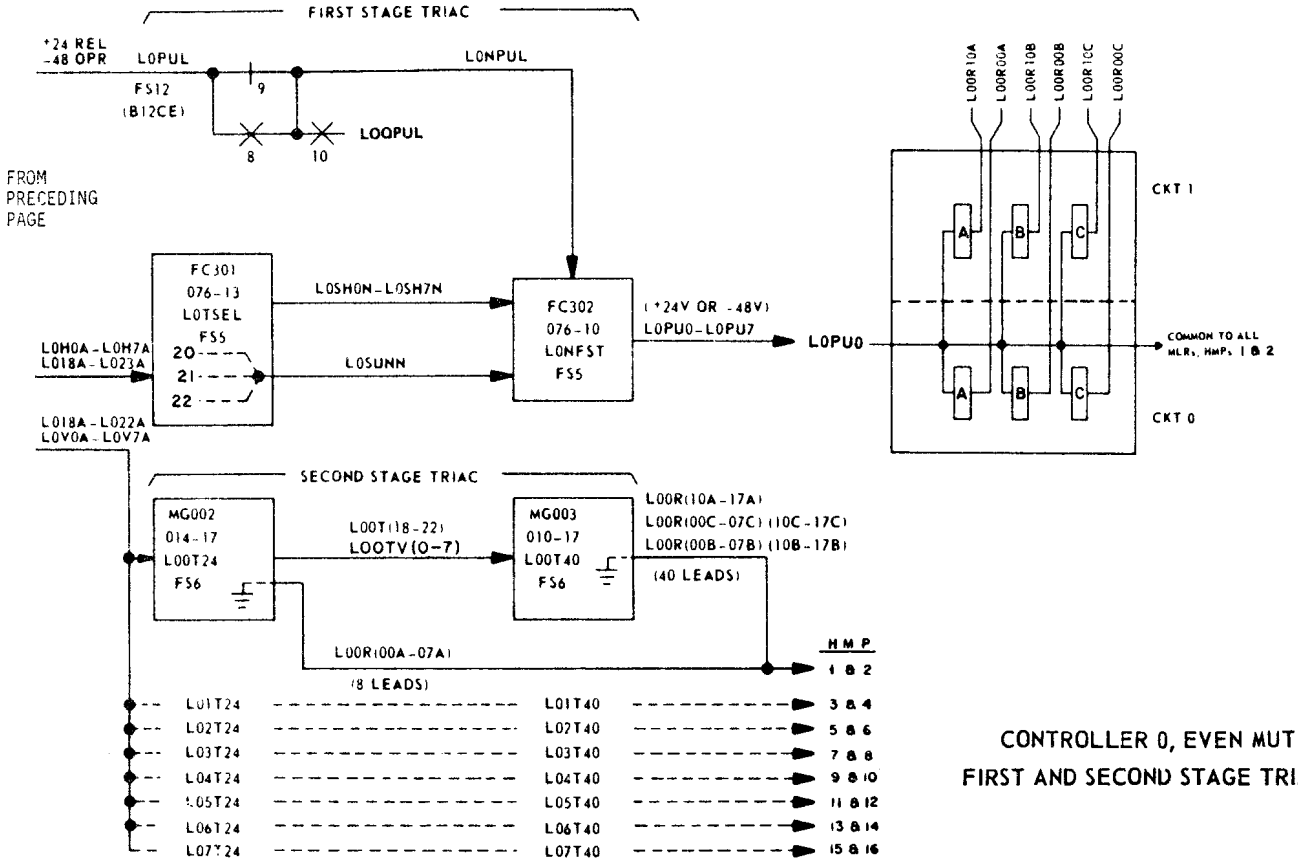


1. WINDOW LETS ADDRESS INTO FA775
2. ACTIVE WHEN ADDRESS IS IN FA775, CLOSES WINDOW STARTS ORDER PROCESSING SEQUENCE (TIMING BOARD FB289)
3. 1:4 SELECT FOR SCANNER ROW
4. 1:16 SELECT FOR SCANNER ROW
5. ACTIVATES AND TIMES THE NEGATIVE (RESET) AND POSITIVE (INTERROGATE) DRIVES IN FB288
6. NEGATIVE AND POSITIVE DRIVE LEADS TO FC330
7. SCANNER ROW INTERROGATE LEADS
8. GATES READOUT INTO SCAB REGISTERS
9. GATES SCAB REGISTERS ONTO SCAB 0 AND 1
10. RESETS SCAB REGISTERS AND CONTROLLER CP FA775
11. STROBES OR GATES FOR LESS–THAN AND GREATER–THAN FAILURES
12. LESS–THAN AND GREATER–THAN INDICATION LEADS

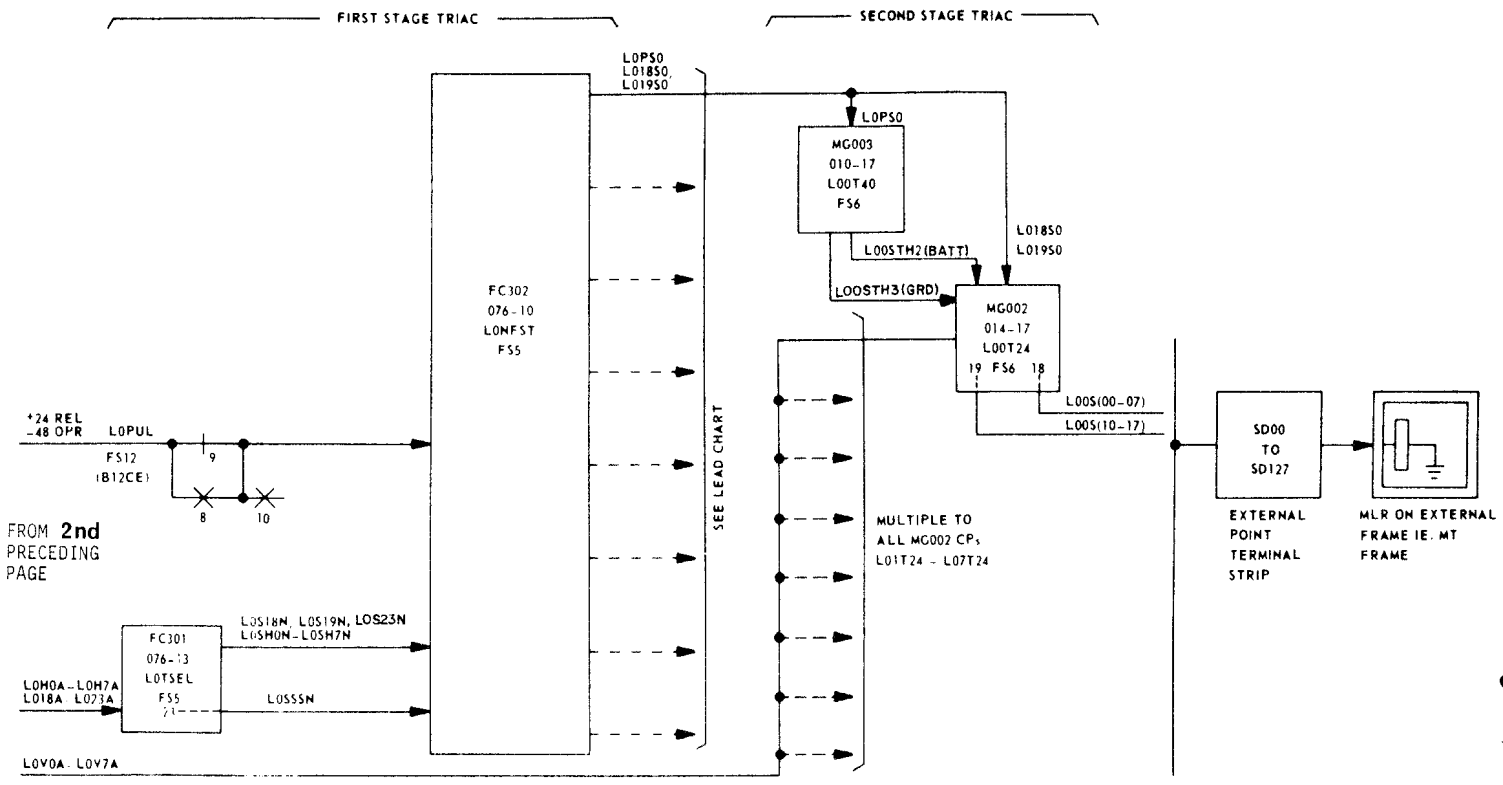
SCANNER BLOCK DIAGRAM (CONTROLLER 0) MUT

MUT (EVEN), CONTROLLER 0, NORMAL ORDER, (BAY 0) FOR UNIVERSAL TRUNK





CONTROLLER 0, EVEN MUT
FIRST AND SECOND STAGE TRIAC



MUT (EVEN), CONTROLLER 0, NORMAL ORDER FOR EXTERNAL POINT SELECTION

PUAB BITS, ROW, DR LEAD AND SEL LEAD MATRIX
(CONTROLLERS 0 AND 1)

PUAB BITS	ROW 0	1	2	3	DRXX A/B
8	0	1	2	3	00
9	8	9	10	11	01
10	16	17	18	19	02
11	24	25	26	27	03
12	32	33	34	35	04
13	40	41	42	43	05
14	48	49	50	51	06
15	56	57	58	59	07
	O/I SEL X.				
	0	1	2	3	

ROW 4	5	6	7	DRXX A/B
4	5	6	7	08
12	13	14	15	09
20	21	22	23	10
28	29	30	31	11
36	37	38	39	12
44	45	46	47	13
52	53	54	55	14
60	61	62	63	15
O/I SEL X.				
0	1	2	3	

NOTE: DRXXA DESIGNATIONS = CONTROLLER 0
DRXXB DESIGNATIONS = CONTROLLER 1

THE CHART SHOWS...

- **PUAB BITS TO ROW SELECTION**
- **DR LEAD SELECTION (SD1A338 – B13AA, B13AB)**
- **SEL LEAD SELECTION (SD1A338 – B13AA, B13AB)**

CIRCUIT PACK LOCATIONS,
FIRST STAGE TRIAC SELECTION
FS5 AND FS10

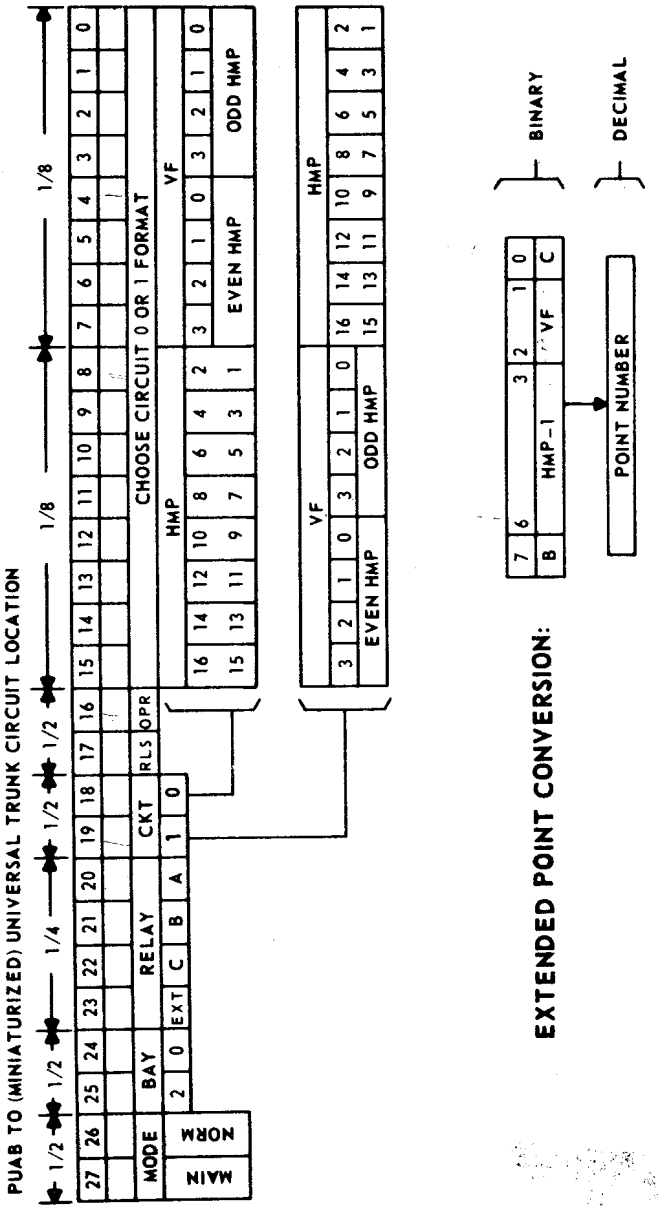
	MUT (EVEN)		HMPs	MUT (ODD)	
	CONTROLLER 0	CONTROLLER 1		CONTROLLER 0	CONTROLLER 1
NORMAL MODE CP LOCATIONS	BAY 0 076-13, 076-10 (FC 301), (FC 302)	BAY 2 076-18, 076-20 (FC 301), (FC 302)	1-16	BAY 0 176-13, 176-10 (FC 301), (FC 302)	BAY 2 176-18, 176-20 (FC 301), (FC 302)
QUARANTINE MODE CP LOCATIONS	BAY 2 076-13, 076-11 (FC 301), (FC 302)	BAY 0 076-18, 076-19 (FC 301), (FC 302)	1-16	BAY 2 176-13, 176-11 (FC 301), (FC 302)	BAY 0 176-18, 176-19 (FC 301), (FC 302)

CIRCUIT PACK LOCATIONS
SECOND STAGE TRIAC SELECTION
FS6 AND FS11

HMP NO.	MUT (EVEN)		MUT (ODD)	
	(MG002)* (MG003)**	(MG002)* (MG003)**	(MG002)* (MG003)**	(MG002)* (MG003)**
	BAY 0	BAY 2	BAY 0	BAY 2
16, 15	072-17, 068-17	072-27, 068-27	172-17, 168-17	172-27, 168-27
14, 13	064-17, 060-17	064-27, 060-27	164-17, 160-17	164-27, 160-27
12, 11	054-17, 050-17	054-27, 050-27	154-17, 150-17	154-27, 150-27
10, 9	046-17, 042-17	046-27, 042-27	146-17, 142-17	146-27, 142-27
8, 7	038-17, 034-17	038-27, 034-27	138-17, 134-17	138-27, 134-27
6, 5	030-17, 026-17	030-27, 026-27	130-17, 126-17	130-27, 126-27
4, 3	022-17, 018-17	022-27, 018-27	122-17, 118-17	122-27, 118-17
2, 1	014-17, 010-17	014-27, 010-27	114-17, 110-17	114-27, 110-27

* MG002-8 LDs 'A' MLRs CKT 0 ON 2 HMPs AND 16 LDs EXTERNAL POINTS
** MG003-40 LDs 'A' MLRs CKT 1, "B" AND "C" MLRs CKTs 0 & 1 ON 2 HMPs

PUAB TO (MINIATURIZED) UNIVERSAL TRUNK CIRCUIT LOCATION



5.18

FIRST STAGE TRIAC SELECT LEADS FS5 AND FS10

SECOND STAGE TRIAC SELECT LEADS FS6 AND FS11

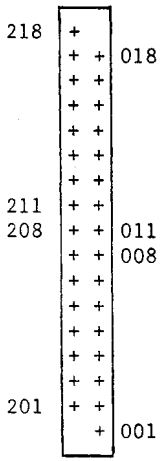
MUT FS5 EVEN	MUT FS10 ODD	BAY 0	BAY 2	HORZ NO.	HMP NO.	MUT FS6 EVEN	MUT FS11 ODD	BAY 0	BAY 2	HORZ NO	CKT 0	CKT 1	VF 0	VF 1	VF 2	VF 3	MLR
L	R	0	1	PU7	16	L	R	0	1	7R	0	1	4	5	6	7	A, B, OR C
					15								0	1	2	3	
				PU6	14					6R			4	5	6	7	
					13								0	1	2	3	
				PU5	12					5R			4	5	6	7	
					11								0	1	2	3	
				PU4	10					4R			4	5	6	7	
					9								0	1	2	3	
				PU3	8					3R			4	5	6	7	
					7								0	1	2	3	
				PU2	6					2R			4	5	6	7	
					5								0	1	2	3	
				PU1	4					1R			4	5	6	7	
					3								0	1	2	3	
				PU0	2					0R			4	5	6	7	
L	R	0	1		1	L	R	0	1		0	1	0	1	2	3	A, B, OR C

HMP	"H" LD.	VF 0	VF 1	VF 2	VF 3
		"V" LD.			
16	7	4	5	6	7
15		0	1	2	3
14	6	4	5	6	7
13		0	1	2	3
12	5	4	5	6	7
11		0	1	2	3
10	4	4	5	6	7
9		0	1	2	3
8	3	4	5	6	7
7		0	1	2	3
6	2	4	5	6	7
5		0	1	2	3
4	1	4	5	6	7
3		0	1	2	3
2	0	4	5	6	7
1		0	1	2	3

HMP TO "H" AND "V" LEADS

EXTERNAL SSD POINT TERMINAL STRIP LOCATION

355 TS PCH ◀	22-01 HMP 4	38-01 HMP 8	54-01 HMP 12	72-01 HMP 16	22-44 HMP 4	38-44 HMP 8	54-44 HMP 12	72-44 HMP 16 ◀ (355 TYPE) TS LOCATION
201	000	032	064	096	128	160	192	224
203	001	033	065	097	129	161	193	225
205	002	034	066	098	130	162	194	226
207	003	035	067	099	131	163	195	227
211	004	036	068	100	132	164	196	228
213	005	037	069	101	133	165	197	229
215	006	038	070	102	134	166	198	230
217	007	039	071	103	135	167	199	231
202	008	040	072	104	136	168	200	232
204	009	041	073	105	137	169	201	233
206	010	042	074	106	138	170	202	234
208	011	043	075	107	139	171	203	235
212	012	044	076	108	140	172	204	236
214	013	045	077	109	141	173	205	237
216	014	046	078	110	142	174	206	238
218	015	047	079	111	143	175	207	239
001	016	048	080	112	144	176	208	240
003	017	049	081	113	145	177	209	241
005	018	050	082	114	146	178	210	242
007	019	051	083	115	147	179	211	243
011	020	052	084	116	148	180	212	244
013	021	053	085	117	149	181	213	245
015	022	054	086	118	150	182	214	246
017	023	055	087	119	151	183	215	247
002	024	056	088	120	152	184	216	248
004	025	057	089	121	153	185	217	249
006	026	058	090	122	154	186	218	250
008	027	059	091	123	155	187	219	251
012	028	060	092	124	156	188	220	252
014	029	061	093	125	157	189	221	253
016	030	062	094	126	158	190	222	254
018	031	063	095	127	159	191	223	255
	SD POINTS							



FRONT VIEW
355 TYPE TS

MG 2 PACK LOCATIONS	
POINTS	MTG PLATE
000-015,128-143	14
016-031,144-159	22
032-047,160-175	30
048-063,176-191	38
064-079,192-207	46
080-095,208-223	54
096-111,224-239	64
112-127,240-255	72

TRIAC SSD POINT NUMBERS, CMT, MUT

HALF 0

FIELD	QUADRANT	ROW 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
0	0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
	1	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
	2	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
	3	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127
1	0	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159
	1	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191
	2	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223
	3	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255
2	0	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287
	1	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319
	2	320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351
	3	352	353	354	355	356	357	358	359	360	361	362	363	364	365	366	367	368	369	370	371	372	373	374	375	376	377	378	379	380	381	382	383
3	0	384	385	386	387	388	389	390	391	392	393	394	395	396	397	398	399	400	401	402	403	404	405	406	407	408	409	410	411	412	413	414	415
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	3	480	481	482	483	484	485	486	487	488	489	490	491	492	493	494	495	496	497	498	499	500	501	502	503	504	505	506	507	508	509	510	511

HALF	FIELD	QUADRANT	ROW	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
1	0	0		512	513	514	515	516	517	518	519	520	521	522	523	524	525	526	527	528	529	530	531	532	533	534	535	536	537	538	539	540	541	542	543
		1		544	545	546	547	548	549	550	551	552	553	554	555	556	557	558	559	560	561	562	563	564	565	566	567	568	569	570	571	572	573	574	575
		2		576	577	578	579	580	581	582	583	584	585	586	587	588	589	590	591	592	593	594	595	596	597	598	599	600	601	602	603	604	605	606	607
		3		608	609	610	611	612	613	614	615	616	617	618	619	620	621	622	623	624	625	626	627	628	629	630	631	632	633	634	635	636	637	638	639
	1	0		640	641	642	643	644	645	646	647	648	649	650	651	652	653	654	655	656	657	658	659	660	661	662	663	664	665	666	667	668	669	670	671
		1		672	673	674	675	676	677	678	679	680	681	682	683	684	685	686	687	688	689	690	691	692	693	694	695	696	697	698	699	700	701	702	703
		2		704	705	706	707	708	709	710	711	712	713	714	715	716	717	718	719	720	721	722	723	724	725	726	727	728	729	730	731	732	733	734	735
		3		736	737	738	739	740	741	742	743	744	745	746	747	748	749	750	751	752	753	754	755	756	757	758	759	760	761	762	763	764	765	766	767
	2	0		768	769	770	771	772	773	774	775	776	777	778	779	780	781	782	783	784	785	786	787	788	789	790	791	792	793	794	795	796	797	798	799
		1		800	801	802	803	804	805	806	807	808	809	810	811	812	813	814	815	816	817	818	819	820	821	822	823	824	825	826	827	828	829	830	831
		2		832	833	834	835	836	837	838	839	840	841	842	843	844	845	846	847	848	849	850	851	852	853	854	855	856	857	858	859	860	861	862	863
		3		864	865	866	867	868	869	870	871	872	873	874	875	876	877	878	879	880	881	882	883	884	885	886	887	888	889	890	891	892	893	894	895
	3	0		896	897	898	899	900	901	902	903	904	905	906	907	908	909	910	911	912	913	914	915	916	917	918	919	920	921	922	923	924	925	926	927
		1		928	929	930	931	932	933	934	935	936	937	938	939	940	941	942	943	944	945	946	947	948	949	950	951	952	953	954	955	956	957	958	959
		2		960	961	962	963	964	965	966	967	968	969	970	971	972	973	974	975	976	977	978	979	980	981	982	983	984	985	986	987	988	989	990	991
		3		992	993	994	995	996	997	998	999	1000	1001	1002	1003	1004	1005	1006	1007	1008	1009	1010	1011	1012	1013	1014	1015	1016	1017	1018	1019	1020	1021	1022	1023

TRIAC SSD POINT NUMBERS, CMT, MUT

HALF	FIELD	"H" SELECT	EVEN "H" SELECT — "V" SELECT *								ODD "H" SELECT — "V" SELECT *							
			0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	0, 1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		2, 3	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
		4, 5	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79
		6, 7	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111
	1	0, 1	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143
		2, 3	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175
		4, 5	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207
		6, 7	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239
	2	0, 1	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271
		2, 3	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303
		4, 5	320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335
		6, 7	352	353	354	355	356	357	358	359	360	361	362	363	364	365	366	367
		0, 1	384	385	386	387	388	389	390	391	392	393	394	395	396	397	398	399
		2, 3	416	417	418	419	420	421	422	423	424	425	426	427	428	429	430	431
		4, 5	448	449	450	451	452	453	454	455	456	457	458	459	460	461	462	463
		6, 7																

HALF	FIELD	"H" SELECT	ODD "H" SELECT — "V" SELECT *							
			0	1	2	3	4	5	6	7
0	0	0, 1	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
		2, 3	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
		4, 5	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
		6, 7	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127
	1	0, 1	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159
		2, 3	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191
		4, 5	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223
		6, 7	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255
	2	0, 1	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287
		2, 3	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319
		4, 5	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351
		6, 7	368	369	370	371	372	373	374	375	376	377	378	379	380	381	382	383
		0, 1	400	401	402	403	404	405	406	407	408	409	410	411	412	413	414	415
		2, 3	432	433	434	435	436	437	438	439	440	441	442	443	444	445	446	447
		4, 5	464	465	466	467	468	469	470	471	472	473	474	475	476	477	478	479
		6, 7															510	511

TEST MLR PTS

1	0	0, 1	512	513	514	515	516	517	518	519	520	521	522	523	524	525	526	527	528	529	530	531	532	533	534	535	536	537	538	539	540	541	542	543
		2, 3	544	545	546	547	548	549	550	551	552	553	554	555	556	557	558	559	560	561	562	563	564	565	566	567	568	569	570	571	572	573	574	575
		4, 5	576	577	578	579	580	581	582	583	584	585	586	587	588	589	590	591	592	593	594	595	596	597	598	599	600	601	602	603	604	605	606	607
		6, 7	608	609	610	611	612	613	614	615	616	617	618	619	620	621	622	623	624	625	626	627	628	629	630	631	632	633	634	635	636	637	638	639
	1	0, 1	640	641	642	643	644	645	646	647	648	649	650	651	652	653	654	655	656	657	658	659	660	661	662	663	664	665	666	667	668	669	670	671
		2, 3	672	673	674	675	676	677	678	679	680	681	682	683	684	685	686	687	688	689	690	691	692	693	694	695	696	697	698	699	700	701	702	703
		4, 5	704	705	706	707	708	709	710	711	712	713	714	715	716	717	718	719	720	721	722	723	724	725	726	727	728	729	730	731	732	733	734	735
		6, 7	736	737	738	739	740	741	742	743	744	745	746	747	748	749	750	751	752	753	754	755	756	757	758	759	760	761	762	763	764	765	766	767
	2	0, 1	768	769	770	771	772	773	774	775	776	777	778	779	780	781	782	783	784	785	786	787	788	789	790	791	792	793	794	795	796	797	798	799
		2, 3	800	801	802	803	804	805	806	807	808	809	810	811	812	813	814	815	816	817	818	819	820	821	822	823	824	825	826	827	828	829	830	831
		4, 5	832	833	834	835	836	837	838	839	840	841	842	843	844	845	846	847	848	849	850	851	852	853	854	855	856	857	858	859	860	861	862	863
		6, 7	864	865	866	867	868	869	870	871	872	873	874	875	876	877	878	879	880	881	882	883	884	885	886	887	888	889	890	891	892	893	894	895
	3	0, 1	896	897	898	899	900	901	902	903	904	905	906	907	908	909	910	911	912	913	914	915	916	917	918	919	920	921	922	923	924	925	926	927
		2, 3	928	929	930	931	932	933	934	935	936	937	938	939	940	941	942	943	944	945	946	947	948	949	950	951	952	953	954	955	956	957	958	959
		4, 5	960	961	962	963	964	965	966	967	968	969	970	971	972	973	974	975	976	977	978	979	980	981	982	983	984	985	986	987	988	989	990	991
		6, 7																															1022	1023

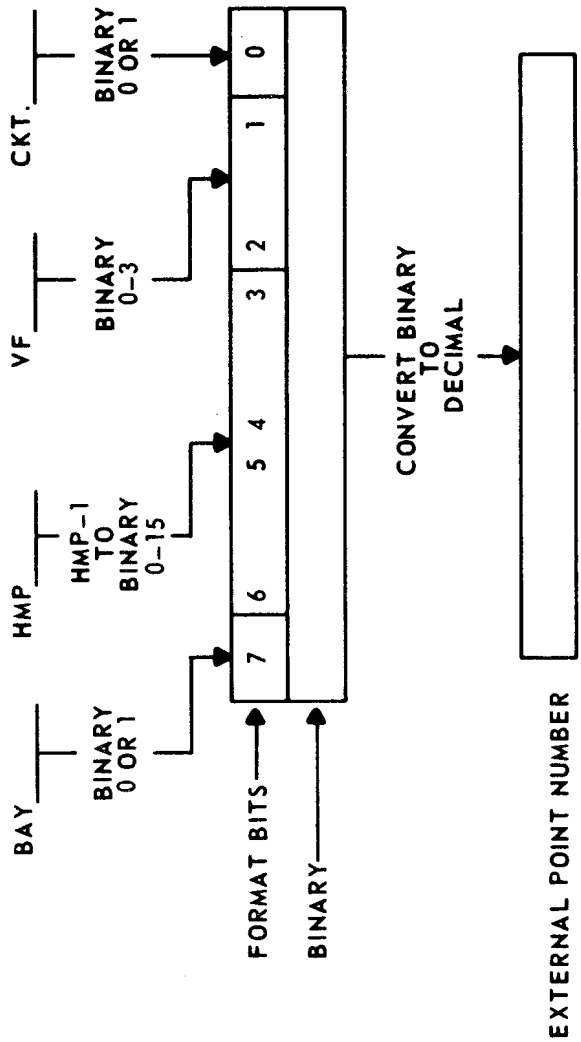
TEST MLR PTS

* EACH "V" SELECT CHOOSES AN ODD AND EVEN NUMBERED POINT.
BIT 18 = 1 CHOOSE EVEN POINT NUMBER
BIT 19 = 1 CHOOSE ODD POINT NUMBER

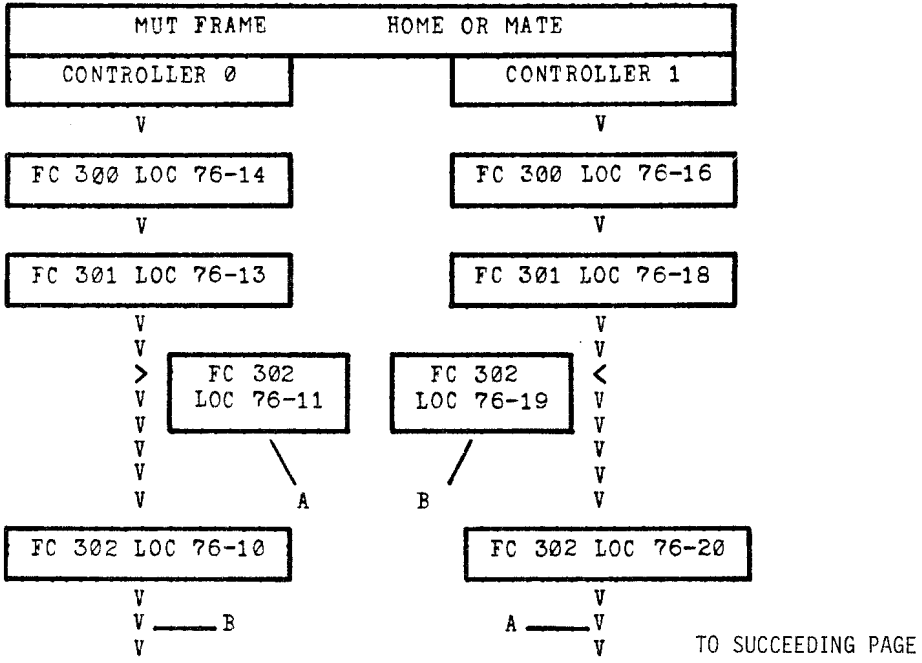
USD, JSD POINT NUMBERS

HALF	FIELD	QUADRANT \ ROW	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
0	3	0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
		1	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
		2	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
		3	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127
1	3	0	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	147	150	151	152	153	154	155	156	157	158	159
		1	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191
		2	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223
		3	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255

CONVERSION OF PHYSICAL LOCATION TO EXTERNAL POINT NUMBER



EXTERNAL POINT LOCATIONS



TO SUCCEEDING PAGE

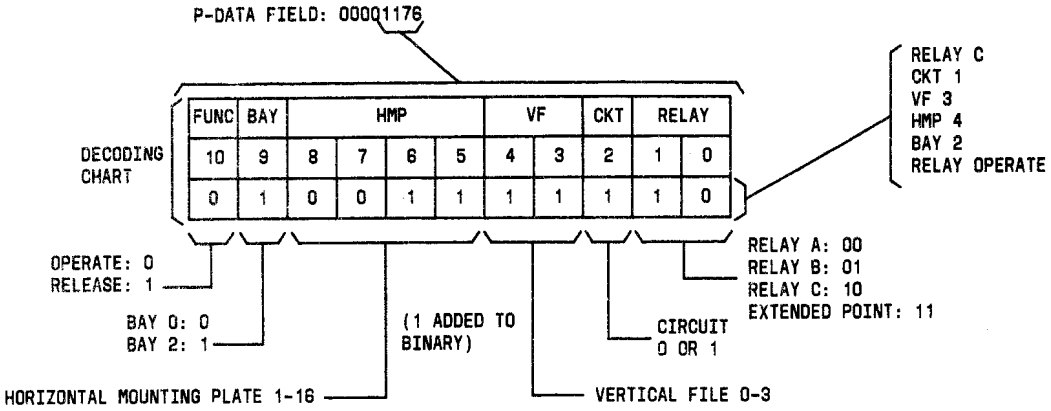
FROM PRECEDING PAGE

V
V
V

	BAY 0				BAY 2			
EXT POINTS	MG002	H	MG003	HMP	MG002	H	MG003	EXT POINTS
112-127	72-17	7	68-17	16,15	72-27	7	68-27	240-255
96-111	64-17	6	60-17	14,13	64-27	6	60-27	224-239
80-95	54-17	5	50-17	12,11	54-27	5	50-27	208-223
64-79	46-17	4	42-17	10, 9	46-27	4	42-27	192-207
48-63	38-17	3	34-17	8, 7	38-27	3	34-27	176-191
32-47	30-17	2	26-17	6, 5	30-27	2	26-27	160-175
16-31	22-17	1	18-17	4, 3	22-27	1	18-27	144-159
00-15	14-17	0	10-17	2, 1	14-27	0	10:27	128-143

CIRCUIT PACK LOCATION OF FERROD MATRIX												
	MUT (EVEN)						MUT (ODD)					
	BAY 0			BAY 0			BAY 0			BAY 0		
	MG001s			MG001s			MG001s			MG001s		
	FERRODS			FERRODS			FERRODS			FERRODS		
HMP NO.	ROWS	15-8	7-0	ROWS	15-8	7-0	ROWS	15-8	7-0	ROWS	15-8	7-0
16, 15	30, 28	072-09,	068-09	62, 60	072-36,	068-36	31, 29	172-09,	168-09	63, 61	172-36,	168-36
14, 13	26, 24	064-09,	060-09	58, 56	064-36,	060-36	27, 25	164-09,	160-09	59, 57	164-36,	160-36
12, 11	22, 20	054-09,	050-09	54, 52	054-36,	050-36	23, 21	154-09,	150-09	55, 53	154-36,	150-36
10, 9	18, 16	046-09,	042-09	50, 48	046-36,	042-36	19, 17	146-09,	142-09	51, 49	146-36,	142-36
8, 7	14, 12	038-09,	034-09	46, 44	038-36,	034-36	15, 13	138-09,	134-09	47, 45	138-36,	134-36
6, 5	10, 8	030-09,	026-09	42, 40	030-36,	026-36	11, 9	130-09,	126-09	43, 41	130-36,	126-36
4, 3	6, 4	022-09,	018-09	38, 36	022-36,	018-36	7, 5	122-09,	118-09	39, 37	122-36,	118-36
2, 1	2, 0	014-09,	010-09	34, 32	014-36,	010-36	3, 1	114-09,	110-09	35, 33	114-36,	110-36
	LSCA			LSCB			RSCA			RSCB		

SCANNER CONTROLLER 0 & 1 - FERROD MATRIX CIRCUIT
MINIATURIZED UNIVERSAL TRUNK (MUT) FRAME



FUNC	UNIVERSAL TRUNK CIRCUIT NUMBER								RELAY	
10	9	8	7	6	5	4	3	2	1	0
1	0	0	1	0	1	1	0	0	0	1

UTCN 14

EXAMPLE OF DETERMINING TRUNK/SERVICE CIRCUIT PHYSICAL LOCATION AND RELAY FUNCTION

SIGNAL DISTRIBUTOR (SD) ERROR PATTERNS

FAILURE CHARACTERISTIC	EQUIPMENT	POSSIBLE CAUSE OF FAILURE
Phase 1 STF	Frame power or software access	• MAC timed out resulting in invalid test • Maintenance interrupt or fuse alarm problem • Mate or test controller not in normal mode or cannot be placed in test point access mode
Phases 2 and 3 STF	SD Controller 0	Diagnostic bus scan points report SD controller fault as follows: 1. States of PU address buffer registers group checks: Scan points — Function • AR or BR — Horizontal or vertical select • DR — Relay select • AP — Apex pulser path 2. Controller Modes Scan points — Function • F, S,T — Test point access, quarantine, test, normal or power-off •DF — Idle or busy condition
Phases 4 and 5 STF	SD Controller 1	
Phases 2 and 4 STF	PU Address Bus 0	PU address bus order fails to enable SD controller or enable verify is not received at CPD enable address
Phases 3 and 5 STF	PU Address Bus 1	• Cable driver(s), cable receiver(s) or bus transformer
Phase 6 Word 1 STF	SD Controller 0 or 1	• Live order or test vertical tests not performed but all other tests passed • PU address bus problem not clear • SD controller mate out-of-service
Phase 6 Words 2-18 STF*	SD Controller 0 or 1	• Test controller in double quarantine – test point access mode (DQTPA) • Service controller operating and releasing relays • Invalid orders processing
Phase 7 STF*	Test controller	Valid load resistor orders sent to each stage 1 output point
Phase 8 STF*	Mate controller	Valid load resistor orders sent to each stage 1 output point
Phase 9 STF*	Test controller	• Load resistor orders with varying field and maintenance modes

* Generic 1E7/1AE7 has additional scan points as follows: pulse detector PD0/PD1, interface and first stage monitors FS0/FS1

TRIAC SIGNAL DISTRIBUTOR ERROR PATTERNS

FAILURE CHARACTERISTIC	SUSPECTED FAULTY CIRCUIT PACK (TYPE)
SD point(s) failing in same vertical file (VF) on all horizontal mounting plates (HMPs)	• Interface circuit (FC300) • Triac selection circuit (FC301) • First stage triac circuit (FC302)
Multiple SD points on two HMPs and same bay	• T-40 point second stage triac circuit (MG003) • T-24 point second stage triac circuit (MG002)
Extended SD points assigned from MUT frame	• T-24 point second stage triac circuit (MG002) • Interface circuit (FC300) • Triac selection circuit (FC301) • First stage triac circuit (FC302)
SD point in same HMP and bay	• T-40 point second stage triac circuit (MG003) • T-24 point second stage triac circuit (MG002)
Crossfire in quarantine mode (may be reported by diagnostic response DR02 TTY message)	• Interface circuit (FC300) • Triac selection circuit (FC301) • First stage triac circuit (FC302)

ORDER SEQUENCE

ENTRY	RELAY	TEST CODE	FUNCTION
1	A	1909	OPERATE
2	A	1908	RELEASE
3	B	1919	OPERATE
4	B	1918	RELEASE
5	C	1929	OPERATE
6	C	1928	RELEASE
7	D	1939	OPERATE
8	D	1938	RELEASE
9	E	1949	OPERATE
10	E	1948	RELEASE
11	F	1959	OPERATE
12	F	1958	RELEASE

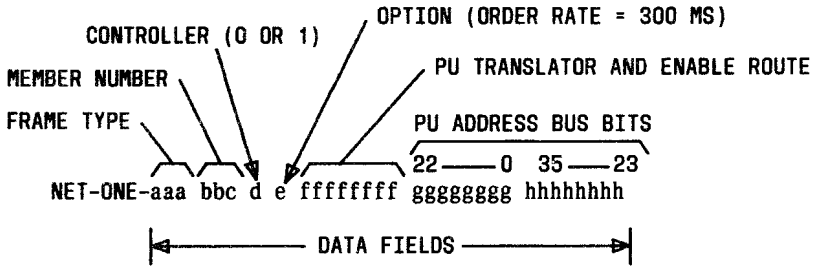
FOR GENERICS 1E6/1AE6 PRECEDE
ORDER CODE WITH A *(STAR)

CODE	FUNCTION	ACTIVITY/COMMAND
0100	BEGIN	SAVE DATA UP TO ACTIVATE CODE FOR USE IN REPETITIVE ORDER=SEQUENCE
0200	ACTIVATE	USE DATA SAVED AND ACT UPON IT REPETITIVELY
03AB	SPECIFIES NUMBER OF DELAY INTERVAL PER ORDER PERIODS	DELAY TO BE INSERTED BETWEEN PREVIOUS ORDER AND FOLLOWING ORDER A = 100 MSEC DELAY INTERVALS B = 25 MSEC DELAY INTERVALS (B IS IGNORED UNLESS A = 0)
0500	STOP	DEACTIVATE PERIPHERAL ORDER BUFFER (POB) ACCESS
0600*	IGNORE RELAY FAILURES	WHEN RELAY FAILURE OCCURS DURING POB ORDER, DO NOT STOP REPETITIVE ACTIONS
* THIS MUST BE KEYED BETWEEN BEGIN AND ACTIVATE CODES OR REPETITIVE ORDER SEQUENCING WILL BE TERMINATED		

CODE EXPLANATIONS

0301ST	DELAY NEXT ORDER BY 25 MSEC	0100ST	BEGIN REPETITIVE ORDER (SEIZE POB)
1929ST	OPERATE C RELAY ON TAT 1	0600ST	IGNORE RELAY FAILURES
0301ST	DELAY NEXT ORDER BY 25 MSEC	1909ST	OPERATE A RELAY ON TAT 1
1928ST	RELEASE C RELAY	0301ST	DELAY NEXT ORDER BY 25 MSEC
0303ST	DELAY NEXT ORDER BY 75 MSEC	1908ST	RELEASE A RELAY
0200ST	ACTIVATE POB		
DIALING SEQUENCE	REPETITIVE ORDERS	DIALING SEQUENCE	REPETITIVE ORDERS

EXAMPLE OF REPETITIVE ORDERS TO OPERATE AND RELEASE A AND C RELAYS ON TAT 1



PU TRANSLATOR AND ENABLE ROUTE

PU TRANSLATOR	ENABLE ROUTE			VARIABLE
	CONTROLLER	PU BUS	CPD	ffffffff
Short Binary – Word	0	0	0	00000007
	0	1	1	00042000
	1	0	1	00002000
	1	1	0	00040000
Long Binary – Word	0	0	0	00000200
	0	1	1	00042200
	1	0	1	00002200
	1	1	0	00040200
USD or SSD	0	0	0	00001400
	0	1	1	00043400
	1	0	1	00003400
	1	1	0	00041400

NET-ONE ORDER WITH VARIABLES IDENTIFIED

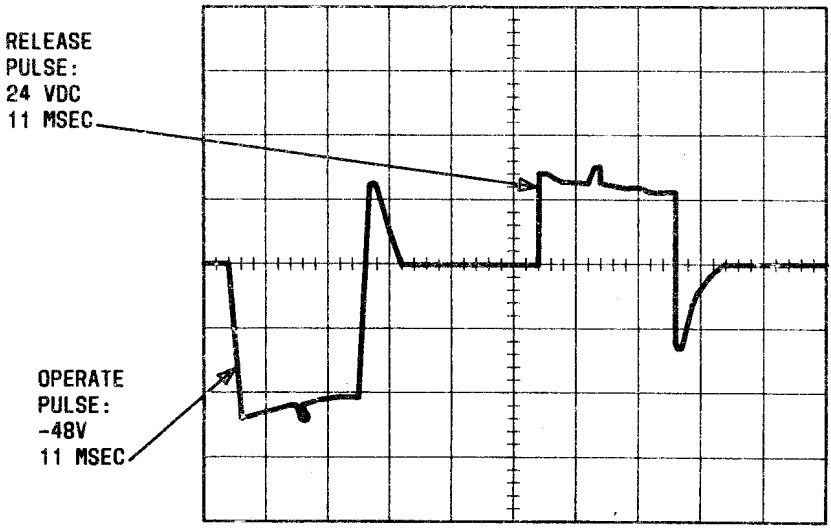
1. Monitor PUL(218) terminal of Pulse and Detector Circuit FB593 for normal operate and release waveforms [FIG. 1] using oscilloscope (Tektronix 465 or equivalent)

   1.1 Set oscilloscope to:

Volts/Div	: 20 V
Time/Div	: 5 MS
Trigger	: Source
Trigger Mode	: Normal
Slope	: Negative
AC-G-DC	: DC
Coupling	: AC
Attenuation	: 10X Probe

   1.2 Connect Vertical Input to PUL (218) on FB593 as follows:

Frame	SD Controller 0	SD Controller 1
MUT (Home)	076-08 (Bay 0)	076-23 (Bay 2)
(Mate)	176-08 (Bay 0)	176-23 (Bay 2)
CMT (Basic)	080-06	080-60
CMT (SSD)	180-07	180-47



NORMAL OPERATE AND RELEASE WAVEFORMS AT PUL (218) FB593

PERIPHERAL BUS CIRCUIT 0 AND 1 TO BUFFER AND MAINTENANCE CIRCUIT FAILURES

FAILURE/TEST * PHASES		SUSPECTED FAULTY CIRCUIT PACKS LOCATION (TYPE FC12 EXCEPT WHERE INDICATED)	FUNCTIONAL FAILURE	PU ADDRESS PARAMETER
AP=1 more than	AP=0 less than	SD Controller 0: 080-17 & 180-17 (FA1201), 080-18 & 180-18 (FA1202), PUAB 0: 080-34, 080-35, 080-36, 080-38, 080-39 & 080-41 (FC13) SD Controller 1: 080-20 & 180-20 (FA1201), 080-19 & 180-19 (FA1202), PUAB 1: 180-34, 180-35, 180-36, 180-38, 180-39 & 180-41 (FC13)	Pulse path select signals are either absent or excessive and condition not detected	One bit set in each register group – HMP(A/B), VF(A/B), Relay Operate/ Release (E), Circuit 0/1(C), Relay A, B, C, or External Point (D), Bay 0/2 (H), Normal/Maintenance (T) Bits 0-27
AR=1 more than	AR=0 less than	SD Controller 0: 080-17 & 180-17 (FA1201) PUAB 0: 080-35 SD Controller 1: 080-20 & 180-20 (FA1201) PUAB 1: 180-35	Horizontal mounting plate (HMP) or vertical file (VF) select signals are either absent or excessive and condition not detected by controller	One bit set in group register A – Bits 8-15
BR=1 more than	BR=0 less than	SD Controller 0: 080-17 & 180-17 (FA1201) PUAB 0: 080-34 SD Controller 1: 080-20 & 180-20 (FA1201) PUAB 1: 180-34	Horizontal mounting plate (HMP) or vertical file (VF) select signals are either absent or excessive and condition not detected by controller	One bit set in group register B – Bits 0-7
DR=1 more than	DR=0 less than	SD Controller 0: 080-18 & 180-18 (FA1202) PUAB 0: 080-36 SD Controller 1: 080-19 & 180-19 (FA1202) PUAB 1: 180-36	Relay A, B, and C or external point select signals are either absent or excessive and condition not detected by controller	One bit set in group register D – Bits 20-23

* Test Phase	SD Controller	PUAB	STF in Test Phases	PU Bus Circuit Suspected To Be Faulty
2	0	0	2 & 4	Circuit 0
3	0	1	3 & 5	Circuit 1
4	1	0		
5	1	1		

CP TYPE REPLACEMENTS

1AE6/1E6 OR EARLIER CP TYPE	CORRESPONDING* REPLACEMENT TYPE
FA1202	FA1810
FB593	FB698
FC300	FC661
FC301	FC662
FC302	FC663
MG003	MG003B
* Generics 1E7/1AE7 and later	

MUT SIGNAL DISTRIBUTOR*

SCAN POINT	CKT 0 BAY 0	CKT 1 BAY 2	CP TYPE
DF	76-08	76-23	FB698
	80-18	80-19	FA1810
	76-09	76-21	FB591
	80-16	80-21	FB592
FS0	76-10	76-20	FC663
	76-11	76-19	FC663
	76-13	76-18	FC662
FS1	76-14	76-16	FC661
	76-09	76-21	FB591
	80-18	80-19	FA1810
PD0	76-10	76-20	FC663
	76-13	76-18	FC662
	76-08	76-23	FB698
	76-14	76-16	FC661
PD1	76-09	76-21	FB591
	76-08	76-23	FB698
	76-13	76-18	FC662
	76-10	76-20	FC663
* MUT frames are designated left (even) and right (odd)			

IMPROVED MINITRUNK DIAGNOSTIC (IMD) TEST GENERICS 1E7/1AE7

SCAN POINT TROUBLE SOURCE INDICATION

SCAN POINT	EXPLANATION
FS0 – First triac stage monitor	Checks each output level from first triac stage for proper voltage/current. PU address data fields are monitored at interface circuit outputs: • Circuit select 0 or 1 (C) • Horizontal select H0 – 7 (A or B)
FS1 – Interface circuit monitor	Checks interface output circuits associated with PU address data fields: • Relay A,B or C select or external point select (D) • Vertical select V0 – 7 (B or A)
PD0 – Pulse detector to load resistor and diodes	Samples amount of current flowing from pulser as follows: Scan Point State PD0 PD1 Definition 0 1 Excessive current 1 0 Insufficient current
PD1 – Pulse detector to diagnostic bus circuit	
DF – Diagnostic status	Indicates SD controller idle or busy state

SD CONTROLLER MODES*

SCAN POINTS	IDLE NORMAL	QUARANTINE/ TEST POINT ACCESS	ENABLE/ NORMAL
F	0	0	1
S	0	1	0
T	0	1	0

* Reported in Phase 6 Word 2

TRIAC SELECTION FAILURES

SCAN POINTS	1ST STG TRIAC	INTFC CKT	1ST STG TRIAC & INTFC CKT	SD CONTR RESET
DF	1	1	1	0
FS0	0	1	0	1
FS1	0	0	1	1

PULSER DETECTOR FAILURES

SCAN POINTS	PLSR CUR LESS THAN	PLSR CUR MORE THAN	IDLE CONTR IN TPA2 OR QTPA2	IDLE CONTR IN DQTPA2 OR TPA2
DF	1	1	0	0
PD0	1	0	0	1
PD1	0	1	0	0

SCANNER ERROR PATTERNS

FAILURE CHARACTERISTICS	POSSIBLE CAUSE OF FAILURE
Phases 1 & 3 – STF	Scanner controller 0
Phases 2 & 4 – STF	Scanner controller 1
Phases 1 & 4 – STF	• PU address bus 0 (PUAB 0) • Scanner answer bus 0 (SCAB 0)
Phases 2 & 3 – STF	• PU address bus 1 (PUAB 1) • Scanner answer bus 1 (SCAB 1)
Phases 1 through 4 – STF	Open ferrod sensor interrogate winding
Scanner answer reply AN00-15 or scanner ASW, AN16*	• Cable driver – -output circuit • Open ferrod readout loop • Ferrod matrix circuit
Multiple failures in AN00-15 & ASW-S*	• Scanner answer bus register circuits • Controller, register, and translator circuits • Scanner timing circuits • Interrogate current driver circuits • Interrogate matrix circuits • Scanner detector
* This failure may be reported by F-level interrupt TTY message	

TROUBLE SHOOTING THE TRIAC SIGNAL DISTRIBUTOR

I. USE DIAGNOSTICS AND REPLACE PACKS INDICATED.

II. USE METHOD OF "SUCCESSIVE CIRCUIT DIVISION" TO ISOLATE FAULTS.

1. CHECK MAJOR "PIVOT" POINTS.

A. PULSE AND DETECTOR CIRCUIT PACK, FB 593, TERMINAL 218 LEAD PUL (PULSE).

B. INTERFACE CIRCUIT PACK, FC 300, INPUTS AND OUTPUTS.

2. OBSERVE CIRCUIT PACK INPUT AND OUTPUT WAVEFORMS.

A. INPUT WAVEFORM INCORRECT - PROCEED TOWARDS BUS CIRCUITRY.

B. OUTPUT WAVEFORM CORRECT - PROCEED TOWARDS TRUNK CIRCUITRY.

C. INPUT CORRECT, OUTPUT INCORRECT - REPLACE CIRCUIT PACK OR FIND FAULT IN LINE TO SUCCEEDING CIRCUIT PACK OR PACKS.

III. STUDY WAVEFORMS

1. COMPARE GOOD AND FAULTY SELECTIONS.

2. WAVEFORMS TO EXPECT

A. INPUTS FROM BUS

a. SELECT - NEGATIVE GOING ABOUT .5 us PULSE FROM ABOUT 1.2v.

b. NO SEL - CONSTANT ABOUT 1.2v.

B. OUTPUT OF +3v LOGIC (CDI) SEE NOTE.

a. LO - $\leq$ .2v

b. HI - $\geq$ .6v - NEXT STAGE IS A TRANSISTOR BASE.
$\geq$ 1.0v- NEXT STAGE IS A CDI INPUT BUFFER.

c. TIMING WAVEFORMS FROM FB592 (TD), TIMING AND DIFFERENTIATOR, ARE ALL CDI LOGIC LEVEL.

d. INTERFACE PACK WAVEFORMS (FC300)

a) INPUT LO $\leq$ .2v
HI $\geq$ .6v

b) OUTPUT

e. PULSER

a) OPERATE

b) RELEASE

c) DECTECTOR ACTIVATED

f. WAVEFORMS ALONG ML RELAY PULSE PATH.

a) FIRST STAGE

b) SECOND STAGE

g. VOLTAGE WAVEFORM ALONG TRIAC GATE SELECTION CIRCUIT.

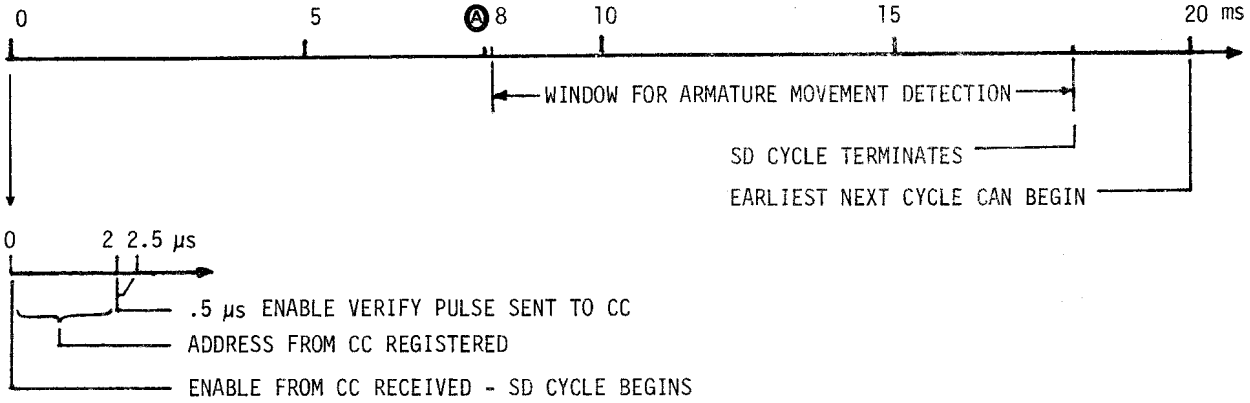
H. CURRENT WAVEFORMS

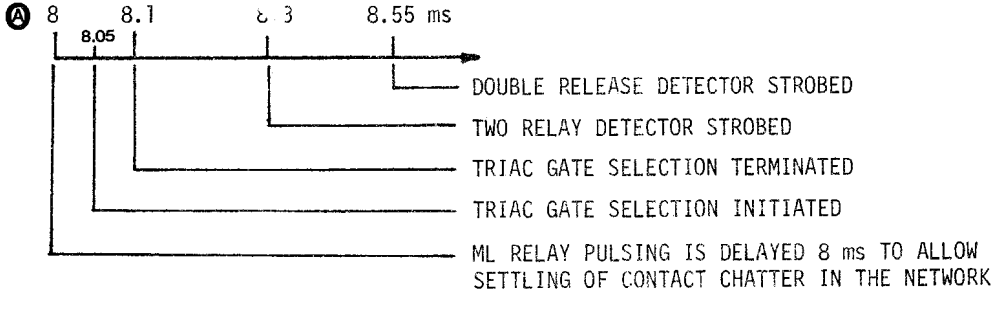
a) ML RELAY PULSE PATH

LAST RESORT!

b) TRIAC GATE CURRENT PATH

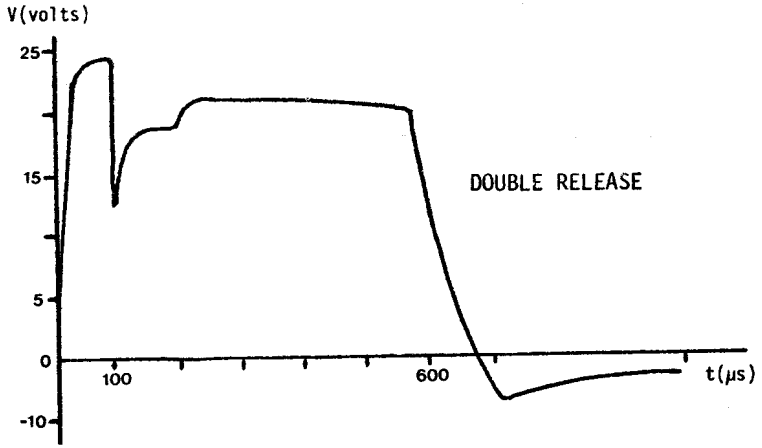
TRIAC SIGNAL DISTRIBUTOR TIMING SEQUENCE

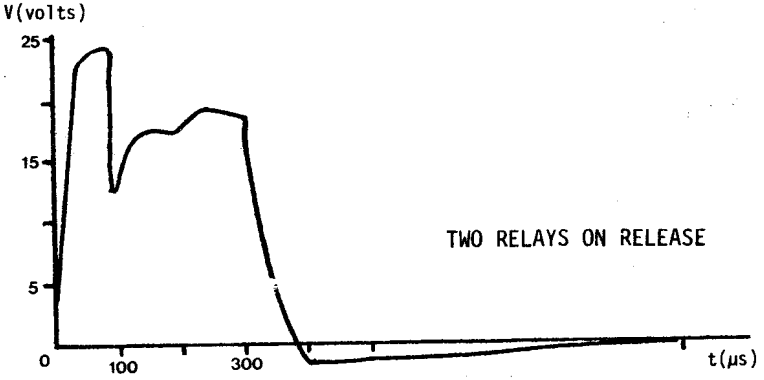


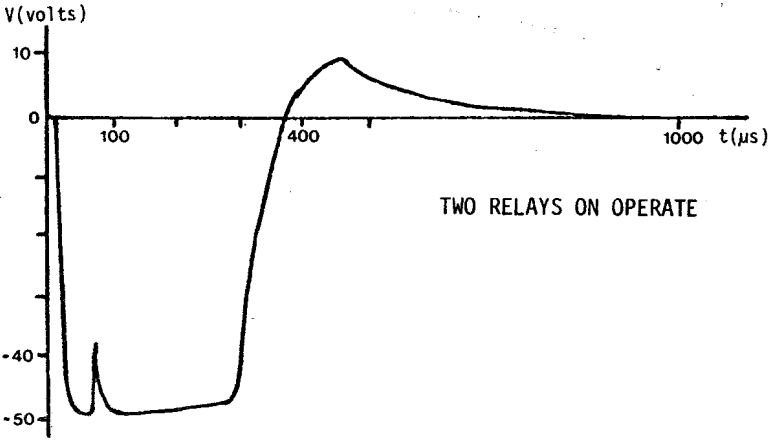


PULSER WAVE FORMS, FB593 (TERM 218)

FAULT CONDITIONS

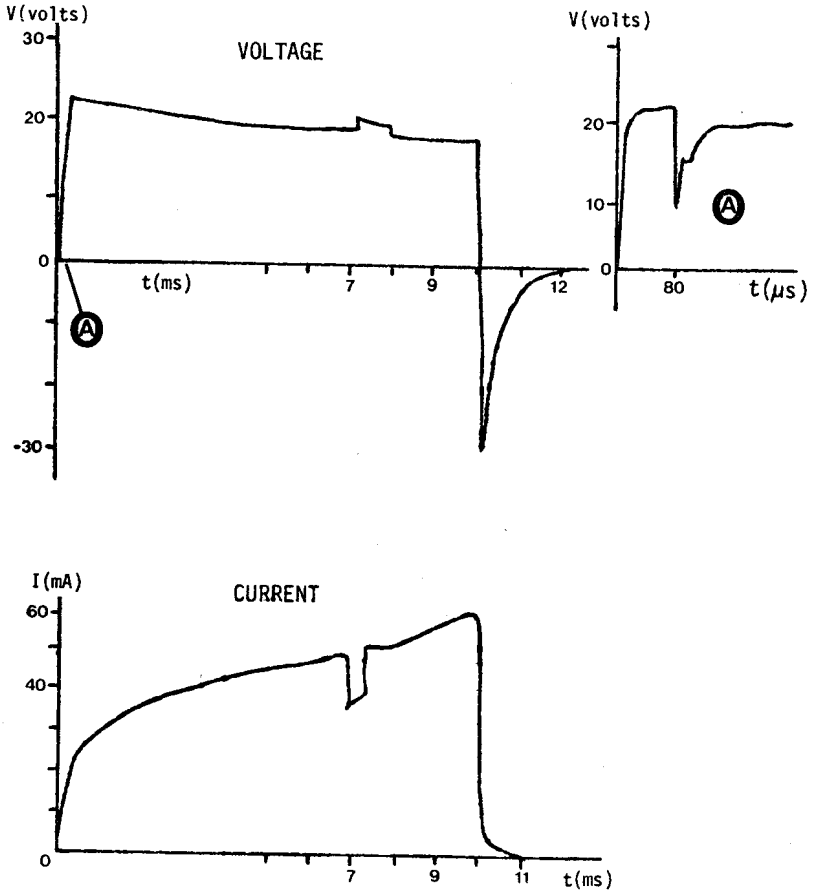






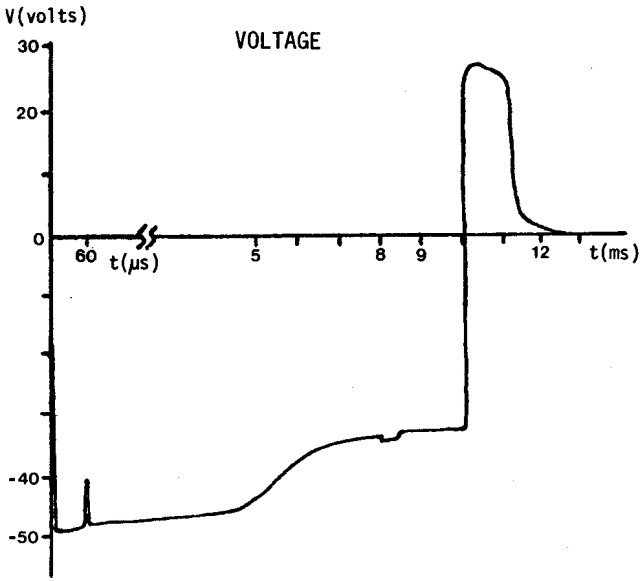
PULSER WAVE FORMS, FB593 (TERM 213)

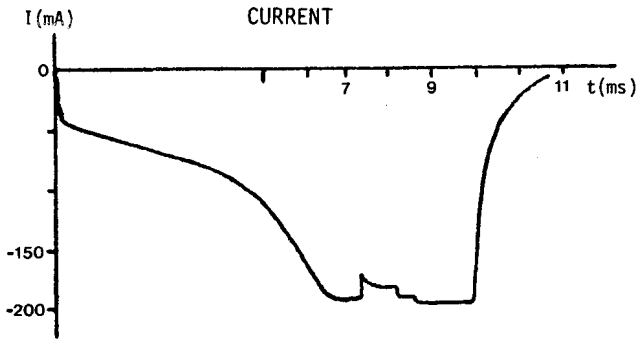
RELEASE +V = 26.25V, -V = -52.5V (AM RELAY)



PULSER WAVE FORMS, FB593 (TERM 213)

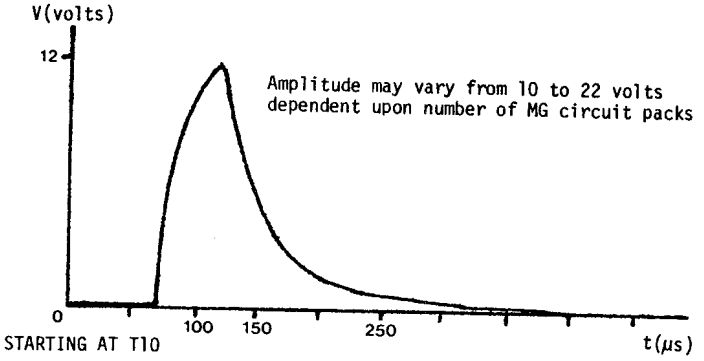
OPERATE +V = 26.25V, -V = -52.5V (AM RELAY)



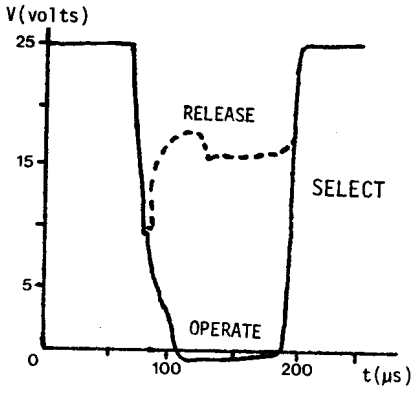


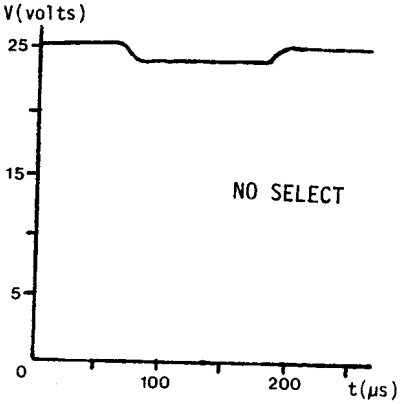
TRIAC GATE SELECTION WAVEFORMS

VERTICAL, HORIZONTAL BITS 18-20 OUTPUT OF FC300 OR INPUT FROM FC324 OR FB591 CURRENT SOURCE TO FC300

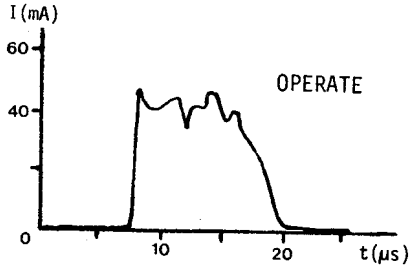


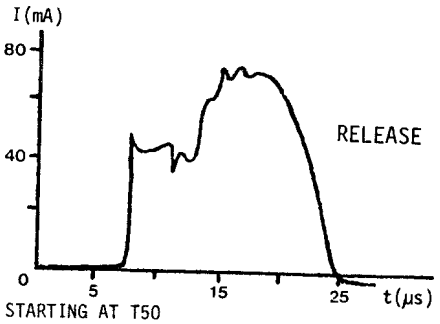
VOLTAGE AT ISOLATION DIODE OF TRIAC GATE CURRENT TRANSISTORS (EXAMPLE - L022F AT FC322)





TRIAC GATE SELECTION CURRENT AT INPUT TO 2ND STAGE TRIAC





Section 6

PERIPHERAL UNIT CONTROLLER – DIGITAL CARRIER TRUNK (PUC – DCT)
PERIPHERAL UNIT CONTROLLER – DATA LINK (PUC – DL)

CONTENTS

1. PUC – DCT

J98732A	PUC-DCT Specifications
UNIT TYPE 61	
SD/CD-3C316	DCT Frame Application
SD/CD-1A477	PUC-DCT
PK-1A473	PUC Diagnostics
ED-3C786-10	Cabling
801-505-156	DCT Equipment Design Requirements

Supporting Documentation

TOP 231-050-015	DCT
BSP 231-049-101	DCT Maintenance Considerations
BSP 231-090-152	DCT Feature

DCT PLUG-IN UNITS

CCU	Combined Channel Unit	J98732BA
TU	Transmit Unit	J98726AA
RU	Receive Unit	J98726AB
SU	Syndes Unit	J98726AG
LIU	Line Interface Unit	J98732AC,AF,AH
TPU	Trunk Processing Unit	J98726AD
A&DCU	Alarm and Digroup Control Unit	J98732AA
DCU	Digroup Control Unit	J98732AB
OIU	Office Interface Unit	J98726AJ
SPTS	Signaling Path Test Set	J98732MH
MBTS	Maintenance Bank Test Set	J98732MJ
PCU	Power Converter Unit	J98738OC
PDU	Power Distribution Unit	J98726AK

2. PUC – DL Applications: RSS, ETS, CCIS

J1A099A	
UNIT TYPE 61	
SD/CD-1A478	PUC DL
PK-1A473	PUC Diagnostics
ED-1A409-10	Cabling

Supporting Documentation

TOP 231-050-027	PUC-DL
BSP 231-090-062	PUC Feature
BSP 231-045-430	PUC Software
BSP 231-037-020	PUC-DL Maintenance
IPC 405-069	

PERIPHERAL UNIT CONTROLLER

WORD LAYOUTS

DCT TRUNK CIRCUIT NUMBER (TCN)

22 — 15	14 — 9	8	7 — 0
	FRAME NUMBER/2	HALF	TRUNK CIRCUIT NUMBER

DCT TRUNK SCANNER NUMBER (TSN)

22 — 16	15 — 10	9	8 — 1	0
	FRAME NUMBER/2	HALF	TRUNK CIRCUIT NUMBER	SC

SC = SCAN POINT

DCT TRUNK DISTRIBUTOR NUMBER (TDN)

22 — 17	16 — 11	10	9 — 2	1	0
	FRAME NUMBER/2	HALF	TRUNK CIRCUIT NUMBER	0	0

DCT PERIPHERAL EQUIPMENT NUMBER (PTW)

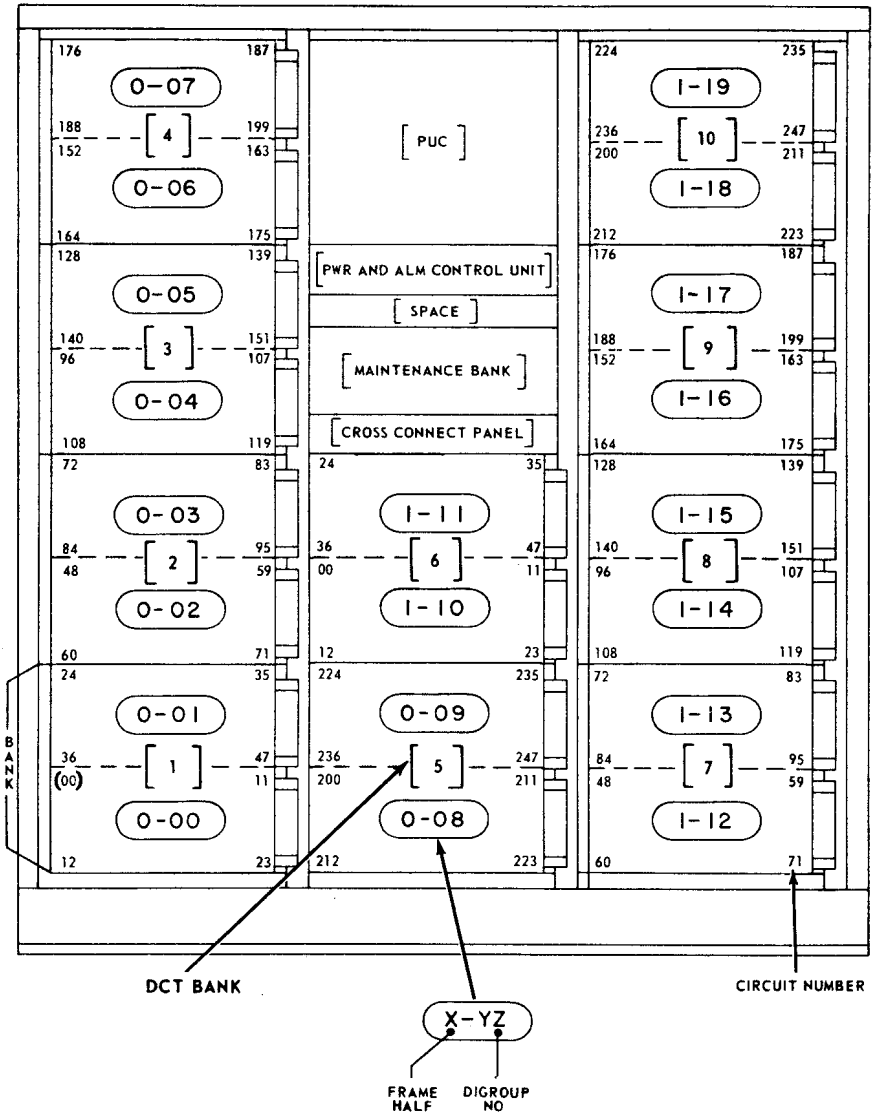
22	21	20	19	18 — 16	15 — 10	9	8 — 1	0
1	1	0	FI	0 0 0	FRAME NUMBER/2	HALF	TRUNK CIRCUIT NUMBER	0

FI = DCT FRAME INDICATOR (=1)

PUC DATA LAYOUT

22		20	19	18	17 — 10	9 — 6	5 — 0
FP		CP	CO	BU		OPERATION	

PUC DCT CHANNEL BANK LAYOUT



FRAME HALF	DIGROUPS	CIRCUIT NUMBERS
0	00-09	00-119 128-247
1	10-19	00-119 128-247

DCT FRAME HALF 0

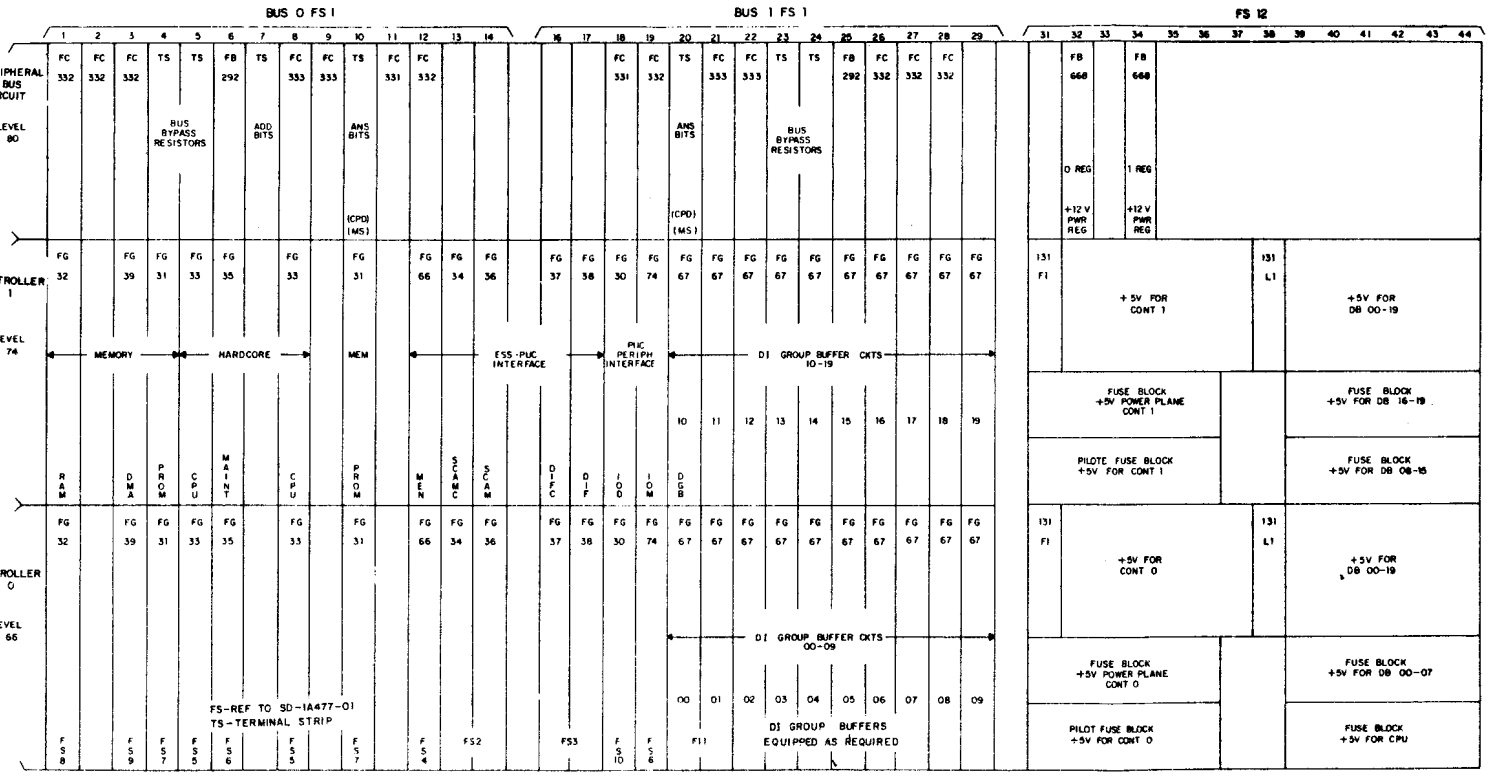
CCU NO.	1		2		3		4		5		BANK
	A	B	A	B	A	B	A	B	A	B	DIGROUP
	0	1	2	3	4	5	6	7	8	9	DIGROUP
1	0	24	48	72	96	128	152	176	200	224	
2	1	25	49	73	97	129	153	177	201	225	
3	2	26	50	74	98	130	154	178	202	226	
4	3	27	51	75	99	131	155	179	203	227	
5	4	28	52	76	100	132	156	180	204	228	
6	5	29	53	77	101	133	157	181	205	229	
7	6	30	54	78	102	134	158	182	206	230	
8	7	31	55	79	103	135	159	183	207	231	
9	8	32	56	80	104	136	160	184	208	232	
10	9	33	57	81	105	137	161	185	209	233	
11	10	34	58	82	106	138	162	186	210	234	
12	11	35	59	83	107	139	163	187	211	235	
13	12	36	60	84	108	140	164	188	212	236	
14	13	37	61	85	109	141	165	189	213	237	
15	14	38	62	86	110	142	166	190	214	238	
16	15	39	63	87	111	143	167	191	215	239	
17	16	40	64	88	112	144	168	192	216	240	
18	17	41	65	89	113	145	169	193	217	241	
19	18	42	66	90	114	146	170	194	218	242	
20	19	43	67	91	115	147	171	195	219	243	
21	20	44	68	92	116	148	172	196	220	244	
22	21	45	69	93	117	149	173	197	221	245	
23	22	46	70	94	118	150	174	198	222	246	
24	23	47	71	95	119	151	175	199	223	247	
	10	11	12	13	14	15	16	17	18	19	DIGROUP
CCU NO.	A	B	A	B	A	B	A	B	A	B	DIGROUP
	6		7		8		9		10		BANK

CIRCUIT NUMBERS — SOFTWARE — HARDWARE NUMBERS

DCT FRAME HALF 1

NOTE: Circuit numbers 120 through 127 and 248 through 255 are not used for DCT application.

DCT DIGROUP TO CIRCUIT NUMBER CONVERSION



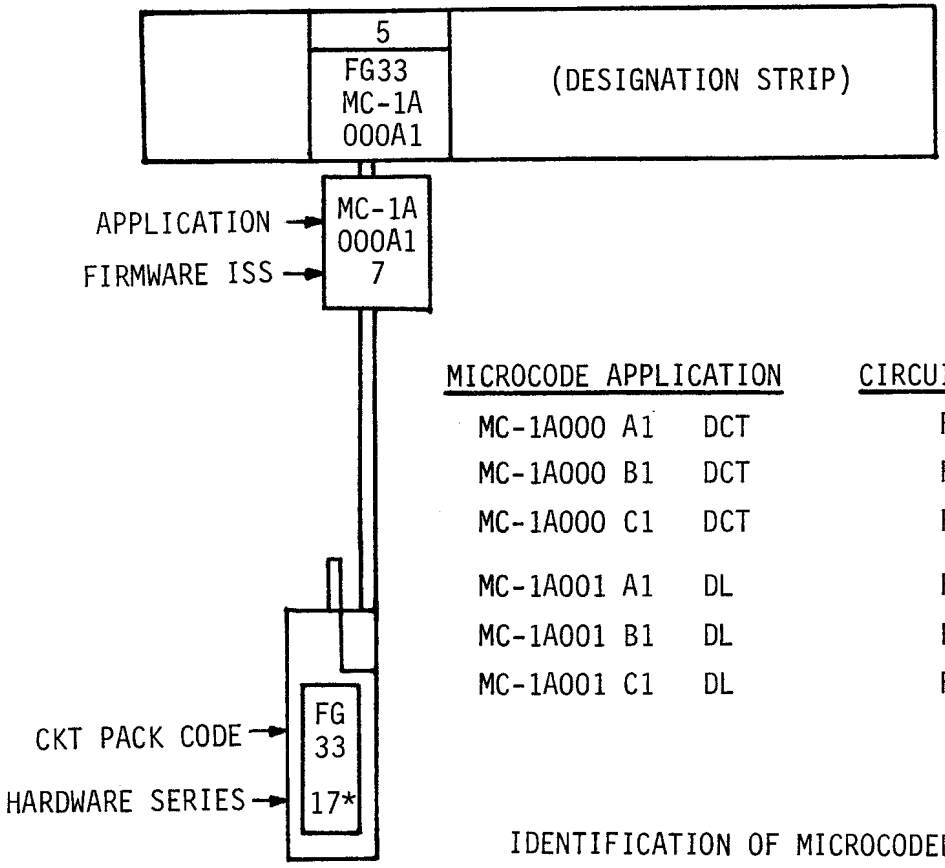
CIRCUIT PACK LAYOUT FOR PUC/DCT

CIRCUIT PACK TYPE AND FUNCTION

TYPE	DESIGNATION	FUNCTION	APPLICATION EQUIPPED FOR
FB292	CONV	+3V Power Converter	Common
FB668	REGFA	+12V Power Regulator	Common
FC331	ENVFO	Enable Receive Verify Driver	Common
FC332	CR	Cable Receiver	Common
FC333	CD	Cable Driver	Common
FG29	RAM	Random Access Memory (8K)	PUC/DL - RSS, ETS
FG30	IOD	Input/Output Decoder	Common
FG31	PROM	Programmable Read Only Memory	Common
FG32	RAM	Random Access Memory (4K)	DCT
FG33	CP	Central Processor Unit	Common
FG36	SCAM	Scan Answer Memory	Common
FG37	DIFC	Data Input FIFO Controller	Common
FG38	DIF	Data Input FIFO	Common
FG39	DMA	Direct Memory Access	Common
FG40	LIUA	Line Interface Unit A	PUC/DL - RSS, ETS
FG66	MEN	Mode and Enable	Common
FG67	DGB	Digroup Buffer	DCT
FG68	LIUB	Line Interface Unit B	PUC/DL - RSS, ETS
FG74	IOM	Input/Output Matcher	Common
FG78	LIUD	Line Interface Unit D	PUC/DL - CCIS
FG79	LIUE	Line Interface Unit E	PUC/DL - CCIS
FG81	LIUC	Line Interface Unit C	PUC/DL - ETS

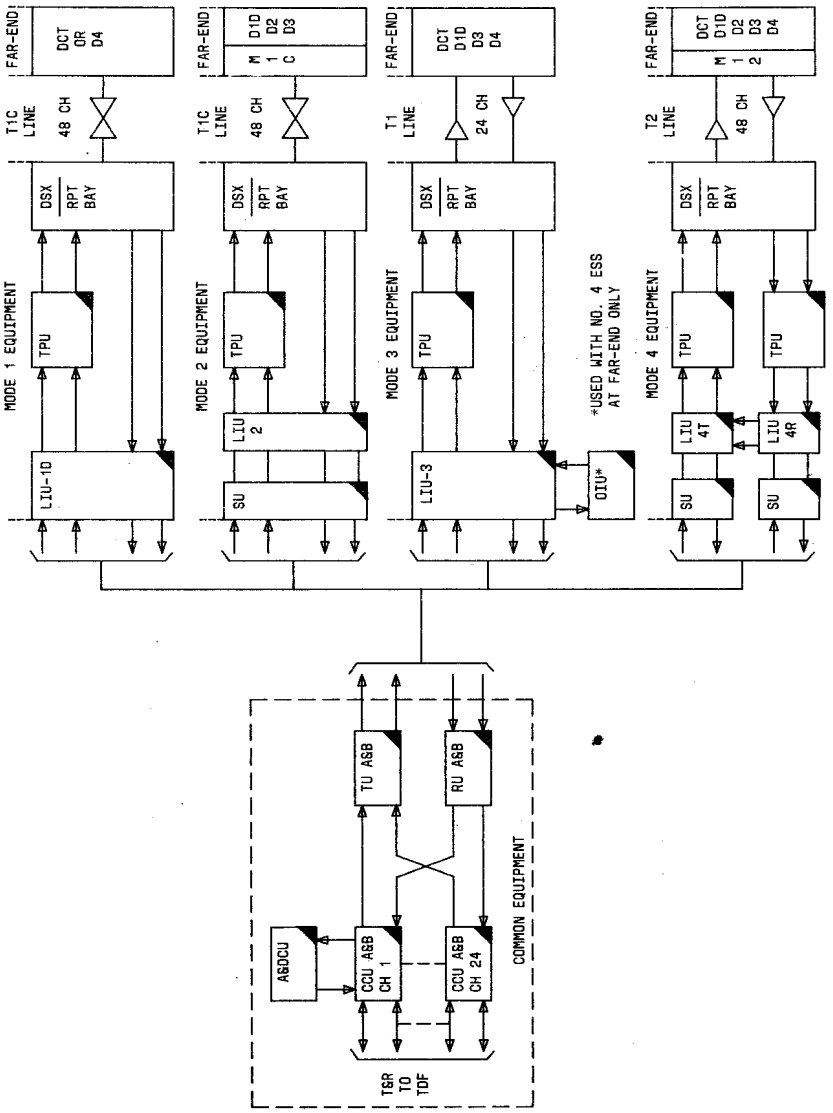
PERIPHERAL UNIT CONTROLLER

SD 1A477 - Digital Carrier Trunk
SD 1A478 - Data Link

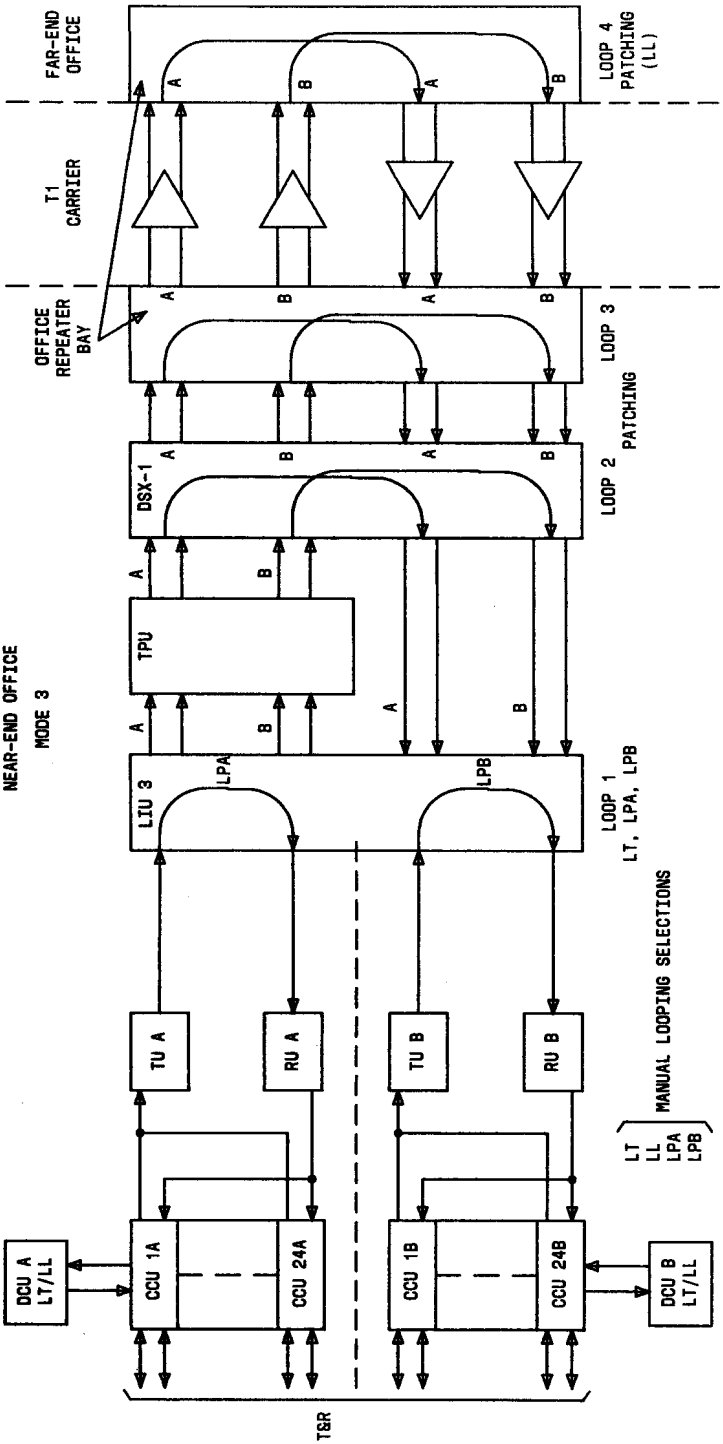


MICROCODE APPLICATION		CIRCUIT PACK CODE	
MC-1A000 A1	DCT	FG 33	
MC-1A000 B1	DCT	FG 31	
MC-1A000 C1	DCT	FG 31	
MC-1A001 A1	DL	FG 33	
MC-1A001 B1	DL	FG 31	
MC-1A001 C1	DL	FG 31	Iss 10 & later

IDENTIFICATION OF MICROCODED CIRCUIT PACKS



DCT EQUIPMENT CONFIGURATION MODE DEPENDENT

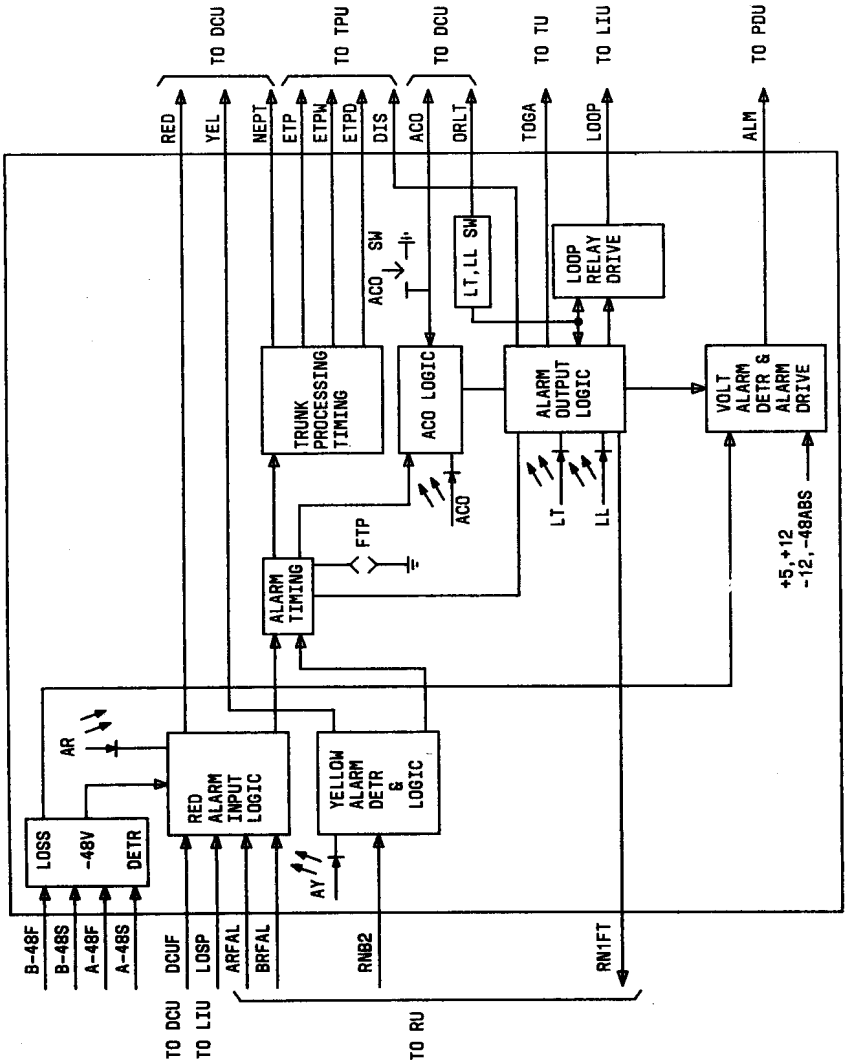


DCT MANUAL SIGNAL LOOPING – EXAMPLE OF MODE 3

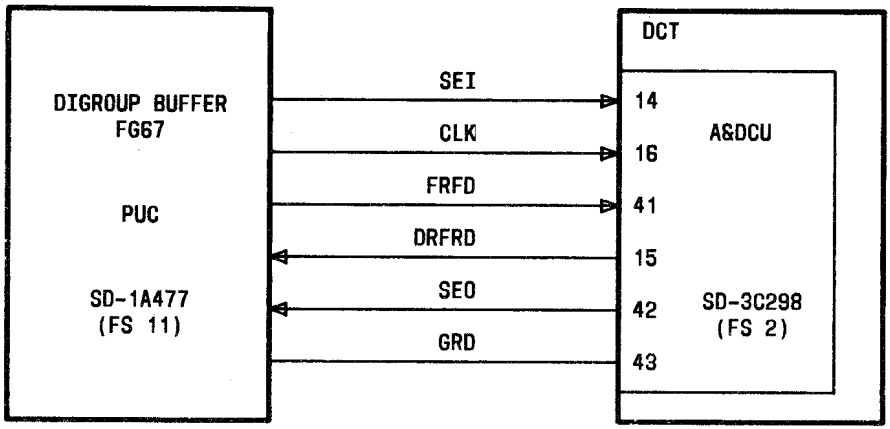
DCT BANK ALARMS

LOCATION OF LAMP	LAMP STATE (LIGHTED)	PROBABLE CAUSE OF TROUBLE OR FUNCTION
PDU	ALM	Bank alarm; fuse or signal failure
PCU	FAIL ACO	Low converter output voltage PCU input switch off
RU	RCV	Loss of framing PCM receive signal
A&DCU	DL	1. Loss of data from PUC 2. Loss of clock from PUC 3. Babbling CCU 4. Glare in DCU to PUC
	AR	Bank alarm for: 1. Loss of −48F or −48S 2. Loss of PUC data 3. Loss of receive signal 4. Loss of receive multiplex
	AY	1. Far-end failure 2. Near-end transmit failure
	ACO	Office alarms have been cleared – depressing ACO
DCU	DL	1. Loss of data from PUC 2. Loss of clock from PUC 3. Babbling CCU 4. Glare in DCU to PUC

LOCATION OF LAMP	LAMP STATE (LIGHTED)	PROBABLE CAUSE OF TROUBLE OR FUNCTION
LIU-2 LIU-4T LIU-4R	PASS	Fast loop test OK
	FAIL	Fast loop test fails; trouble in SU or LIU
	LOC	Fast loop test fails
	REM	Remote (far-end) problem
TPU	TPD-A TPD-B	Digroup (A or B) has completed trunk processing
A&DCU RU	AR,RCV flashing	Improper cross-connect has been made. The T&R is reversed at DSX or office repeater bay
A&DCU	AR,AY flashing	Hierarchy failure Mode 2 and Mode 4 only. Multiplexer at far-end
A&DCU TPU	AY,TPD-A or B flashing	1. Bank in loop mode but digroup has not been removed from service 2. Incorrect attenuation (not enough) in CCU transmit 3. Open CCU (T&R without termination)



DCT ALARM CONTROL UNIT (ACU) ON A & DCU PLUG-IN UNIT



SEI – SERIAL DATA INPUT TO DCU

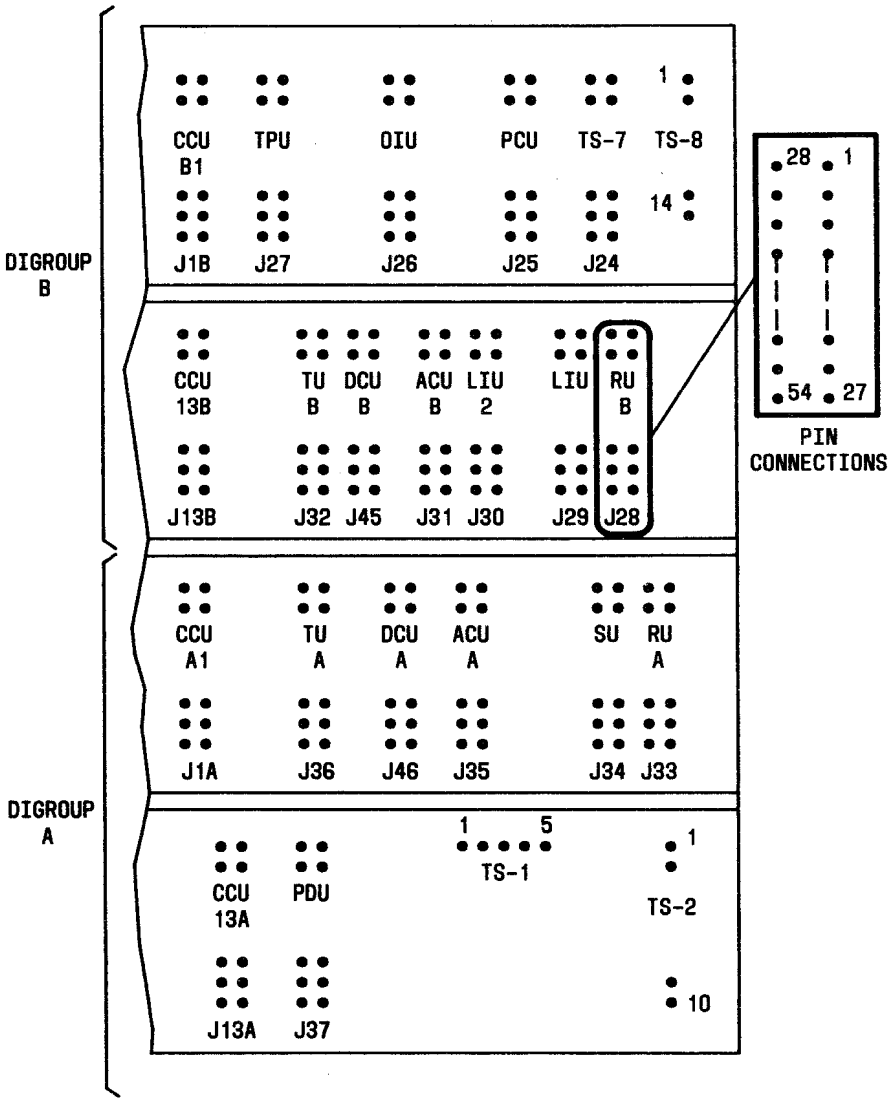
CLK – 333.3 KHz CLOCK PULSE FROM PUC TO DCU

FRFD – FRAME READY FOR DATA (PUC)

DRFRD – DIGROUP READY TO RECEIVE DATA

SEO – SERIAL DATA OUTPUT TO PUC

PUC – DCU DATA LINK



DCT BACKPLANE WIRING

PERIPHERAL BUS CONNECTORIZED CABLE LOCATION

PERIPHERAL UNIT CONTROLLER

ANSWER BUS CABLES	BUS 0	
BITS	IN	OUT
00-07	80-08-310	80-08-110
08-15	80-09-310	80-09-110
ASW	80-08-100	80-09-100
PARITY	80-10-310	80-10-110

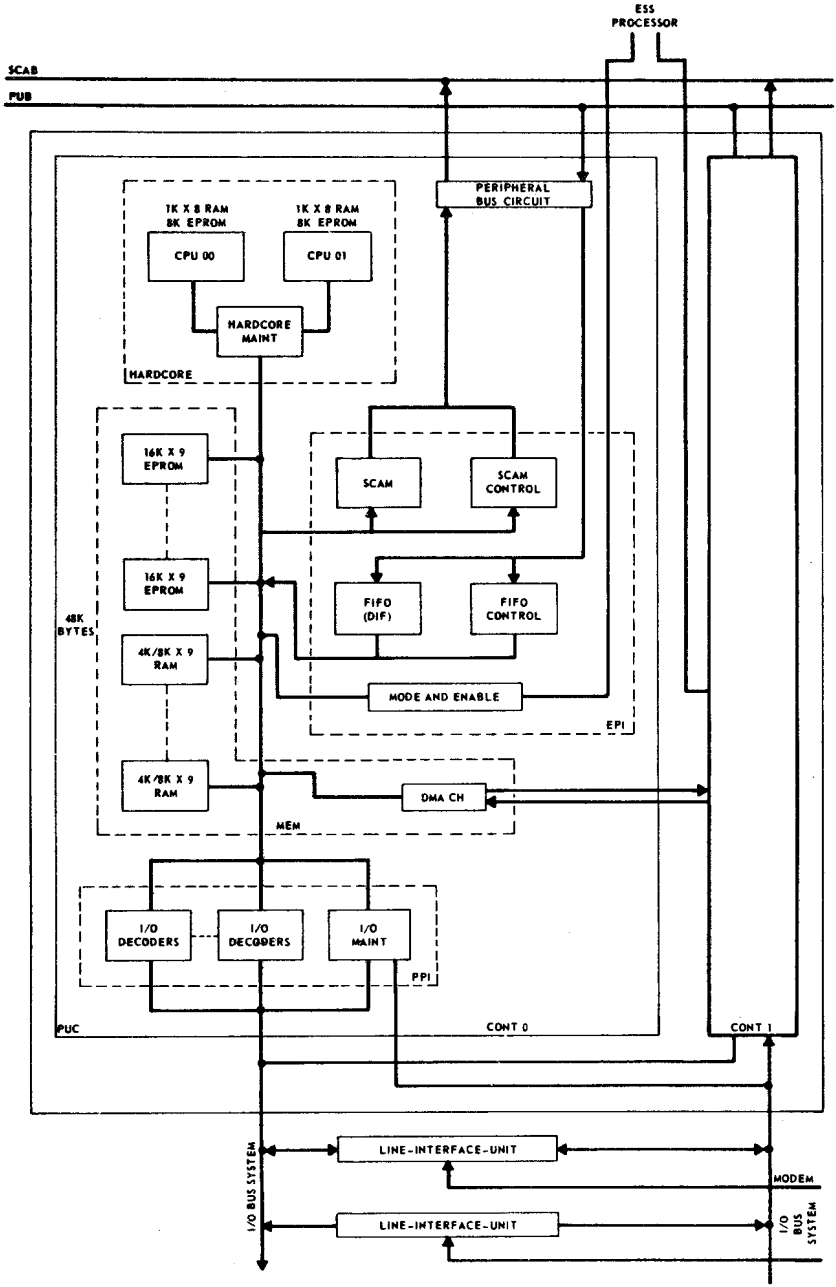
ANSWER BUS CABLES	BUS 1	
BITS	IN	OUT
00-07	80-21-310	80-21-110
08-15	80-22-310	80-22-110
ASW	80-21-100	80-22-100
PARITY	80-20-310	80-20-110

ADDRESS BUS CABLES	BUS 0	
BITS	IN	OUT
00-07	80-01-310	80-01-110
08-15	80-02-310	80-02-110
16-23	80-03-310	80-03-110
24-31	80-07-310	80-07-110
32-37	80-07-300	80-07-100

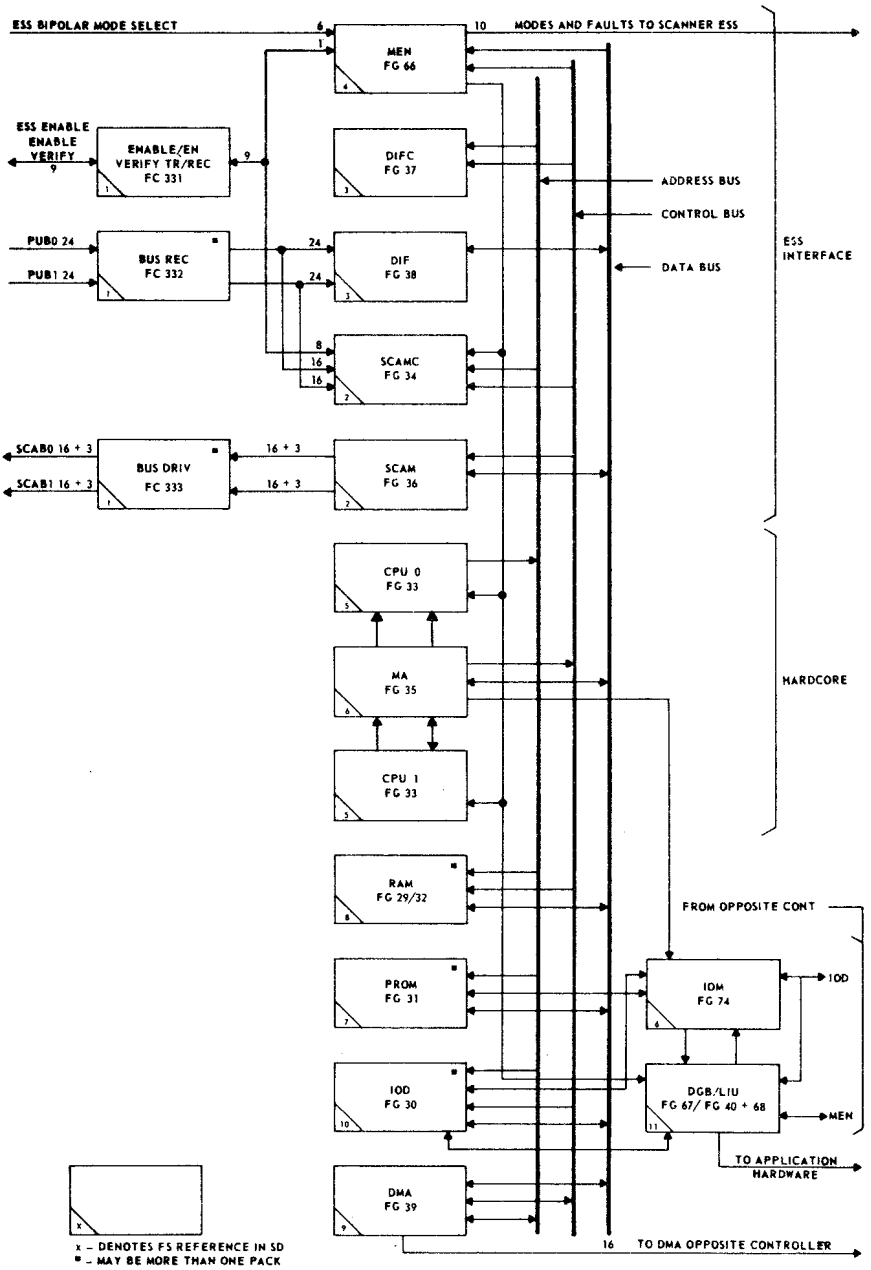
ADDRESS BUS CABLES	BUS 1	
BITS	IN	OUT
00-07	80-26-310	80-26-110
08-15	80-27-310	80-27-110
16-23	80-28-310	80-28-110
24-31	80-29-310	80-29-110
32-37	80-29-300	80-29-100

PUC DIAGNOSTIC PHASES

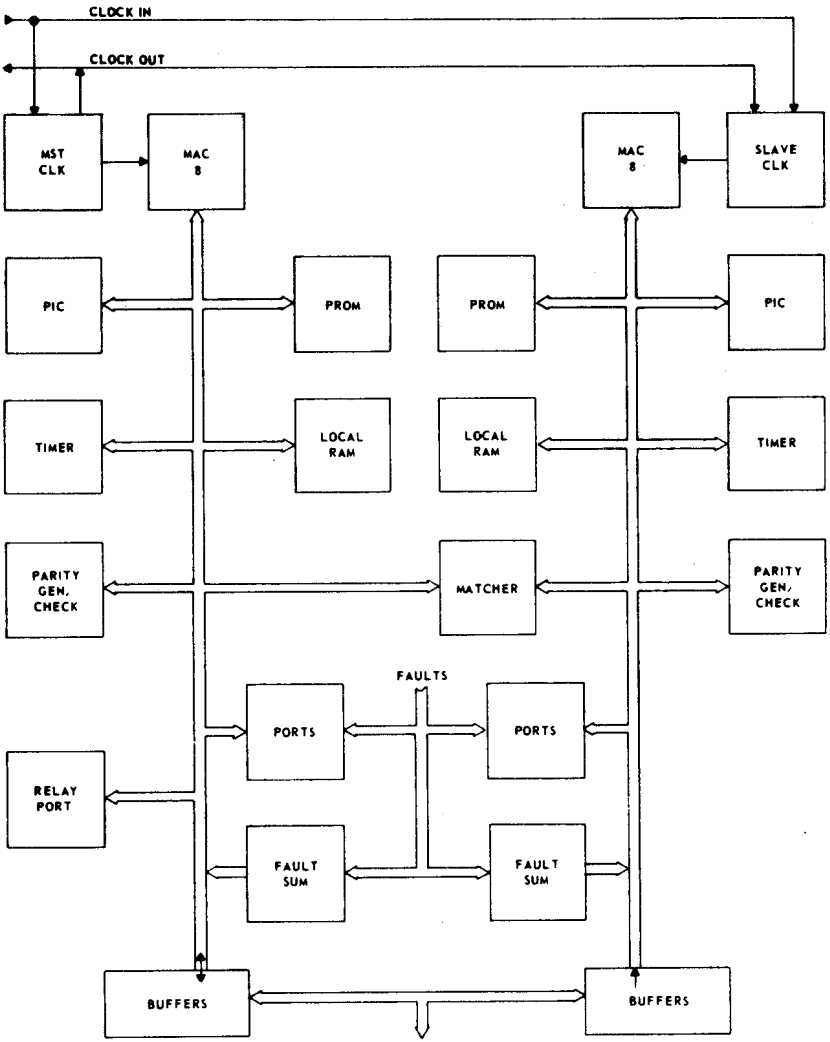
PHASE	HARDWARE TESTED	
1	Power Circuit	
2-5	Scan Memory	- FG34, FG36
6	FIFO	- FG37, FG38, FG66
7	Mode Flip-flops	- FG66
8	PROMs	- FG31
9	RAMs	- FG29, (FG32)
10	SCAM Maint. Circuit	- FG34, FG36
11	DIF Maint. Circuit	- FG38
12	DIFC Maint. Circuit	- FG37
13	Hardcore Matcher	- FG35
14-15	I/O Matcher	- FG74
16	I/O Decoder	- FG30
17	DMA Circuit	- FG39
18	Fault Flip-flops	- FG66
19	None - Reports problems PUC encountered when attempting to go duplex.	



PERIPHERAL UNIT CONTROLLER -- DATA LINK

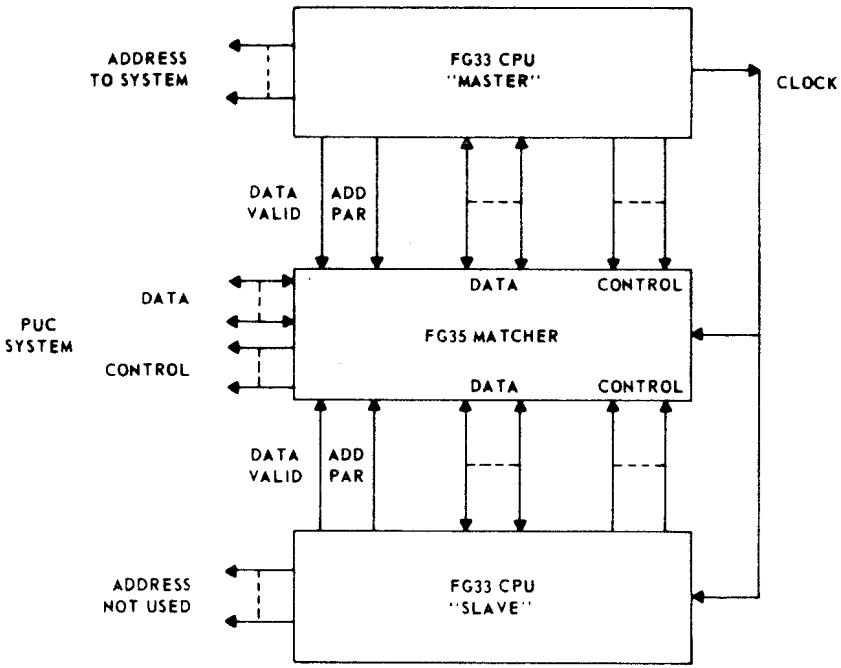


PERIPHERAL UNIT CONTROLLER
CIRCUIT PACK DIVISION



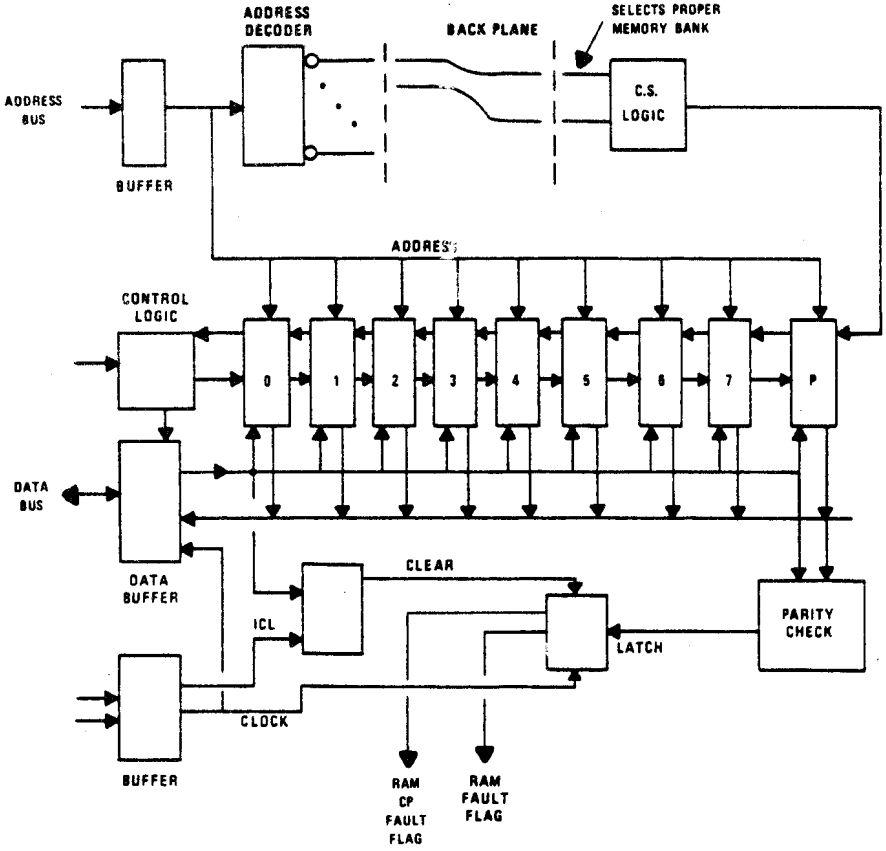
PIC – PROGRAMMABLE INTERRUPT CHIP

HARDCORE BLOCKS



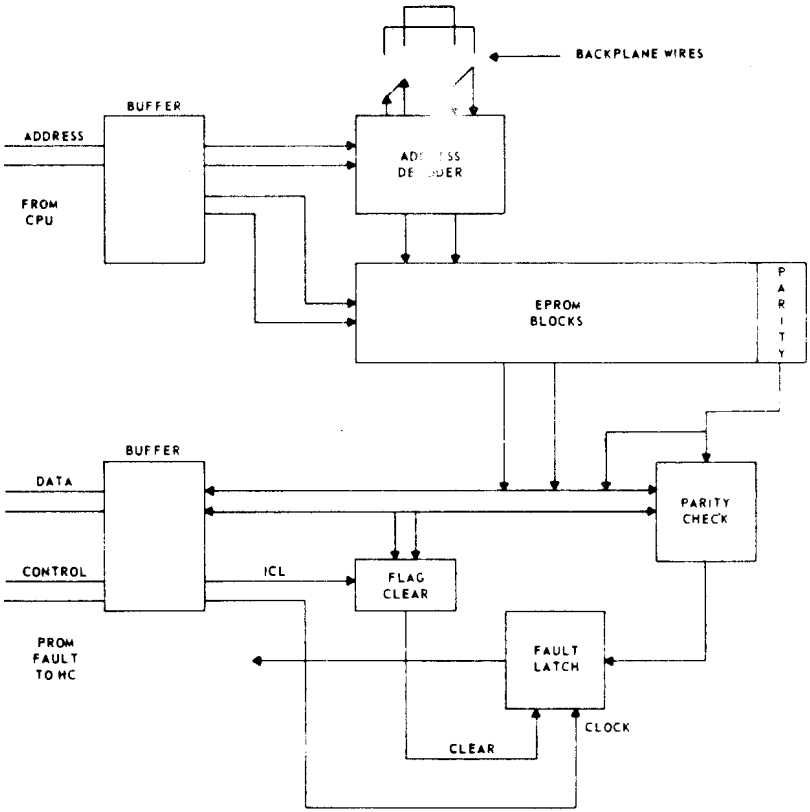
MATCHING OF THE CPU BOARDS IS DONE ON THE FG35. THE MASTER PROVIDES THE CLOCK FOR ALL BOARDS. THE DATA VALID SIGNALS WHEN THE COMPARISON SHOULD BE MADE.

HC BLOCK DIAGRAM FG33, FG35, FG33



NOTE: FG29 CONTAINS TWO BANKS OF RAM CHIPS, WHILE FG32 CONTAINS ONLY ONE BANK

RAM BOARD DESIGN FG 29–32



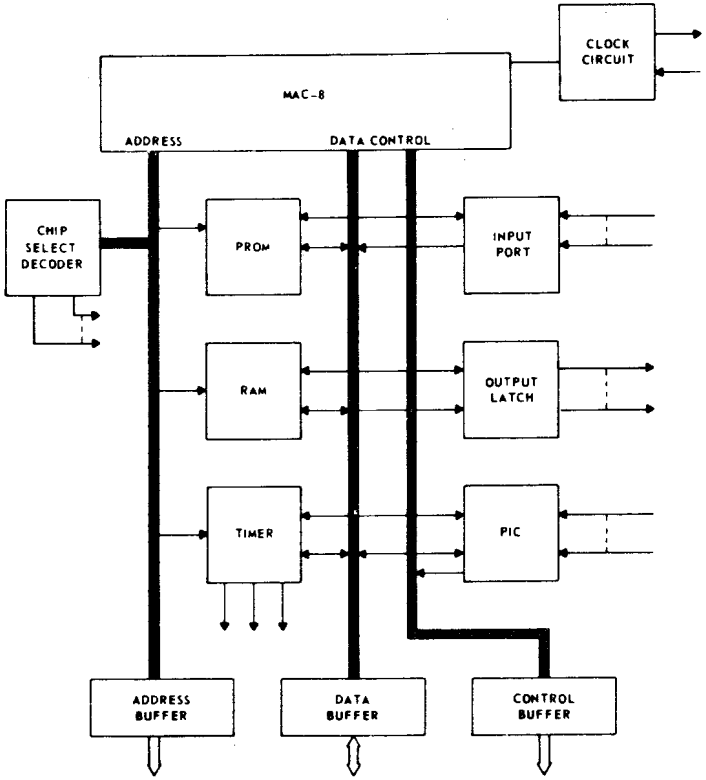
THE PROM BOARD FG 31 DECODES THE UPPER ADDRESS BITS AS A FUNCTION OF BACKPLANE WIRES. PARITY IS CHECKED ON ALL READS. IF BAD PARITY IS DETECTED A FAULT IS LATCHED.

CAUTION: FG 31 BOARDS ARE NOT INTERCHANGEABLE DUE TO UNIQUE PROGRAM DATA ENCODED ON EPROM CHIPS.

FG31 PROM BOARD

ADDRESS SPACE (HEXADECIMAL)	BACKPLANE WIRE		BACKPLANE WIRE	
	SELECT LEAD	PROM PIN	ENABLE LEAD	CHIP SELECT
1st 16K: 2XXX	SEL 00 (PROM)	PROM 0	EN 0	CS 0
3XXX	SEL 01	1	EN 1	CS 1
4XXX	SEL 02	2	EN 2	CS 2
5XXX	SEL 03	3	EN 3	CS 3
			EN 4	CS 4
			EN 5	CS 5
			EN 6	CS 6
			EN 7	CS 7
2nd 16K: 6XXX	SEL 10 (PROM)	0	EN 0	CS 0
7XXX	SEL 11	1	EN 1	CS 1
8XXX	SEL 12	2	EN 2	CS 2
9XXX	SEL 13	3	EN 3	CS 3
			EN 4	CS 4
			EN 5	CS 5
			EN 6	CS 6
			EN 7	CS 7
3rd 16K: AXXX	SEL 20 (PROM)	0	EN 0	CS 0
BXXX	SEL 21	1	EN 1	CS 1
CXXX	SEL 22	2	EN 2	CS 2
DXXX	SEL 23	3	EN 3	CS 3
			EN 4	CS 4
			EN 5	CS 5
			EN 6	CS 6
			EN 7	CS 7

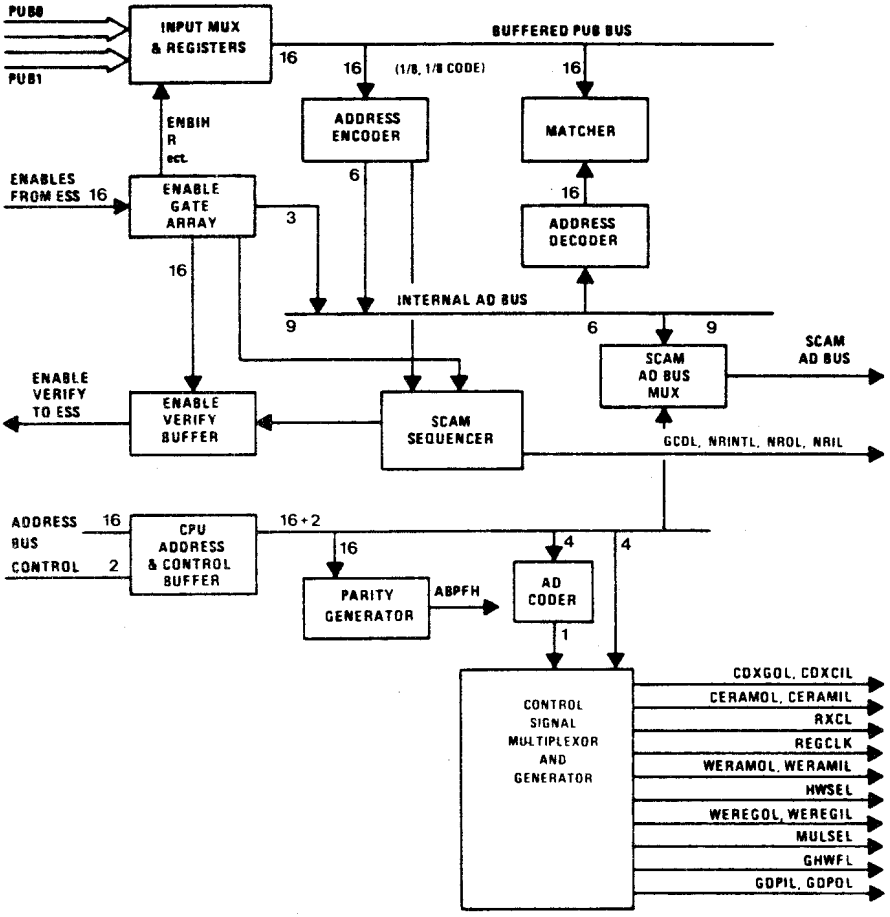
RELATIONSHIP BETWEEN AVAILABLE ADDRESS SPACE ON AN FG 31
AND THE RESPECTIVE CHIP SELECT LEADS FOR UP TO THREE FG 31
CIRCUIT PACKS



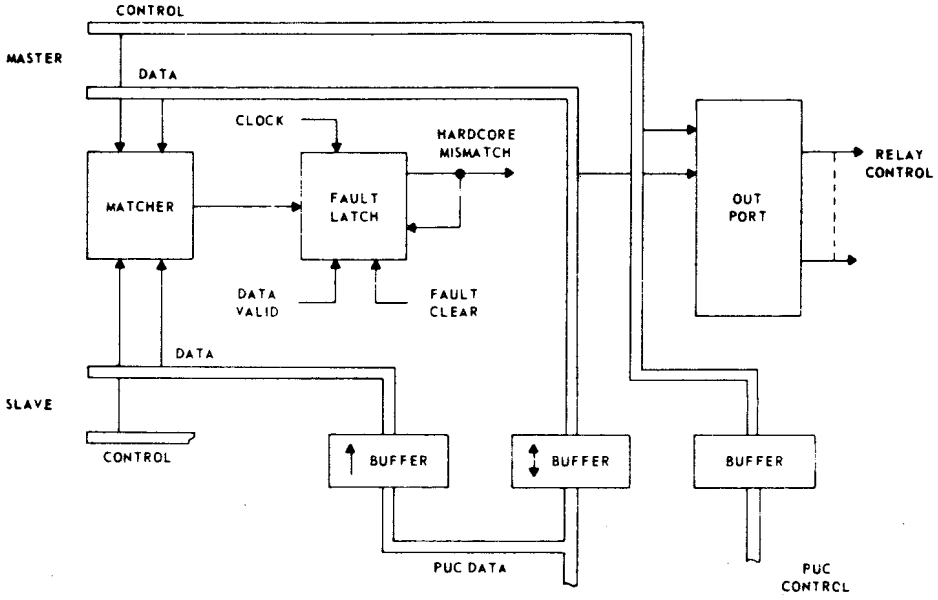
THE FG 33 HAS ALL THE FUNCTIONAL PARTS FOR A COMPLETE PROCESSING UNIT.

CPU	INPUT PORT
PROM	OUTPUT LATCH
RAM	INTERRUPT PROCESSOR
TIMER	CHIP SELECT DECODER

CPU BLOCK DIAGRAM FG 33



SCANNER ANSWER MEMORY CONTROLLER FG 34

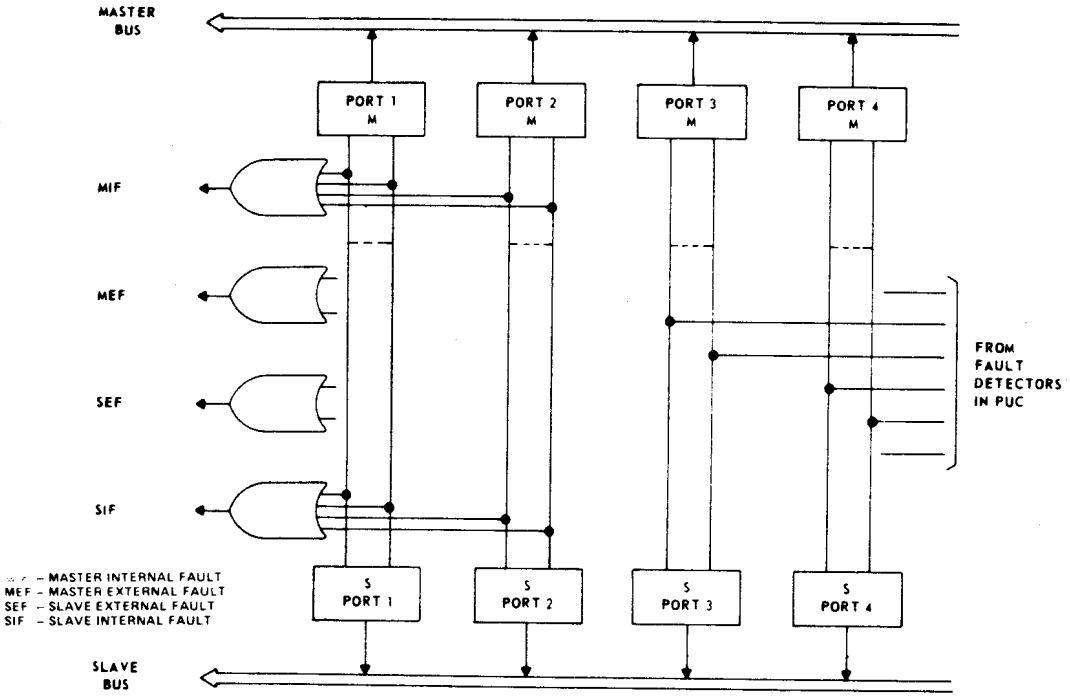


THE FG 35 MATCHING LOGIC DETECTS ANY DIFFERENCES BETWEEN MASTER AND SLAVE CPU'S.

THE DATA BUFFERS ALLOW THE MASTER CPU TO TRANSMIT AND RECEIVE DATA. THE SLAVE CAN RECEIVE DATA ONLY.

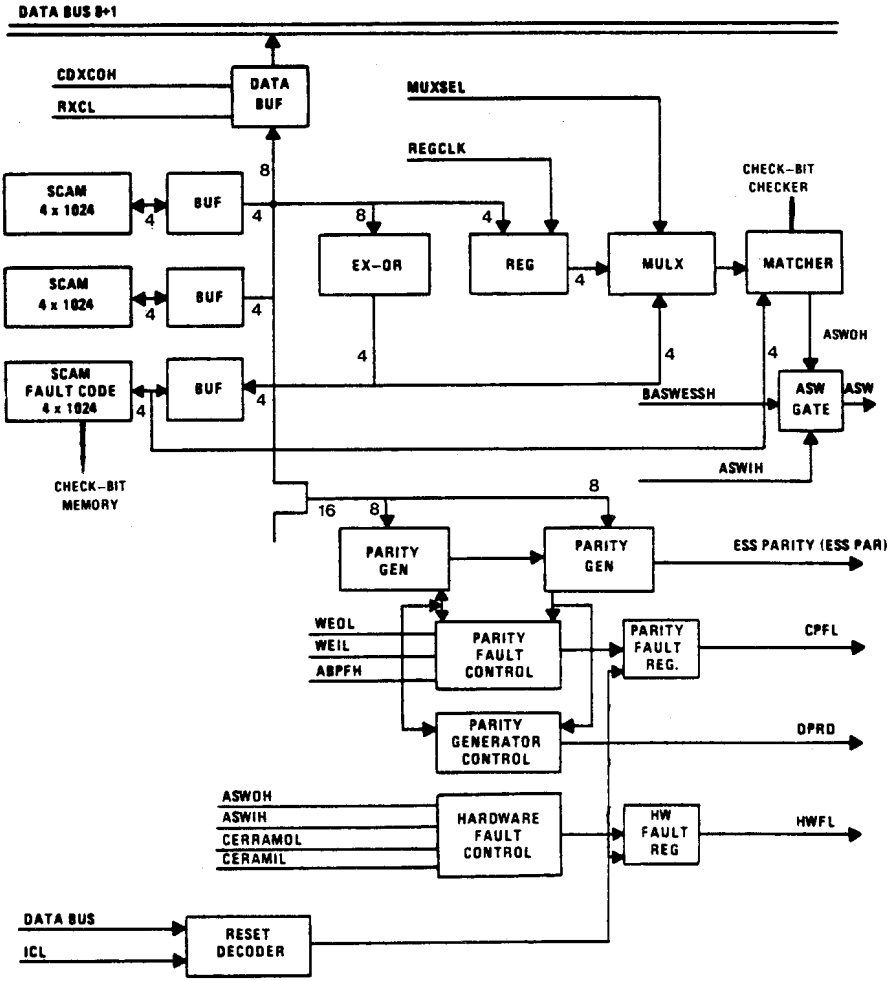
THE MASTER CONTROL SIGNALS ARE BUFFERED AND SENT TO PUC BOARDS.

FG35 MATCHER AND BUFFERS

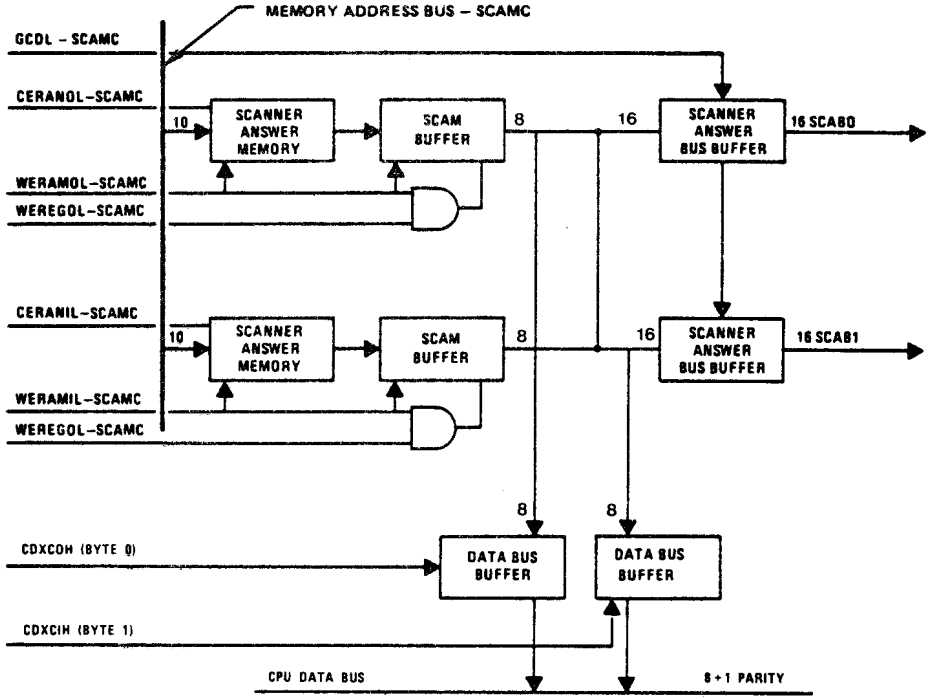


TEST PORTS ON THE FG 35 ALLOW THE MAINTENANCE FIRMWARE TO LOCATE FAULTS. DUPLICATION OF THE PORTS AND 'OR' GATES ALLOWS DETECTION OF FAILURES IN THIS CIRCUIT.

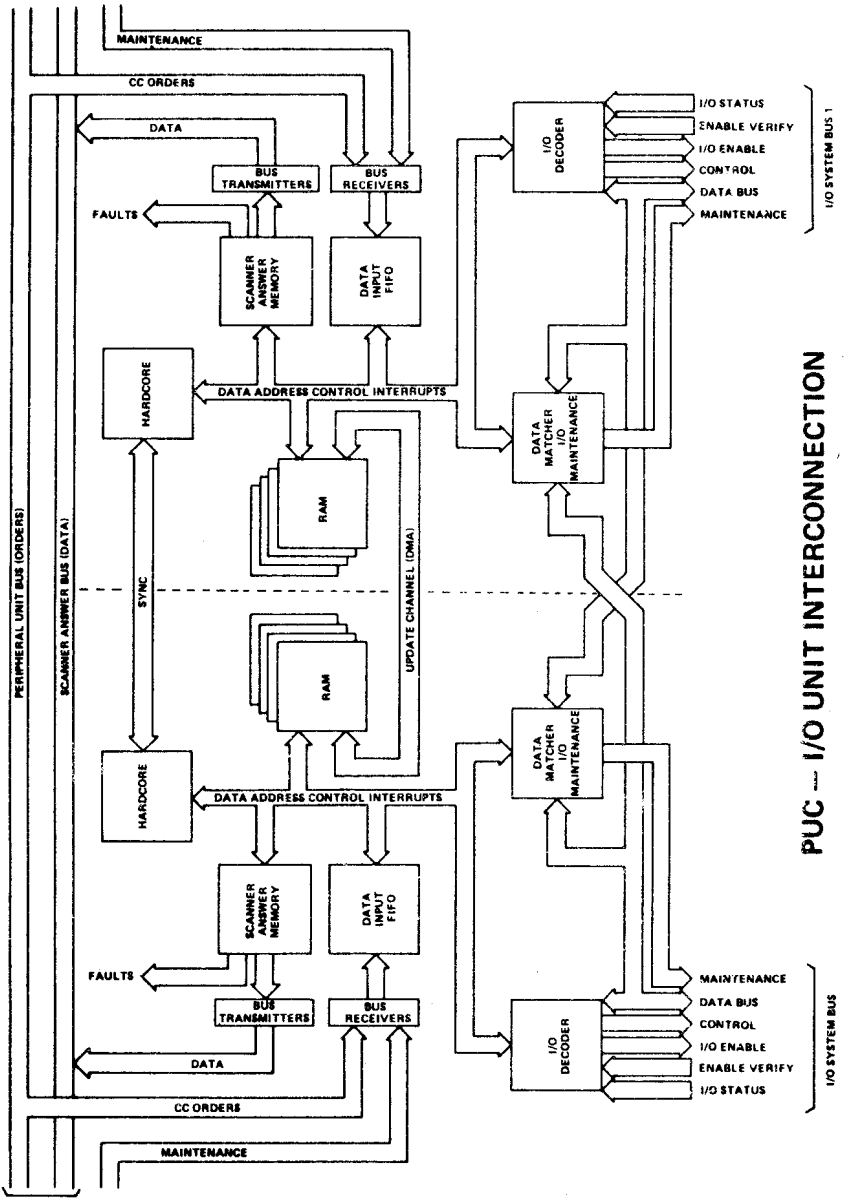
FG35 TEST PORTS



SCAM FG 36
(MAINTENANCE AND SELF CHECKING 8–BIT SLICE)

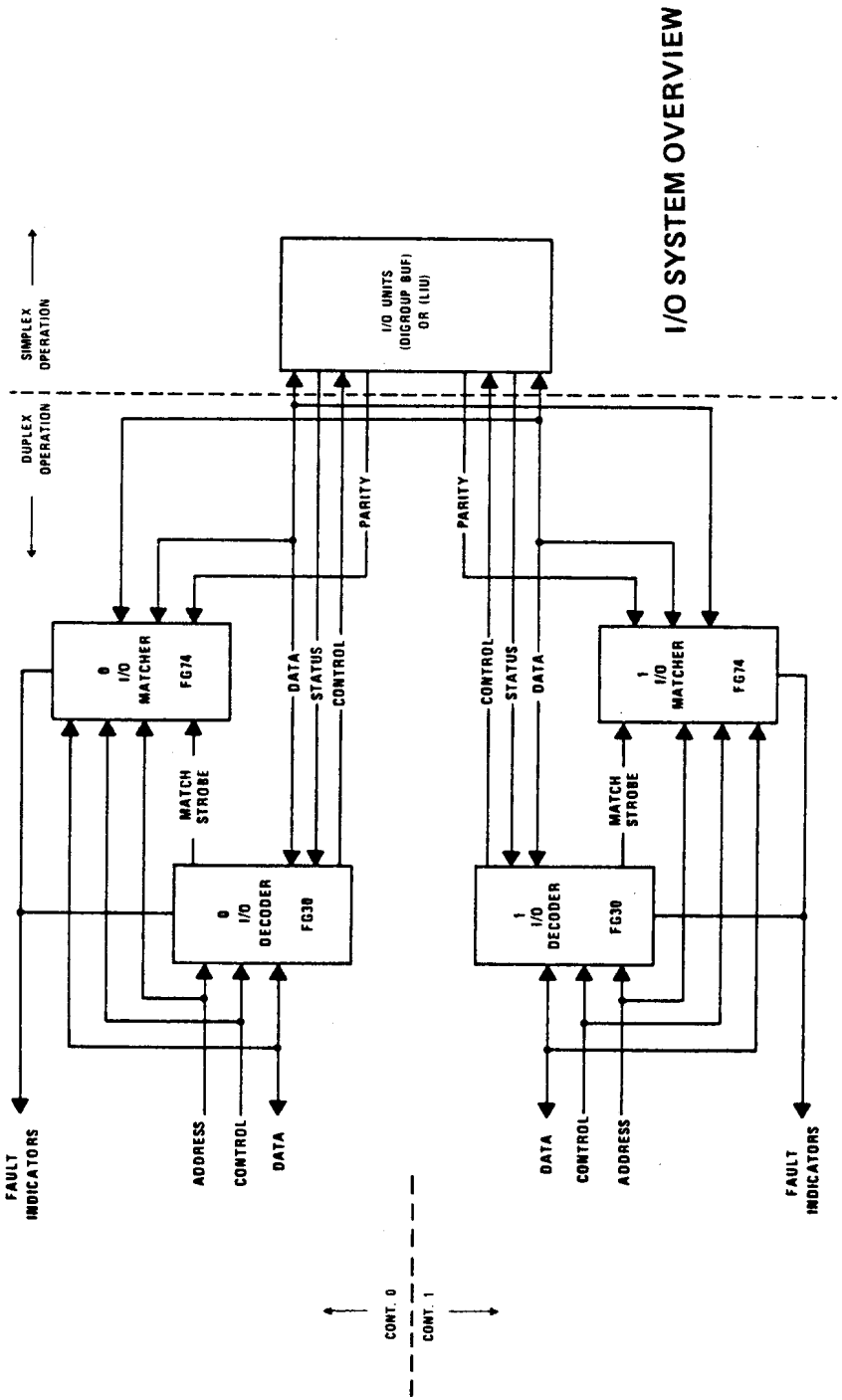


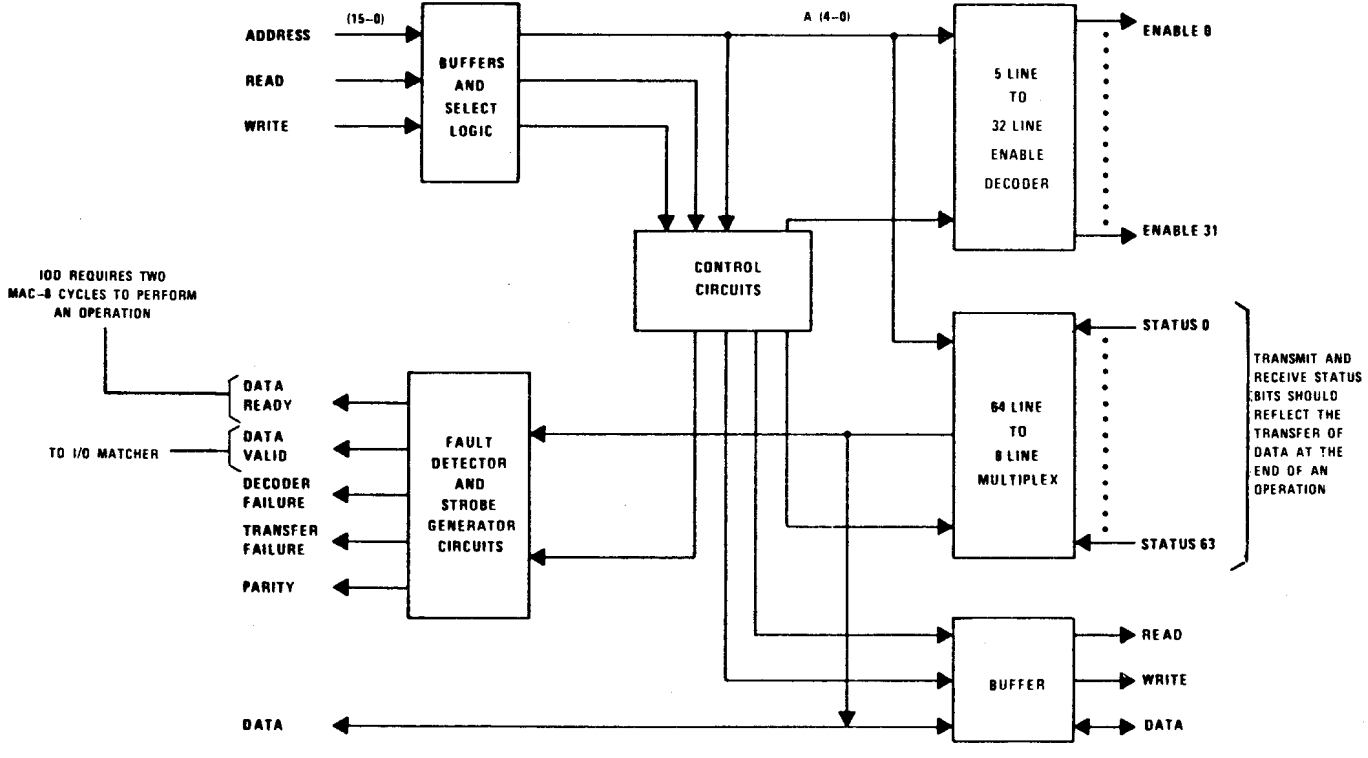
SCANNER ANSWER MEMORY FG 36 (BASIC OPERATION)



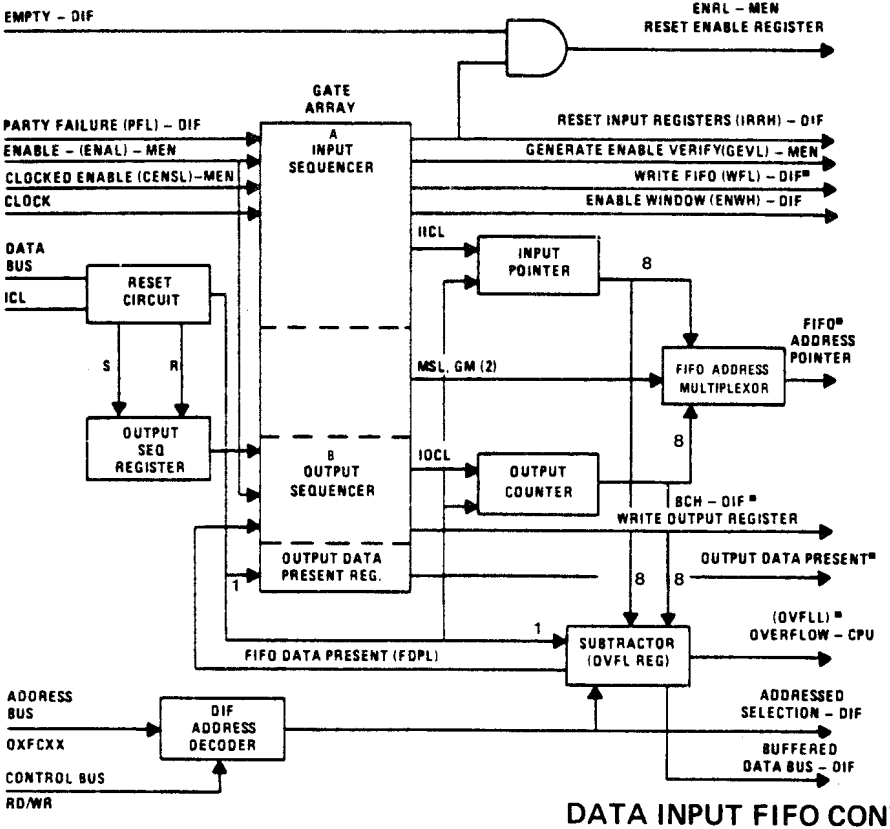
PUC — I/O UNIT INTERCONNECTION

28


I/O SYSTEM OVERVIEW
SIMPLEX OPERATION
DUPLEX OPERATION
I/O UNITS (DIGROUP BUF) OR (LIU)
PARITY
PARITY
0 I/O MATCHER FG74
1 I/O MATCHER FG74
DATA
STATUS
CONTROL
CONTROL
STATUS
DATA
MATCH STROBE
MATCH STROBE
0 I/O DECODER FG30
1 I/O DECODER FG30
FAULT INDICATORS
ADDRESS
CONTROL
DATA
DATA
CONTROL
ADDRESS
FAULT INDICATORS
CONT. 0
CONT. 1

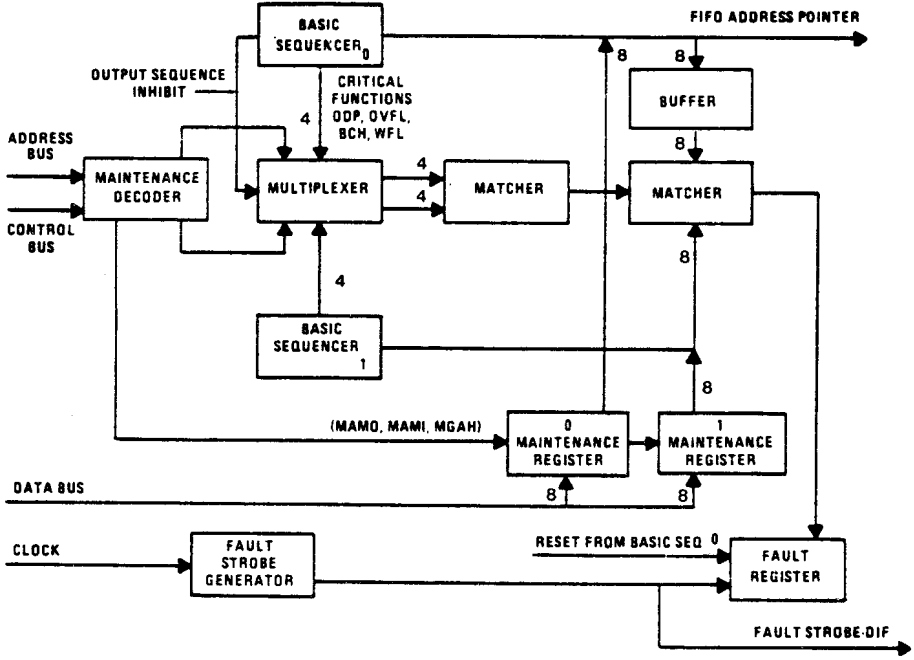


I/O DECODER FG 30

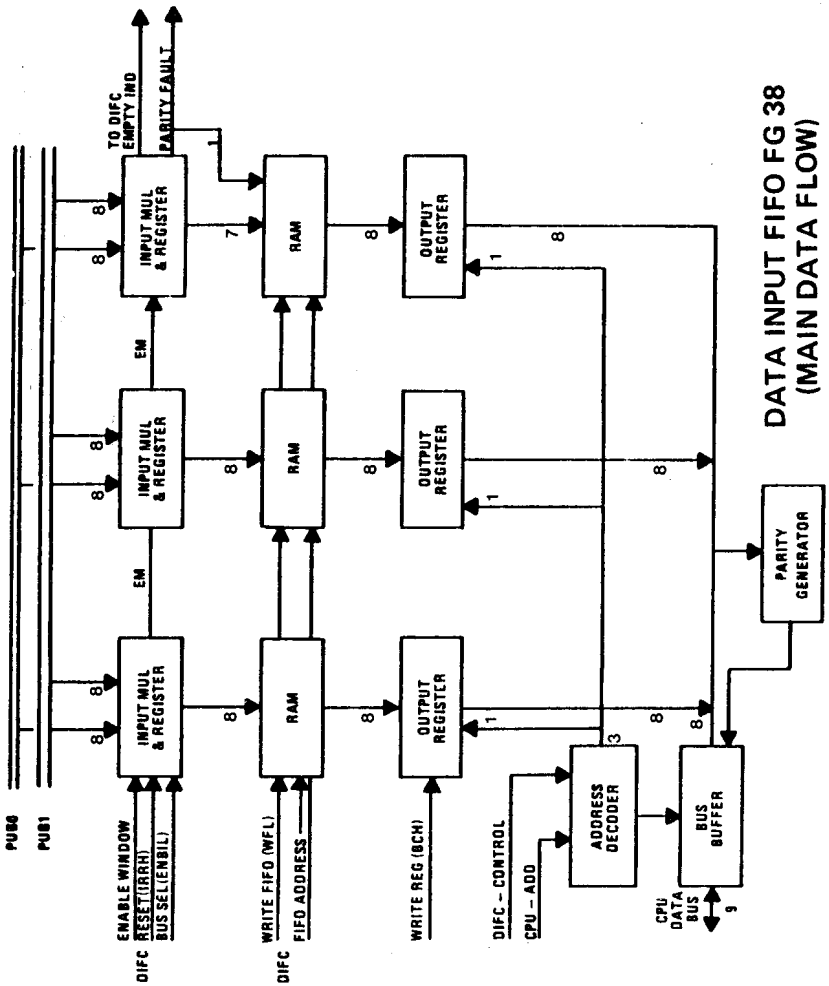


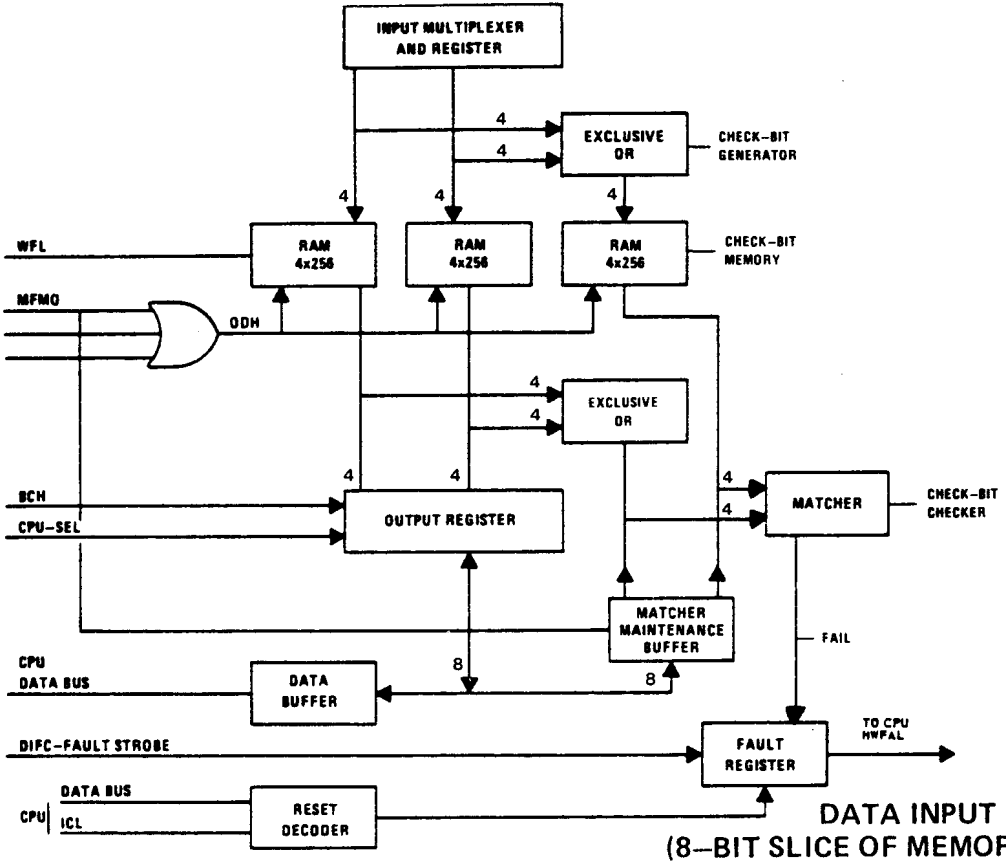
*CRITICAL FUNCTIONS

DATA INPUT FIFO CONTROLLER FG 37
(BASIC FUNCTION)

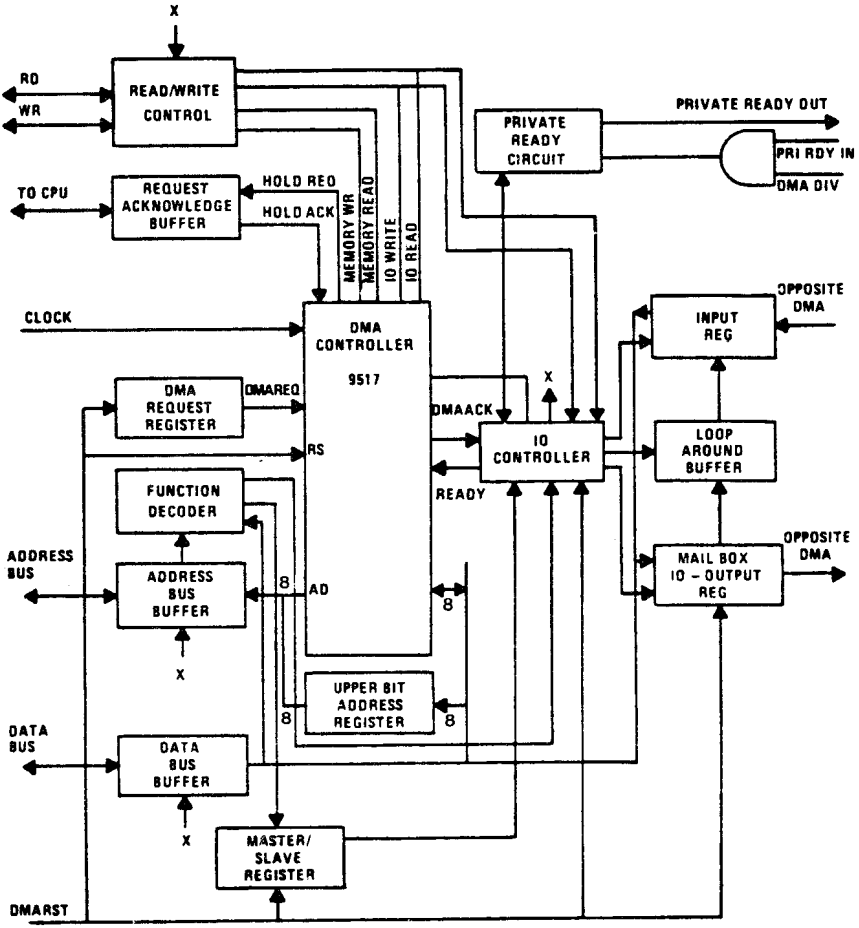


DATA INPUT FIFO CONTROLLER FG 37
(SELF CHECKING AND MAINTENANCE)

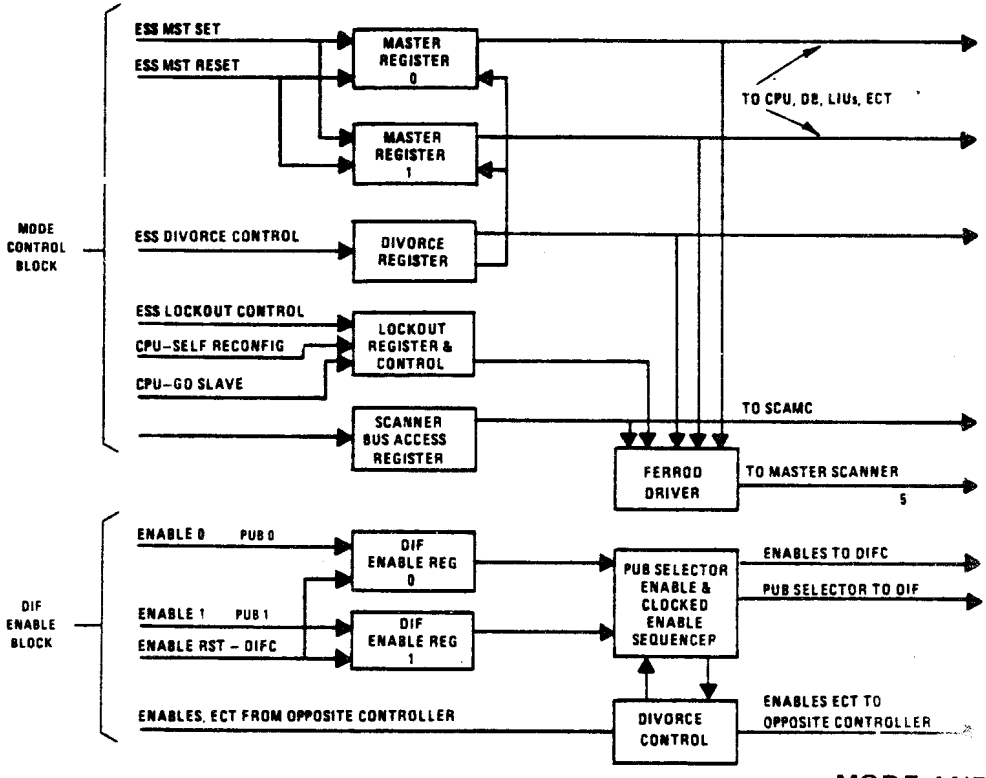

DATA INPUT FIFO FG 38
(MAIN DATA FLOW)
PUB0
PUB1
ENABLE WINDOW
DIFC RESET(IRRH)
BUS SEL(ENBIL)
WRITE FIFO (WFL)
DIFC FIFO ADDRESS
WRITE REG (BCH)
DIFC - CONTROL
CPU - ADD
CPU DATA BUS
TO DIFC EMPTY IND
PARITY FAULT
INPUT MUL & REGISTER
RAM
OUTPUT REGISTER
ADDRESS DECODER
BUS BUFFER
PARITY GENERATOR
EM



DATA INPUT FIFO FG 38
(8-BIT SLICE OF MEMORY FAULT CHECKING)

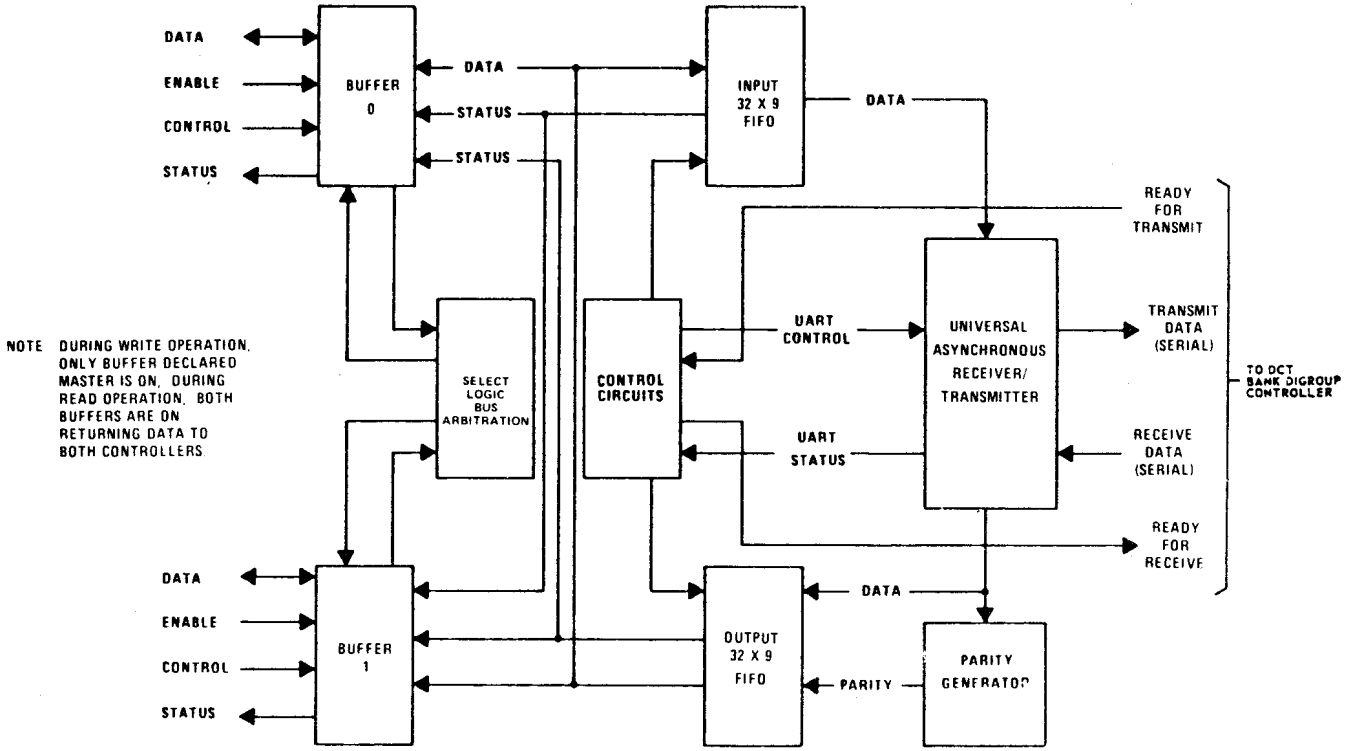


DIRECT MEMORY ACCESS FG 39



MODE AND ENABLE CIRCUIT (MEN) FG 66
(MODE AND ENABLE PART)

MODE AND ENABLE CIRCUIT (MEN) FG 66
(FAILURE INDICATOR BLOCK)



DIGROUP BUFFER FG 67

SECTION 7

LINE LINK/TRUNK LINK NETWORK

CONTENTS

LINE LINK NETWORK (LLN)

Line Switch Frame - 4:1 (LSF)
Unit Type 13 (LN00-15), 10 (LN16-31)

REMREED	FERREED
SD/CD-1A326	SD/CD-1A106
J1A081AA	J1A028A
TLM-1A326-01	TLM-1A106
PK-1A028-02	PK-1A028-01

Line Switch Frame - 2:1 (LSF)
Unit Type 13 (LN00-15), 10 (LN16-31)

REMREED	FERREED
SD/CD-1A325	SD/CD-1A106
J1A080AA	J1A028C
TLM-1A325	TLM-1A134
PK-1A028-02	PK-1A028-01

Junctor Switch Frame (JSF)
Unit Type 14 (LN00-15), 11 (LN16-31)

REMREED	FERREED
SD/CD-1A328	SD/CD-1A108
J1A075AB	J1A029A
TLM-1A328	TLM-1A108
PK-1A028-02	PK-1A028-01

Line Scanner - 4:1 (LS)
Unit Type 12 (LN00-15), 9 (LN16-31)

REMREED	FERREED
SD/CD-1A326	SD/CD-1A115
J1A081AA	J1A028AD
TLM-1A326-02	TLM-1A115
PK-1A027-01	PK-1A027-A1

Line Scanner - 2:1 (LS)

Unit Type 12 (LN00-15), 9 (LN16-31)

REMREED	FERREED
SD/CD-1A332	SD/CD-1A111
J1A080AB	J1A028CA
TLM-1A332	TLM-1A111
PK-1A027-01	PK-1A027-A1

TRUNK LINK NETWORK (TLN)

Trunk Switch Frame (TSF)

Unit Type 16

REMREED	FERREED
SD/CD-1A327	SD/CD-1A107
J1A075AA	J1A030A
TLM-1A327	TLM-1A107
PK-1A028-02	PK-1A028-01

Junctor Switch Frame (JSF)

Unit Type 15

REMREED	FERREED
SD/CD-1A328	SD/CD-1A108
J1A075AB	J1A029A
TLM-1A328	TLM-1A108
PK-1A028-02	PK-1A028-01

SUPPORTING DOCUMENTATION

TOP 231-051-002 Remreed frames
TOP 231-051-022 Remreed frames (1A7/1AE7 only)
BSP 231-049-330 Remreed maintenance considerations
TOP 231-051-003 Ferreed frames
BSP 231-049-331 Ferreed maintenance considerations

EQUIPMENT DESIGN REQUIREMENTS

BSP 820-101-150 LSF-ferreed
BSP 820-104-150 TSF-ferreed
BSP 820-106-150 JSF-ferreed
BSP 820-104-152 TSF-remreed

F, S, AND T POINT LAYOUT - 2:1 LINE SWITCH FRAME

	CONTROLLER SCAN POINTS			
	F	S	T	CONDITION
0	0	0	0	IDLE
1	0	0	1	TPAQ
2	0	1	0	RESET
3	0	1	1	QUAR
4	1	0	0	ENABLED
5	1	0	1	TPA
6	1	1	0	
7	1	1	1	POWER OFF

CONVERSION CHART

NET 00 = 00 - 07
NET 01 = 08 - 15
NET 02 = 16 - 23
NET 03 = 24 - 31
NET 04 = 32 - 39
NET 05 = 40 - 47
NET 06 = 48 - 55
NET 07 = 56 - 63
NET 08 = 64 - 71
NET 09 = 72 - 79
NET 10 = 80 - 87
NET 11 = 88 - 95
NET 12 = 96 - 103

OCTAL ORDER LAYOUT - 2:1 LINE SWITCH FRAME

22 20	19 16	15 14	13 12	11 10	9	8 6	5	4	3 2	1 0
ORDER		ST 1 SW	ST 1 LV		BAY	CONC	SO		ST 0 SW	ST 0 LV

ORDER:
1 = CONN CO OPEN
2 = FCG
3 = TEST
4 = HIGH & DRY
5 = CONN CO CLOSED
7 = RESTORE CO

TEST ORDERS:
QUARANTINE = 14010000
TPA = 14020000
RELEASE = 14030000
STG = 14040054

F, S, AND T POINT LAYOUT - 4:1 LINE SWITCH FRAME

	CONTROLLER SCAN POINTS			
	F	S	T	CONDITION
0	0	0	0	IDLE
1	0	0	1	TPAQ
2	0	1	0	RESET
3	0	1	1	QUAR
4	1	0	0	ENABLED
5	1	0	1	TPA
6	1	1	0	
7	1	1	1	POWER OFF

CONVERSION CHART

NET 00 = 00 - 07
NET 01 = 08 - 15
NET 02 = 16 - 23
NET 03 = 24 - 31
NET 04 = 32 - 39
NET 05 = 40 - 47
NET 06 = 48 - 55
NET 07 = 56 - 63
NET 08 = 64 - 71
NET 09 = 72 - 79
NET 10 = 80 - 87
NET 11 = 88 - 95
NET 12 = 96 - 103

OCTAL ORDER LAYOUT - 4:1 LINE SWITCH FRAME

22 20	19 16	15 14	13 12	11 10	9	8 6	5 4	3 0
ORDER		ST 1 SW	ST 1 LV		BAY	CONC	ST 0 SW	ST 0 LV

ORDER: 1 = CONN CO OPEN
2 = FCG
3 = TEST
4 = HIGH & DRY
5 = CONN CO CLOSED
7 = RESTORE CO

TEST ORDERS: QUARANTINE = 14000000
TPA = 14000030
RELEASE = 14000020
STG = 14040054

F, S, AND T POINT LAYOUT - LINE SCANNER

	CONTROLLER SCAN POINTS			
	F	S	T	CONDITION
0	0	0	0	POWER ON (OLD)
1	0	0	1	
2	0	1	0	
3	0	1	1	POWER ON (NEW)
4	1	0	0	
5	1	0	1	
6	1	1	0	
7	1	1	1	POWER OFF

OCTAL ORDER LAYOUT - LINE SCANNER

22 10	9 7	6 4	3 0
	MST SIG ROW	LST SIG ROW	

LAYOUT TO DISPLAY SCAN POINTS AT MASTER CONTROL CENTER

LINE SCANNER ROW CODE = 011

22 21	20 18	17 13	12 10	9	8 6	5 4	3 0
	CODE	LINE LINK NUMBER	LSF	BAY	CONC	SWITCH	LEVEL

F, S, AND T POINT LAYOUT - TRUNK SWITCH FRAME

	CONTROLLER SCAN POINTS			
	F	S	T	CONDITION
0	0	0	0	IDLE
1	0	0	1	TPAQ
2	0	1	0	RESET
3	0	1	1	QUAR
4	1	0	0	ENABLED
5	1	0	1	TPA
6	1	1	0	
7	1	1	1	POWER OFF

OCTAL ORDER LAYOUT - TRUNK SWITCH FRAME

22 20	19 14	13 12	11 9	8 6	5 3	2 0
ORDER		GRID	ST 0 SW	ST 0 LV	ST 1 SW	ST 1 LV

ORDER: 1 = CONNECT
3 = TEST

TEST ORDERS: QUARANTINE = 14001000
TPA = 14002000
RELEASE = 14003000
STG = 14004000

F, S, AND T POINT LAYOUT - JUNCTOR SWITCH FRAME

	CONTROLLER SCAN POINTS			
	F	S	T	CONDITION
0	0	0	0	IDLE
1	0	0	1	TPAQ
2	0	1	0	RESET
3	0	1	1	QUAR
4	1	0	0	ENABLED
5	1	0	1	TPA
6	1	1	0	FCG
7	1	1	1	POWER OFF

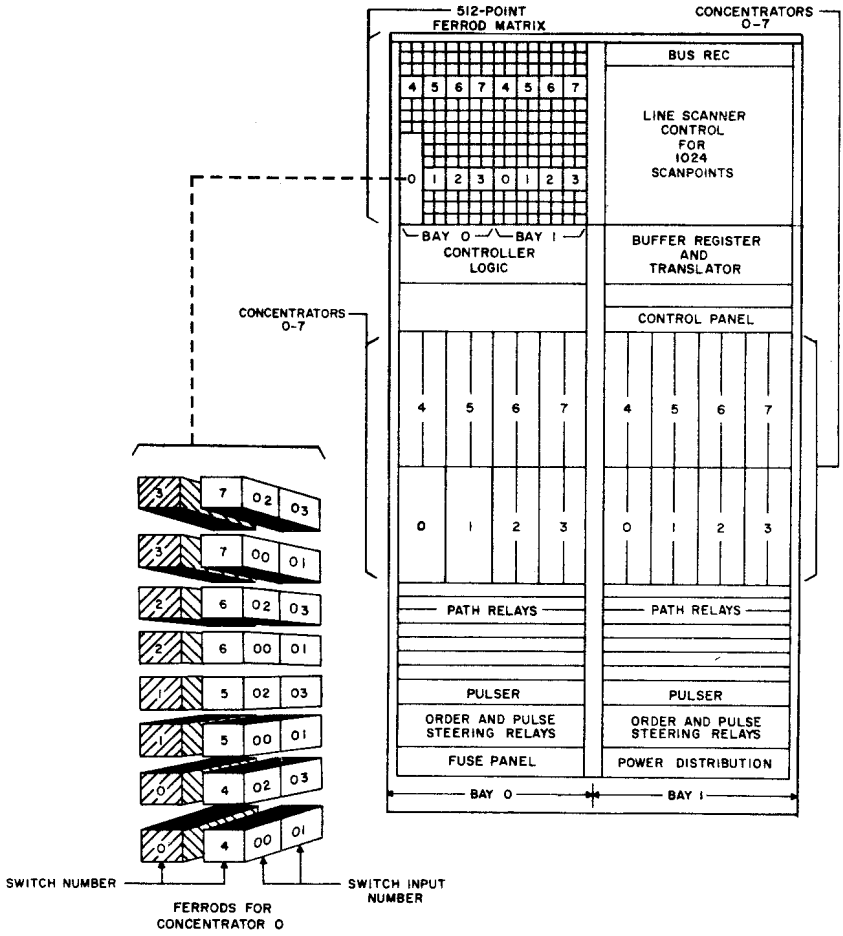
OCTAL ORDER LAYOUT - JUNCTOR SWITCH FRAME

22 20	19 14	13 12	11 9	8 6	5 3	2 0
ORDER		GRID	ST 0 SW	ST 0 LV	ST 1 SW	ST 1 LV

TEST ORDERS:
QUARANTINE = 14001000
TPA = 14002000
RELEASE = 14003000
STG = 14004000

ORDER:
0 = REMOVE NT
1 = CONNECT
2 = CONNECT WITH FCG
3 = TEST
5 = CONNECT VERIFY (LOOP START)
6 = OPERATE NT
7 = CONNECT VERIFY (GROUND START)

HOME LINE SWITCHING FRAME
(2:1 CONCENTRATION)

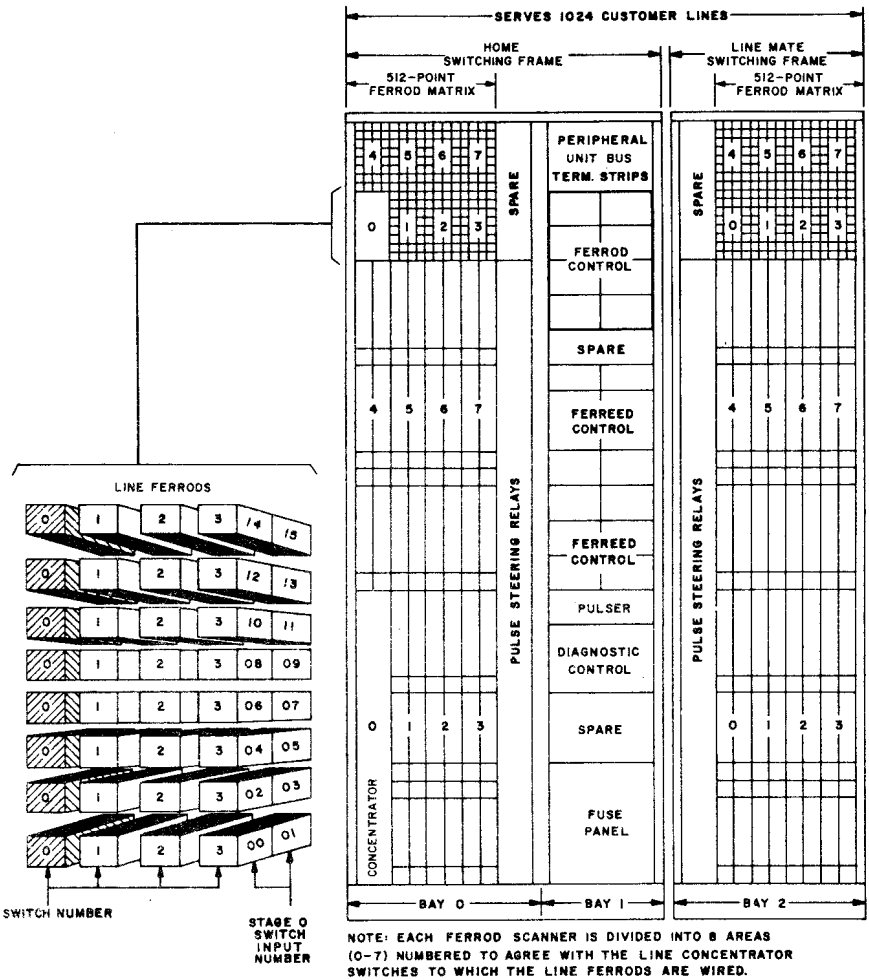


NOTE:

THE MATE FRAME IS IDENTICAL TO THE HOME FRAME EXCEPT THAT IT DOES NOT CONTAIN SCANNER CONTROL CIRCUITS.

Line Scanner With 2 to 1 Concentration (Ferreed)

LINE SWITCHING FRAME
(4:1 CONCENTRATION)

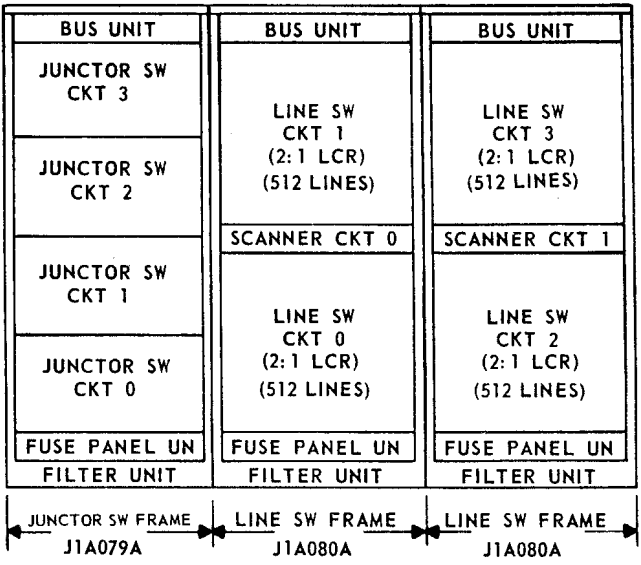


NOTE: EACH FERROD SCANNER IS DIVIDED INTO 8 AREAS (0-7) NUMBERED TO AGREE WITH THE LINE CONCENTRATOR SWITCHES TO WHICH THE LINE FERRODS ARE WIRED.

8 SHADED PAIRS OF FERRODS ARE SCANNED SIMULTANEOUSLY

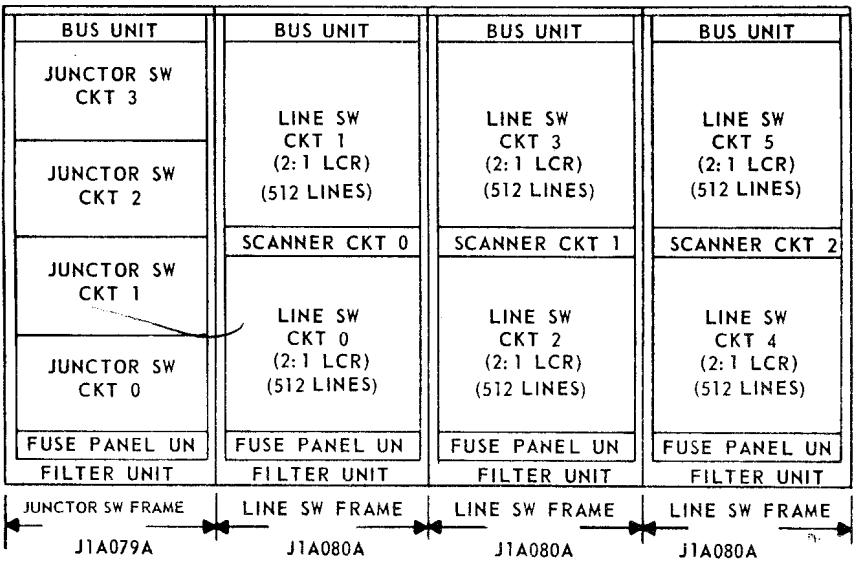
	(0, 2) BAY	(0-7) CONC	(0-3) SW NO	(00-15) SW INPUT	
FERROD DESIGNATION					

Line Scanner with 4 to 1 Concentration (Ferreed)



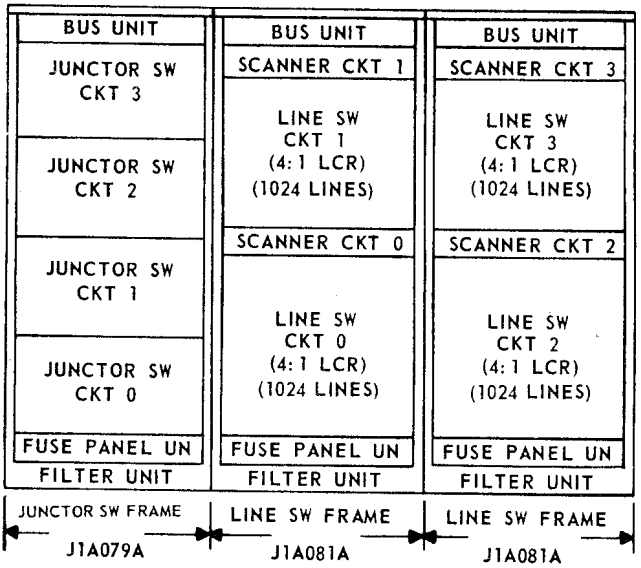
NETWORK ARRANGEMENT OF 2 TO 1 LLN

1024 PATHS WITH ACCESS TO 2048 SUBSCRIBER LINES



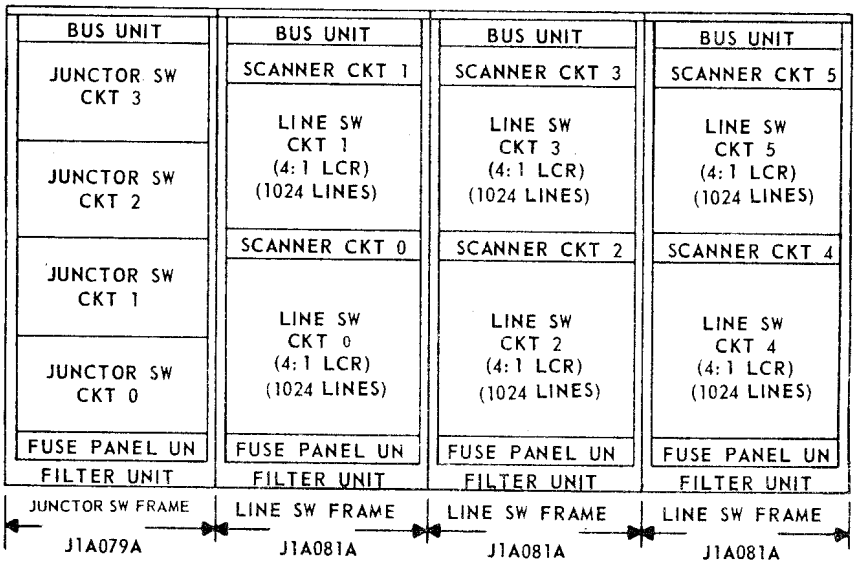
NETWORK ARRANGEMENT OF 3 TO 1 LLN

1024 PATHS WITH ACCESS TO 3072 SUBSCRIBER LINES



NETWORK ARRANGEMENT OF 4 TO 1 LLN

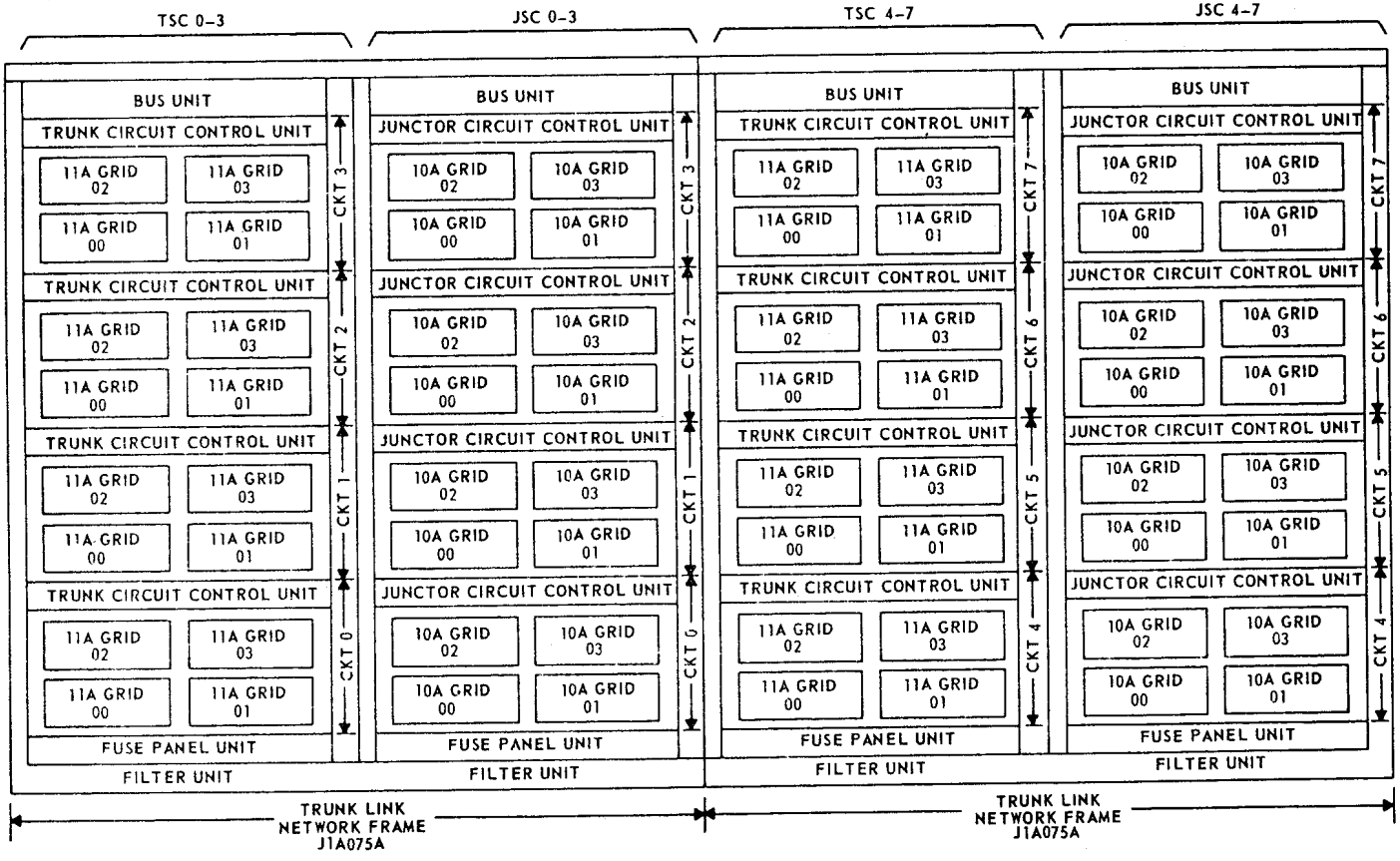
1024 PATHS WITH ACCESS TO 4096 SUBSCRIBER LINES



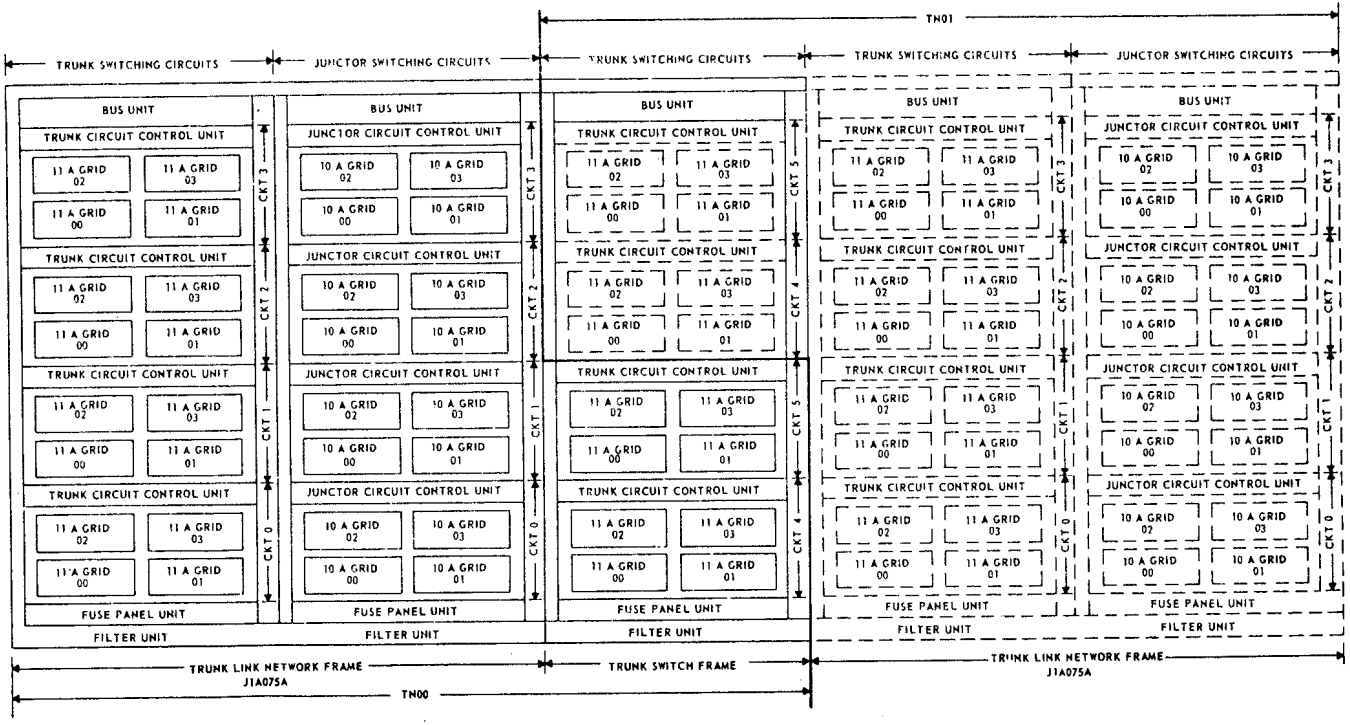
NETWORK ARRANGEMENT 6 TO 1 LLN

1024 PATHS WITH ACCESS TO 6144 SUBSCRIBER LINES

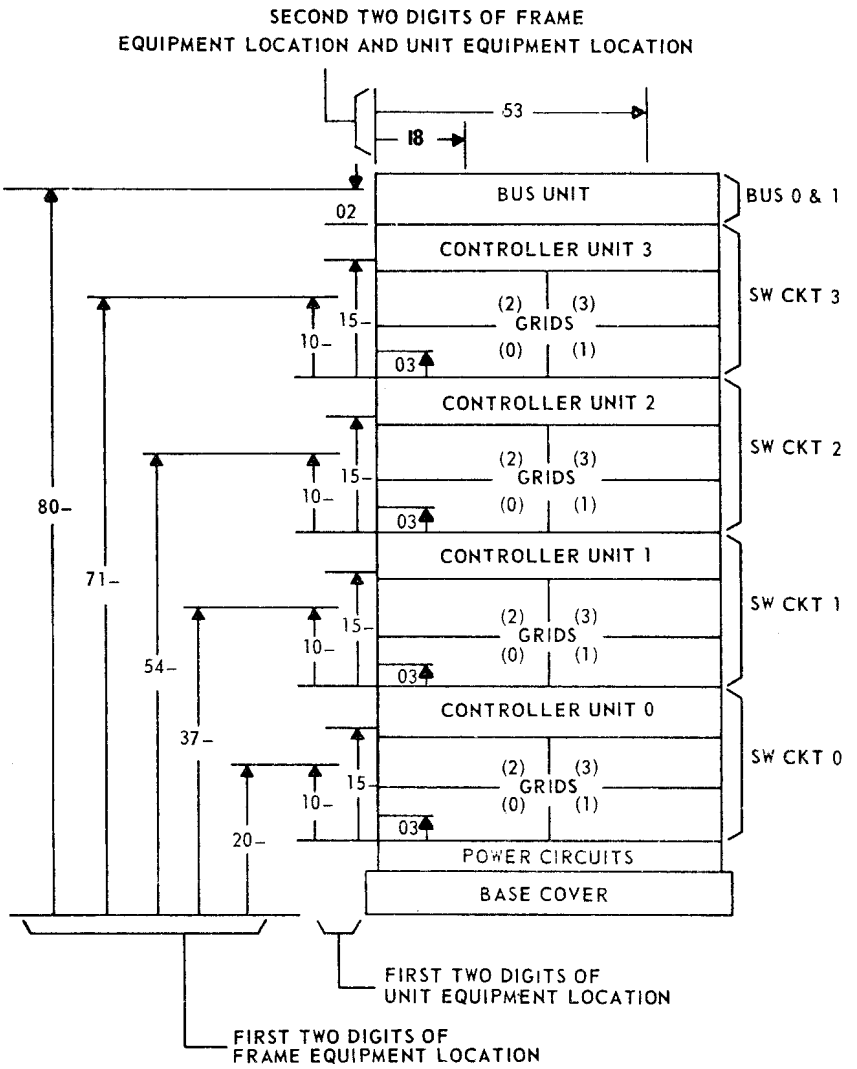
2048 TLN ARRANGEMENT



TLN, TCR 1.5:1 ARRANGEMENT



FRAME EQUIPMENT TO UNIT EQUIPMENT



4:1 LSC SHARED OR CRITICAL CIRCUIT PACKS

CIRCUIT PACK	NAME	FUNCTION	LOCATION
FC137	Input Line Selector	Selects the input level (0-15) with the OP10-OP13 or 1P18-1P111 P-leads on all orders that close the cut-offs in concentrators 0-3; orders 5 or 7 (normal from controller 0) and orders 13 or 15 (crossfire from controller 1).	02-23 FS7
FC137		Selects the input level (0-15) with the OP20-OP23 or 1P28-1P211 P-leads on all orders that close the cut-offs in concentrators 4-7; orders 5 or 7 (normal from controller 0) and orders 13 or 15 (crossfire from controller 1).	02-25 FS7
FC137		Selects the input level (0-15) with the OP10-OP13 or 1P18-1P111 P-leads on all orders that open the cut-offs in concentrators 0-3; orders 1 or 4 (normal from controller 0) and orders 9 or 12 (crossfire from controller 1).	02-27 FS7
FC137		Selects the input level (0-15) with the OP20-OP23 or 1P28-1P211 P-leads on all orders that open the cut-offs in concentrators 4-7; orders 1 or 4 (normal from controller 0) and orders 9 or 12 (crossfire from controller 1).	02-29 FS7
FC137		Selects the input level (0-15) with the 1P10-1P13 or OP18-OP111 P-leads on all orders that close the cut-offs in concentrators 8-11; orders 5 or 7 (normal from controller 1) and orders 13 or 15 (crossfire from controller 0).	06-40 FS7
FC137		Selects the input level (0-15) with the 1P20-1P23 or OP28-OP211 P-leads on all orders that close the cut-offs in concentrators 12-15; orders 5 or 7 (normal from controller 1) and orders 13 or 15 (crossfire from controller 0).	06-42 FS7
FC137		Selects the input level (0-15) with the 1P10-1P13 or OP18-OP111 P-leads on all orders that open the cut-offs in concentrators 8-11; orders 1 or 4 (normal from controller 1) and orders 9 or 12 (crossfire from controller 0).	06-44 FS7
FC137		Selects the input level (0-15) with the 1P20-1P23 or OP28-OP211 P-leads on all orders that open the cut-offs in concentrators 12-15; orders 1 or 4 (normal from controller 1) and orders 9 or 12 (crossfire from controller 0).	06-46 FS7
FC134	Diagnostic Control Circuit	Provides certain inhibit and mode control functions to controllers during diagnostics. Works in conjunction with other packs. Uses power supply from both controllers.	02-59 FS10
FC133	Test Point Access Circuit	Contains test point and quarantine relays; reflects F, S, and T points to master scanner for both controllers. Uses power supply from both controllers.	02-63 FS10

REFERENCE - SD1A326

4:1 LSC CONTROLLER PACKS

CIRCUIT PACK	NAME	FUNCTION	CONTROLLER LOCATION	
			0	1
FB292	+3v DC-DC Converter	Converts +24v to +3v to supply CP's FA774, FA772, FA773, FC130, and FB497 or FB297.	02-03 FS12	02-13
FA774	Three 4-bit Registers	Converts P.U. address bits 0-11 from bus 0 or 1 to the group 1 and half of the group 2 P-leads.	02-04 FS2	02-14
FA774		Converts P.U. address bits 12-23 from bus 0 or 1 to the group 3 and half of the group 2 P-leads.	02-05 FS2	02-16
FA772	Two 6-bit Registers and Translation Circuits	Converts P.U. address bits 24-35 from bus 0 or 1 to the (0 or 1)H or (0 or 1)M leads, the group 4 P-leads and the order group leads.	02-06 FS2	02-17
FA773	Controller Logic and Group Check Circuit	Processes enable, enable verify, controller reset (bit 36), group check and other functions.	02-07 FS4	02-18
FB290	Cut-Through and Gate Driver Ckt.	Used primarily in group check functions. Generates the A, B, and C leads for the six translator lead groups. Prevents the associated controller from accessing the mate concentrators unless the other controller is quarantined. Provides gate driving far the lead groups in the FA774's and FA772.	02-08 FS3	02-19
FC130	Diagnostic Bus Driver Circuit	Converts the low voltage leads from the IC's to the +24v levels required on the diagnostic bus. Has a few other functions.	02-09 FS5	02-20
FB297 or FB497	Enable Timer and Pulser Sequence Ckt.	Provides timing for enabling translators and generating enable verify; generates the group check window; controls timing and reset signals for pulser circuit; drives pulser circuit.	02-10 FS6	02-21
FB296	Pulser Circuit	Generates the 4.0 amp pulse through the concentrator grid to open or close remanent reed contacts.	02-51 FS6	02-55
FB287	Order Group Node Selector	Selects the order nodes with the OR1-OR7 leads and the P14-P17 P-leads for concentrators 0-3 (in controller 0) or concentrators 8-11 (in controller 1). Used on home orders.	02-42 FS7	06-59
FB287		Selects the order nodes with the OR1-OR7 leads and the P24-P27 P-leads for concentrators 4-7 (in controller 0) or concentrators 12-15 (in controller 1). Used on home orders.	02-43 FS7	06-60
FB287		Selects the order nodes with the OR9-OR15 leads and the P112-P115 P-leads for concentrators 8-11 (in controller 0) or concentrators 0-3 (in controller 1). Used on cross-fire orders.	02-44 FS7	06-61
FB287		Selects the order nodes with the OR9-OR15 leads and the P212-P215 P-leads for concentrators 12-15 (in controller 0) or concentors 4-7 (in controller 1). Used on cross-fire orders.	02-45 FS7	06-62

4:1 LSC CONTROLLER PACKS (CONT'D)

CIRCUIT PACK	NAME	FUNCTION	CONTROLLER LOCATION	
			0	1
FB286	Concentrator Node Selector	Develops the nodes for the stage 0 and 1 switches in the home concentrators with the P34-P37 P-leads and the A40-A43 concentrator pair leads from the FC139 pack. Used on home orders.	02-40 FS7	06-57
FB286		Develops the nodes for the stage 0 and 1 switches in the mate concentrators with the P312-P315 P-leads and the A48-A411 concentrator pair leads from the FC139 pack. Used on crossfire orders.	02-41 FS7	06-58
FC438	Mate Access and Release Path Selector	Selects the output level with the OP20-OP23 P-leads and provides pulse steering with the OOR1-OOR7 order group leads far concentrators 0 to 3. Used on home orders to controller 0.	02-32 FS7	
FC438		Selects the output level with the OP10-OP13 P-leads and provides pulse steering with the OOR1-OOR7 order group leads far concentrators 4 to 7. Used on home orders to controller 0.	02-34 FS7	
FC438		Selects the output level with the OP28-OP211 P-leads and provides pulse steering with the OOR9-OOR15 order group leads for concentrators 8-11 on controller 0 crossfire orders.	02-36 FS7	
FC438		Selects the output level with the OP18-OP111 P-leads and provides pulse steering with the OOR9-OOR15 order group leads for concentrators 12-15 on controller 0 crossfire orders.	02-38 FS7	
FC438		Selects the output level with the 1P20-1P23 P-leads and provides pulse steering with the 10R1-10R7 order group leads for concentrators 8-11 on controller 1 home orders.		06-48 FS7
FC438		Selects the output level with the 1P10-1P13 P-leads and provides pulse steering with the 10R1-10R7 order group leads for concentrators 12-15 on controller 1 home orders.		06-51 FS7
FC438		Selects the output level with the 1P28-1P211 P-leads and provides pulse steering with the 10R9-10R15 order group leads for concentrators 0-3 on controller 1 crossfire orders.		06-53 FS7
FC438		Selects the output level with the 1P18-1P111 P-leads and provides pulse steering with the 10R9-10R15 order group leads for concentrators 4-7 on controller 1 crossfire orders.		06-55 FS7
FC139	Concentrator Pair and Group Selector	Selects the concentrator group (0-3) with the P34-P37 or P312-P315 P-leads; selects the concentrator pair (0-3) home or 0-3 mate) with the P40-P43 or P44-P48 P-leads; selects on of the test leads (P31A-P34A) with the P30-P33 P-leads and the OR3 order group lead on test orders.	02-39 FS7	06-56

LINE SCANNER CONTROLLER PACKS (2:1 AND 4:1)

CIRCUIT PACK	NAME	FUNCTION	CONTROLLER LOCATION	
			0	1
FB292	+3v DC-DC Converter	Converts +24 to +3v to supply CP's FA777 or FA775, FB288, FB289, FC330 and FC135.	0*-03 FS6 2:1 FS18 4:1	0*-20
FC135	Scanner Detection Circuit	Accepts the readout matrix bits 0-15 from the even rows (associated with the even LSC in 2:1) in concentrators 0 to 15.	0*-05 FS5 2:1 FS17 4:1	0*-22
FC135	Scanner Detection Circuit	Accepts the readout matrix bits 0-15 from the odd rows (associated with the odd LSC in 2:1) in concentrators 0 to 15.	0*-07 FS5 2:1 FS17 4:1	0*-24
FA777 (2:1) FA775 (4:1)	Scanner Controller Register and Translator	Translates P.U. bus bits 0-15 to select the row to be interrogated; Accepts the enable; generates the enable verify; Generates the ASWS; Accepts bit 16 to generate the test order functions.	0*-08 FS3 2:1 FS15 4:1	0*-25
FC330	Interrogate Matrix	Selects one of the 16 scanner rows to be interrogated in concentrators 0 to 3.	0*-09 FS3 2:1 FS15 4:1	0*-26
FC330		Selects one of the 16 scanner rows to be interrogated in concentrators 4 to 7.	0*-10 FS3 2:1 FS15 4:1	0*-27
FC330		Selects one of the 16 scanner rows to be interrogated in concentrators 8 to 11.	0*-14 FS3 2:1 FS15 4:1	0*31
FC330		Selects one of the 16 scanner rows to be interrogated in concentrators 12 to 15.	0*-15 FS3 2:1 FS15 4:1	0*-32
FB288	Interrogate Current Drivers	Drives the interrogate current for 1 out of 4 rows selected in a concentrator; Checks that exactly one of these four are selected to help generates the ASWS.	0*-12 FS3 2:1 FS15 4:1	0*-29
FB289	Scanner Timing	Provides enable timing and scanner sequencing functions; Accepts bit 36 (controller reset); Buffers the maintenance test functions from the +3v to the +24v level.	0*-16 FS3 2:1 FS15 4:1	0*-33

* 02-xx in SD1A332 (2:1 line scanner), 06-xx in SD1A326 (4:1 line scanner)

TSC SHARED or CRITICAL CIRCUIT PACKS

CIRCUIT PACK	NAME	FUNCTION	LOCATION
FB294	trunk grid node selector	Selects stage 0 and 1 node leads for grids 0 and 1 with the order group and group 5 P-leads from the controller 0 or 1 FA772 packs.	15-31 FS7
FB294		Selects stage 0 and 1 node leads for grids 2 and 3 with the order group and group 5 P-leads from the controller 0 or 1 FA772 packs.	15-40 FS7
FC131	input level selector	Selects 1 of 4 test order functions with OP31-OP34 and OOR3 leads (This portion not shared). Also selects input levels for grids 0-1 with group 1 P-leads from controller 0 or 1 FA772's.	15-33 FS7
FC131		Selects 1 of 4 test order functions with 1P31-1P34 and 1OR3 leads (this portion not shared). Also selects input levels for grids 2-3 with group 1 P-leads from controller 0 or 1 FA772's.	15-42 FS7
FC132	output level selector	Selects output levels (from stage 1) for grids 0-1 with the group 2 and 4 P-leads from controller 0 or 1 FA772's.	15-35 FS7
FC132		Selects output levels (from stage 1) for grids 2-3 with the group 2 and 4 P-leads from controller 0 or 1 FA772's.	15-44 FS7
FC134	diagnostic control circuit	Provides certain inhibit and mode control functions to controllers during diagnostics. Works in conjunction with several other packs. Uses power supply from both controllers.	15-59 FS11
FC133	test point access circuit	Contains test point and quarantine relays; reflects F, S, and T points to master scanner for both controllers. Uses power supply from both controllers.	15-63 FS11

REFERENCE - SD1A327

TSC and JSC CONTROLLER PACKS

CIRCUIT PACK	NAME	FUNCTION	CONTROLLER LOCATION	
			0	1
FB292	+3v DC-DC Converter	Converts +24v to +3v to supply CP's FA772, FA773, FC130 and FB295.	15-03 FS12 TSC FS15 JSC	15-18
FA772	Two 6-bit register and translator circuits	Translates P.U. bus bits 0-7 and 16-19 to group 1 and 2 "P-leads".	15-04 FS2 TSC, JSC	15-19
FA772		Translates P.U. bus bits 8-15, 20-21, and 24-25 to group 3 and 4 "P-leads".	15-05 FS2 TSC, JSC	15-20
FA772		Translates P.U. bus bits 26-35 to group 5 "P-leads", order group leads, and H or M leads.	15-06 FS2 TSC, JSC	15-21
FA773	Controller logic and group check circuit	Processes the enable, enable verify, controller reset (bit 36), group check, and other controller functions. Also controls the FCG interrogate action (from bit 37) and the NT vertical functions in JSC's only.	15-07 FS4 TSC, JSC	15-22
FC130	Diagnostic bus driver circuit	Converts the low voltage leads from the IC's to the +24v levels required on the diagnostic bus. Has a few other functions.	15-08 FS5 TSC, JSC	15-23
FB290	Cut-through and gate driver circuit	Generates the A and B group check leads, and the C and CT (H/M) gate driver leads for the six lead groups in the translators.	15-09 FS3 TSC, JSC	15-24
FB295	Enable timer and pulse driver circuit	Timing for enabling translators, timing for generating enable verify, and drives the pulser circuit. Generates group check window.	15-12 FS6 TSC, JSC	15-27
FB296	Pulser circuit	Generates the 4.0 amp pulse through the grid to open or close remanent reed contacts.	15-51 FS6 TSC, JSC	15-55
~~FB291~~ 298 JSC only	FCG detector and test vertical circuit	Connects FCG detector or test vertical to the FA773 according to the order leads from the FA772's.	15-11 FS13 JSC	15-26

REFERENCES - SD1A327 TSC
SD1A328 JSC

JSC SHARED or CRITICAL CIRCUIT PACKS

CIRCUIT PACK	NAME	FUNCTION	LOCATION
FB293	junctor grid node selector	Selects stage 0 and 1 node leads for grids 0 and 1 with the order group and group 5 P-leads from the FA772 packs in controller 0 or 1.	15-31 FS7
FB293		Selects stage 0 and 1 node leads for grids 2 and 3 with the order group and group 5 P-leads from the FA772 padks in controllers 0 or 1.	15-40 FS7
FC131	input level selector	Selects 1 of 4 test order functions with 0P31-0P34 and 00R3 leads (this portion not shared). Also selects input levels for grids 0-1 with group 1 P-leads from controller 0 or 1 FA772's.	15-33 FS7
FC131		Selects 1 of 4 test order functions with 1P31-1P34 and 10R3 leads (this portion not shared). Also selects input levels for grids 2-3 with group 1 P-leads from controller 0 or 1 FA772's.	15-42 FS7
FC132	output level selector	Selects output levels for grid 0 with the group 2 P-leads from the FA772's in controllers 0 or 1.	15-35 FS7
FC132		Selects output levels for grid 1 with the group 4 P-leads from the FA772's in controllers 0 or 1.	15-37 FS7
FC132		Selects output levels for grid 2 with the group 2 P-leads from the FA772's in controllers 0 or 1.	15-44 FS7
FC132		Selects output levels for grid 3 with the group 4 P-leads from the FA772's in controllers 0 or 1.	15-46 FS7
FC134	diagnostic control circuit	Provides certain inhibit and mode control functions to controllers during diagnostics. Works in conjunction with several other packs. Uses power supply from both controllers	15-59 FS14
FC133	test point access circuit	Contains test point and quarantine relays; reflects F, S, and T points to master scanner for both controllers. Uses power supply from both controllers.	15-63 FS14

REFERENCE - SD1A328

PERIPHERAL BUS
CONNECTORIZED CABLE LOCATION

LINE SWITCH FRAME

ANSWER BUS CABLES	BUS 0	
BITS	IN	OUT
00-07	80-19-310	80-19-110
08-15	80-20-310	80-20-110
ASW	80-21-310	80-21-110

ANSWER BUS CABLES	BUS 1	
BITS	IN	OUT
00-07	80-34-310	80-34-110
08-15	80-35-310	80-35-110
ASW	80-36-310	80-36-110

ADDRESS BUS CABLES	BUS 0	
BITS	IN	OUT
00-07	80-11-310	80-11-110
08-15	80-12-310	80-12-110
16-23	80-13-310	80-13-110
24-31	80-14-310	80-14-110
32-37	80-15-310	80-15-110

ADDRESS BUS CABLES	BUS 1	
BITS	IN	OUT
00-07	80-26-310	80-26-110
08-15	80-27-310	80-27-110
16-23	80-28-310	80-28-110
24-31	80-29-310	80-29-110
32-37	80-30-310	80-30-110

PERIPHERAL BUS CONNECTORIZED CABLE LOCATION

JUNCTOR SWITCH FRAME

ADDRESS BUS CABLES	BUS 0	
BITS	IN	OUT
00-07	80-11-310	80-11-110
08-15	80-12-310	80-12-110
16-23	80-13-310	80-13-110
24-31	80-14-310	80-14-110
32-37	80-15-310	80-15-110

ADDRESS BUS CABLES	BUS 1	
BITS	IN	OUT
00-07	80-26-310	80-26-110
08-15	80-27-310	80-27-110
16-23	80-28-310	80-28-110
24-31	80-29-310	80-29-110
32-37	80-30-310	80-30-110

ENABLE AND SYNC POINTS FOR LSF 2:1

ENABLE	INPUT PIN	COLOR	SYNC POINT	CKT	CPD
00P	80-20-101	BL1W	80-16-308	LSF1	0
00N	-001	BL2W		LSF1	0
00P	-102	OR1W	-306	LSC	0
00N	-002	OR2W		LSC	0
00P	-103	GR1W	80-16-304	LSF0	0
00N	-003	GR2W		LSF0	0
-	-104	BR1W		-	-
-	-004	BR2W		-	-
11P	-105	BL1W	80-31-307	LSF1	0
11N	-005	BL2W		LSF1	0
11P	-106	OR1W	-305	LSC	0
11N	-006	OR2W		LSC	0
11P	-107	GR1W	-303	LSF0	0
11N	-007	GR2W		LSF0	0
-	-108	BR1W		-	-
-	-008	BR2W		-	-

ENABLE	INPUT PIN	COLOR	SYNC POINT	CKT	CPD
10P	80-35-101	BL1W	80-16-307	LSF1	1
10N	-001	BL2W		LSF1	1
10P	-102	OR1W	-305	LSC	1
10N	-002	OR2W		LSC	1
10P	-103	GR1W	80-16-303	LSF0	1
10N	-003	GR2W		LSF0	1
-	-104	BR1W		-	-
-	-004	BR2W		-	-
01P	-105	BL1W	80-31-308	LSF1	1
01N	-005	BL2W		LSF1	1
01P	-106	OR1W	-306	LSC	1
01N	-006	OR2W		LSC	1
01P	-107	GR1W	80-31-304	LSF0	1
01N	-007	GR2W		LSF0	1
-	-108	BR1W		-	-
-	-008	BR2W		-	-

ENABLE AND SYNC POINTS FOR LSF 4:1

ENABLE	INPUT PIN	COLOR	SYNC POINT	CKT	CPD
00P	80-20-101	BL1W	80-16-308	LSC1	0
00N	-001	BL2W		LSC1	0
00P	-102	OR1W	-306	LSF1	0
00N	-002	OR2W		LSF1	0
00P	-103	GR1W	-304	LSC0	0
00N	-003	GR2W		LSC0	0
00P	-104	BR1W	80-16-302	LSF0	0
00N	-004	BR2W		LSF0	0
11P	-105	BL1W	80-31-307	LSC1	0
11N	-005	BL2W		LSC1	0
11P	-106	OR1W	-305	LSF1	0
11N	-006	OR2W		LSF1	0
11P	-107	GR1W	-303	LSC0	0
11N	-007	GR2W		LSC0	0
11P	-108	BR1W	80-31-301	LSF0	0
11N	-008	BR2W		LSF0	0

ENABLE	INPUT PIN	COLOR	SYNC POINT	CKT	CPD
10P	80-35-101	BL1W	80-16-307	LSC1	1
10N	-001	BL2W		LSC1	1
10P	-102	OR1W	-305	LSF1	1
10N	-002	OR2W		LSF1	1
10P	-103	GR1W	-303	LSC0	1
10N	-003	GR2W		LSC0	1
10P	-104	BR1W	80-16-301	LSF0	1
10N	-004	BR2W		LSF0	1
01P	-105	BL1W	80-31-308	LSC1	1
01N	-005	BL2W		LSC1	1
01P	-106	OR1W	-306	LSF1	1
01N	-006	OR2W		LSF1	1
01P	-107	GR1W	-304	LSC0	1
01N	-007	GR2W		LSC0	1
01P	-108	BR1W	80-31-302	LSF0	1
01N	-008	BR2W		LSF0	1

ENABLE AND SYNC POINTS FOR TSF, JSF

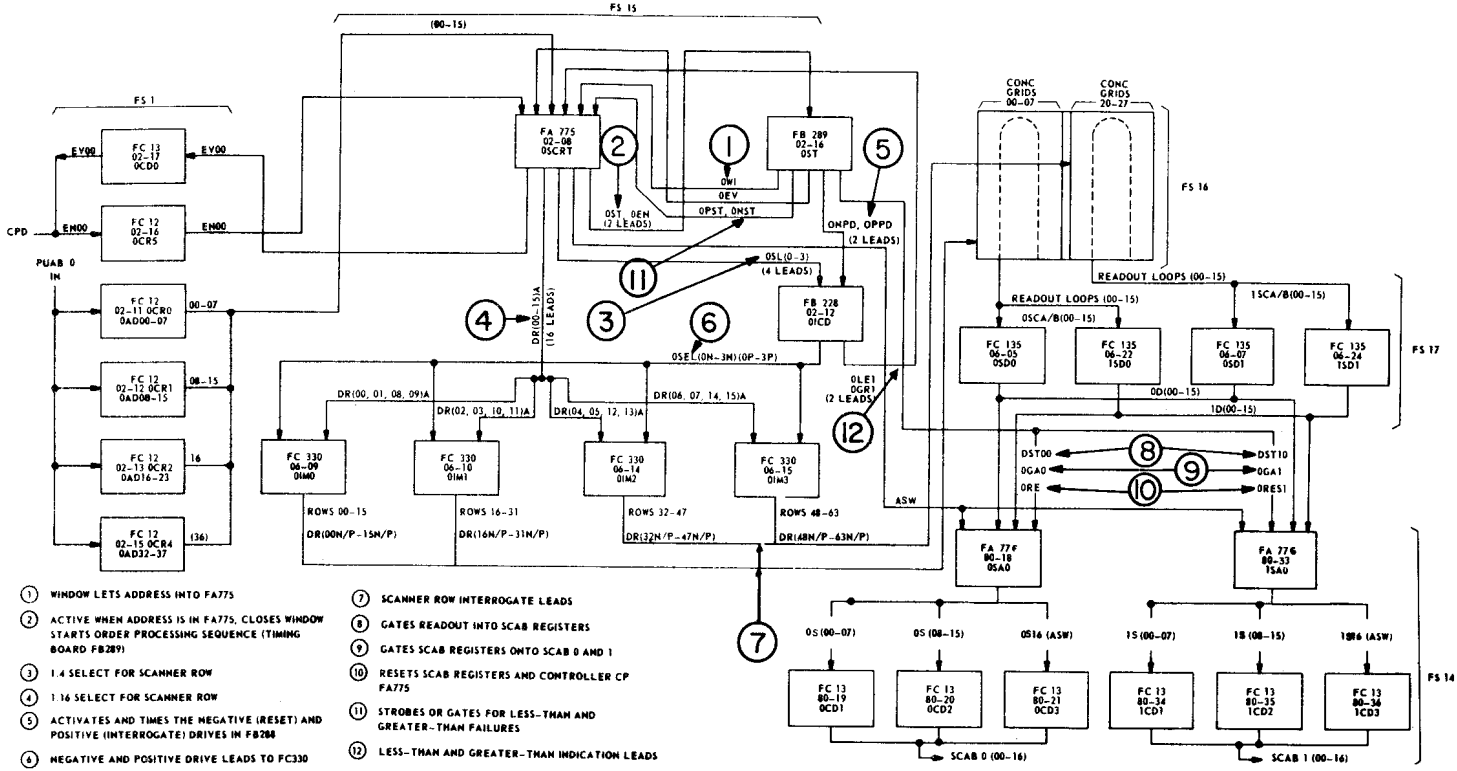
CONT 0

ENABLE	INPUT PIN	COLOR	SYNC POINT	CKT	CPD
00P	80-16-311	BL1W	80-16-308	3	0
00N	-211	BL2W		3	0
10P	-312	BL1W	-307	3	1
10N	-212	BL2W		3	1
00P	-313	OR1W	-306	2	0
00N	-213	OR2W		2	0
10P	-314	OR1W	-305	2	1
10N	-214	OR2W		2	1
00P	-315	GR1W	-304	1	0
00N	-215	GR2W		1	0
10P	-316	GR1W	-303	1	1
10N	-216	GR2W		1	1
00P	-317	BR1W	-302	0	0
00N	-217	BR2W		0	0
10P	-318	BR1W	-301	0	1
10N	-218	BR2W		0	1

BLUE → CONT

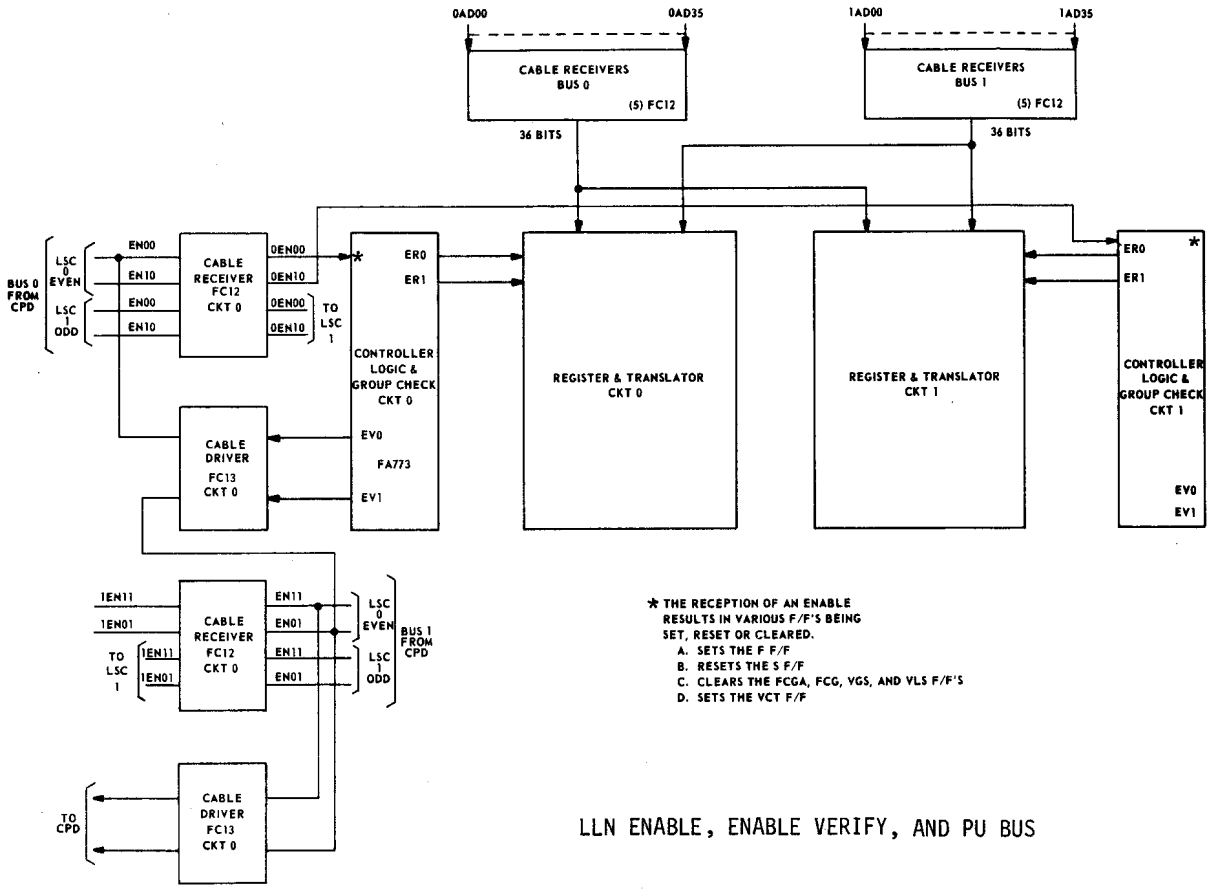
CONT 1

ENABLE	INPUT PIN	COLOR	SYNC POINT	CKT	CPD
01P	80-31-311	BL1W	80-31-308	3	1
01N	-211	BL2W		3	1
11P	-312	BL1W	-307	3	0
11N	-212	BL2W		3	0
01P	-313	OR1W	-306	2	1
01N	-213	OR2W		2	1
11P	-314	OR1W	-305	2	0
11N	-214	OR2W		2	0
01P	-315	GR1W	-304	1	1
01N	-215	GR2W		1	1
11P	-316	GR1W	-303	1	0
11N	-216	GR2W		1	0
01P	-317	BR1W	-302	0	1
01N	-217	BR2W		0	1
11P	-318	BR1W	-301	0	0
11N	-218	BR2W		0	0



1. WINDOW LETS ADDRESS INTO FA775
2. ACTIVE WHEN ADDRESS IS IN FA775, CLOSES WINDOW STARTS ORDER PROCESSING SEQUENCE (TIMING BOARD FB289)
3. 1:4 SELECT FOR SCANNER ROW
4. 1:16 SELECT FOR SCANNER ROW
5. ACTIVATES AND TIMES THE NEGATIVE (RESET) AND POSITIVE (INTERROGATE) DRIVES IN FB288
6. NEGATIVE AND POSITIVE DRIVE LEADS TO FC330
7. SCANNER ROW INTERROGATE LEADS
8. GATES READOUT INTO SCAB REGISTERS
9. GATES SCAB REGISTERS ONTO SCAB 0 AND 1
10. RESETS SCAB REGISTERS AND CONTROLLER CP FA775
11. STROBES OR GATES FOR LESS-THAN AND GREATER-THAN FAILURES
12. LESS-THAN AND GREATER-THAN INDICATION LEADS

4:1 LINE SCANNER BLOCK DIAGRAM (CONTROLLER 0) SD-1A326

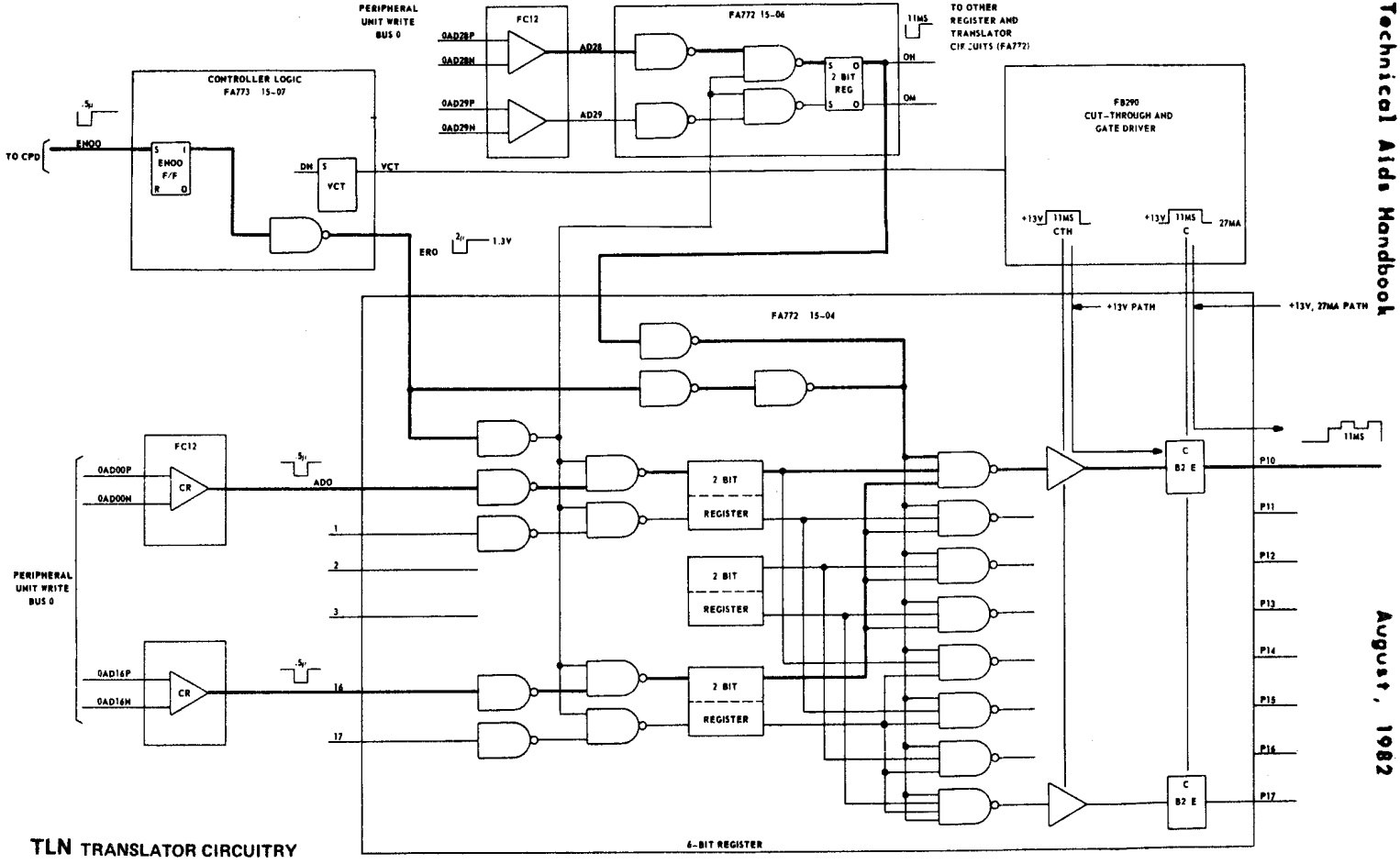


★ THE RECEPTION OF AN ENABLE RESULTS IN VARIOUS F/F'S BEING SET, RESET OR CLEARED.
- A. SETS THE F F/F
- B. RESETS THE S F/F
- C. CLEARS THE FCGA, FCG, VGS, AND VLS F/F'S
- D. SETS THE VCT F/F

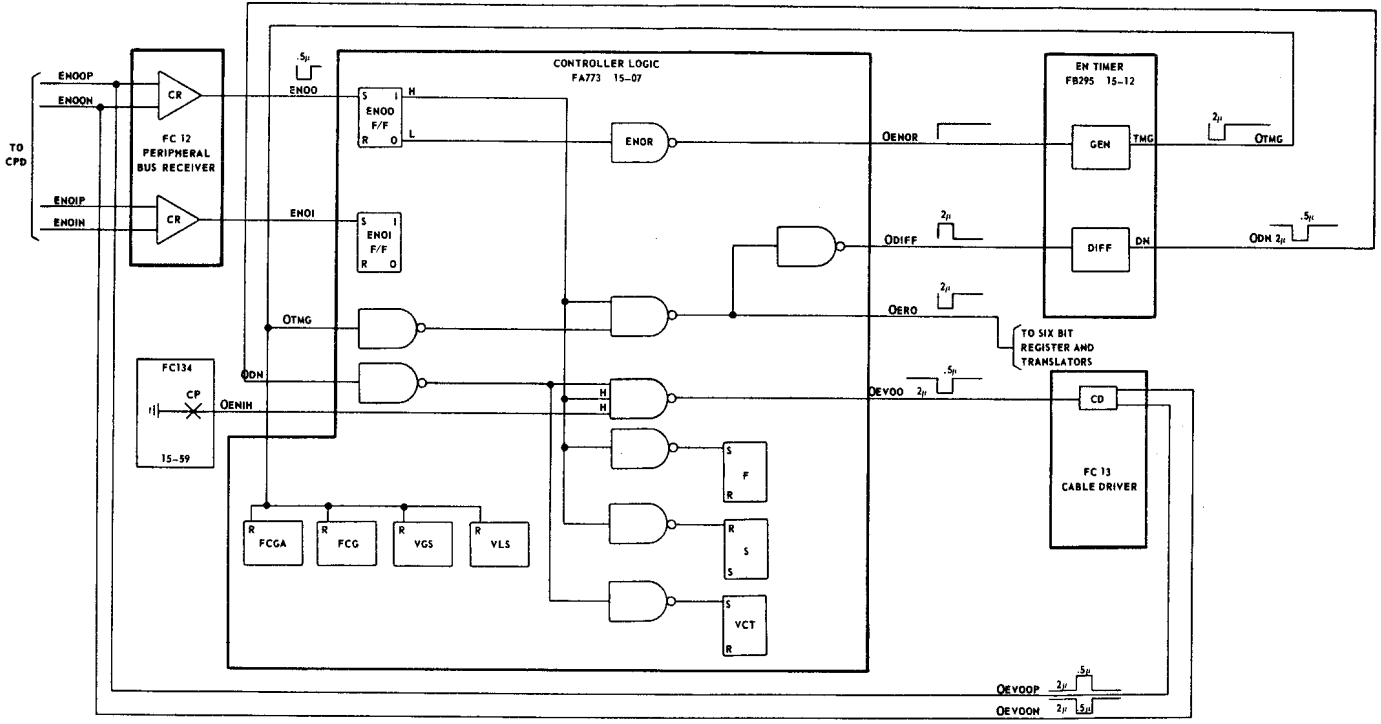
LLN ENABLE, ENABLE VERIFY, AND PU BUS

REMREED LINE SCANNER ANSWER 4:1 (2:1)

WCH/80

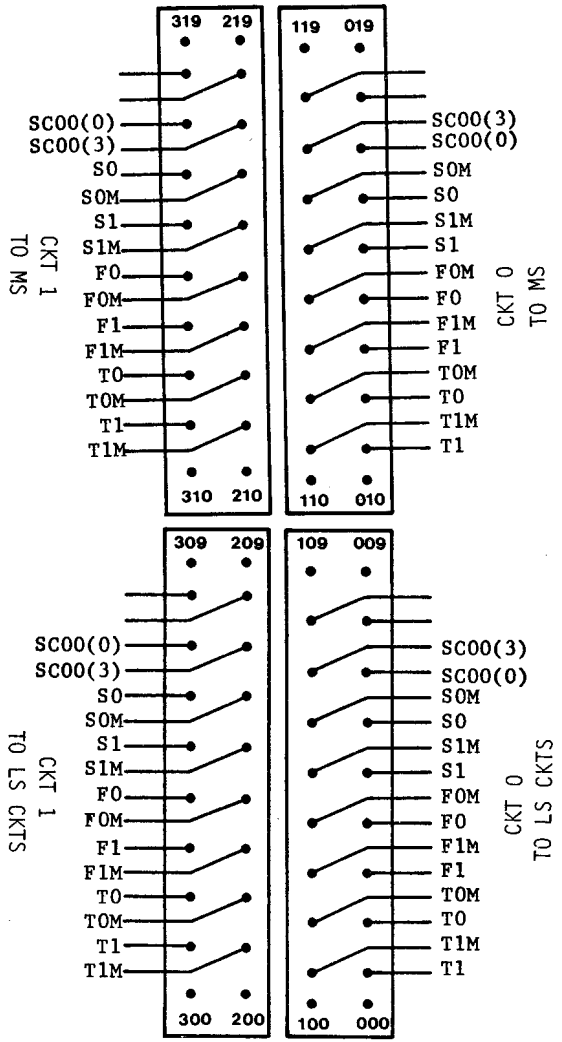


TLN TRANSLATOR CIRCUITRY

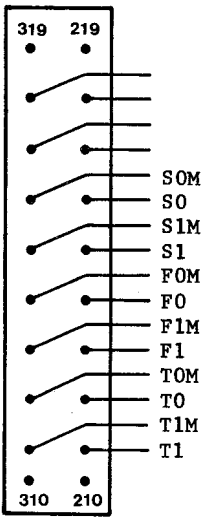


TLN ENABLE, CONTROLLER 0

FST CABLES, LSF

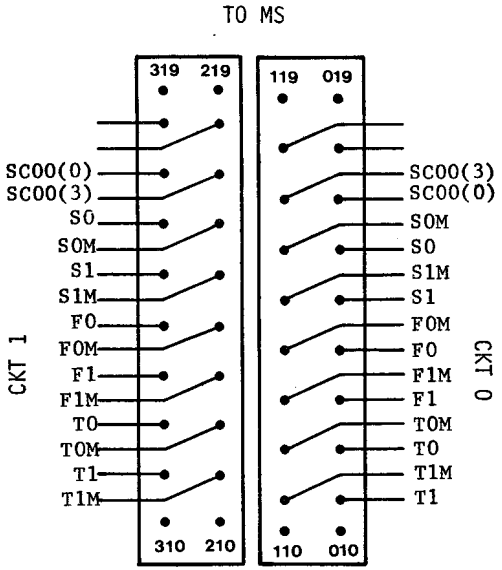


CONN 80-66

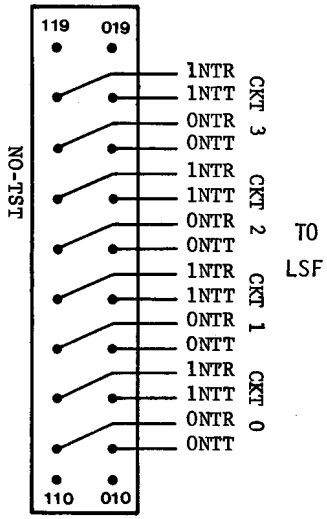


15-67
UNIT CONN

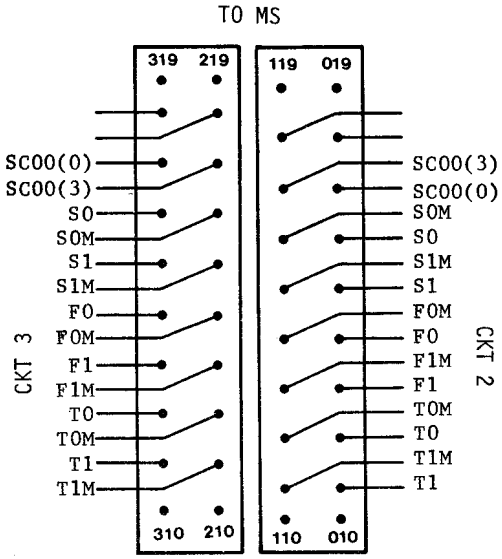
FST CABLES, JSF, TSF



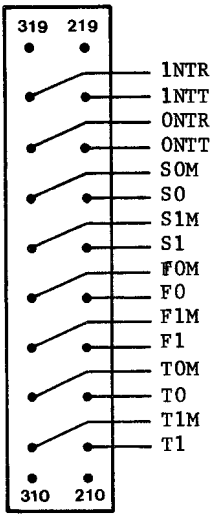
CONN 80-66



CONN 80-65

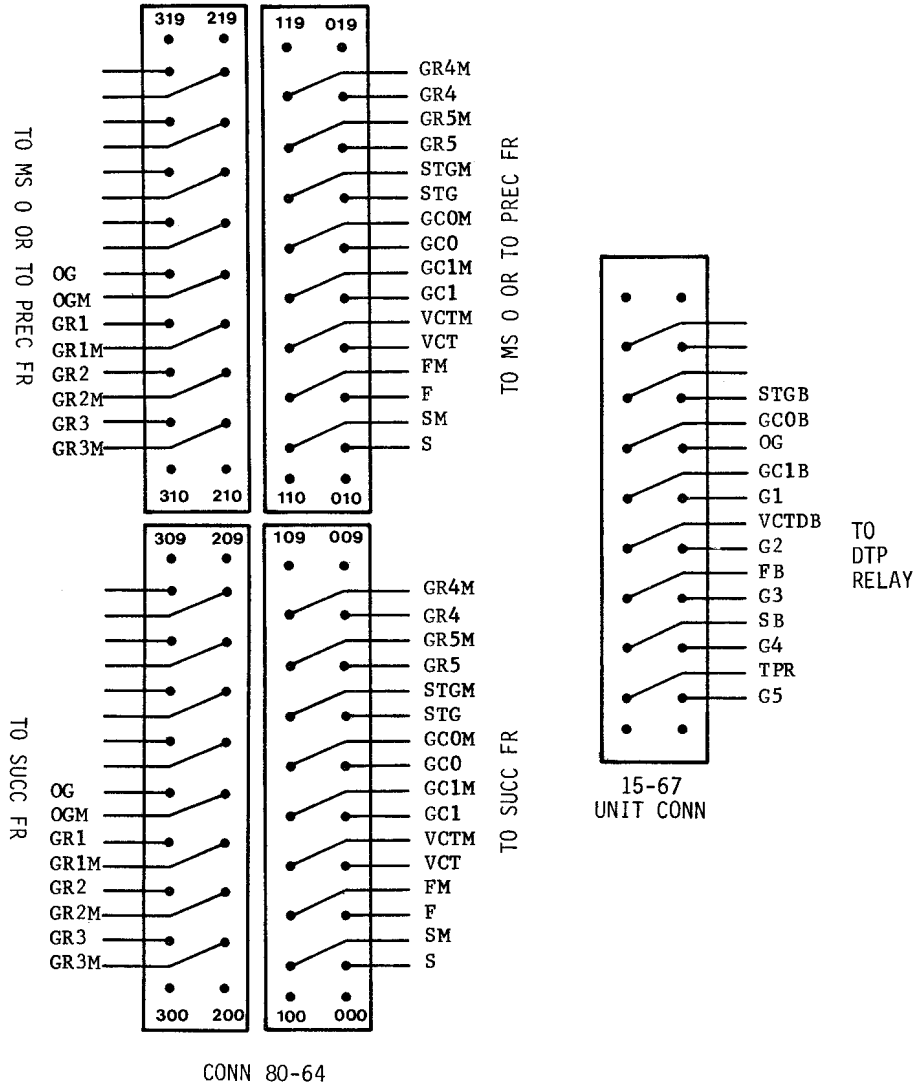


CONN 80-67



15-67
UNIT CONN

DIAGNOSTIC BUS CABLES, TSF, JSF, LSF



RELATED INPUT MESSAGES - NETWORK FRAMES

FAB-MB- aa b cc d e f g h i.

REMOVES SPECIFIED LINKS FROM SERVICE.

FAB-RESTORE- aa b cc d e f g h i.

RETURNS SPECIFIED LINKS TO SERVICE.

FAB-SET- aa bb c d e f gg h i.

SETS A PARTIAL PATH IN ANY NETWORK FRAME. LINKS IN PATH MUST HAVE BEEN BUSIED USING FAB-MB MESSAGES.

FAB-STATUS- aa b cc d e f g h i.

DETERMINES PRESENT CONDITION OF LINK OR SWITCH SPECIFIED.

NET-DGN- aaa bb c d e.

REQUESTS DIAGNOSTIC, QUARANTINING, OR RESTORAL OF THE SIGNAL DISTRIBUTOR OR NETWORK CONTROLLER SPECIFIED.

NET-ONE- aaa bb c d e ffffffff gggggggg hhhhhhhh.

ALLOWS SINGLE ORDER TO BE SENT REPEATEDLY TO A NETWORK OR SIGNAL DISTRIBUTOR FRAME.

NET-LINE- aaa aaaa bbbb.

IDENTIFIES OTHER NETWORK TERMINATION (LINE OR TRUNK) IF LINE IS IN USE ON A CALL

T-SCAN- a b cc d ee ff.

READS ONE SCAN POINT OR A ROW OF POINTS IN THE SCANNER SPECIFIED.

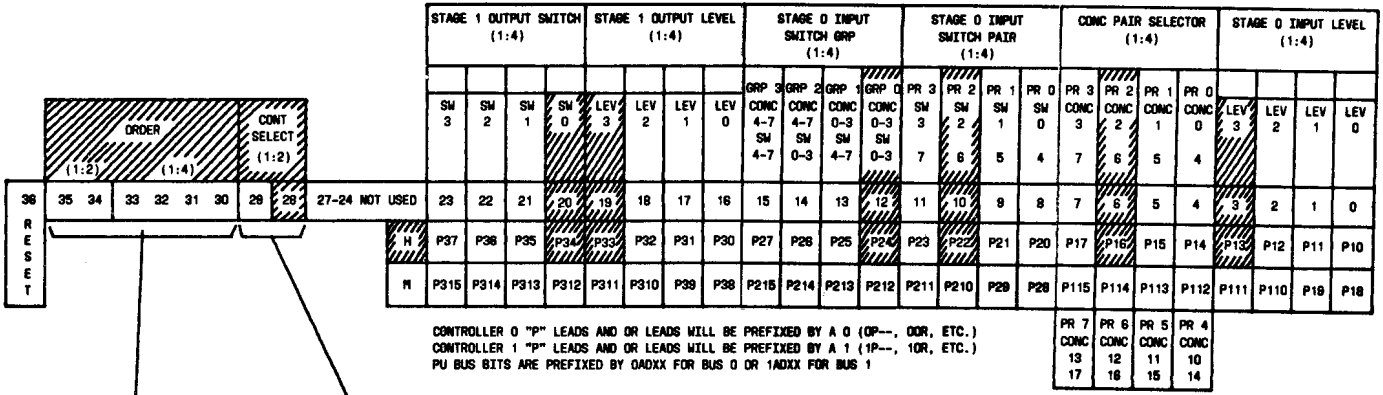
VFY-TNN- aa bb c d e f.

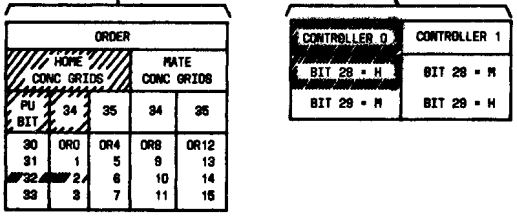
VERIFIES A TRUNK NETWORK NUMBER ON A TSF

VFY-UNTY-15 aaa bbbb.

PRINTS CONTENTS OF AUX BLOCK ASSOCIATED WITH UNIT TYPE AND MEMBER NUMBER

REFERENCE: IM-6A001-01





2:1 LSC — PU ADDRESS TO TRANSLATOR P-LEADS

PU BUS BIT	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HOME CONCENTRATOR GRID	RESET		X	OR3	OR2	OR1	OR0			P43	P42	P41	P40	P37	P36	P35	P34	P33	P32	P31	P30	P27	P26	P25	P24	P23	P22	P21	P20	P17	P16	P15	P14	P13	P12	P11	P10
		X		OR7	OR6	OR5	OR4																															
MATE CONCENTRATOR GRID	RESET		X	OR11	OR10	OR9	OR8			P47	P46	P45	P44	P315	P314	P313	P312	P311	P310	P39	P38	P215	P214	P213	P212	P211	P210	P29	P28	P115	P114	P113	P112	P111	P110	P19	P18
		X		OR15	OR14	OR13	OR12																														

										CONC 3 OR 7	CONC 2 OR 6	CONC 1 OR 5	CONC 0 OR 4	CONC 4-7 SW 263	CONC 4-7 SW 061	CONC 0-3 SW 263	CONC 0-3 SW 061	SW 1 OR 3	SW 1 OR 3	SW 0 OR 2	SW 0 OR 2															
														GRP 3	GRP 2	GRP 1	GRP 0	ODD A LINK	EVEN A LINK	ODD A LINK	EVEN A LINK															
										CONCENTRATOR GRID PAIR				STAGE 0 SWITCH GROUP				STAGE 0 SWITCH																		

CONTROLLER 0	CONTROLLER 1
AD28 = H	AD28 = M
AD28 = M	AD28 = H

CONTROLLER 0 OR LEADS AND P-LEADS WILL BE PREFIXED BY A 0 (0PXX, 0ORX, ETC.)

CONTROLLER 1 OR LEADS AND P-LEADS WILL BE PREFIXED BY A 1 (1PXX, 1ORX, ETC.)

PU BUS BITS ARE PREFIXED BY A 0AD FOR BUS 0, AND A 1AD FOR BUS 1 (0AD35, 1AD35 ETC.)

CONC PR	GRIDS
0	0,4
1	1,5
2	2,6
3	3,7
4	20,24
5	21,25
6	22,26
7	23,27

NORMAL MODE — CONC GROUPS

CONTLR 0 — 0
CONTLR 0 — 1
CONTLR 1 — 2
CONTLR 1 — 3

HOME CONCENTRATOR GRID (0-7)

		STAGE 0 INPUT LEVEL				STAGE 1 OUTPUT SWITCH				STAGE 1 OUTPUT LEVEL			
		P10	P11	P12	P13	P27	P26	P25	P24	P23	P22	P21	P20
CONC GRIDS 0-3 OR 20-23	P14	0	1	2	3	3	2	1	0	3	2	1	0
	P15	4	5	6	7								
	P16	8	9	10	11								
	P17	12	13	14	15								
		P20	P21	P22	P23	P17	P16	P15	P14	P13	P12	P11	P10
CONC GRIDS 4-7 OR 24-27	P24	0	1	2	3	3	2	1	0	3	2	1	0
	P25	4	5	6	7								
	P26	8	9	10	11								
	P27	12	13	14	15								

MATE CONCENTRATOR GRID (0-7)

		STAGE 0 INPUT LEVEL				STAGE 1 OUTPUT SWITCH				STAGE 1 OUTPUT LEVEL			
		P18	P19	P110	P111	P215	P214	P213	P212	P211	P210	P29	P29
CONC GRIDS 0-3, 20-23	P112	0	1	2	3	3	2	1	0	3	2	1	0
	P113	4	5	6	7								
	P114	8	9	10	11								
	P115	12	13	14	15								
		P28	P29	P210	P211	P115	P114	P113	P112	P111	P110	P18	P18
CONC GRIDS 4-7, 24-27	P212	0	1	2	3	3	2	1	0	3	2	1	0
	P213	4	5	6	7								
	P214	8	9	10	11								
	P215	12	13	14	15								

4:1 LSC — PU Address to Translator P-Leads

4:1 LSF

STAGE 0 SWITCH
0 = (20 or 22) and (16 or 17)
1 = (20 or 22) and (18 or 19)
2 = (21 or 23) and (16 or 17)
3 = (21 or 23) and (18 or 19)

STAGE 1 LEVEL
0 = (08 and 20 or 21) or (00 and 22 or 23)
1 = (09 and 20 or 21) or (01 and 22 or 23)
2 = (10 and 20 or 21) or (02 and 22 or 23)
3 = (11 and 20 or 21) or (03 and 22 or 23)

STAGE 1 SWITCH
0 = (12 and 20 or 21) or (04 and 22 or 23)
1 = (13 and 20 or 21) or (05 and 22 or 23)
2 = (14 and 20 or 21) or (06 and 22 or 23)
3 = (15 and 34 or 35) or (07 and 22 or 23)

HOME CONCENTRATORS = 28 (controller 0), 29 (controller 1)
MATE CONCENTRATORS = 29 (controller 0), 28 (controller 1)

ØR0	not used	= 34 and 30
ØR1	close stage 0 and 1, open cutoff	= 34 and 31
ØR2	close stage 1, open stage 0, cutoffs unchanged	= 34 and 32
ØR3	test	= 34 and 33
ØR4	open stage 0, open cutoffs	= 35 and 30
ØR5	close stage 0 and 1, close cutoffs	= 35 and 31
ØR6	not used	= 35 and 32
ØR7	open stage 0, close cutoffs	= 35 and 33

CONCENTRATOR
0 = 24 and (20 or 21)
1 = 25 and (20 or 21)
2 = 26 and (20 or 21)
3 = 27 and (20 or 21)
4 = 24 and (22 or 23)
5 = 25 and (22 or 23)
6 = 26 and (22 or 23)
7 = 27 and (22 or 23)

20 = group 0
21 = group 2
22 = group 1
23 = group 3

STAGE 0 LEVEL
0 = (00 and 04 and 20 or 21) or (08 and 12 and 22 or 23)
1 = (01 and 04 and 20 or 21) or (09 and 12 and 22 or 23)
2 = (02 and 04 and 20 or 21) or (10 and 12 and 22 or 23)
3 = (03 and 04 and 20 or 21) or (11 and 12 and 22 or 23)
4 = (00 and 05 and 20 or 21) or (08 and 13 and 22 or 23)
5 = (01 and 05 and 20 or 21) or (09 and 13 and 22 or 23)
6 = (02 and 05 and 20 or 21) or (10 and 13 and 22 or 23)
7 = (03 and 05 and 20 or 21) or (11 and 13 and 22 or 23)
8 = (00 and 06 and 20 or 21) or (08 and 14 and 22 or 23)
9 = (01 and 06 and 20 or 21) or (09 and 14 and 22 or 23)
10 = (02 and 06 and 20 or 21) or (10 and 14 and 22 or 23)
11 = (03 and 06 and 20 or 21) or (11 and 14 and 22 or 23)
12 = (00 and 07 and 20 or 21) or (08 and 15 and 22 or 23)
13 = (01 and 07 and 20 or 21) or (09 and 15 and 22 or 23)
14 = (02 and 07 and 20 or 21) or (10 and 15 and 22 or 23)
15 = (03 and 07 and 20 or 21) or (11 and 15 and 22 or 23)

ORDER

ORDER GROUP						GRP 6		GRP 5		GRP 4		NA		GRP 3		GRP 2		GRP 1		GRP 4				GRP 3				GRP 2				GRP 1			
35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

NN10 LINE 5 INSERTED HERE

TRANSLATION OF GROUPS TO OBTAIN P-LEADS

GRP 6	
CONT 0	CONT 1
BIT 28 H (GRIDS 0 & 1) BIT 29 M (GRIDS 2 & 3)	BIT 28 M (GRIDS 0 & 1) BIT 29 H (GRIDS 2 & 3)

CONTROLLER 0					
	GRP 6		GRP 5		
	29	28	27	26	
OP50		X		X	GRID 0
OP51		X	X		GRID 1
OP52	X			X	GRID 2
OP53	X		X		GRID 3

CONTROLLER 1					
	GRP 6		GRP 5		
	29	28	27	26	
1P50	X			X	GRID 2
1P51	X		X		GRID 3
1P52		X		X	GRID 0
1P53		X	X		GRID 1

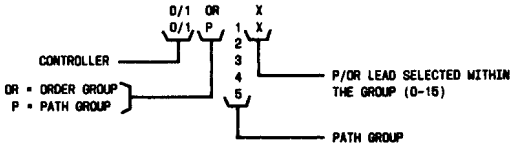
STAGE 0		STAGE 1		CONT 0 GRID	CONT 1 GRID
INPUT SWITCH	INPUT LEVEL	OUTPUT SWITCH	OUTPUT LEVEL		
GRP 3 P 30-37	GRP 1 P 10-17	GRP 4 P 40-47	GRP 2 P 20-27	0	2
GRP 3 P 30-37	GRP 1 P 10-17	GRP 4 P 20-27	GRP 2 P 40-47	1	3
GRP 3 P 38-315	GRP 1 P 18-115	GRP 4 P 48-415	GRP 2 P 28-215	2	0
GRP 3 P 38-315	GRP 1 P 18-115	GRP 2 P 28-215	GRP 4 P 48-415	3	1

SWITCH AND LEVEL WILL EQUAL P LEAD NUMBER
P 30 - P 37 = INPUT SWITCH 0-7
P 38 - P315 = INPUT SWITCH 0-7

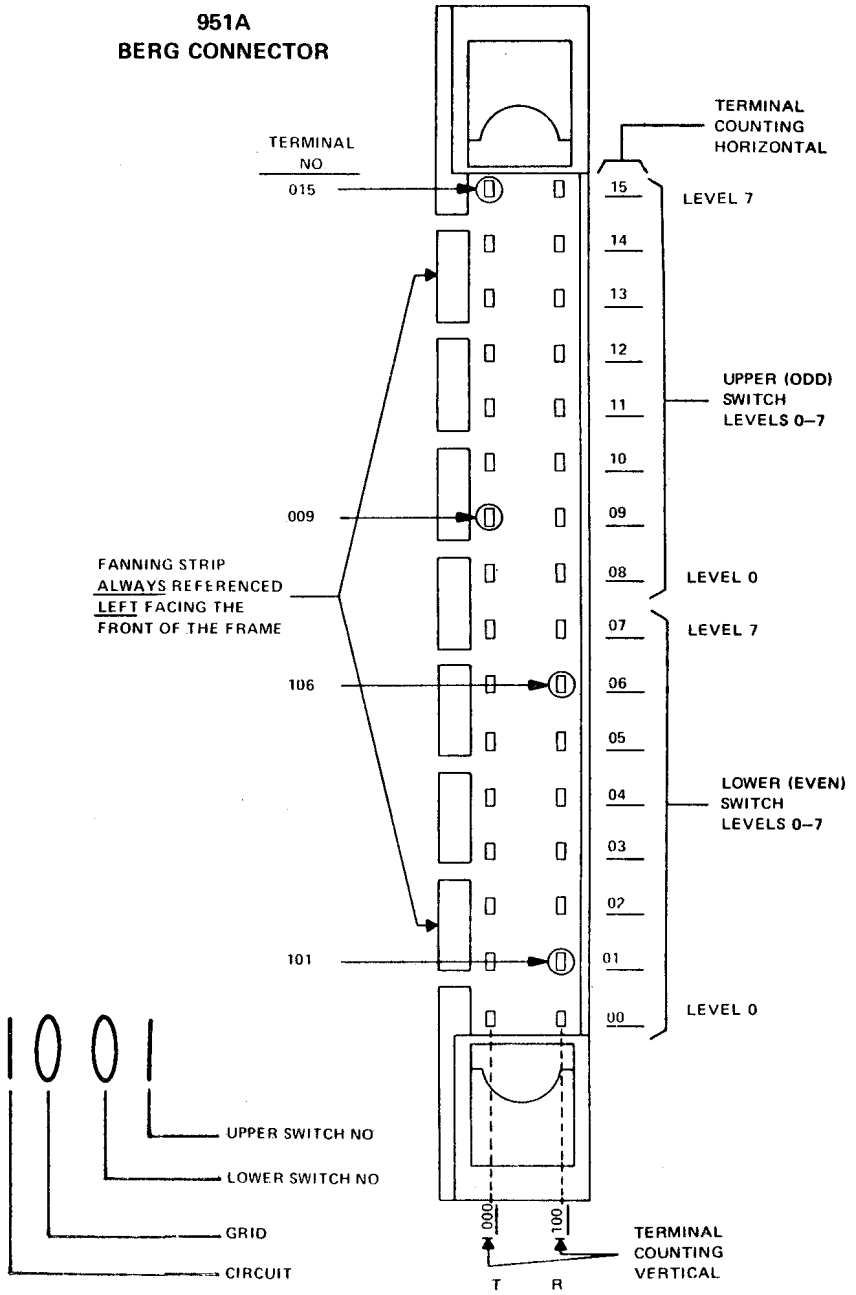
PU ADDRESS BIT

	1/8	OR	35	34	33	32	31	30
GRP 4	1/8	P4	25	24	15	14	13	12
GRP 3	1/8	P3	21	20	11	10	9	8
GRP 2	1/8	P2	18	18	7	6	5	4
GRP 1	1/8	P1	17	16	3	2	1	0
OP - LEADS CONT 0		0 OR 8		X				X
		1 OR 9		X			X	
		2 OR 10		X		X		
1P - LEADS CONT 1		3 OR 11		X	X			
		4 OR 12	X					X
		5 OR 13	X				X	
		6 OR 14	X			X		
		7 OR 15	X		X			

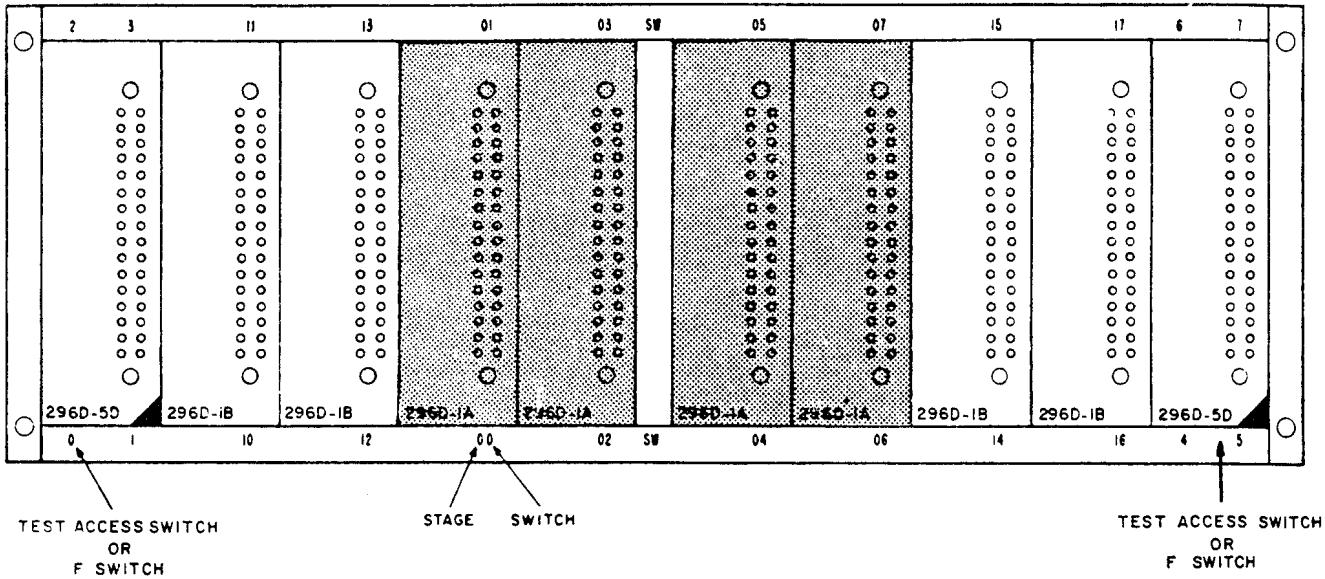
HOME
MATE



TSC AND JSC ADDRESS BITS TO PATH CONTROL LEADS


951A
BERG CONNECTOR
TERMINAL NO
015
009
106
101
FANNING STRIP
ALWAYS REFERENCED
LEFT FACING THE
FRONT OF THE FRAME
TERMINAL
COUNTING
HORIZONTAL
15
14
13
12
11
10
09
08
07
06
05
04
03
02
01
00
LEVEL 7
UPPER (ODD)
SWITCH
LEVELS 0–7
LEVEL 0
LEVEL 7
LOWER (EVEN)
SWITCH
LEVELS 0–7
LEVEL 0
UPPER SWITCH NO
LOWER SWITCH NO
GRID
CIRCUIT
000
100
T
R
TERMINAL
COUNTING
VERTICAL

10A JUNCTOR GRID ORGANIZATION

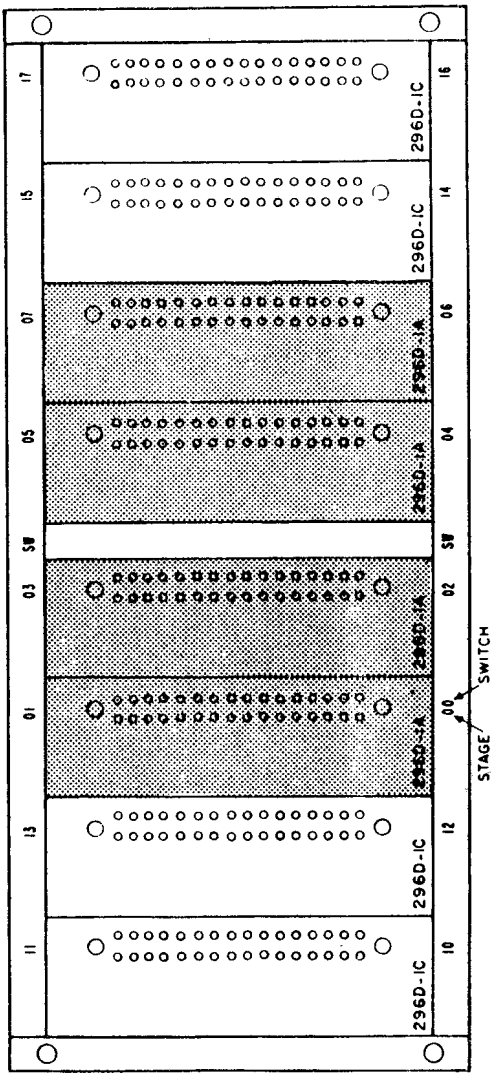


STAGE 0

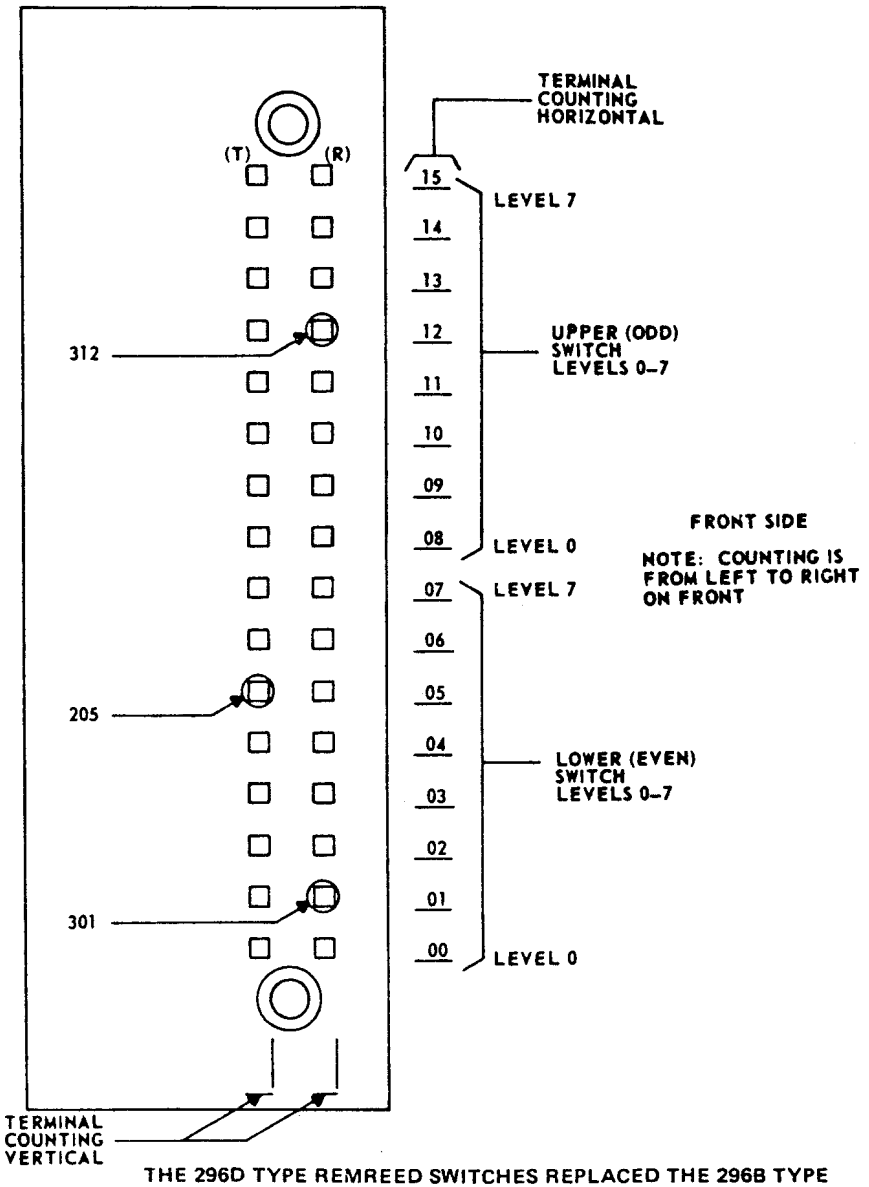
STAGE 1

TEST ACCESS SWITCH OR F SWITCH

11A TRUNK GRID ORGANIZATION

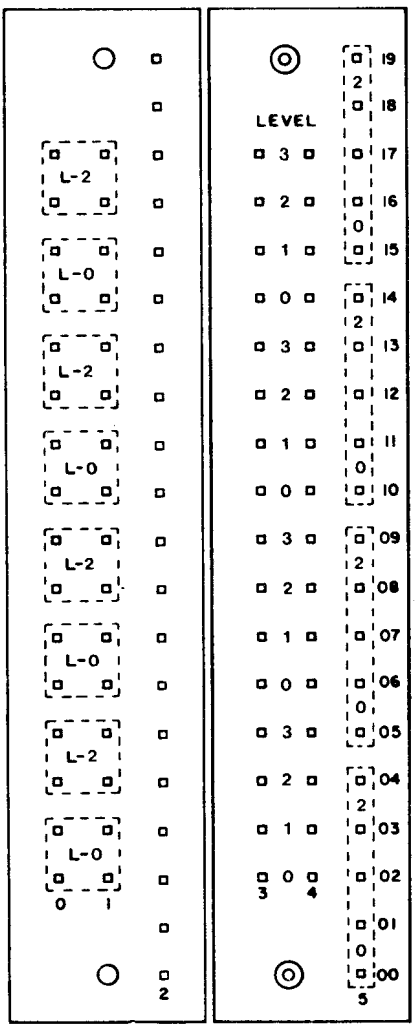


296D TYPE REMREED SWITCH

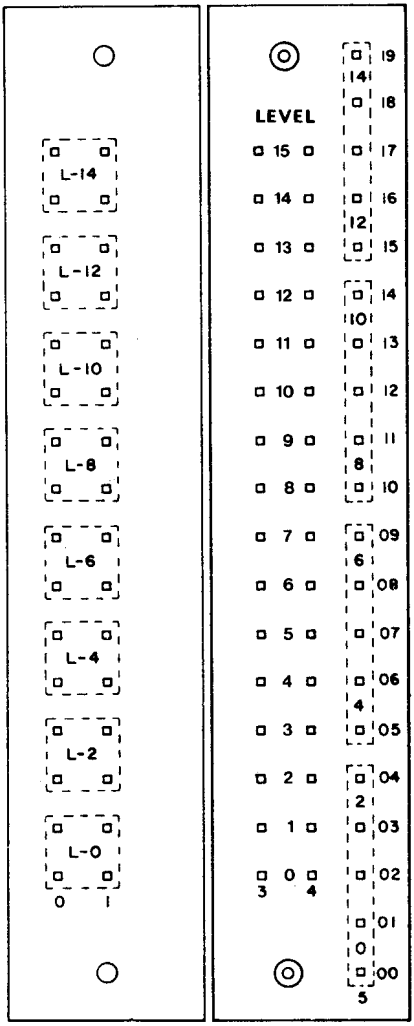


THE 296D TYPE REMREED SWITCHES REPLACED THE 296B TYPE REMREED SWITCHES WHICH WERE USED IN THE EARLY 1A ESS NETWORKS USING 10A AND 11A GRIDS. THE 296B HAD FOUR VERTICAL ROWS OF TERMINALS. IN ADDITION TO THE TWO VERTICAL ROWS OF TERMINALS USED TO ACCESS THE TIP AND RING PATH THERE WERE TWO ROWS OF TERMINALS ON THE LEFT SIDE OF THE SWITCH PACKAGE TO GAIN ACCESS TO THE PULSE PATH. THESE PULSE PATH TERMINALS HAVE BEEN ELIMINATED ON THE 296D TYPE SWITCH PACKAGES LEAVING ACCESS ONLY TO THE TIP AND RING PATH.

REMREED SWITCH PACKAGE TYPE 296D – (FRONT VIEW)

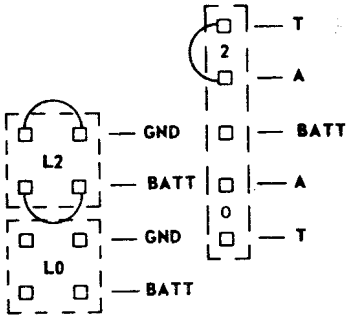


SWITCH AS PART OF 12A CONCENTRATOR GRID. 12B GRID SWITCH OMITS COLUMN 2.

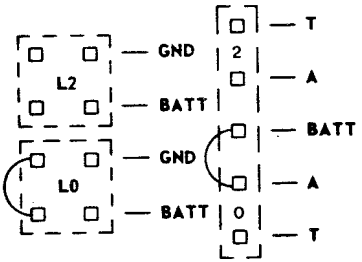


REMREED SWITCH IN 13B CONCENTRATION GRID

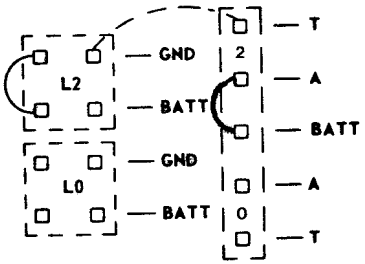
STRAPPING 296D FOR LOOP START, GROUND START, AND NO-TEST VERTICAL



STRAPPING FOR LOOP-START
FIGURE A

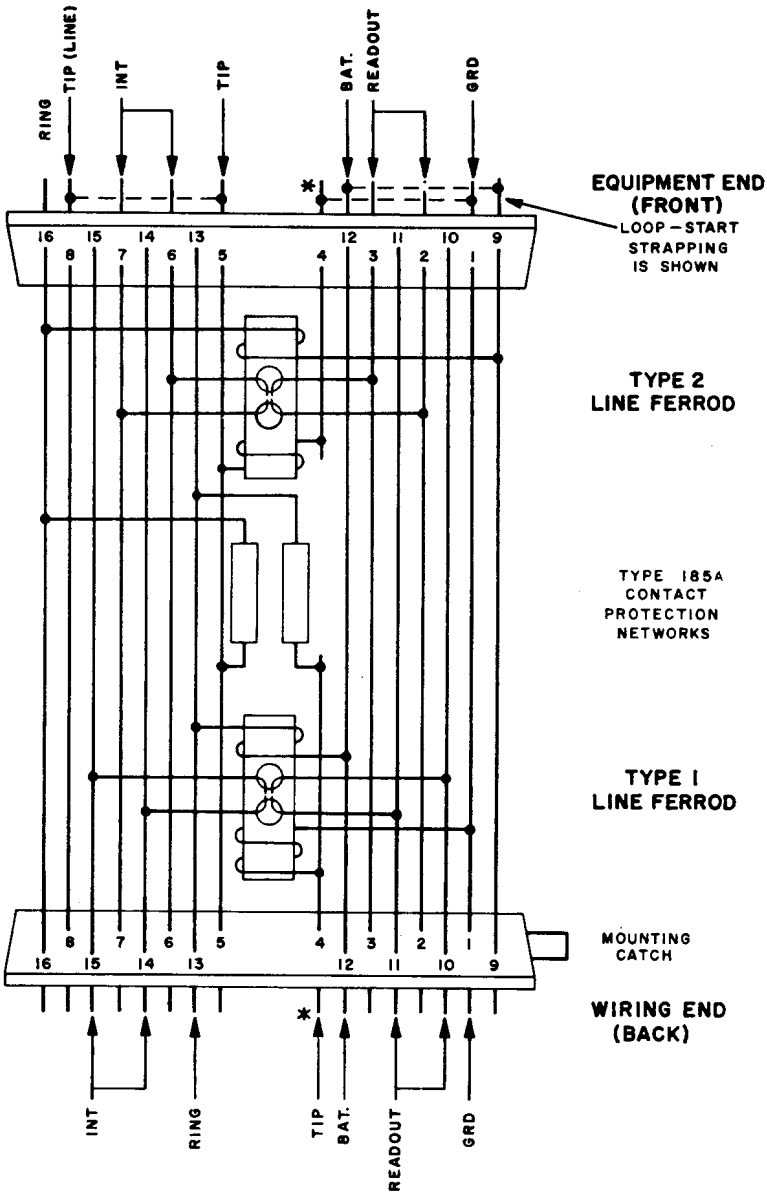


STRAPPING FOR GROUND-START
FIGURE B



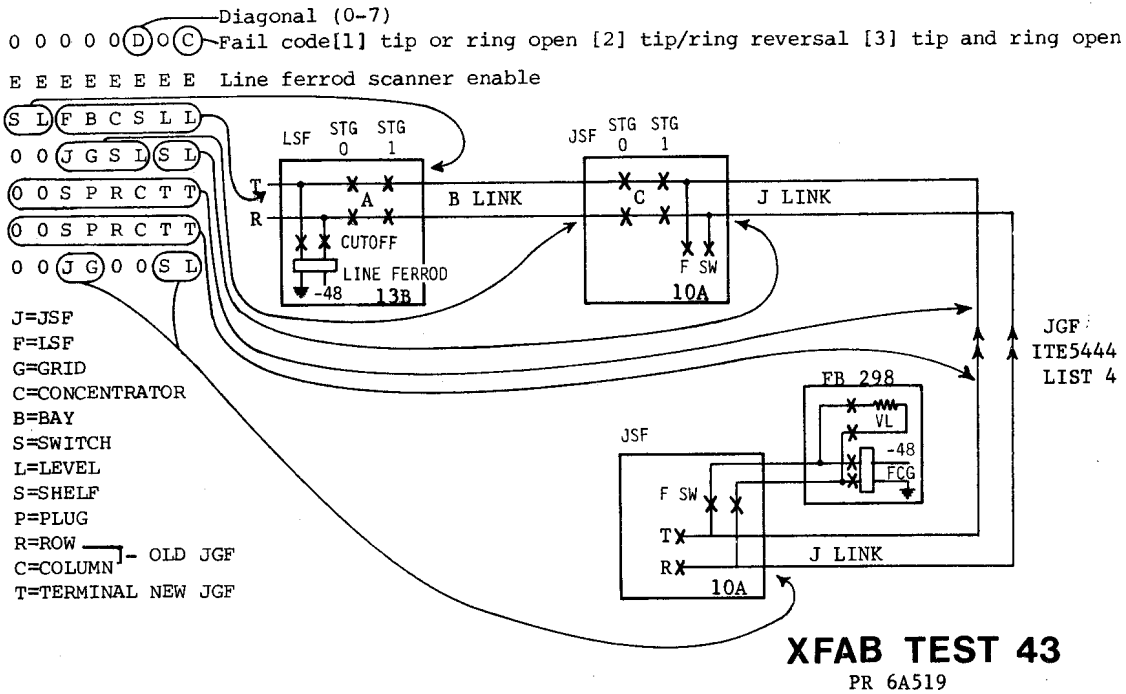
STRAPPING FOR NO-TEST LEN
(WITHOUT 23A APPARATUS)
FIGURE C

FOR STRAPPING NO-TEST VERTICAL CONNECTION ON 12B OR 13B CONCENTRATOR GRID USING 23A APPARATUS UNIT, SEE SD1A325 (2:1 LSF) OR SD1A326 (4:1 LSF).



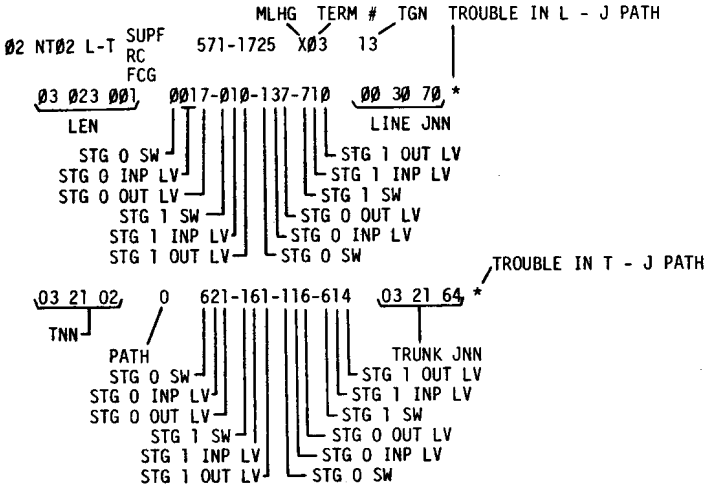
* NO. 4 WIRE ROD IS CUT BETWEEN THE FRONT AND BACK FERROD UNIT

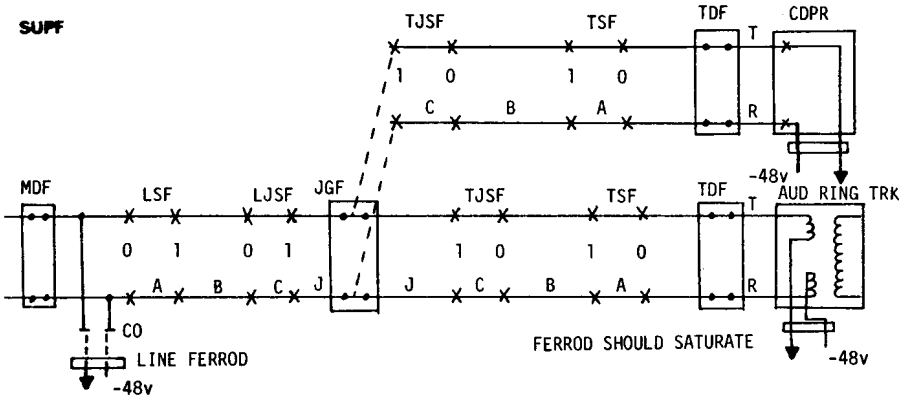
Wiring Arrangement of Type 1B Ferrod Sensor Assembly

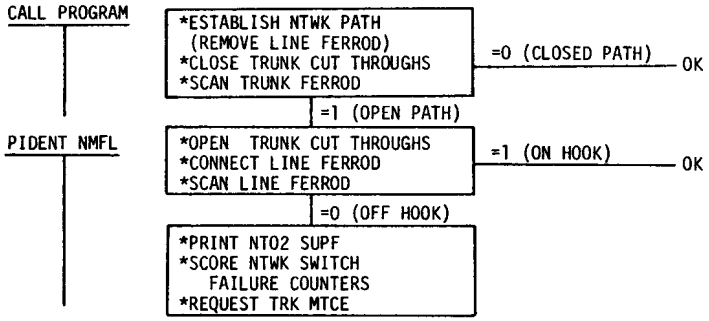


XFAB TEST 43

PR 6A519







METHOD OF PERFORMING TEST

Whenever a network connection is completed in the ESS office, a supervisory check is made to verify the continuity of the newly established path. In theory this test should detect opens in the trunks or switching network. In fact, many of the failure messages are a result of line or trunk problems external to the ESS machine.

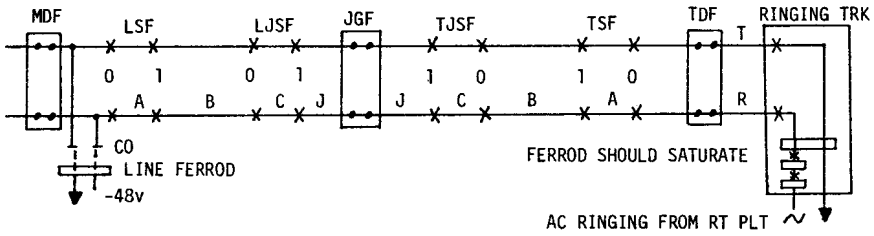
POSSIBLE CAUSES OF TROUBLE

1. Broken cross-connect on trunk frame.
2. Defective trunk units or switches (trk ckt to line path).
3. Split pulse paths in the ESS network.
4. Crossed lines on the MDF or in the cable. Tip of one line crossed to the ring of another causes excessive supervisory failures.
5. Application of breakdown tone to a line. Voltmeter tests of such lines will not show a DC trouble, and the line must be monitored to detect the tone.
6. JGF plug or jack troubles.
7. Crosses or grounds on lines which fall between the saturation point of the line ferrod (~ 4800-5200Ω) and a CDPR or RA trunk (~ 2700Ω). LEN to CDPR path.

MEANS OF REDUCING FAILURES

1. Application of cable tone to a line only with the coils removed.
2. Close surveillance of T-T supervision failures to identify bad trunks.
3. Repeated failures to one switch frame could indicate either a split pulse path of a deteriorating pulser.

RC



METHOD OF PERFORMING TEST

While ringing current is being applied to a line, an AC continuity check is made to assure that sufficient current is flowing in the circuit. This test will detect open lines or keysets with insufficient capacitance.

In this test the failure will not be printed out until after the originating party abandons the connection. If the ringing is tripped, for any reason, the failure message will not be printed.

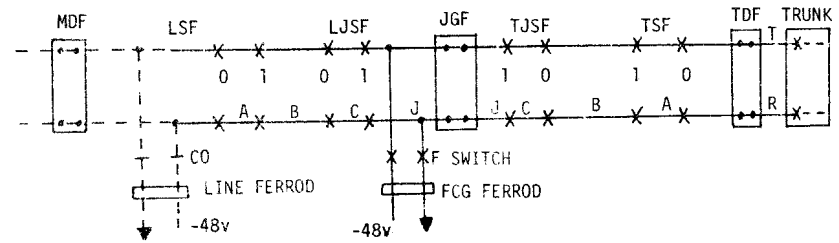
POSSIBLE CAUSES OF TROUBLE

1. Defective switches or ringing trunks.
2. Open cross connect on MDF.
3. Lines put into translations too soon or not removed properly when service has been discontinued.
4. 400B keyset unit is the primary cause. Due to its design, causes false failures.

MEANS OF REDUCING FAILURES

1. Analyze printouts for repeated failures to the MLHG.
2. Periodically check the RC failures for repeated ringing trunk failures.
3. Coordinate cross connect work with service order TTY entries.

FCG



FCG (cont'd)

METHOD OF PERFORMING TEST

When a network connection is established, it is checked for the presence of a false cross or ground on the tip and ring connection. This test is performed with stage 0 of the LSF open to remove the line. However, the trunk unit is associated with the test since the crosspoints of the TSF are closed. Generally failures of this type indicate a problem within the ESS trunk or network.

The FCG test is made from the No Test Vertical associated with the JSF. When attempting to isolate a failure in the combined mode, one controller cannot test for FCG in the grids normally controlled by the other controller. By removing a JSF controller, half of the FCG testing in that frame is eliminated.

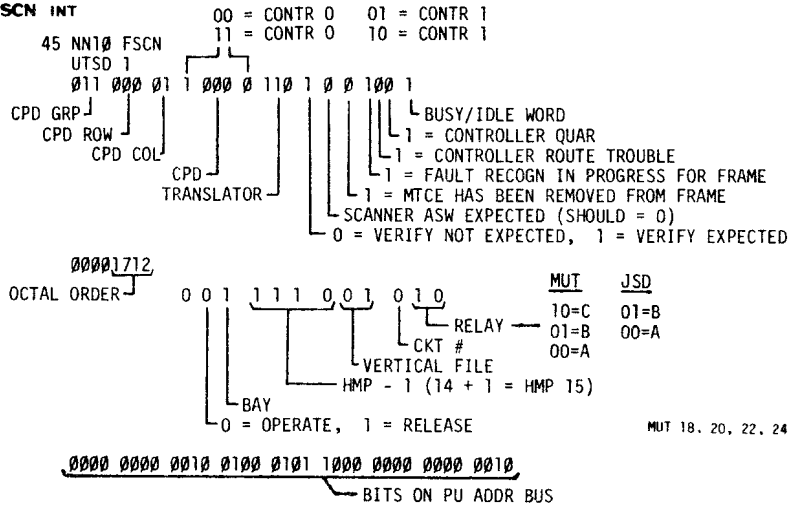
POSSIBLE CAUSES OF TROUBLE

1. Cross connect touching on TDF.
2. JGF crosses in plugs or jacks.
3. Defective switches (closed trunk cutoff).
4. Stuck "F" switches.
5. Defective trunk units

MEANS OF REDUCING FAILURES

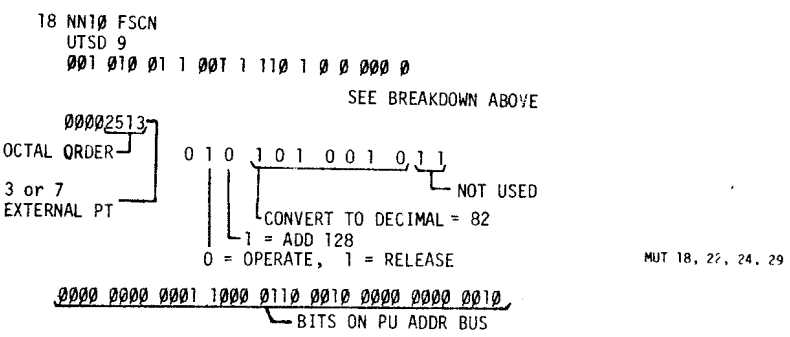
1. Logging all failures to identify patterns early.
2. Use "MN02 MISC" messages on mtce TTY to identify trunks associated with transient FCG failures.

FSCN INT



FSCN failures indicate that the signal distributor either failed to see a MLR (magnetic latching relay) operate or release.

FSCN EXT



FSCN SSD

```
Ø5 NN1Ø FSCN
   SSD ØØ6
   Ø11 Ø11 Ø1 Ø ØØØ 1 11Ø 1 Ø Ø 1Ø1 Ø
                                  SEE BREAKDOWN ABOVE

   ØØØØØ22Ø
OCTAL ORDER        0 0 0  0 1 0  0 1 0  0 0 0
                   |   |   |     |     |     |
        0 = OPERATE|   |   |     |     |     |FIELD
        1 = RELEASE    |   |     |ROW
                       |   |QUADRANT
                       |HALF
```

CMT 24, 26

```
   ØØØØ ØØØØ ØØØ1 ØØØ1 Ø1Ø1 ØØØØ Ø1ØØ ØØØØ Ø1ØØ
                                  |BITS ON PU ADDR BUS
```

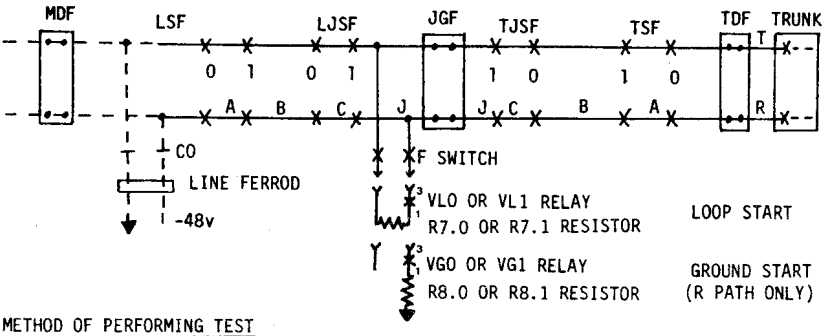
RVFY

```
26 NN1Ø RVFY
   LJSW Ø21
   111 1Ø1 1Ø 1 ØØØ Ø 1ØØ 1 Ø Ø ØØØ 1
                          BREAKDOWN ON PREVIOUS PAGE

   26Ø35617
   |||||||STG 1 LV
   ||||||STG 1 SW
   |||||STG 0 LV
   ||||STG 0 SW
   |||GRID
   ||N/A
   |ORDER

   1ØØØ 1Ø1Ø 1Ø1Ø ØØ1Ø Ø11Ø 1ØØØ ØØ1Ø ØØ1Ø Ø1ØØ
                                  |BITS ON PU ADDR BUS
```

```
26 NT1Ø L&J RVFY   Ø2 226 ØØ1   571-1747   XØ5   Ø2 13 17
                   LEN                    MLHG  TERM #   JNN
                                                or MJ
```



METHOD OF PERFORMING TEST

When an ESS line disconnects, a test is made to verify that the line equipment restores properly and thus will be able to detect a new origination. To perform the test, a resistance loop or ground is connected from the junctor switch frame to the line ferrod. This resistance simulates an origination and the line ferrod is scanned to see if it is saturated. Failure to saturate the line ferrod results in the error printout.

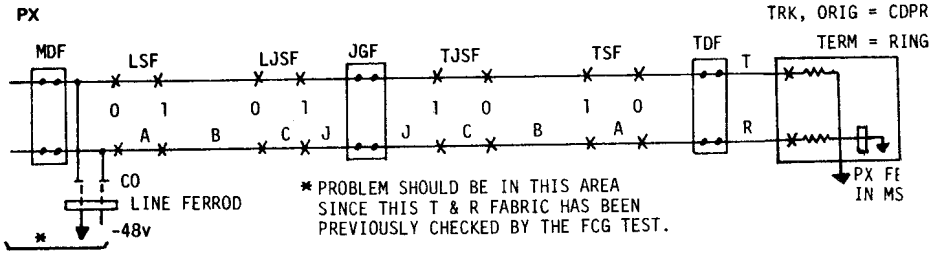
POSSIBLE CAUSES OF TROUBLE

1. Defective cutoff switch not closing through to line ferrod.
2. Translations incorrect or line ferrod wiring incorrect.
3. Tip ground from a blown coil on MDF or T-T cross.
4. Open "F" switch contacts or troubles in the restore verify circuit.

MEANS OF REDUCING FAILURES

1. Check ALIT printout every morning to pick up failures from previous night's automatic line insulation tests.
2. Periodically check the RVFY printouts for failure patterns to one particular JSF.

PX



CONTINUOUSLY CLOSED CROSSPOINT ON THE RING SIDE OF THE LINE.

METHOD OF PERFORMING TEST

Prior to applying either dial tone or ringing current to a line, a power cross test is made. This test looks for the presence of a positive foreign potential in excess of 50 volts.

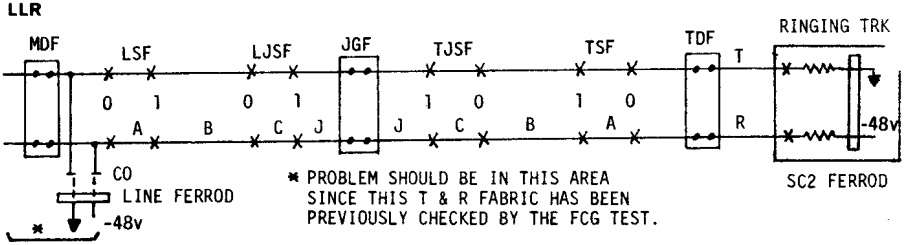
POSSIBLE CAUSES OF TROUBLE

1. Crosses with power lines.
2. CDPR trunk low sensitivity.
3. Positive DC on subscriber line.
4. Incorrect use of cable breakdown set.

MEANS OF REDUCING FAILURES

1. Adherence to standard practices when using breakdown sets.
2. Investigating each PX that is received.

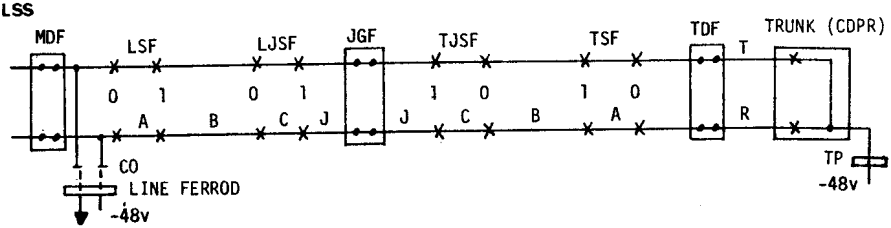
LLR



PRIOR TO RINGING THE CALLED SUBSCRIBER, A PRE-TRIP TEST IS MADE TO INSURE THAT A FALSE TRIP OF RINGING WILL NOT OCCUR CAUSING A FALSE AMA OR COIN CHARGE TO BE MADE AGAINST THE ORIGINATING CUSTOMER.

TIP AND RING REVERSAL IN THE PATH WILL CAUSE AN LLR.
LOW T-R RESISTANCE IN CALLED SUBSCRIBER LINE OR RINGING TRUNK CIRCUIT.

LSS



TIP PARTY HAS 1000Ω GROUND (OFF HOOK)
RING PARTY HAS NONE.
THIS CAN BE TESTED VIA LTTP OR STATION RINGER TEST CODE.

TWO PARTY TESTS ARE MADE ON ORIGINATING SUBSCRIBER LINE - ONE IS MADE PRIOR TO DIAL TONE (PT1) AND ANOTHER IS MADE AFTER ALL DIGITS ARE DIALED (PT2).

IF ONE TEST SHOWS RING PARTY AND SECOND TEST SHOWS TIP PARTY OR VICE VERSA, A LINE SECURITY SCAN FAILURE EXISTS. THE POSSIBILITY OF CHARGING THE WRONG CUSTOMER CAN OCCUR.

SECTION 8

JUNCTOR (J) FRAME

(J1A031D)

CONTENTS

JUNCTOR SCANNER, UNIT TYPE 17
SD-1A214
CD-1A214
PK-1A027 SCANNER RAW DATA DOC
TLM-1A214
ED-1A170-16

AND

JUNCTOR SIGNAL DISTRIBUTOR (JSD), UNIT TYPE 18
SD-1A216
CD-1A216
TLM-1A216
ED-1A170-16

SUPPORTING DOCUMENTATION
TLM-1A110 JUNCTOR
SD-1A119 COMMUNICATIONS BUS CKT
SD-1A129 MISCELLANEOUS CKT
BSP 231-049-315 JUNCTOR REDISTRIBUTION-RECENT CHANGE AND VERIFICATION
TOP 231-051-001

F, S, AND T POINT LAYOUT - JUNCTOR SCANNER

	CONTROLLER SCAN POINTS			
	F	S	T	CONDITION
0	0	0	0	POWER ON (OLD)
1	0	0	1	
2	0	1	0	
3	0	1	1	POWER ON (NEW)
4	1	0	0	
5	1	0	1	
6	1	1	0	
7	1	1	1	POWER OFF

OCTAL ORDER LAYOUT - JUNCTOR SCANNER

22 10	9 7	6 4	3 0
	MST SIG ROW	LST SIG ROW	

LAYOUT TO DISPLAY SCAN POINTS AT MASTER CONTROL CENTER

JUNCTOR SCANNER ROW CODE = 010

22 21	20 18	17 15	14 10	9	8 5	4 3	2	1	0
	CODE		FRAME NUMBER	BAY	HMP-1	VF	CKT	PORT	

F, S, AND T POINT LAYOUT - JUNCTOR SIGNAL DISTRIBUTOR

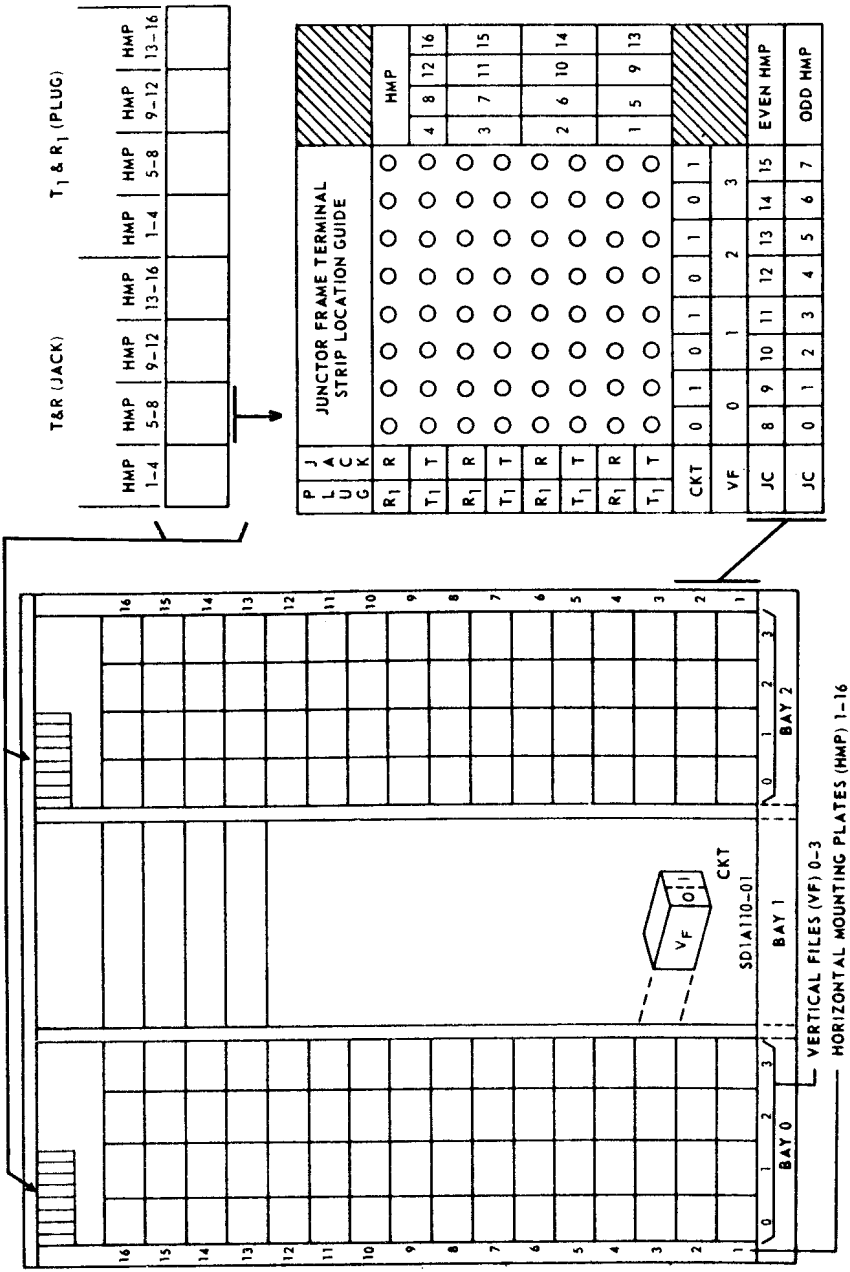
	CONTROLLER SCAN POINTS			
	F	S	T	CONDITION
0	0	0	0	IDLE
1	0	0	1	QUAR
2	0	1	0	
3	0	1	1	TPAQ
4	1	0	0	ENABLED
5	1	0	1	
6	1	1	0	TPA
7	1	1	1	POWER OFF

OCTAL ORDER LAYOUT - JUNCTOR SIGNAL DISTRIBUTOR

22 11	10	9	8 5	4 3	2	1 0
	OPR	BAY	HMP-1	VF	CKT	RELAY

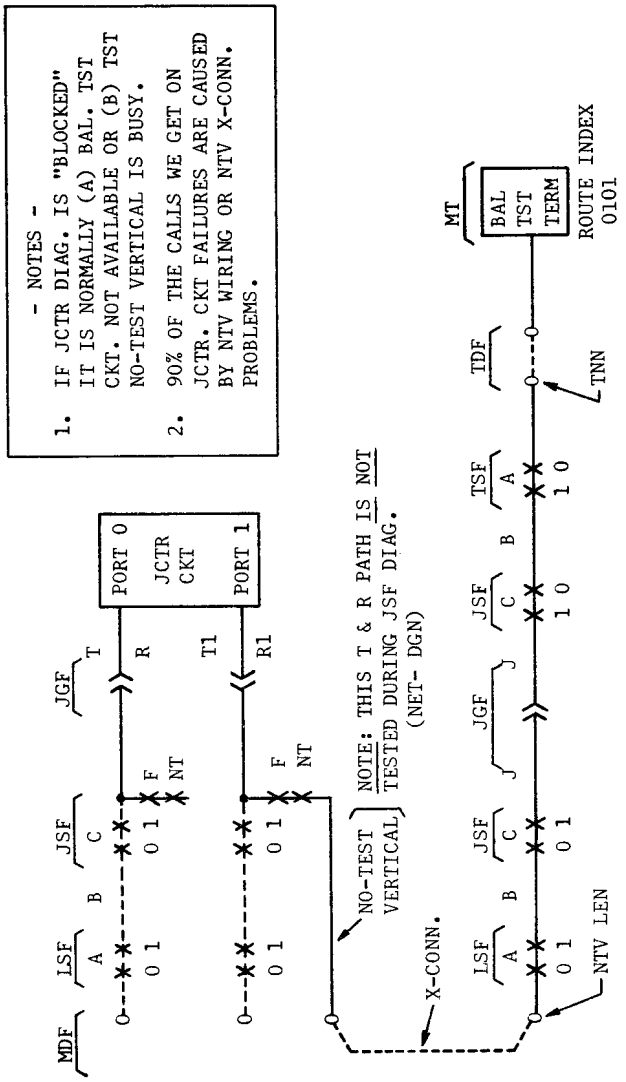
OPR = 0 OPERATE
= 1 RELEASE

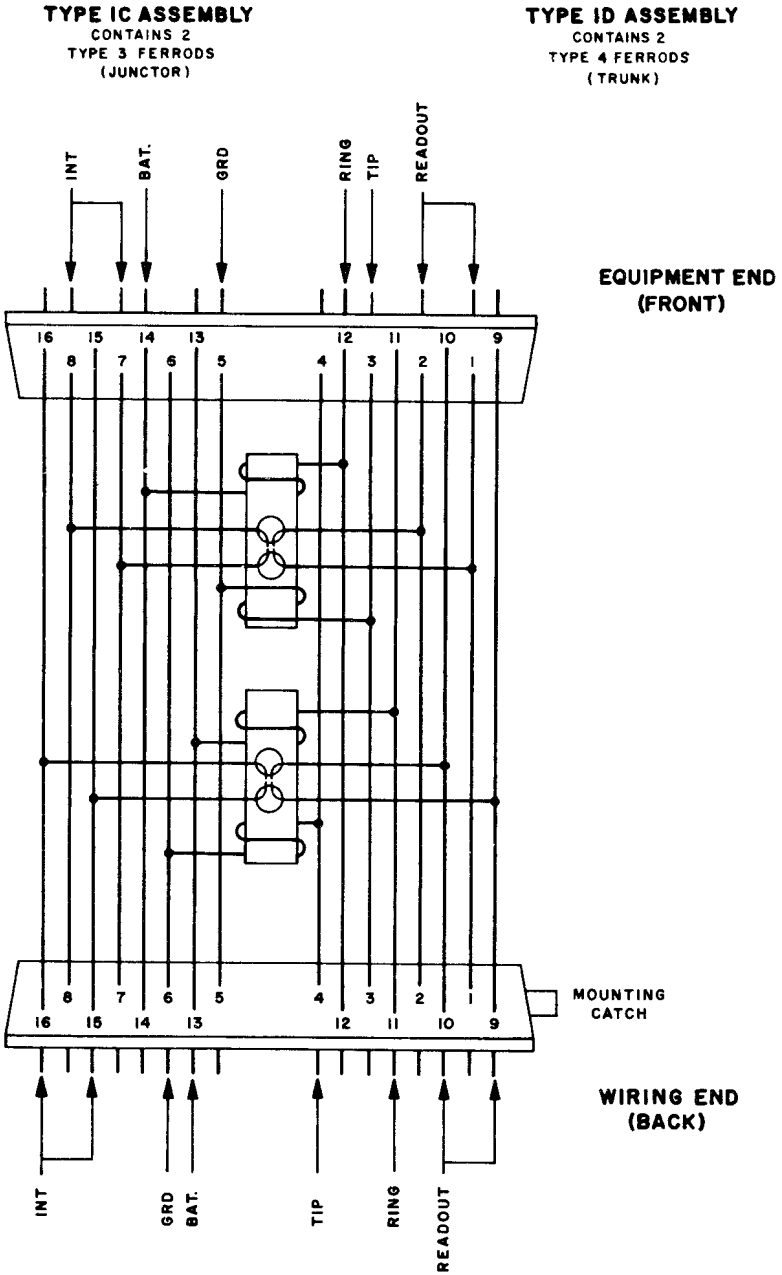
JUNCTOR FRAME TERMINAL STRIP



	SSD - JCT SSD	CMT				MUT			
		IN	OUT			IN	OUT	IN	OUT
	MISC	080-03	080-62	080-63	180-03	080-11	080-12	180-12	180-11
AR	050	201	201			216	216	216	216
ARM	060	001	001			215	215	215	215
BR	051	202	202			214	214	214	214
BRM	061	002	002			213	213	213	213
DR	052	203	203			212	212	212	212
DRM	062	003	003			211	211	211	211
DF	054	205	205			206	206	206	206
DFM	064	005	005			205	205	205	205
AP	053	204	204			208	208	208	208
APM	063	004	004			207	207	207	207
FO	032	206/212			206	204			204
FOM	042	006/012			006	203			203
SO	033	207			207	202			202
SOM	043	007			007	201			201
TO	034	208			208	018			018
TOM	044	008			008	017			017
F1	035	/213			201	016			016
F1M	045	/013			001	015			015
S1	036				202	014			014
S1M	046				002	013			013
T1	037				203	012			012
T1M	047				003	011			011
SC003			006			217			
SC013			007						
SC00			206			218			
SC10			207						
	FOR 288 MISC TS		FOR 355A TS				FOR 355A TS		

NETWORK CONNECTION (VIA NO-TEST VERTICAL)
TO BALANCE TERMINATION FOR JUNCTOR CKT. DIAG.





Wiring Arrangements of Type 1C or 1D Ferrod Assembly

USD, JSD POINT NUMBERS

HALF	FIELD	QUADRANT	ROW 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
0	3	0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
		1	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
		2	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
		3	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127
1	3	0	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	147	150	151	152	153	154	155	156	157	158	159
		1	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191
		2	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223
		3	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255

SECTION 9

JUNCTOR GROUPING (JG) FRAME (12-FILE) J1A085A

CONTENTS

SD-1A340
CD-1A340
ED-1A341-10

SUPPORTING DOCUMENTATION

BSP 820-110-151

JGF SWITCH AND LEVEL TO TR CONNECTIONS

SWITCH \ LEVEL	0	1	2	3	4	5	6	7
7	JGF EVEN SHELF 7 PLUG 0	JGF ODD SHELF 7 PLUG 1	JGF EVEN SHELF 7 PLUG 2	JGF ODD SHELF 7 PLUG 3	JGF EVEN SHELF 6 JACK 4	JGF ODD SHELF 6 JACK 5	JGF EVEN SHELF 6 JACK 6	JGF ODD SHELF 6 JACK 7
6	JGF EVEN SHELF 6 PLUG 0	JGF ODD SHELF 6 PLUG 1	JGF EVEN SHELF 6 PLUG 2	JGF ODD SHELF 6 PLUG 3	JGF EVEN SHELF 7 JACK 4	JGF ODD SHELF 7 JACK 5	JGF EVEN SHELF 7 JACK 6	JGF ODD SHELF 7 JACK 7
5	JGF EVEN SHELF 5 PLUG 0	JGF ODD SHELF 5 PLUG 1	JGF EVEN SHELF 5 PLUG 2	JGF ODD SHELF 5 PLUG 3	JGF EVEN SHELF 4 JACK 4	JGF ODD SHELF 4 JACK 5	JGF EVEN SHELF 4 JACK 6	JGF ODD SHELF 4 JACK 7
4	JGF EVEN SHELF 4 PLUG 0	JGF ODD SHELF 4 PLUG 1	JGF EVEN SHELF 4 PLUG 2	JGF ODD SHELF 4 PLUG 3	JGF EVEN SHELF 5 JACK 4	JGF ODD SHELF 5 JACK 5	JGF EVEN SHELF 5 JACK 6	JGF ODD SHELF 5 JACK 7
3	JGF EVEN SHELF 3 PLUG 0	JGF ODD SHELF 3 PLUG 1	JGF EVEN SHELF 3 PLUG 2	JGF ODD SHELF 3 PLUG 3	JGF EVEN SHELF 2 JACK 4	JGF ODD SHELF 2 JACK 5	JGF EVEN SHELF 2 JACK 6	JGF ODD SHELF 2 JACK 7
2	JGF EVEN SHELF 2 PLUG 0	JGF ODD SHELF 2 PLUG 1	JGF EVEN SHELF 2 PLUG 2	JGF ODD SHELF 2 PLUG 3	JGF EVEN SHELF 3 JACK 4	JGF ODD SHELF 3 JACK 5	JGF EVEN SHELF 3 JACK 6	JGF ODD SHELF 3 JACK 7
1	JGF EVEN SHELF 1 PLUG 0	JGF ODD SHELF 1 PLUG 1	JGF EVEN SHELF 1 PLUG 2	JGF ODD SHELF 1 PLUG 3	JGF EVEN SHELF 0 JACK 4	JGF ODD SHELF 0 JACK 5	JGF EVEN SHELF 0 JACK 6	JGF ODD SHELF 0 JACK 7
0	JGF EVEN SHELF 0 PLUG 0	JGF ODD SHELF 0 PLUG 1	JGF EVEN SHELF 0 PLUG 2	JGF ODD SHELF 0 PLUG 3	JGF EVEN SHELF 1 JACK 4	JGF ODD SHELF 1 JACK 5	JGF EVEN SHELF 1 JACK 6	JGF ODD SHELF 1 JACK 7

JNN= 00 0 0 0 0

- LEVEL, SWITCH — SEE CHART TO DETERMINE ODD/EVEN-SHELF-PLUG/JACK
- GRID, FRAME — SEE PLUG/JACK CHART TO DETERMINE TERMINAL
- NETWORK — DETERMINE VF LOCATION AT JGF

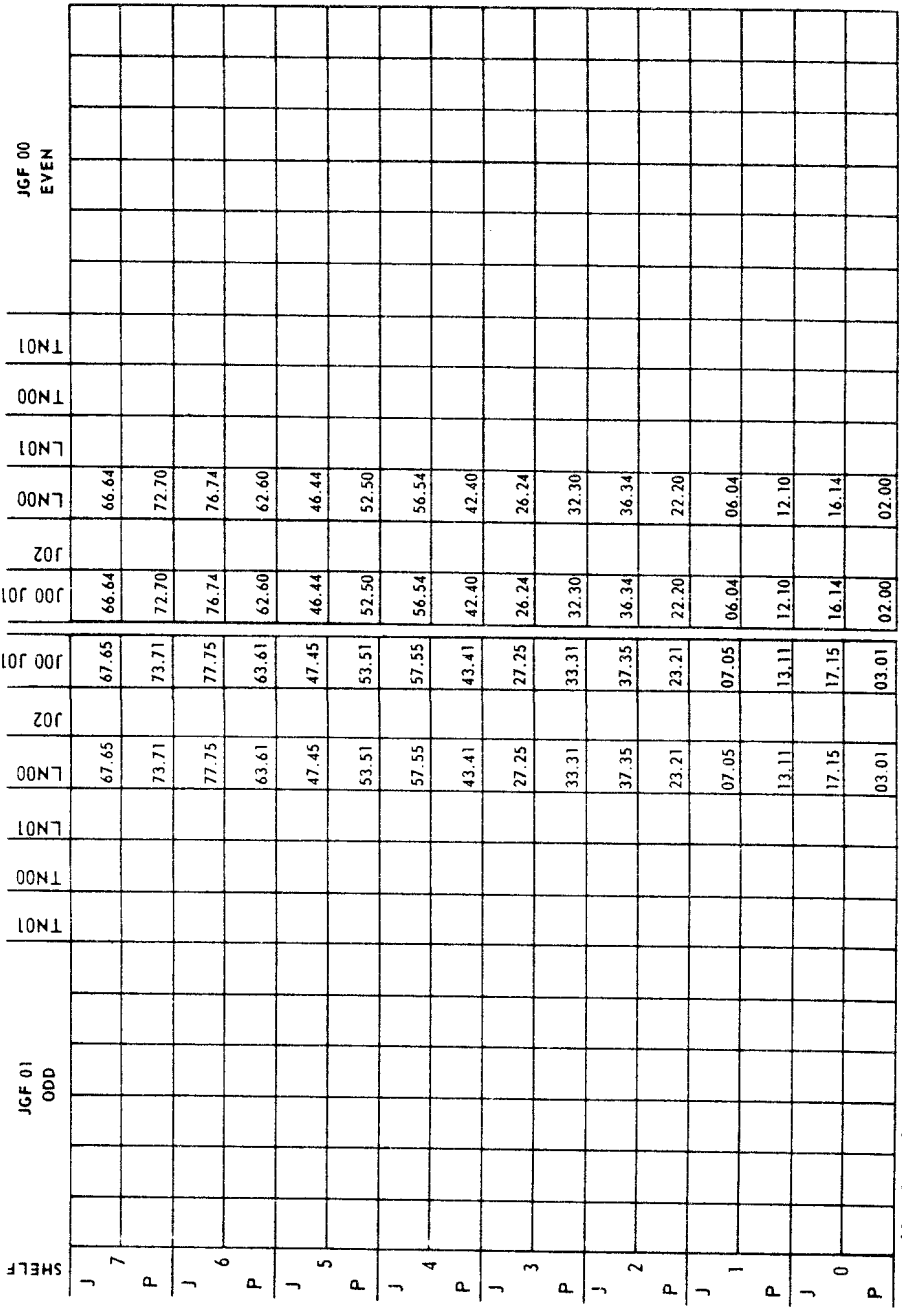
JSF	GRID	SHELF 0 1	2 3	4 5	6 7
3	3	00	10	20	30
	2	33	03	13	23
	1	32	02	12	22
	0	31	01	11	21
2	3	30	00	10	20
	2	23	33	03	13
	1	22	32	02	12
	0	21	31	01	11
1	3	20	30	00	10
	2	13	23	33	03
	1	12	22	32	02
	0	11	21	31	01
0	3	10	20	30	00
	2	03	13	23	33
	1	02	12	22	32
	0	01	11	21	31

PLUG TERMINAL STRIP

JSF	GRID	
3	3	33
	2	32
	1	31
	0	30
2	3	23
	2	22
	1	21
	0	20
1	3	13
	2	12
	1	11
	0	10
0	3	03
	2	02
	1	01
	0	00

JACK CONNECTOR

JG FRAME, J1A085A
REAR VIEW



SECTION 10

TRUNK PANELS (TRK PNLS)

CONTENTS

TLTP
TRUNK AND LINE TEST
J1A042A&B

UNIT TYPE 8 (MEMBER NUMBER = 0)

SD-1A132
CD-1A132
ED-J1A042

TLTP
TRUNK AND LINE TEST
J6A001A

UNIT TYPE 8 (MEMBER NUMBER = 0)

SD-6A005
CD-6A005
ED-J6A001-A

STTP
SUPPLEMENTARY TRUNK TEST
J1A042C

UNIT TYPE 8 (MEMBER NUMBER >0)

SD-1A256
CD-1A256
ED-1A042C

MTTP
MANUAL TRUNK TEST POSITION
J1A042F

UNIT TYPE 8 (Member Number >0)

SD-1A418
CD-1A418
ED-1A042

SUPPORTING DOCUMENTATION
BSP 820-502-150

TLTP, STT, OR MTTP* TESTING ORDER FORMAT

LAMP INDICATIONS

EQUIPMENT STATE

Steady - TNN is idle
60 IPM - Locked out
120 IPM - Disabled

REG LAMP
Steady - Traffic idle
60 IPM - Traffic busy

PROGRESS AND ERROR

5 second steady - Success
60 IPM - System failure
120 IPM - Translation or human error

* Status lamps indicate status of TNN

TEST CODES XX

First Digit		Second Digit
0	No substitute trunk	Normal automatic trunk prog. TST
1	Use substitute trunk	Permanent busy TST
2	Repeat test 32 times	Synchronous TST
3	Repeat with sub. trunk	Non-synchronous TST
4	Raw data print	Not used
5	Raw data with sub. trunk	Continuity and polarity TST
6	Raw data - repeat	Same as "0" but remove all failing trunks from service on a T.G. DGN
7	Raw - repeat with sub. trunk	

TRUNK TESTING

PRIOR TO 1E6, 1AE6

DIAGNOSE A TNN

Keys: TRK, TST, OP
TT Dial: TNN, XX, START

DIAGNOSE A TRK GRP

Keys: TRK, TST
TT Dial: TGN, XX, START

1E6, 1AE6 AND LATER OR MTTP

DIAGNOSE A TNN

Keys: TRUNK/TNN, TST
TT Dial: TNN, *, XX, #

DIAGNOSE A TRK GRP

Keys: TST
TT Dial: TGN, *, XX, #

OPERATION OF CPD POINTS

TNN ON ACCESS TRUNK (1 - 3)

PRIOR TO 1E6, 1AE6

Keys: TST, OP
TT Dial: A, B, C, D, START

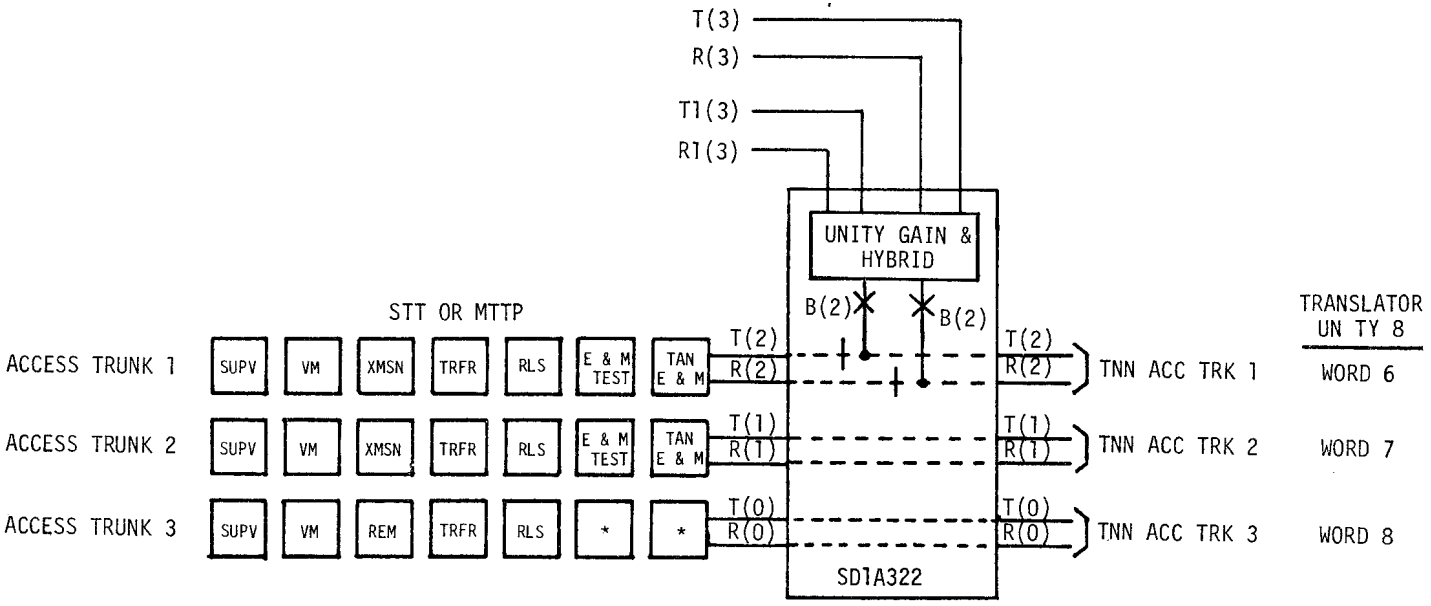
1E6, 1AE6 AND LATER

Keys: TST, TRK/TNN
TT Dial: *, A, B, C, D, #

CPD POINT	RELAY	(A) ACCESS TRUNK	(B) GROUP	(C) CKT SD PT	(D) OP/REL
0	A	1 - 3	9	0	0 - 9
1	B	1 - 3	9	1	0 - 9
2	C	1 - 3	9	2	0 - 9
3	D	1 - 3	9	3	0 - 9
4	E	1 - 3	9	4	0 - 9
5	F	1 - 3	9	5	0 - 9
6	G	1 - 3	9	6	0 - 9
7	H	1 - 3	9	7	0 - 9
8	J	1 - 3	9	8	0 - 9
9	K	1 - 3	9	9	0 - 9
10	L	1 - 3	8	0	0 - 9
11	M	1 - 3	8	1	0 - 9
12	N	1 - 3	8	2	0 - 9
13	O	1 - 3	8	3	0 - 9
14	P	1 - 3	8	4	0 - 9
15	Q	1 - 3	8	5	0 - 9

OP/REL	
0	CPD POINT RESET
1	CPD POINT SET
2	
3	
4	RELAY RELEASE (COMMON)
5	RELAY OPERATE (COMMON)
6	RELAY RELEASE (INT APPL)
7	RELAY OPERATE (INT APPL)
8	RELAY RELEASE (INDIVIDUAL)
9	RELAY OPERATE (INDIVIDUAL)

REFERENCE: HB 275 SECT 520 AND 523
BSP 231-130-301
TOP 231-050-006 (1E6/1AE6)
TOP 231-050-007 (MTTP, 1E7/1AE7)
TOP 231-050-008 (STTP, 1E7/1AE7)
TOP 231-050-009 (TLTP, 1E7/1AE7)



ASSOCIATION OF STT/MTTP ACCESS TRUNK NUMBER TO SD1A322-01 PORT (2-WIRE ONLY) AND TNN CONTAINED IN WORDS 6, 7, AND 8 OF UNIT TYPE 8 TRANSLATION (SECT 30, PA 591003) NO. 1 ESS (SECT 256, PA6A002) NO. 1A ESS.

REPEATEDLY OPERATE RELAY OR CPD POINT ON TRUNKS HELD ON ACCESS TRUNKS

BASIC FOUR DIGIT CODES

0100	SIEZE POB
03ab	TIME DELAY a = Quantity of 250 msec delays b = Quantity of 25 msec delays (0-9)
0600	IGNORE RELAY FAILURES
0200	ACTIVATE POB
0500	TERMINATE TEST (Zero the POB)

EXAMPLE OF REPEATEDLY OPERATING THE A, B, AND C RELAYS OF A TNN ON ACCESS 1

0100	SIEZE POB
0600	IGNORE RELAY FAILURES
1909	OPERATE A RELAY
0302	DELAY 50 msec
1919	OPERATE B RELAY
0320	DELAY 500 msec
1929	OPERATE C RELAY
0310	DELAY 250 msec
1908	RELEASE A RELAY
0310	DELAY 250 msec
1918	RELEASE B RELAY
0310	DELAY 250 msec
1928	RELEASE C RELAY
0310	DELAY 250 msec
0200	ACTIVATE POB

PROCEDURE

(1E5, 1AE5 AND EARLIER)

1. BRING TRUNK UP ON ACCESS
2. OPERATE "TEST", "OP"
3. DIAL FOUR DIGITS, THEN "ST" FOR EACH STEP
4. TO TERMINATE TEST, DIAL 0500, "ST"

(1E6, 1AE6 AND LATER OR MTTP)

1. BRING TRUNK UP ON ACCESS
2. OPERATE "TEST"
3. RELEASE "TRUNK/TNN" AND "OP"
4. DIAL *, FOUR DIGITS AND "ST/#" FOR EACH STEP
5. TO TERMINATE TEST, DIAL 0500, "ST/#"

RINGING & TONE PLANT
LEAD FUNCTIONS

LEAD	ESS DESIG	FUNCTION
AR1		AUDIBLE RINGING TONE
AR2		" " "
AR3		" " "
AR30		PRECEDENCE AUD RING TONE, 30 IPM
BT1	BT	BUSY TONE, CONTINUOUS
BT3	BT60	BUSY TONE, 60 IPM
BT4	BT120	BUSY TONE, 120 IPM
HT1	HT	HIGH TONE, CONTINUOUS
HT2	HT120	HIGH TONE, 120 IPM
HT3	HT60	HIGH TONE, 60 IPM
MT1		CALL WAITING TONE
MT2		BUSY VERIFICATION TONE
PT		PREEMPT TONE
ROH		RECEIVER OFF HOOK, PERMANENT SIG
SAR1		SIMULATED AUDIBLE RINGING
SAR2		" " "
SAR3		" " "
TT		DIAL TONE

REFERENCES - J87801A 812A RINGING & TONE
J86834A 808A RINGING & TONE
SD81737 812A
SD1A218 TONE OR REC ANN CKT

Section 11

TRUNKS AND SERVICE

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Schematic Drawing Number	Page
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TRUNK AND SERVICE CIRCUIT SCHEMATIC DRAWING INDEX

SD NBR	CODE	J DRAWING		TITLE
03501-01	035	NJ-035AA-1		CUSTOM CALLING FEATURE DEMONSTRATION
1A121-02	NONE	J1A041BB-1		DS (105A Data Set Unit Assoc With MCCTTY-1
1A130-01	100	J1A033FB-1		INT APLQ
1A133-01	106	J1A033FD-1		MA SCAN APLQ
1A141-01	050	J1A033FK-1		LIT CKT
1A142-01	095	J1A046A-1		SRV OBS CKT
1A146-01	102	J1A033FH-1		SIG DISTR APLQ
1A147-01	NONE	J1A041BB-1		DS (105A Data Set Unit Assoc With MCCTTY-1
1A147-01	NONE	J1A041BA-1	MD	MTTY (Transmit & Receive Unit
1A147-01	NONE	J1A041BB-1	MD	DS (105A DATA SET UNIT)
1A147-02	NONE	J1A041BD-1		UNIV INPUT/OUTPUT TRANS & RECV UNIT (UTTY)
1A150-01	052	J1A033FL-2		MF TST ENV
1A152-01	054	J1A033FG-2		T PRES DET
1A153-01	055	J1A033FE-1		TST CHT RING AND CC
1A155-01	057	J1A033FM-2		DP RCVR TST
1A157-01	058	J1A033FS-1		STA RNGR TST
1A157-01	077	J1A033FS-1		TT STA/RNGR TST COMB W/O AUTOMATIC SPEED CHECKING OF TT DIALERS
1A157-01	077	J1A033GT-1		TT STA RNGR TST COMB WITH AUTOMATIC SPEED CHECKING OF TT DIALERS
1A157-01	077	J1A033FS-1		TT STA RNGR TST COMB WITH AUTOMATIC SPEED CHECKING OF TT DIALERS
1A160-01	103	J1A033FA-1		AUX L
1A163-01	016	J1A033CA-1	MD	2-WAY TRK DP (INCOMING BY-LINK)
1A163-01	049	J1A033CA-1	MD	2-WAY TRK DP
1A163-02	016	J1A033CA-2		TWO-WAY TRK DP (INCOMING BY-LINK)
1A163-02	049	J1A033CA-2		DP
1A163-05	016	J1A088CA-1		TWO WAY TRK DP PULSING (INCOMING BY-LINE)
1A163-05	049	J1A088CA-1		TWO WAY TRK DP
1A165-01	002	J1A032BB-1	MD	OGT LOC TDM
1A165-02	002	J1A032BB-2		OGT LOC TDM
1A165-05	002	J1A084BB-1		Outgoing Trunk Local and Tandem
1A166-01	004	J1A032AB-1	MD	INC TRK LOC TDM
1A166-02	004	J1A032AB-2		INC TRK LOC TDM
1A166-02	178	J1A032AB-2		INC TRK LOC TDM

SD NBR	CODE	J DRAWING		TITLE
1A166-05	004	J1A084AB-1		Incoming Trunk Local and Tandem
1A166-05	161	J1A084AB-1		INCOMING TRUNK LOCAL AND TANDEM
1A166-05	179	J1A084AB-1		INCOMING TRUNK LOCAL AND TANDEM
1A168-01	061	J1A033DB-2		RING 1 & 2 PTY
1A168-05	061	J1A088DB-1		RINGING CIRCUIT FOR INDIVIDUAL AND 2 PARTY
1A169-01	008	J1A033BA-1		OGT 3CL SWBD
1A169-05	008	J1A088BA-1		OGT TRK TO SWBD 3CL
1A172-01	027	J1A033DC-1		TL CUT THRU FOR LOCAL OFFICE ORIGINATING
1A172-01	063	J1A033DC-1		CUST DP RCVR
1A172-01	064	J1A033DC-1		TT CALL DET AND CUST DP RCVR
1A172-05	063	J1A088DC-1		CUSTOMER DIAL PULSE RECEIVER
1A172-05	064	J1A088DC-1		TOUCH-TONE CALLING RECEIVER/CUSTOMER DIAL PULSE RECEIVER
1A173-01	027	J1A033DD-2		TL CUT THRU FOR LOCAL OFFICE ORIGINATING
1A173-01	028	J1A033DD-2		TL CUT THRU SERVICE FOR DISTANT OFFICE ORIGINATING
1A173-01	029	J1A033DD-2		TT & INC TIE TRK COMBINATION
1A173-01	064	J1A033DD-2		TT CALL DET AND CUST DP RCVR
1A173-01	157	J1A033DD-2		TOUCH-TONE DP RECEIVER HILO 4W SWITCHING
1A175-01	019	J1A033DF-2		MF XTMR/SO COMBINATION
1A175-01	066	J1A033DF-2		MF XMTR
1A176-01	067	J1A032BC-3		NET ACS
1A176-01	067	J1A032BC-2	MD	NET ACS
1A176-05	067	J1A084BC-1		Network Access
1A177-01	009	J1A033BB-2		OTG VERIF REQ & INCPT
1A177-05	009	J1A088BB-1		VERIFICATION REQUEST AND INTERCEPT
1A178-01	028	J1A033DH-1		TL CUT THRU SERVICE FOR DISTANT OFFICE ORIGINATING
1A178-01	029	J1A033DH-1		TT & INC TIE TRK COMBINATION
1A178-01	068	J1A033DH-1		TRK DP RCVR
1A179-01	027	J1A033DL-1		TL CUT THRU FOR LOCAL OFFICE ORIGINATING
1A179-01	028	J1A033DL-1		TL CUT THRU SERVICE FOR DISTANT OFFICE ORIGINATING
1A179-01	069	J1A033DL-1		TRK DP XMTR
1A180-01	070	J1A033DM-1		RP REC
1A181-01	071	J1A033DN-1		RP XMTR

SD NBR	CODE	J DRAWING		TITLE
1A184-01	017	J1A032AD-3		INC TRK 3W
1A184-01	017	J1A032AD-2	MD	INC TRK 3W
1A184-05	017	J1A084AD-1		Incoming Trunk 3rd Wire Coin Control
1A186-01	018	J1A033AA-1		INC TRK LTD NO.14 OR NO. 3
1A187-01	011	J1A032BD-2		OGT LTD
1A187-01	011	J1A032BD-1	MD	OGT LTD
1A187-05	011	J1A084BD-1		Outgoing Trunk to Test Desk #14
1A188-01	072	J1A033DK-2		RING TRK
1A190-01	012	J1A032BE-3		OGT RSD NO. 2
1A190-05	012	J1A084BE-1		Outgoing Trunk to Repair Service Desk #2
1A190-31	012	J1A032BE-2	MD	OGT RSD No. 2
1A192-01	013	J1A032CB-1	MD	TWO-WAY TRK
1A192-02	013	J1A032CB-2		TWO-WAY TRK
1A192-05	013	J1A084CB-1		Two Way Trunk for Swbd No. 3CL
1A193-01	074	J1A032DB-3		IAO TRK
1A193-01	074	J1A032DB-2	MD	1AO TRK
1A193-05	074	J1A084DB-1		Intraoffice Trunk
1A195-01	075	J1A033DP-1		PCI TRMTR
1A196-01	076	J1A033DS-1		PCI XMTR TST
1A199-01	077	J1A033FR-1		TT STA/RNGR TST COMB W/O AUTOMATIC SPEED CHECKING OF TT DIALERS
1A199-01	077	J1A033FR-1		TT STA RNGR TST COMB WITH AUTOMATIC SPEED CHECKING OF TT DIALERS
1A203-01	015	J1A032BF-2		OGT TO XBAR TDM OR TSPS NO. 1
1A203-01	015	J1A032BF-1	MD	OGT TO XBAR TDM
1A203-05	015	J1A084BF-1		Outgoing Trunk to XBAR Tandem or TSPS No. 1
1A210-01	104	J1A033GA-1		REM MA SCAN APLQ
1A211-01	062	J1A033DR-1		COIN CONTROL

SD NBR	CODE	J DRAWING		TITLE
1A218-01	078	J1A032DC-2		TONE OR ANN
1A218-01	078	J1A032DC-1	MD	TONE OR ANN
1A218-05	078	J1A084DC-1		Tone or Recorded Ancmt
1A220-01	003	J1A033AB-2		INC TRK SXS
1A220-01	003	J1A033AB-1	MD	INC TRK SxS
1A220-05	003	J1A088AB-1		INC TRK FROM SXS /REV BATTERY SUPERVISION
1A221-01	079	J1A033DT-3		ANN
1A221-01	079	J1A033DT-1	MD	AUD R & REC ANN
1A221-05	079	J1A088DT-1		AUDIBLE RING AND RECORDED ANCMT
1A222-01	080	J1A033DU-1		PS-PARTIAL D HOLD
1A222-05	080	J1A088DU-1		PERMANENT SIGNAL PARTIAL DIAL HOLDING
1A223-01	006	J1A033BE-1		OGT TO 3C OR 3CL SWBD
1A223-05	006	J1A088BE-1		OGT TRK TO SWBD 3C OR 3CL
1A224-01	005	J1A033AC-1		INC TRK FROM SWBD 3C OR 3CL
1A224-05	005	J1A088AC-1		INK TRK FROM SWBD 3C OR 3CL
1A225-01	081	J1A033FW-1		COMB MW & LP AROUND TST
1A226-01	082	J1A033FT-1		CONT-POL TEST
1A227-01	083	J1A033FU-1		TRMSN TST TERM
1A228-01	099	J1A033FV-1		REM SIG DIST APLQ
1A231-01	098	J1A033FY-1		GRD CROSS DET
1A234-01	097	J1A033FF-1		PS MON LO
1A235-01	096	J1A033FN-1		CS MON LO
1A236-01	021	J1A033CB-1	MD	TWO-WAY TRK MF 4W
1A236-02	021	J1A033CB-2		TWO WAY TRK MF PULSING
1A236-05	021	J1A088CB-1		TWO WAY TRUNK MF PULSING
1A237-01	022	J1A033CC-1	MD	TWP-WAY TRK DP-4W TERM
1A237-01	022	J1A033CC-2	MD	2-WAY
1A237-01	048	J1A033CC-2	MD	2-WAY TRK DP 4W TERM
1A237-02	022	J1A033CC-3		TWO WAY TRUNK DP
1A237-02	048	J1A033CC-3		TWO-WAY TRK DP (INCOMING BY-LINK)
1A237-05	022	J1A088CC-1		TWO WAY TRUNK DP
1A237-05	048	J1A088CC-1		TWO WAY TRUNK DP (INCOMING BY-LINK)

SD NBR	CODE	J DRAWING		TITLE
1A238-01	023	J1A033CD-1	MD	TWO-WAY TRK
1A239-01	035	J1A033JD-1		DP RPTR
1A239-05	035	J1A088JD-1		DP REPEATER WITH PULSE CORRECTION
1A240-01	030	J1A033CK-1		LONG HAUL FX TRK
1A241-01	031	J1A033CF-1		FX TRK
1A241-01	159	J1A033CF-1		SHORT HAUL FX TRUNK WITH CITY OF ORIGIN APPLIQUE
1A244-01	042	J1A033DY-1	MD	ATND LP
1A245-01	040	J1A033JA-1		ATTND TRK 2-WIRE
1A245-05	040	J1A088JA-1		ATTENDANT TRUNK: 2-WIRE
1A246-01	065	J1A033DW-1		MF RCVR
1A248-01	041	J1A033JB-1		ATND TRK 4-WIRE
1A248-05	041	J1A088JB-1		ATTENDANT TRUNK: 4-WIRE
1A249-01	043	J1A033JC-1	MD	3 PORT CONF
1A250-01	044	J1A033JE-2		6 PORT CONF
1A252-01	007	J1A032CC-2		TWO-WAY MF
1A252-01	007	J1A032CC-1	MD	TWO-WAY MF
1A252-05	007	J1A084CC-1		Two Way Trunk MF Pulsing
1A254-01	010	J1A033BG-1		OGT CZ DIALING
1A255-01	014	J1A033BF-1		OGT LOC CN OVT-STK C
1A261-01	108	J1A033GB-1		P MS MON LO
1A262-01	199	J1A033GD-1	MD	TR DATA TRMTR
1A263-01	053	J1A033GC-1		TT DETR TST
1A264-01	024	J1A033CG-1		TWO-WAY TRK
1A266-01	025	J1A032AE-1	MD	INC TRK LOC TDM-DEL DIAL
1A266-02	025	J1A032AE-2		INC TRK LOC TDMDEL DIAL
1A266-02	051	J1A032AE-2		INC TRK LOC TDMDEL DIAL
1A266-05	025	J1A084AE-1		Incoming Trunk W/Delayed Dial
1A266-05	051	J1A084AE-1		Incoming Trunk W/Delayed Dial
1A283-01	042	J1A033JF-1		ATND LOOP WITH AUTONOMOUS TERMINATION
1A283-05	042	J1A088JF-1		ATTENDANT LOOP TRUNK WITH AUTONOMOUS TERM
1A284-01	043	J1A033JG-1		3-PORT CONF WITH AUTONOMOUS TERMINATION
1A284-05	043	J1A088JG-1		3 PORT CONFERENCE WITH AUTONOMOUS TERM.
1A287-01	026	J1A033CH-1		TWO-WAY TRK DP FOR PREEMPT DETECTION

SD NBR	CODE	J DRAWING	TITLE
1A295-01	059	J1A033JH-1	COIN CONTROL
1A297-01	056	J1A033GJ-1	SPL L APLQ
1A300-01	027	J1A033JJ-1	TL CUT THRU FOR LOCAL OFFICE ORIGINATING
1A300-01	028	J1A033JJ-1	TL CUT THRU SERVICE FOR DISTANT OFFICE ORIGINATING
1A300-01	090	J1A033JJ-1	TL CUT THRU
1A302-01	NONE	J1A033CJ-1	DATA LINK CIRCUIT
1A303-01	033	J1A033JK-1	TEST COUPLER CIRCUIT
1A310-01	032	J1A033GS-1	COMBINED MILLIWATT AND BALANCE TERMINATION TEST CIRCUIT
1A311-01	045	J1A033AD-1	CAMA INC TRK SXS
1A311-05	045	J1A088AD-1	CAMA INC FROM SXS
1A312-01	046	J1A032AF-1	CAMA INC TRK MF MF PULSING
1A312-05	046	J1A084AF-1	Incoming Trunk MF Pulsing
1A313-01	034	J1A033BH-1	CAMA OGT TRK TO CAMA,POS 3C OR 3CL SWBD
1A315-01	047	J1A033BJ-1	CAMA: OGT TO CAMA POS. In REMOTE LOC -LOOP SIGNALING
1A316-01	036	J1A033BK-1	CAMA: OGT TO CAMA POS. IN REMOTE LOCATION
1A317-01	NONE	J1A033JM-1	CALL WAITING & CAMA SUSPENSION SIGNALING UNIT
1A318-01	NONE	J1A033JN-1	CALL WAITING CAMA SUSPENSION SIGNALING UNIT
1A319-01	039	J1A033CL-1	LINE ACCESS TRUNK
1A319-05	039	J1A088CL-1	LINE ACCESS TRUNK
1A321-01	038	J1A033AE-1	INCOMING TRUNK FROM TRAFFIC POSITION SYSTEM NO. 1
1A321-05	038	J1A088AE-1	INC TRK FROM TSPS
1A322-01	107	J1A033JP-1	NETWORK ACCESS AND TERMINAL BALANCE TEST ACCESS
1A331-01	110	J1A033JR-1	ECHO SUPPRESSOR TEST TERMINATION
1A339-01	037	J1A033GV-1	SWITCHING CONTROL CENTER TALK AND MONITOR CIRCUIT
1A342-01	159	J1A033JS-1	SHORT HAUL FX TRUNK WITH CITY OF ORIGIN APPLIQUE
1A342-01	200	J1A033JS-1	City of Origin Applique
1A353-01	201	J1A089AA-1	Attendant Interface
1A358-01	084	J1A033CM-1	Two Way Trunk ACD Service MF Pulsing
1A359-01	085	J1A033CN-1	Two Way Trunk ACD Service DP Pulsing

SD NBR	CODE	J DRAWING		TITLE
1A360-01	158	J1A033CP-1		Foreign Exchange Trunk ACD Service
1A361-01	111	J1A090BA-1	MD	TWO WAY TRUNK HILO 4-Wire Switching
1A361-02	111	J1A090BA-2		Two Way Trunk HILO 4-Wire Switching
1A362-01	112	J1A090BB-1	MD	Two Way Trunk HILO 4-Wire Switching
1A362-02	112	J1A090BB-2		TWO WAY: E&M SURVN
1A364-01	114	J1A090BM-1	MD	DIR ACC TRK HILO 4-W Switching
1A364-02	114	J1A090BM-2		DIR ACC TRK HILO 4-W Switching
1A366-01	116	J1A091BB-1		INC TRK /SXS E&M SUPVN
1A366-02	116	J1A091BB-2		INC TRK/SXS E&M SUPVN
1A367-01	117	J1A090BC-1	MD	INC LOOP REV BAT. SUPVN
1A367-02	117	J1A090BC-2		INC LOOP REV BAT. SUPVN
1A368-01	118	J1A090BD-1	MD	Incoming Trunk HILO 4-Wire Switching
1A368-02	118	J1A090BD-2		Incoming Trunk HILO 4-Wire Switching
1A369-01	119	J1A033NF-1		TOUCH-TONE TRANSMITTER TEST (EPSCS)
1A371-01	121	J1A091BC-1		INC TRK/SXS REV BATTERY
1A373-01	123	J1A090BE-1	MD	Outgoing Trunk HILO 4-Wire Switching
1A373-02	123	J1A090BE-2		Outgoing Trunk HILO 4-Wire Switching
1A374-01	124	J1A090BF-1	MD	Outgoing Trunk HILO 4-Wire Switching
1A374-02	124	J1A090BF-2		Outgoing Trunk HILO 4-Wire Switching
1A375-01	125	J1A033MH-1		TOUCH TONE TRANSMITTER (EPSCS)
1A378-01	128	J1A033MC-1		DIAL PULSE TRANSMITTER HILO 4-WIRE SWITCHING
1A379-01	129	J1A033MA-1		MULTIFREQUENCY RECEIVER HILO 4-WIRE SWITCHING
1A380-01	130	J1A033MB-1		MULTIFREQUENCY TRANSMITTER HILO 4-WIRE SWITCHING
1A381-01	131	J1A033NA-1		MULTIFREQUENCY TEST ENVIRONMENT HILO 4-WIRE SWITCHING
1A382-01	132	J1A033NB-1		TONE PRESENCE DETECTOR HILO 4-WIRE SWITCHING
1A383-01	133	J1A090BG-1	MD	Tone or RCD ANCMT HILO 4-W Switching
1A383-02	133	J1A090BG-2		Tone or RCD ANCMT HILO 4-W Switching
1A384-01	134	J1A033MD-1		AUDIBLE RING AND RECORD ANOUNCEMENT HILO 4-WIRE
1A385-01	135	J1A033NC-1		TOUCH-TONE DETECTOR TEST HILO 4-WIRE SWITCHING
1A386-01	136	J1A033ND-1		COMBINED 100/102 TEST UNIT HILO 4-WIRE SWITCHING
1A388-01	138	J1A033ME-1		104/105 TEST COUPLER HILO 4-WIRE SWITCHING
1A389-01	139	J1A033MF-1		ECHO SUPPRESSOR TEST TERM HILO 4-WIRE SWITCHING

SD NBR	CODE	J DRAWING		TITLE
1A390-01	140	J1A033MG-1		DIAL PULSE RECEIVER HILO 4-WIRE SWITCHING
1A390-01	157	J1A033MG-1		TOUCH-TONE DP RECEIVER HILO 4W SWITCHING
1A391-01	141	J1A033NE-1		OPERATIONAL TEST TERMINATION HILO 4-WIRE SWITCHING
1A392-01	142	J1A090BH-1	MD	HILO Interface Trunk HILO 4-Wire Switching
1A392-02	142	J1A090BH-2		HILO Interface Trunk HILO 4-Wire Switching
1A393-01	143	J1A033BM-1		OGT AUXILIARY COMBINED OPERATOR OFFICE TRK HILO 4-WIRE SWITCHING
1A394-01	144	J1A033BL-1		OGT TO CAMA 3C, 3CL SWBD, OR TSPS HILO 4-WIRE SWITCHING
1A395-01	145	J1A033BN-1		OGT TO CAMA OR 3C, 3CL SWBD HILO 4-WIRE SWITCHING
1A396-01	146	J1A090BJ-1	MD	Two Way Trunk HILO 4-Wire Switching
1A396-02	146	J1A090BJ-2		Two Way Trunk HILO 4-Wire Switching
1A397-01	147	J1A090BK-1	MD	Trunk Test Access HILO 4-Wire Switching
1A397-02	147	J1A090BK-2		Trunk Test Access HILO 4-Wire Switching
1A399-01	149	J1A033MK-1		6 PORT CONFERENCE (EPSCS)
1A415-05	162	J1A088CK-1		FOREIGN EXCHANGE LONG HAUL
1A416-05	163	J1A088CF-1		FOREIGN EXCHANGE SHORT HAUL
1A431-01	101	J1A033GW-1		CPD PULSE STRETCHER HILO 4-WIRE SWITCHING
1A436-01	088	J1A033JT-1		CCIS CONTINUITY CHECK TRANSCEIVER
1A438-01	300	J1A033GY-1		SIGNAL DISTRIBUTOR APPLIQUE
1A440-01	164	J1A032DD-1		PAGING INTERFACE
1A451-01	205	J1A033PB-1		CCIS 2-WIRE CONTINUITY CHECK DIAGNOSTIC TEST
1A453-01	203	J1A033ML-1		CCIS HILO CONTINUITY CHECK TRANSCEIVER
1A454-01	204	J1A033NH-1		CCIS HILO 4-WIRE CONTINUITY CHECK DIAGNOSTIC TEST
1A456-01	165	J99382AA-1		VSG LOOP AROUND TRK
1A458-01	167	J1A033JV-2		TOUCH-TONE TRANSMITTER
1A458-01	167	J1A033JV-1	MD	TOUCH-TONE TRANSMITTER
1A459-01	168	J1A033PA-1		TRANSMITTER TEST
1A462-01	170	J1A033PE-1		TWO-WAY TRK CKT FOR VOICE STG SYS SERVICE

SD NBR	CODE	J DRAWING	TITLE
1A473-01	173	J1A033CR-1	TWO-WAY E&M TRK, 4W
1A474-01	174	J1A033CS-1	TWO-WAY E&M TRK, 2W
1A475-01	175	J1A033CT-1	FOREIGN EXCHANGE TRK, LONG HAUL
1A476-01	176	J1A033CU-1	FOREIGN EXCHANGE TRK DIAL PULSE REPEATING
1A482-01	169	J1A033PH-1	LOOP RANGE EXTENSION TEST UNIT
1A483-01	198	J1A033MR-1	3-PORT CONF BRDG, FOR HILO 4-WIRE SWITCHING
1A484-01	197	J1A033BP-1	OUTGOING HILO TRK
1A491-01	207	J1A032BH-1	OGT TRK TO TSPS
1A491-05	207	J1A084BH-1	OGT TRK TO TSPS
1A492-01	208	J1A032BJ-1	OGT TRK TO TSPS E&M SUPVN
1A492-05	208	J1A084BJ-1	TWO WAY TRK INBAND SIG
1A493-01	206	J1A033JW-1	IMPROVED TEST COUPLER
1A565-05	209	J1A088PM-1	BRIDGING 2-WIRE TRUNK UNIT
1A608-02	182	J1A091BE-2	INC TRK/SXS E&M SUPVN
1A609-02	184	J1A091BF-2	INCOMING SXS E&M SUPVN
1C650-01	091	J99388C-2	TOUCH-TONE CALLING RECEIVER
1C650-01	064	J99388C-2	TOUCH-TONE CALLING RECEIVER/CUSTOMER DIAL PULSE RECEIVER
2A027-01	101	J2A003BL-2	CPD APPLIQUE
3B000-01	019	J3B001B-1	MF XTMR/SO COMBINATION
97757-01	165	J99392BA-1	VSG LOOP AROUND TRK

SECTION 12

NO. 1 ESS PROCESSOR

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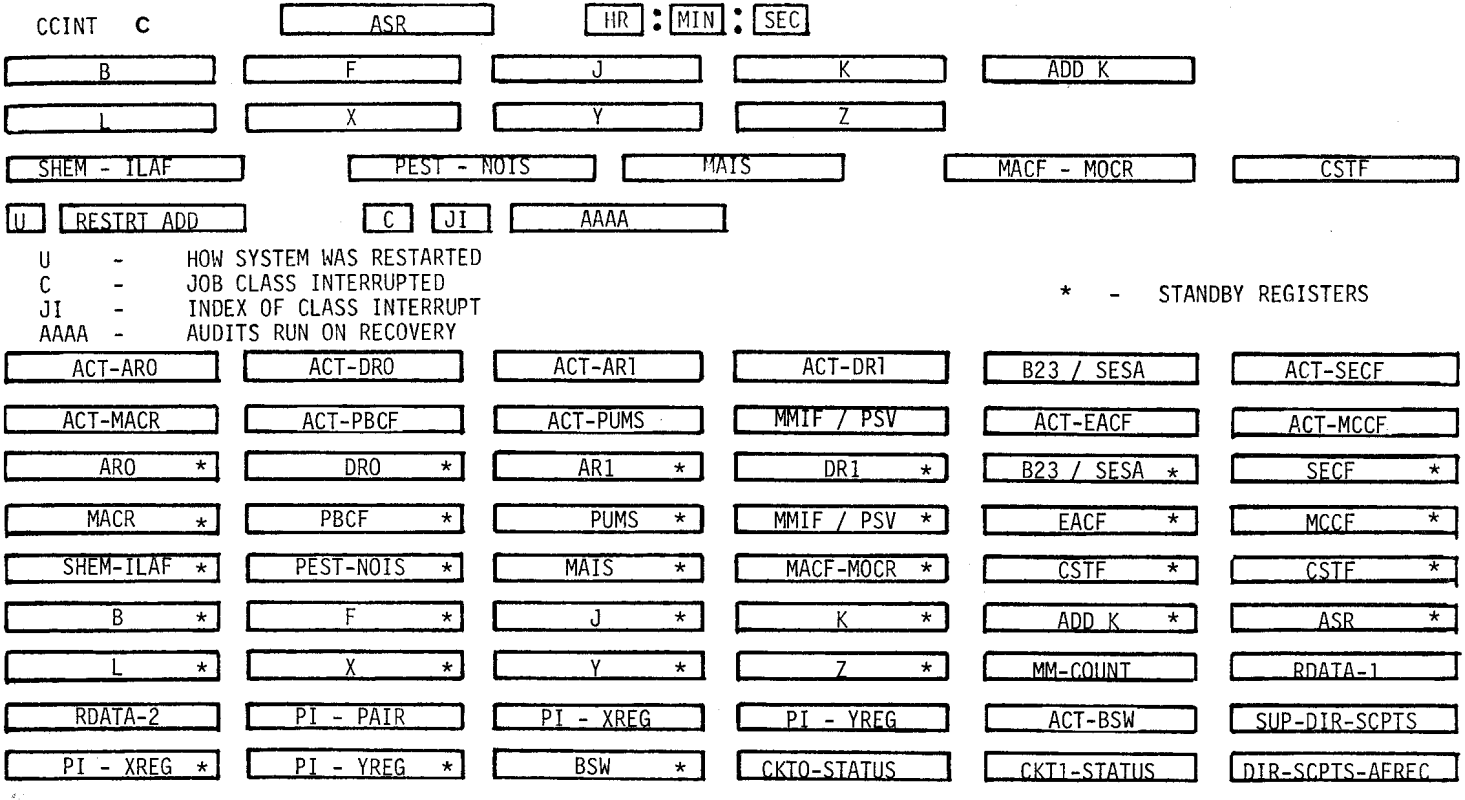

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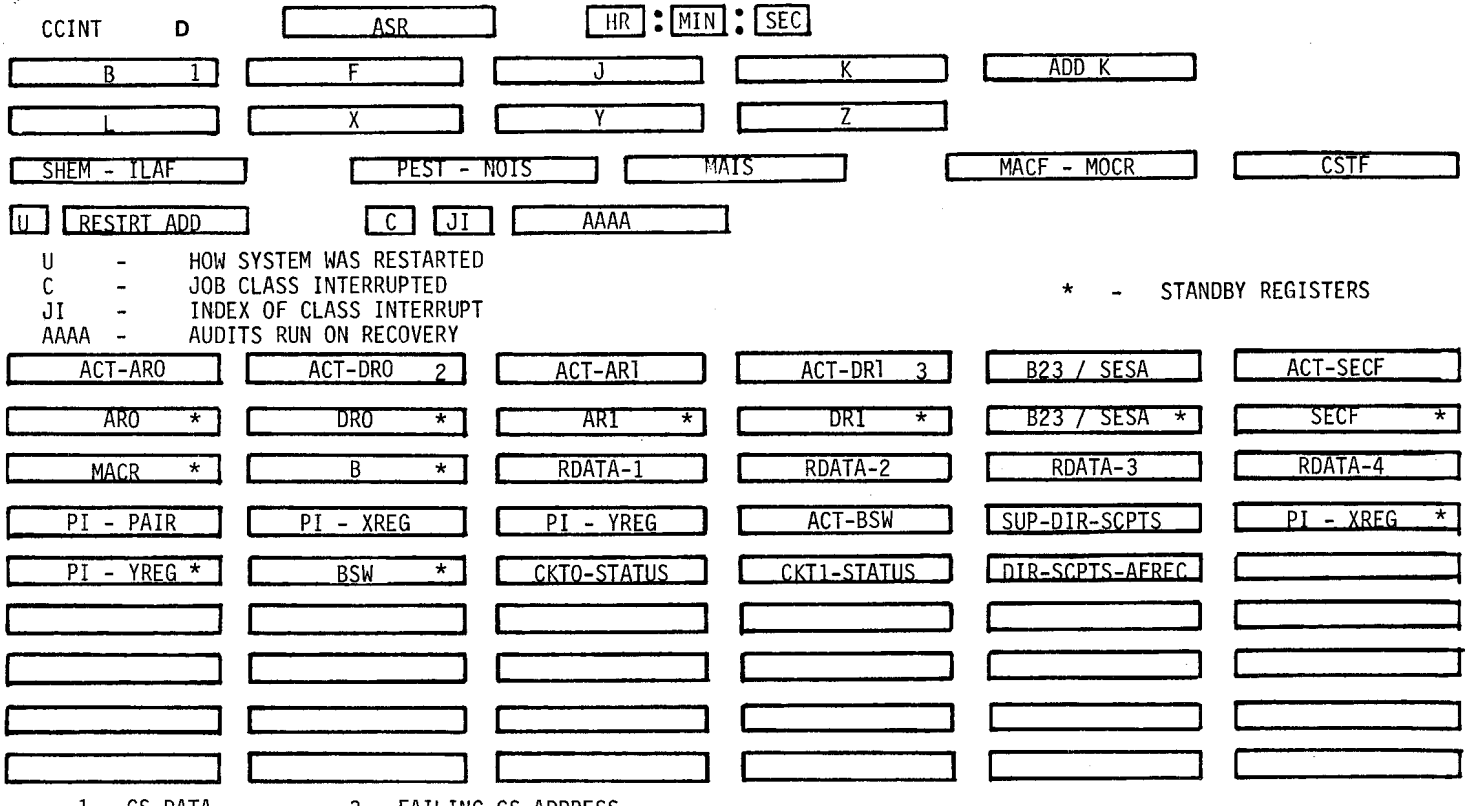

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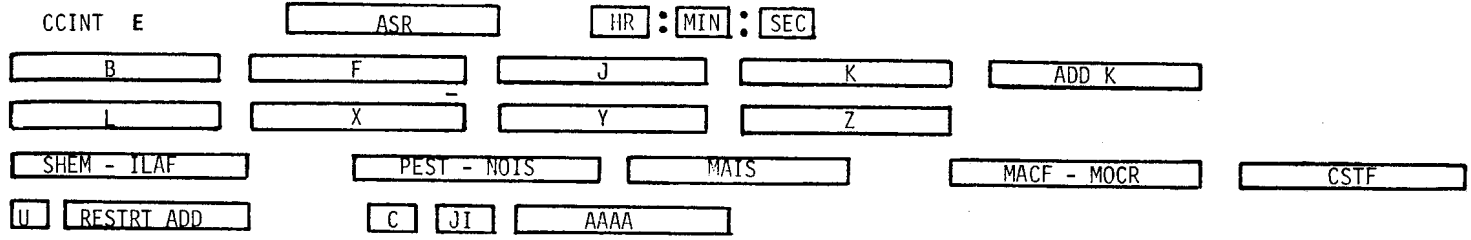


U - HOW SYSTEM WAS RESTARTED
C - JOB CLASS INTERRUPTED
JI - INDEX OF CLASS INTERRUPT
AAAA - AUDITS RUN ON RECOVERY

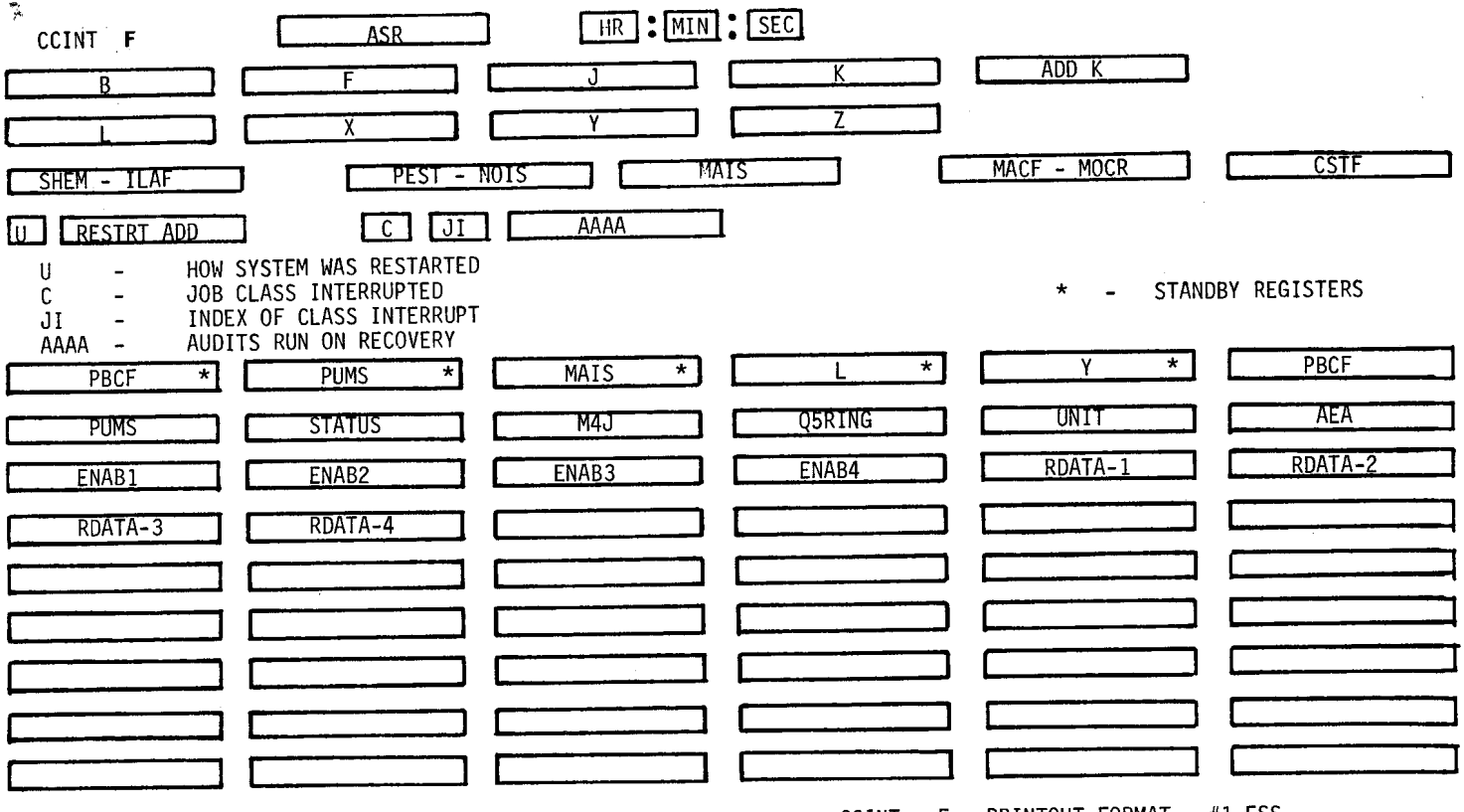
* - STANDBY REGISTERS

ACT-ARO 1	ACT-DRO 2	ACT-AR1 3	ACT-DR1 4	B23 / SESA	ACT-SECF
ARO 1*	DRO 2*	AR1 3*	DR1 4*	B23 / SESA *	SECF *
MACR	MCCF				

1 - BITS 19 - 0 BOWR (SBY)
2 - FAILING PS ADDRESS UNLESS "V" BIT RESET

3 - BITS 43 - 20 BOWR (SBY)
4 - BITS 43 - 20 BOWR (ACT)

CCINT E PRINTOUT FORMAT #1 ESS



CCINT F PRINTOUT FORMAT #1 ESS

PROGRAM STORE AND CALL STORE BUS SELECTION IN CC

Ten flip-flops are required to determine which central control is working with which program store and call store bus. They are the AU, PBO, PBA, PBT, CBO, CBA, CBT, OL3, and MRP. These flip-flops have the following significance:

AU - central control status. 0 = CC0 active, 1 = CC1 active

PBO, CBO - 1 = active CC sends on both busses

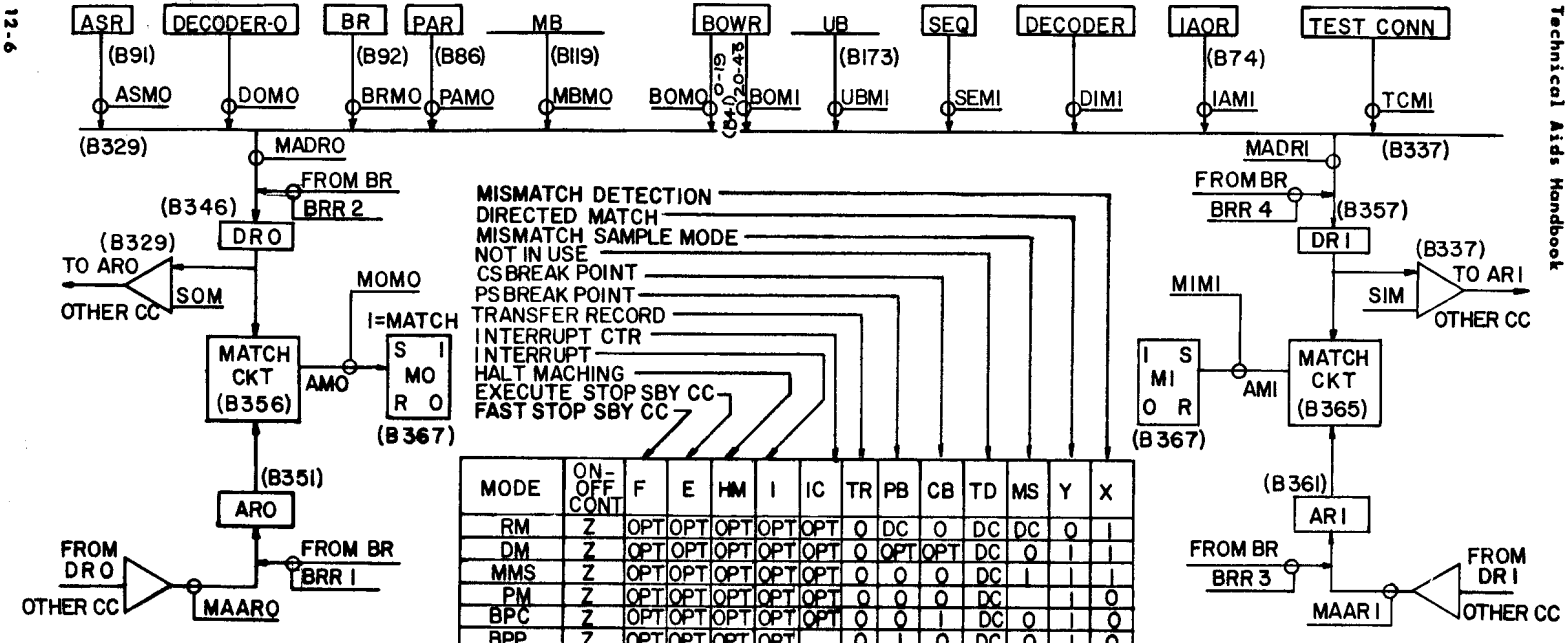
PBA, CBA - this flip-flop defines the active bus, ie, which bus is to be used by the active CC

PBT, CBT - 1 = standby bus is not used

OL3 - offline operation. 1 = bus selection for maintenance and control instructions is handled the same as for normal instructions (controlled by PBO, PBA, PBT, CBO, CBA, and CBT). 0 = active CC sends addresses on both busses and each CC will receive from the bus specified by the MRP, MRC flip-flop

MRP, MRC - maintenance and control instructions. 1 = receive from bus 1, 0 = receive from bus 0

PS bus	PBT	PBA	PBO	Active CC		Standby CC	
CS bus	CBT	CBA	CBO	Send	Rec	Send	Rec
	0	0	0	0	0	1	1
	0	1	0	1	1	0	0
	1	0	0	0	0	X	0
	1	1	0	1	1	X	1
	0	0	1	0&1	0	X	1
	0	1	1	0&1	1	X	0
	1	0	1	0&1	0	X	0
	1	1	1	0&1	1	X	1
0 = F/F reset 1 = F/F set				0 = bus 0 1 = bus 1 X = neither bus			



MODE	ON-OFF CONT	F	E	HM	I	IC	TR	PB	CB	TD	MS	Y	X
RM	Z	OPT	OPT	OPT	OPT	OPT	0	DC	0	DC	DC	0	1
DM	Z	OPT	OPT	OPT	OPT	OPT	0	OPT	OPT	DC	0	1	1
MMS	Z	OPT	OPT	OPT	OPT	OPT	0	0	0	DC	1	1	1
PM	Z	OPT	OPT	OPT	OPT	OPT	0	0	0	DC		1	0
BPC	Z	OPT	OPT	OPT	OPT	OPT	0	0	1	DC	0	1	0
BPP	Z	OPT	OPT	OPT	OPT		0	1	0	DC	0	1	0
BPCP	Z	OPT	OPT	OPT	OPT	OPT	0	1	1	DC	0	1	0
BPCS PH1	Z	OPT	OPT	OPT	OPT	OPT	0	0	1	DC	1	1	0
BPCS PH2	Z			OPT		OPT	0	0	1	DC	1	1	0
BPPS PH1	Z	OPT	OPT	OPT	OPT		0	1	0	DC	1	1	0
BPPS PH2	Z			OPT		OPT	0	1	0	DC	1	1	0
BPCPS PH1	Z	OPT	OPT	OPT	OPT	OPT	0	1	1	DC	1	1	0
BPCPS PH2	Z			OPT		OPT	0	1	1	DC	1	1	0
TRR	Z	OPT	OPT		OPT		1	DC	DC	DC	DC	0	DC
B-TEST	B						DC	DC	DC	DC	DC	DC	DC
B → (B311)		11	10	9	8	7	6	5	4	3	2	1	0
Z → (B385)		MOCR BB6 (4012) (B368)											

NO.1 ESS
MATCHER CIRCUIT

WCH/80

ROUTINE MATCHING (MOCR=0.1401)				
WR=1	BR	10T16	IAOR	10T16
RE or PU=1	MB	10T16	IAOR	10T16
EC=1	BOWRR	10T16	BOWRL	10T16
NONE & MC=0	PAR	10T16	UB OTB & 16T22	
NONE & MC=1	PAR	10T16	UB	10T16
NONE & MC=2	MB	10T16	SEQ 0	10T16
NONE & MC=3	MB	10T16	SEQ 1	10T16
CONDITION	MATCHER 0		MATCHER 1	

MATCH CYCLE COUNTER — ERROR CORRECTION — READ — WRITE — PERPHERAL OPER.

MC1	MC0	EC	RE	WR	PU	MI	MO
19	18	17	16	15	14	13	12

MACF BB7 (4014) (B367)

MACR BB5 (4010) (B372)

TIME OF MATCH MATCHER 1	TIME OF MATCH MATCHER 0
00 NO MTCH	00 NO MTCH
01 10 T 16	01 10 T 16
10 OT8	10 OT8
11 16T22	11 16T22

DATA MATCHED MATCHER 1	DATA MATCHED MATCHER 0
000 NO MATCH	000 NO MATCH
001 SEQ 0 (MC=10) SEQ 1 (MC=11)	001 PAR
010 UB	010 MB
011 BOWR (20-43)	011 BOWR (0-19)
100 IAOR	100 BR
101 TEST CONN	101 ASR
110 DEC GRP 1	110 DEC GRP 0
PRESENT CONT	PRESENT CONT
111 OF ARO, DR1	111 OF ARO, DR0

NO.1 ESS MATCHER CIRCUIT

WCH/80

ELIMINATE EXTRA TIME OUT CYCLES
RESET TIME OUT COUNTER
FF SET WHEN TOCR=COUNTER
PROG CONTROLLED TIME OUT
INHIB SEQ TIME OUT
INHIB TIME OUT INTERRUPT
TIME OUT COUNTER

EETO	RTOC	SHTO	PCTO	ISTO	ITOI	TOCR 5	4	3	2	1	0	TI1	TI0	TO1	TO0	PI2	PI1	PI0	P02	P01	P00
21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

SPINT C, CX

JOB	HR : MIN : SEC

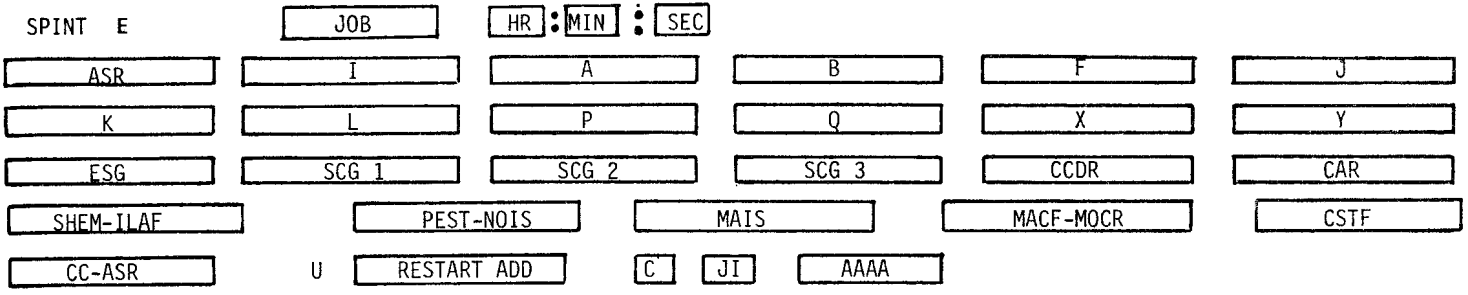
ASR	I	A	B	F	J
K	L	P	Q	X	Y
ESG	SCG 1	SCG 2	SCG 3	CCDR	CAR
SHEM-ILAF	PEST-NOIS	MAIS	MACF-MOCR	CSTF	
CC-ASR	U	RESTART ADD	C	JI	AAAA

U - HOW SYSTEM RESTARTED
C - JOB CLASS INTERRUPTED
JI - INDEX OF TASK INTERRUPTED
AAAA - AUDITS RUN ON RECOVERY

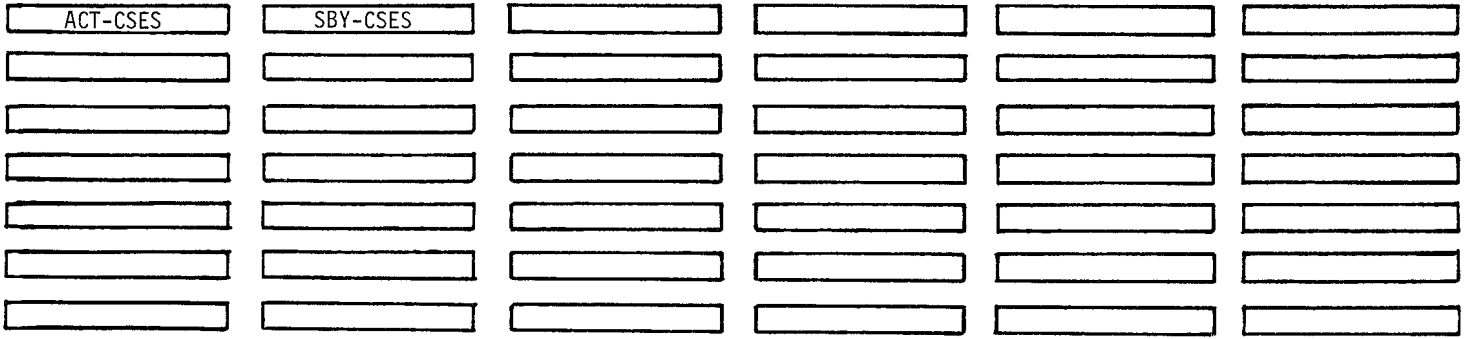
ACT-MRI	ACT-MRE	ACT-CSBC	ACT-CSES	SBY-B +	SBY-SCG2 +
SBY-MRI +	SBY-MRE +	SBY-CSBC +	SBY-CSES +	SBY-ESG +	RDATA-1 +
RDATA-2 +	RDATA-3 +	RDATA-4 +			

+ - NOT PRINTED FOR "CX" INTERRUPTS

SPINT C, CX PRINTOUT FORMAT #1 ESS



U - HOW SYSTEM RESTARTED
C - JOB CLASS INTERRUPTED
JI - INDEX OF TASK INTERRUPTED
AAAA - AUDITS RUN ON RECOVERY



SPINT E OUTPUT FORMAT #1 ESS

SPINT K, KX

JOB	HR : MIN : SEC

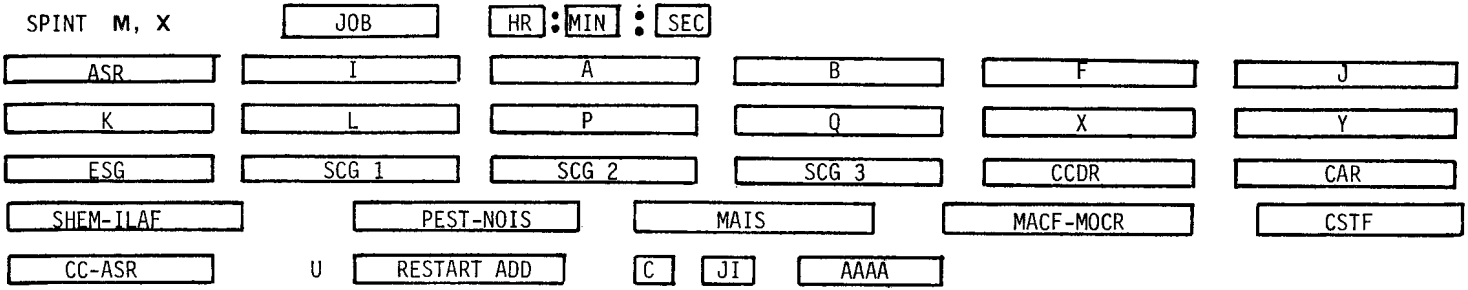
ASR	I	A	B	F	J
K	L	P	Q	X	Y
ESG	SCG 1	SCG 2	SCG 3	CCDR	CAR
SHEM-ILAF	PEST-NOIS	MAIS	MACF-MOCR	CSTF	
CC-ASR	U	RESTART ADD	C	JI	AAAA

U - HOW SYSTEM RESTARTED
C - JOB CLASS INTERRUPTED
JI - INDEX OF TASK INTERRUPTED
AAAA - AUDITS RUN ON RECOVERY

HOP-ENTRY +	HOP-POINTER +				

+ - NOT USED FOR "KX" INTERRUPTS

SPINT K, KX PRINTOUT FORMAT #1 ESS



U - HOW SYSTEM RESTARTED
C - JOB CLASS INTERRUPTED
JI - INDEX OF TASK INTERRUPTED
AAAA - AUDITS RUN ON RECOVERY

ACT-MRI	ACT-MRE	ACT-CSBC	ACT-CSES	ACT-PBC	ACT-DER
SBY-MRI	SBY-MRE	SBY-CSBC	SBY-CSES	SBY-PBC	SBY-DER
SBY-ASR	SBY-I	SBY-A	SBY-B	SBY-F	SBY-J
SBY-K	SBY-L	SBY-P	SBY-Q	SBY-X	SBY-Y
SBY-ESG	SBY-SCG1	SBY-SCG2	SBY-SCG3	SBY-CCDR	SBY-CAR
ACT-MACO	SBY-MACO	MM COUNT	TST ADDR	TST DATA	

SPINT M, X PRINTOUT FORMAT #1 ESS

SPINT P, PF, PI, PM | JOB | HR : MIN : SEC

ASR	I	A	B	F	J
K	L	P	Q	X	Y
ESG	SCG 1	SCG 2	SCG 3	CCDR	CAR
SHEM-ILAF	PEST-NOIS	MAIS	MACF-MOCR	CSTF	
CC-ASR	U	RESTART ADD	C	JI	AAAA

U - HOW SYSTEM RESTARTED
C - JOB CLASS INTERRUPTED
JI - INDEX OF TASK INTERRUPTED
AAAA - AUDITS RUN ON RECOVERY

SBY-PBC	SBY-DER	SBY-F	SBY-L	SBY-Y	SBY-ESG
SBY-SCG1	SBY-SCG2	SBY-SCG3	PBC	DER	STATUS
M4J	O5RING	UNIT	AEA	ENABL1	ENABL2
ENABL3	ENABL4	RDATA-1	RDATA-2	WRD-0	WRD-1
WRD-2	WRD-3	WRD-4	WRD-5	WRD-6	WRD-7
WRD-8	WRD-9	WRD-10	WRD-11	WRD-12	WRD-13
WRD-14	WRD-15				

SPINT P, PF, PI, PM (FOR PUC) PRINTOUT FORMAT #1 ESS

SPINT P, PF, PI, PM

JOB	HR : MIN : SEC				
ASR	I	A	B	F	J
K	L	P	Q	X	Y
ESG	SCG 1	SCG 2	SCG 3	CCDR	CAR
SHEM-ILAF	PEST-NOIS	MAIS	MACF-MOCR	CSTF	
CC-ASR	U RESTART ADD	C	JI	AAAA	

U - HOW SYSTEM RESTARTED
C - JOB CLASS INTERRUPTED
JI - INDEX OF TASK INTERRUPTED
AAAA - AUDITS RUN ON RECOVERY

* - STANDBY SP REGISTERS

PBC *	DER *	F *	L *	Y *	ESG *
SCG 1 *	SCG 2 *	SCG 3 *	PBC	DER	STATUS
M4J	Q5RING	UNIT	AEA	ENABL 1	ENABL 2
ENABL 3	ENABL 4	RDATA-1	RDATA-2	RDATA-4	

SPINT P, PF, PI, PM (NON-PUC) PRINTOUT FORMAT #1 ESS

SPINT PU, PX, S | JOB | HR : MIN : SEC

ASR	I	A	B	F	J
K	L	P	Q	X	Y
ESG	SCG 1	SCG 2	SCG 3	CCDR	CAR
SHEM-ILAF	PEST-NOIS	MAIS	MACF-MOCR	CSTF	
CC-ASR	U	RESTART ADD	C	JI	AAAA

U - HOW SYSTEM RESTARTED
C - JOB CLASS INTERRUPTED
JI - INDEX OF TASK INTERRUPTED
AAAA - AUDITS RUN ON RECOVERY

SPINT PU, PX, S PRINTOUT FORMAT #1 ESS

SPINT U, UX

JOB	HR : MIN : SEC

ASR	I	A	B	F	J
K	L	P	Q	X	Y
ESG	SCG 1	SCG 2	SCG 3	CCDR	CAR
SHEM-ILAF	PEST-NOIS	MAIS	MACF-MOCR	CSTF	
CC-ASR	U	RESTART ADD	C	JI	AAAA

U - HOW SYSTEM RESTARTED
C - JOB CLASS INTERRUPTED
JI - INDEX OF TASK INTERRUPTED
AAAA - AUDITS RUN ON RECOVERY

MRI	MRE	CSBC	TST-ADDR	+ RDATA-1	+ RDATA-2
+ RDATA-3	+ RDATA-4				

+ - NOT PRINTED FOR "UX" INTERRUPTS

SPINT U, UX PRINTOUT FORMAT #1 ESS

PS0			
0		1	
107	117	127	137
03	07	13	17
106	116	126	136
105	115	125	135
02	06	12	16
104	114	124	134
103	113	123	133
01	05	11	15
102	112	122	132
101	111	121	131
00	04	10	14
100	110	120	130

PS1			
		0	
*	*	107	117
		03	07
		106	116
*	*	105	115
		02	06
		104	114
*	*	103	113
		01	05
		102	112
*	*	101	111
		00	04
		100	110

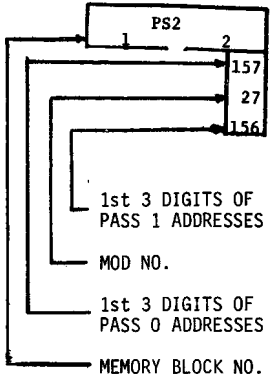
PS2			
1		2	
127	137	147	157
13	17	23	27
126	136	146	156
125	135	145	155
12	16	22	26
124	134	144	154
123	133	143	153
11	15	21	25
122	132	142	152
121	131	141	151
10	14	20	24
120	130	140	150

PS3			
2		3	
147	157	167	177
23	27	33	37
146	156	166	176
145	155	165	175
22	26	32	36
144	154	164	174
143	153	163	173
21	25	31	35
142	152	162	172
141	151	161	171
20	24	30	34
140	150	160	170

PS4			
3		4	
167	177	207	217
33	37	43	47
166	176	206	216
165	175	205	215
32	36	42	46
164	174	204	214
163	173	203	213
31	35	41	45
162	172	202	212
161	171	201	211
30	34	40	44
160	170	200	210

PS5			
4		5	
207	217	227	237
43	47	53	57
206	216	226	236
205	215	225	235
42	46	52	56
204	214	224	234
203	213	223	233
41	45	51	55
202	212	222	232
201	211	221	231
40	44	50	54
200	210	220	230

KEY:



PS6			
5		6	
227	237	247	257
53	57	63	67
226	236	246	256
225	235	245	255
52	56	62	66
224	234	244	254
223	233	243	253
51	55	61	65
222	232	242	252
221	231	241	251
50	54	60	64
220	230	240	250

PS7			
6		7	
247	257	267	277
63	67	73	77
246	256	266	276
245	255	265	275
62	66	72	76
244	254	264	274
243	253	263	273
61	65	71	75
242	252	262	272
241	251	261	271
60	64	70	74
240	250	260	270

PS8			
7		10	
267	277	307	317
73	77	103	107
266	276	306	316
265	275	305	315
72	76	102	106
264	274	304	314
263	273	303	313
71	75	101	105
262	272	302	312
261	271	301	311
70	74	100	104
260	270	300	310

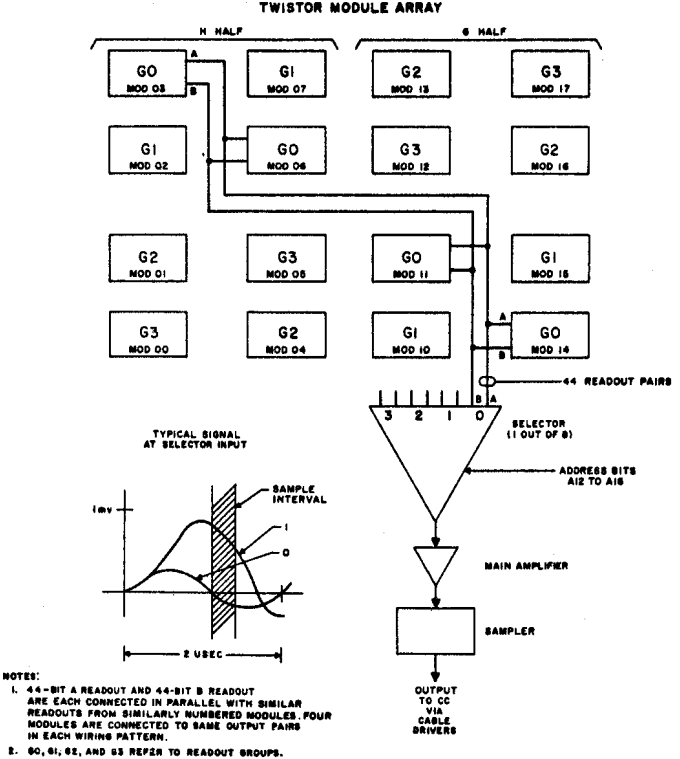
PS9			
10		11	
307	317	327	337
103	107	113	117
306	316	326	336
305	315	325	335
102	106	112	116
304	314	324	334
303	313	323	333
101	105	111	115
302	312	322	332
301	311	321	331
100	104	110	114
300	310	320	330

PS10			
11		12	
327	337	347	357
113	117	123	127
326	336	346	356
325	335	345	355
112	116	122	126
324	334	344	354
323	333	343	353
111	115	121	125
322	332	342	352
321	331	341	351
110	114	120	124
320	330	340	350

PS 11			
12		13	
347	357	367	377
123	127	133	137
346	356	366	376
345	355	365	375
122	126	132	136
344	354	364	374
343	353	363	373
121	125	131	135
342	352	362	372
341	351	361	371
120	124	130	134
340	350	360	370

* SAME AS LAST MEMORY BLOCK IN OFFICE

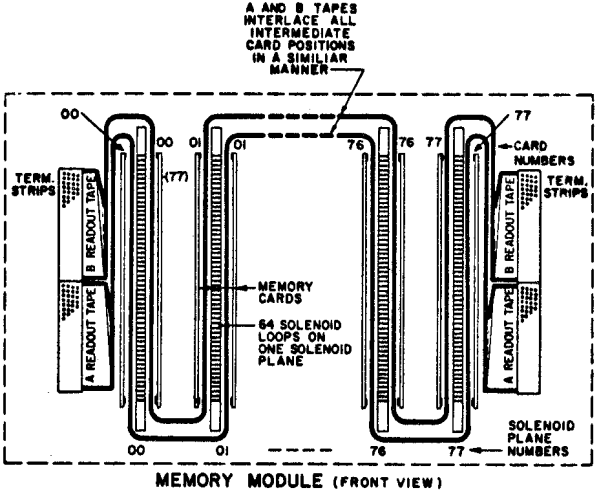
PS ADDRESS AND MEMORY BLOCK LAYOUT



NOTES:

1. 44-BIT A READOUT AND 44-BIT B READOUT ARE EACH CONNECTED IN PARALLEL WITH SIMILAR READOUTS FROM SIMILARLY NUMBERED MODULES. FOUR MODULES ARE CONNECTED TO SAME OUTPUT PAIRS IN EACH WIRING PATTERN.
2. G0, G1, G2, AND G3 REFER TO READOUT GROUPS.

Program Store Readout Connections



MEMORY MODULE (FRONT VIEW)

NOTES:

1. ALL NUMBERING IS OCTAL.
2. WORDS ON EACH CARD ARE NUMBERED 00 THROUGH 77.
3. CARDS TO RIGHT OF SOLENOID PLANES ARE CALLED PASS 0 CARDS; CARDS TO LEFT OF SOLENOID PLANES ARE CALLED PASS 1 CARDS.
4. INFORMATION IS CONTAINED ON ONLY ONE SIDE OF EACH CARD. PASS 0 CARDS AND PASS 1 CARDS HAVE INFORMATION ON OPPOSITE SIDES.
5. PASS 0 AND PASS 1 REFER TO WRITING SEQUENCE WHEN CARDS ARE IN MEMORY CARD WRITER.

"B" TAPE	"A" TAPE
PASS 0 - EVEN CARDS	PASS 0 - ODD CARDS
PASS 1 - ODD CARDS	PASS 1 - EVEN CARDS

Program Store Answer Bus Testing in No. 1 ESS Offices Where PS-0 and PS-1 are in the Same PS Bus Community

Due to the physical location of Program Store Frames in many No. 1 ESS Offices both PS-0 and PS-1 have been engineered and installed on the same PS Bus Community (A or B). This presents a problem when adding a PS Frame to the other Bus Community.

The present "MOD-5" Bus Test Programs require that either PS-0 or PS-1 be in the PS-Bus Community to be tested in order to test the PS Answer Bus. The following is a method by which the A or B Community PS Answer Bus can be tested when PS-0 or PS-1 are not in the Community to be tested. This method utilizes normal Offline procedures and one (possibly two) PS Memory Card(s) from a "MOD-5" Bus Test Program.

1. Utilizing the Program MAP for the "MOD-5" Program Test Set Locate the PS Memory Card(s) containing the seven (7) Test Words starting at symbolic address "ROTP". This (These) cards will be referred to as "TEST CARD(S)".

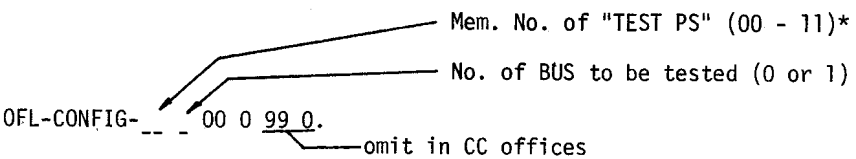
2. Select a Program Store in the PS Bus Community(A or B) to be tested. This will be referred to as the "TEST PS". * The "TEST PS" must have one or two consecutive Memory Cards (depending on no. of TEST CARDS), containing FILL (either Generic FILL or Xlation FILL). These FILL Cards must be of the same "PASS" No. as the "TEST CARDS". The location of these memory cards will be referred to as "TEST CARD LOCATION(S)".

3. T-READ the FILL CARD(S) to verify that the entire card(s) are in fact FILL (ie: All addresses on the Card(s) are either Generic or Xlation FILL).

4. Determine the address of symbolic "ROTP" when the "TEST CARD(S)" are placed in the "TEST CARD LOCATION(S)" of the "TEST PS". This is the "START ADDRESS OF TEST WORDS".

5. Initiate Bus Testing by input messages as follows:

PS ANSWER BUS TEST
Offline Program



Test Card in H Half of TEST PS	Test Card in G Half of TEST PS
OFL-PROG-0013310000203/	OFL-PROG-0013310000203/
007100_____/ START ADDRESS OF TEST WORDS	007100_____/
0527600000000/	0525200000000/
0527600000001/	0525200000001/
0527600000002/	0525200000002/
0527600000003/	0525200000003/
0527600000004/	0525200000004/
0527600000005/	0525200000005/
0527600000006/	0525200000006/
0000000000000/	0000000000000/
0000000000000/	0000000000000/
0000000000000/	0000000000000/
0000000000000/	0000000000000/
0001000015707/	0001000015707/
3777737777777.	3777737777777.

*If it is necessary to use an untested (added) PS as the "TEST PS" use Mem. No. 00 in the OFL-CONFIG- message. It should be noted that under this condition the problems encountered in performing the Bus Test may be caused by the untested "TEST PS" and may not be bus problems.

6. After OFL messages have been successfully completed remove the Original Translation or Generic FILL Card(s) from "TEST CARD LOCATION(S)" and insert the "TEST CARDS".

7. If an untested (added) PS is being used as the "TEST PS" it will have to be configured on the Offline Bus (0 or 1) by setting the Send and Receive FF on the PS with PS Bus Control Card (ITE: 4742). Care should be taken to be sure that this PS does not Send on the Active PS Bus(ie: Set TBL FF associated with the ACTIVE PS Bus and reset SEND FF's FOR THE HALF (H or G) not being used for Test).

   If the system for any reason should attempt to reconfigure PS's and/or PS Buses be prepared to Set TBL FF for the bus being Tested on the untested (added) PS.

   The above FF controls can all be accomplished with the ITE 4742 Bus Control Card.

8. Utilizing on oscilloscope perform Bus Test using scope patterns in the Program Listing for the PS Answer Bus Test.

9. When Bus Test is completed Set both Bus TBL FF's with switches on Bus Control Card if an added PS was used as "TEST PS".

10. Remove "TEST CARD(S)" and insert Original FILL Cards in "TEST CARD LOCATION(S)".

    RETURN TEST CARD(S) TO PROPER
    LOCATION(S) IN MOD 5 TEST SET

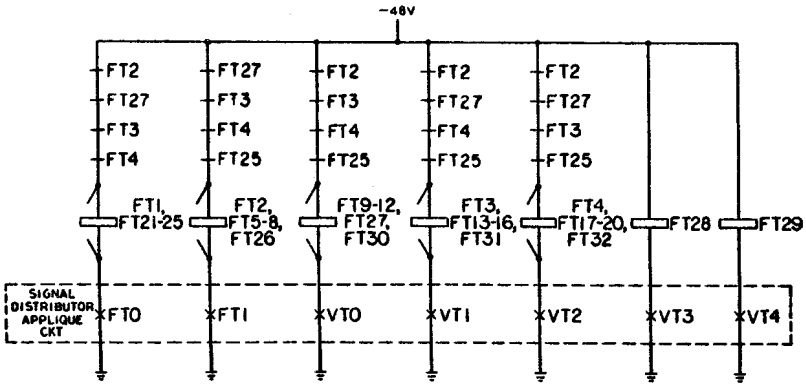
11. Input message OFL-MODE-03.

SIGNAL DISTRIBUTOR OUTPUT *

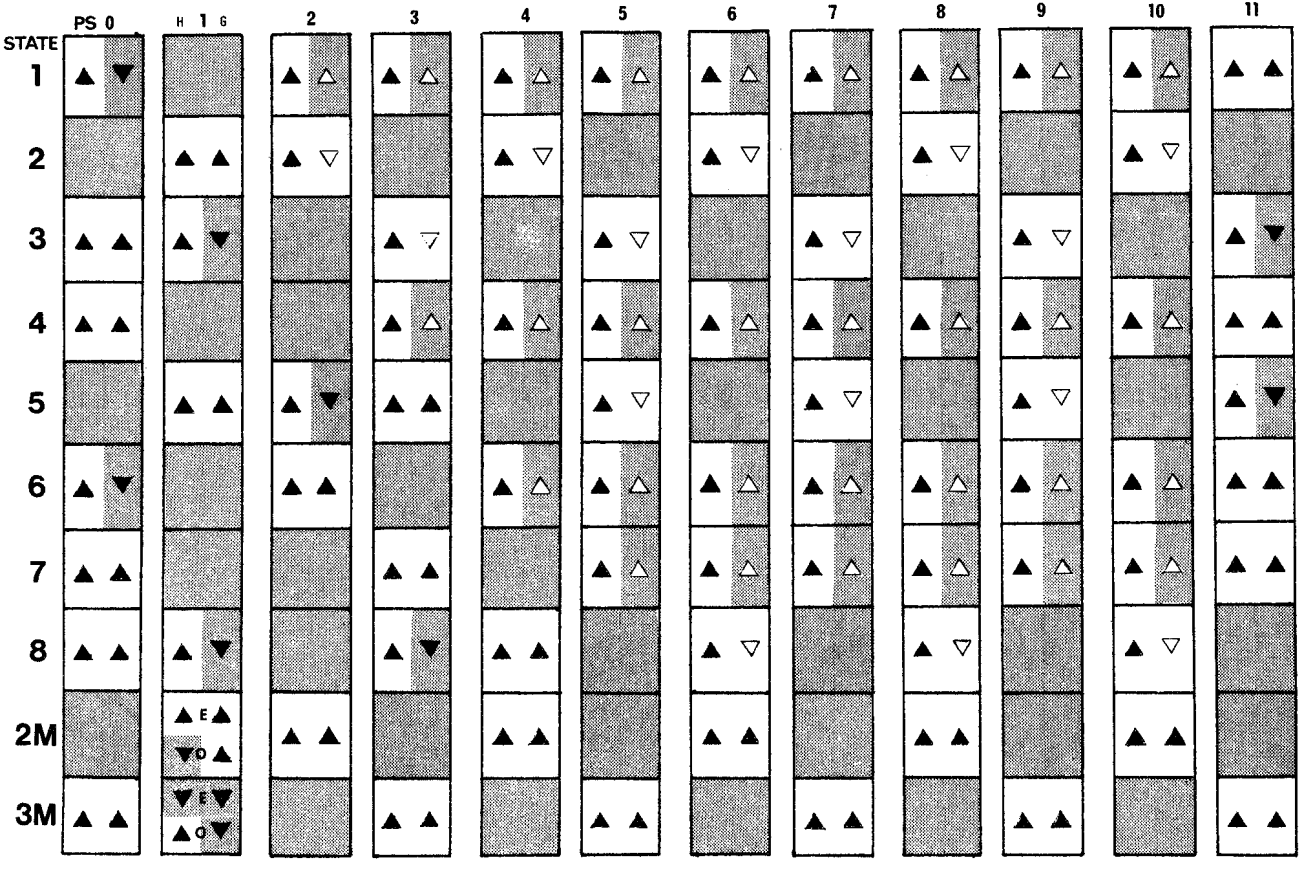
RELAY STATE	SDVT4	SDVT3	SDVT2	SDVT1	SDVT0	SDFT1	SDFT0
1	0	0	0	0	0	0	0
2	0	0	0	0	0	0	1
3	0	0	0	0	0	1	0
4	0	0	0	0	1	0	0
5	0	1	0	0	1	0	0
6	1	0	0	0	1	0	0
7	1	1	0	0	1	0	0
8	0	0	0	1	0	0	0
9	1	0	0	1	0	0	0
10	1	1	0	1	0	0	0
11	0	0	1	0	0	0	0
12	0	1	1	0	0	0	0
13	1	0	1	0	0	0	0
14	1	1	1	0	0	0	0
15	1	1	0	0	0	0	0

* RELAYS THAT ARE OPERATED WHEN THE ASSOCIATED SD OUTPUT IS OPERATED (=1):

SD	RELAYS	
FT0	FT1,FT21-FT25	Operation of one SD relay - FT0, FT1, VT0, VT1, VT2 will render operation of others ineffective through contacts of FT2, FT3, FT4, FT25, or FT27 relay.
FT1	FT2,FT5-FT8,FT26	
VT0	FT9-FT12,FT27,FT30	
VT1	FT3,FT13-FT16,FT31	
VT2	FT4,FT17-FT20,FT32	
VT3	FT28	
VT4	FT29	



PS STATE CONTROL



DOWN ALWAYS
TROUBLE F/F SET

DOWN NORMALLY
LAST STORE UP

DOWN ALWAYS
SEND F/F RESET

UP NORMALLY
LAST STORE DOWN

UP ALWAYS

E CONFIGURATION WITH EVEN QUANTITY OF PSs

O CONFIGURATION WITH ODD QUANTITY OF PSs

A10 PACK IN PS 1 AT 234-22. ENPS WILL RESET WHEN FR SETS. WITHOUT A10, ENPS IS SET.

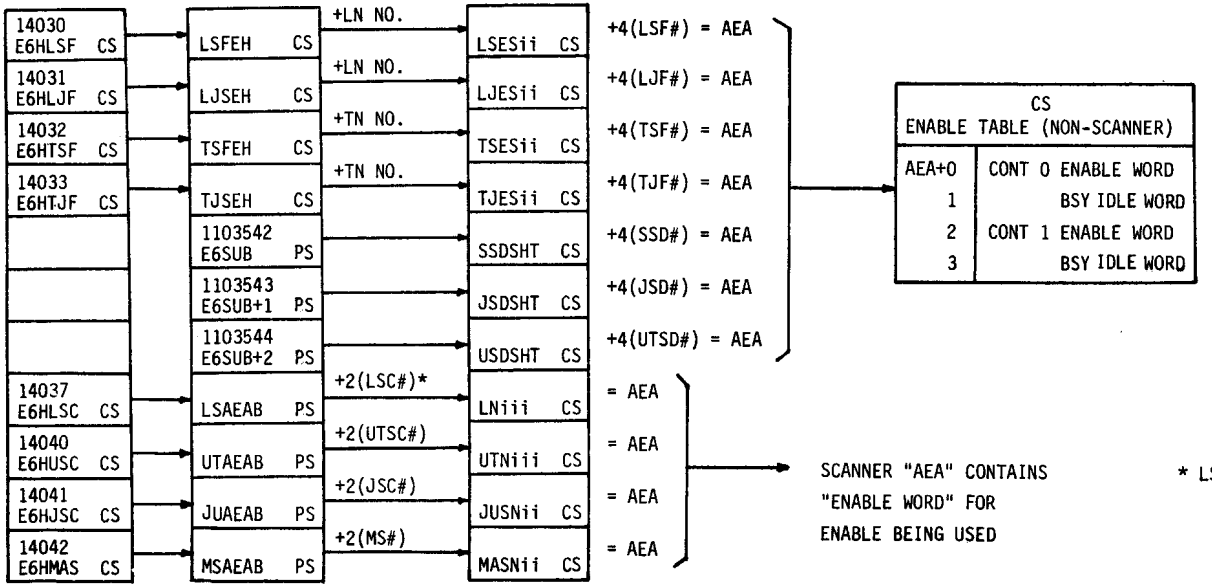
#1 ESS ENABLE WORD LAYOUT

ENABLE WORD LAYOUT (IN ENABLE TABLE)

22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GRP			ROW			COLUMN		PUB NO	CPD PAIR			NO	TRANSLATOR			EV	ASW	PRI TBL	FLT REC ACT	RTE SEN	CON OS	BI WD

SHORT BINARY	0	0	0
LONG BINARY	0	0	1
LSF (4:1)	0	1	0
LSF (2:1)	0	1	1
JSF or TSF	1	0	0
CPD ADDR BUS (LB)	1	0	1
SIG DISTR (SD)	1	1	0
SCANNER	1	1	1

- BSY IDLE WORD USED
- CONTROLLER OUT OF SERV
- ROUTE SENSITIVE
- FAULT RECOGNITION ACTIVE
- PRIMARY TROUBLE
- ALL SEEMS WELL EXPECTED
- ENABLE VERIFY EXPECTED



CENTRAL CONTROL BUFFER BUS SYSTEM

LOC	OCTAL ADDRESS	REGISTER OR GROUP NAME		F.S.	TEST CONN	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	4000-1	ARO	EXTERNAL MATCH REG. ARO	83	226-10	ARO-23 RWC *	ARO-22 RWC	ARO-21 RWC	ARO-20 RWC	ARO-19 RWC	ARO-18 RWC	ARO-17 RWC	ARO-16 RWC	ARO-15 RWC	ARO-14 RWC	ARO-13 RWC	ARO-12 RWC	ARO-11 RWC	ARO-10 RWC	ARO-9 RWC	ARO-8 RWC	ARO-7 RWC	ARO-6 RWC	ARO-5 RWC	ARO-4 RWC	ARO-3 RWC	ARO-2 RWC	ARO-1 RWC	ARO-0 RWC
2	4002-3	DRO	INTERNAL MATCH REG. DRO	83	226-25	DRO-23 RWC *	DRO-22 RWC	DRO-21 RWC	DRO-20 RWC	DRO-19 RWC	DRO-18 RWC	DRO-17 RWC	DRO-16 RWC	DRO-15 RWC	DRO-14 RWC	DRO-13 RWC	DRO-12 RWC	DRO-11 RWC	DRO-10 RWC	DRO-9 RWC	DRO-8 RWC	DRO-7 RWC	DRO-6 RWC	DRO-5 RWC	DRO-4 RWC	DRO-3 RWC	DRO-2 RWC	DRO-1 RWC	DRO-0 RWC
3	4004-5	ARI	EXTERNAL MATCH REG. ARI	84	224-35	ARI-23 RWC *	ARI-22 RWC	ARI-21 RWC	ARI-20 RWC	ARI-19 RWC	ARI-18 RWC	ARI-17 RWC	ARI-16 RWC	ARI-15 RWC	ARI-14 RWC	ARI-13 RWC	ARI-12 RWC	ARI-11 RWC	ARI-10 RWC	ARI-9 RWC	ARI-8 RWC	ARI-7 RWC	ARI-6 RWC	ARI-5 RWC	ARI-4 RWC	ARI-3 RWC	ARI-2 RWC	ARI-1 RWC	ARI-0 RWC
4	4006-7	DRI	INTERNAL MATCH REG. DRI	84	228-35	DRI-23 RWC *	DRI-22 RWC	DRI-21 RWC	DRI-20 RWC	DRI-19 RWC	DRI-18 RWC	DRI-17 RWC	DRI-16 RWC	DRI-15 RWC	DRI-14 RWC	DRI-13 RWC	DRI-12 RWC	DRI-11 RWC	DRI-10 RWC	DRI-9 RWC	DRI-8 RWC	DRI-7 RWC	DRI-6 RWC	DRI-5 RWC	DRI-4 RWC	DRI-3 RWC	DRI-2 RWC	DRI-1 RWC	DRI-0 RWC
5	4010-1	MACR	MATCH CONTROL REG. **	85	328-43			EETO RWC EMMS	RTOC WC EMMS	SHTO RWC EMMS	PCTO RWC EMMS	ISTO RWC EMMS	ITOI RWC EMMS	TOCR-5 RWC EMMS	TOCR-4 RWC EMMS	TOCR-3 RWC EMMS	TOCR-2 RWC EMMS	TOCR-1 RWC EMMS	TOCR-0 RWC EMMS	TI-1 RWC EMMS	TI-0 RWC EMMS	TO-1 RWC EMMS	TO-0 RWC EMMS	PI-2 RWC EMMS	PI-1 RWC EMMS	PI-0 RWC EMMS	PO-2 RWC EMMS	PO-1 RWC EMMS	PO-0 RWC EMMS
6	4012-3	MOCR	MATCH MODE CONTROL REG.	85	314-44													F RWC	E RWC	HM RWC	I RWC	IC RWC	TR RWC	PB RWC	CB RWC	TD RWC	MS RWC	Y RWC	X RWC
7	4014-5	MACF	MATCH CYCLE CONTROL FF'S	85	324-05		MRP RWC	MRC RWC		MC-1 (MC23) RWC	MC-0 (MC13) RWC	EC RWC	RE RWC	WR RWC	PU RWC	MI R***	MO R***												
8	4016-7	CSTF	CPD CONTROLLED STATUS FF'S	75	314-37 232-41		ACSFM (M) R,CPDUN		(305)W			OL3 R CPDUN	IMMA R CPDBI	PST R CPDBI	B-TST R CPDUN	V-BIT R CPDUN	DI R CPDUN	OL2 R CPDUN	OLI R CPDUN	CWC R CPDBI	CW R CPDBI	CBT R CPDUN	CBA R CPDUN	CBO R CPDUN	PBT R CPDUN	PBA R CPDUN	PBO R CPDUN	TCC R CPDUN	AU R CPDUN
9	4020-1	PBCF	PERIPHERAL BUS CONTROL FF'S	80 67	318-36 210-33		SCBB RW	SCBA RW	CPDB RW	PUP (ZI) RW	PUPCK (ZI) RW	RAMPCK (ZI) RW	IPURPF (ZI) RW	FIRM R	SR R	IASWS (R), RW													
10	4022-3	PUMS	PERIPHERAL UNIT MAINT. SUMMARY	78 19	232-41		ASWS R	Y23 R	PCC R	PCB R	PCA R	MCE R	ASWCPD R	EXBR-7 R	EXBR-6 R	EXBR-5 R	EXBR-4 R	EXBR-3 R	EXBR-2 R	EXBR-1 R	EXBR-0 R	EXAR-7 R	EXAR-6 R	EXAR-5 R	EXAR-4 R	EXAR-3 R	EXAR-2 R	EXAR-1 R	EXAR-0 R
11	4024-5	SESA	STORE ERROR SUMMARY - A	78 24	324-35																X23 R	PFC RW	ASWC-1 RW	ASWC-0 RW	PF RW	DBEF RW	ADEF RW	ASWPF-1 RW	ASWPF-0 RW
12	4026-7	SECF	STORE ERROR COUNTER FF'S	78 57	318-42		CEOV R	CSEC-4 R	CSEC-3 R	CSEC-2 R	CSEC-1 R	CSEC-0 R	2EOV R	PS2EC-4 R	PS2EC-3 R	PS2EC-2 R	PS2EC-1 R	PS2EC-0 R	IEOV R	PSIEC-4 R	PSIEC-3 R	PSIEC-2 R	PSIEC-1 R	PSIEC-0 R			RCSEC W *	RPS2EC W *	RPSIEC W *
13	4030-1	MSCF	MILLISECOND CLOCK STATE FF'S	89	108-40													CLI2 R	CLII R	CLIO R	CLO9 R	CLO8 R	CLO7 R	CLO6 R	CLO5 R	CLO4 R	CLO3 R	CLO2 R	CLO1 R
14	4032-3	EACF	EMERG. ACTION CONTROL FF'S	88	320-38			EAC3 RW	EAC2 RW	EACI RW	EACO RW	SC-3 RW	SC-2 RW	SC-1 RW	SC-0 RW														
15	4034-5	PSV	PULSE SOURCES (V-POSITIONS)	77,64, 76,85, 79,63	326-16 324-30	ENTJ R	SPSALW W,WV	CLEARH WV	RFTWIST (CCC2) W,WV	SFTWIST (CCCI) W,WV	RMDIA W,WV	SMDIA W,WV	GOPU WV	PCKCKR W,WV	INTI W,WV	INTO W,WV	REOL (SOL) W,WV	CCST W,WV	SCCR W,WV	FSTOP W,WV	ESTOP RW,WV	A5MSB (RESM) W,WV	S5MSR (STBYC) W,WV	RESET W,WV	FCG W,WV	ST-SPB W,WV	STP-SPB RW,WV	ST-SPA W,WV	STP-SPA RW,WV
16	4036-7	MMIF	MISCELLANEOUS MAINT. FF'S	76 63	320-32 326-14	MCII R	SCCT RW	CPDT RW			PTA RW	CCOI RW																	
17	4040-1	MCCD	MCC DATA INSERT	74	328-37	MCC-23 R	MCC-22 R	MCC-21 R	MCC-20 R	MCC-19 R	MCC-18 R	MCC-17 R	MCC-16 R	MCC-15 R	MCC-14 R	MCC-13 R	MCC-12 R	MCC-11 R	MCC-10 R	MCC-9 R	MCC-8 R	MCC-7 R	MCC-6 R	MCC-5 R	MCC-4 R	MCC-3 R	MCC-2 R	MCC-1 R	MCC-0 R
18	4042-2	MAIS	MAINT. INTER RUPT SOURCES	79,90, 49,31	326-14		CPDRM R	CPDEN R	PERF RWC *	SETO RWC *	LTO RWC *	CE RWC *	PURPF (ZI)RWC*	PURMM (ZI)RWC*	TCL RWC *	BPI RWC *	TRI RWC *		PUEI RWC *	PUEE RWC *	SPBT RWC *	SPAT RWC *	PSRRF RWC *	CSRRF RWC *	MMII RWC *	MMIO RWC *	EAI RWC *		MCCI RWC *
19	4044-5	NOIS	NORMAL INTER RUPT SOURCES	79	326-15																	CCC-1 RWC *	CCC-0 RWC *	SPB RWC *	SPBC RWC *	SPA RWC *	SPAC RWC *	J5 RWC *	H5 RWC *
20	4046-7	PEST	PEST CONTROL FF'S	79	328-35		ISPB RWC	ISPA RWC	IINT RWC	IPUEI RWC	IPUEE RWC	IPIT RWC	ISPAT RWC	IPSF RWC	ICSF RWC	ICCC RWC	IJ5 RWC	IH5 RWC											
21	4050-1	ILAF	INTERRUPT LEVEL ACTIVITY FF'S	63	324-30													CSFI RW *	IHO RW *	LAK RW *	LAJ RW *	LAH RW *	LAG RW *	LAF RW *	LAE RW *	LAD RW *	LAC RW *	LAB RW *	LAA RW *
22	4052-3	MCCF	MASTER CONTROL CENTER FF'S	79 74	328-14 328-35		EMPU R	EMPC R	EMCC R	MIN-7 R	MIN-6 R	MIN-5 R	MIN-4 R	MIN-3 R	MIN-2 R	MIN-1 R	MIN-0 R												
23	4054-5	BBTC	BUFFER BUS TEST CONN	74	328-36	TC-23 R	TC-22 R	TC-21 R	TC-20 R	TC-19 R	TC-18 R	TC-17 R	TC-16 R	TC-15 R	TC-14 R	TC-13 R	TC-12 R	TC-11 R	TC-10 R	TC-9 R	TC-8 R	TC-7 R	TC-6 R	TC-5 R	TC-4 R	TC-3 R	TC-2 R	TC-1 R	TC-0 R
24	4056-7	EMC	EMERGENCY MODE CONTROL	80	NONE	DFM23 R	DFMI3 R	MRM23 R	MRMI3 R															EMCK5 R	EMCK4 R	EMCK3 R	EMCK2 R	EMCKI R	EMCKO R
25	4060	ACR	AUXILIARY CONTROL REG.	97	NONE		IPICSE (Z6), RW																						
26	4061	APS	AUXILIARY PULSE SOURCES	97	NONE																								ISAPIU (ZG), W

ACCESS NOTES

R = READABLE VIA READ MEMORY ORDERS.
W = WRITEABLE VIA WRITE MEMORY ORDERS.
C = WRITEABLE VIA CONTROL WRITE OPERATIONS.
* = INDICATES BITS WHICH HAVE WRITE CONTROL (W AND OR C) THAT DIFFERS FROM THE STANDARD METHODS EMPLOYED. THE BITS INVOLVED ARE:
ARO-23, DRO-23, ARI-23 & DRI-23 --- THE LEAST SIGNIFICANT BIT OF THE ADDRESS IS USED AS THE DATA SOURCE.
RCSEC, RPS2EC & RPSIEC --- WHEN ZERO IS WRITTEN, THE ASSOCIATED COUNTER IS RESET. WRITING A ONE HAS NO EFFECT.
ALL WRITEABLE BITS OF MAIS, NOIS & ILAF --- WHEN A ONE IS WRITTEN, THE FLIP FLOP IS RESET. WRITING A ZERO HAS NO EFFECT.

** = FOR W AND C ACCESS, MACR IS ACTUALLY SPLIT INTO TWO PARTS. ADDRESS 4010 GATES INTO BITS 0 - 9 AND ADDRESS 4011 GATES INTO BITS 10 - 21. R ACCESS IS NORMAL. ALL BITS ARE WRITEABLE BY A SINGLE EMMS ORDER.
*** = R ACCESS TO MO & MI READS THE ZERO SIDE OF THESE FF'S.
EMMS = WRITEABLE VIA EMMS ORDERS.
CPDUN = CONTROLLED IN BOTH CC'S SIMULTANEOUSLY VIA TWO UNIPOLAR POINTS.
CPDBI = CONTROLLED SEPARATELY IN EACH CC BY 1 BIPOLAR CPD POINT PER CC.
WV = WRITEABLE VIA WV ORDERS.

EQUIPMENT NOTES

(M) = EXISTS ONLY IN CC'S WHICH HAVE THE M OPTION.
(R) = EXISTS ONLY IN CC'S WHICH HAVE THE R OPTION.
(ZG) = EXISTS ONLY IN CC'S WHICH HAVE THE ZG OPTION.
(ZI) = EXISTS ONLY IN CC'S WHICH HAVE OPTIONS ZI, 43, AND 44.
(305) = ONLY EXISTS IN SOME CC'S, AND IN SUCH CASES, ONLY ON A TEMPORARY BASIS. SEE SD-1A105-01 NOTE 305.

MISCELLANEOUS NOTES

(X...X) = ACTUAL NAME OF FUNCTION USED IN THE CC SD (SUPPLIED ONLY WHEN IT DIFFERS SIGNIFICANTLY FROM THE BIT NAMES USED IN THIS FIGURE).

12-24/25

CC ACCESSIBLE SIGNAL PROCESSOR LOCATIONS FOR READ OPERATIONS

FS	TITLE	GATE LEAD	UNMASKED BUS AND CCDR BIT POSITIONS FOR CC READ OPERATIONS																							OCT CCAR ADDR
			22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
65	SPECIAL CONTROL GROUP NO. 1	CG1UB1									IMS1	INHE1	MCCR1	ECM1	1EMO	1ES1	MCC1	INT1	ASX51	SXS1	ASPS1	SPS1	MNM1A	DIV1	ACT1	0022
66	SPECIAL CONTROL GROUP NO. 2	CG2UB1			FS6 BR231	FS16 PSFF31	FS16 PS231	FS16 PSFF11	FS15 NFF51A	FS15 NFF41A	FS15 NFF31A	FS15 NFF21A	FS15 NFF11A	FS13 IFF41A	FS13 IFF31A	FS13 IFF21A	FS13 IFF11A		PR1	FFA1B	FF51	FF41	FF31	FF21	FF11	0023
64	MATCH CONTROL	MACOUB1												MCV1	MCO1	MCE11	MCE01	MPE21	MPE11	MPE01	MCI11	MCI01	MPI21	MPI11	MPI01	0026
61	CALL STORE BUS CONTROL	CSBCUB1						ROCS0	RICS0	ROCC0	R1CC0	SOCC1	S1CC1	SOCS1	S1CS1	TB11	TBL01	CCBT1	CCBN	CCB01	OL31	MRC1	CBT1	CBA1	CB01	0027
62	PERIPHERAL BUS CONTROL	PBCUB1				BG01	BFGA1	SCA00	AA01	AA11	GB1	FGA1	PFO1	PF11	SCR1	FINH1	OL21	OL11	SCB81	SCBA1	PBMB1	PBMA1	CDMB1	CDMA1	CPDB1	0030
70	SP ERROR SUM. GROUP	ESGUB1									CAM1	PER1	FS43 CPDEM1	FS46 CPDRM1		FS63 CCASWE1	FS63 CCASWI1	MUS1	MEE1	MEI1	ME1	PEE1	PEI1	CSEE1	CSEI1	0031
63	CALL STORE ERROR SUM.	CSEUB1												FS12 RC231	FS12 RC121A	FS12 SPAW1	FS12 DR1	CEOV1	CSEC41	CSEC31	CSEC21	CSEC11	CSEC01	SPASW1	WPF1	0024
42	CPD DIAG ECHO REG	DERUB1	ASWS1	FS45 T231	PCC1	PCB1	PCA1	MCE1	ASWCPD1	EXBR71	EXBR61	EXBR51	EXBR41	EXBR31	EXBR21	EXBR11	EXBR01	EXAR71	EXAR61	EXAR51	EXAR41	EXAR31	EXAR21	EXAR11	EXAR01	0025
59	CRITICAL ADDRESS REG	CARUB1										CAR131	CAR121	CAR111	CAR101	CAR091	CAR081	CAR071	CAR061	CAR051	CAR041	CAR031	CAR021	CAR011	CAR001	0032
19	CALL STORE ADDRESS REG	ARUB1									AR141	AR131	AR121	AR111	AR101	AR091	AR081	AR071	AR061	AR051	AR041	AR031	AR021	AR011	AR001	0004
6	BUFFER REGISTER	BRUB1	BR221	BR211	BR201	BR191	BR181	BR171	BR161	BR151	BR141	BR131	BR121	BR111	BR101	BR091	BR081A	BR071A	BR061A	BR051	BR041A	BR031A	BR021A	BR011A	BR001A	0005
35	F REGISTER	FRUB1	FR221	FR211	FR201	FR191	FR181	FR171	FR161	FR151	FR141	FR131	FR121	FR111	FR101	FR091	FR081	FR071	FR061	FR051	FR041	FR031	FR021	FR011	FR001	0006
27	JUMP REGISTER	JRUB1	J221	J211	J201	J191	J181	J171	J161	J151	J141	J131	J121	J111	J101	J091	J081	J071	J061	J051	J041	J031	J021	J011	J001	0007
29	ACCUMULATOR REG (K REG)	KRUB1	KR221	KR211	KR201	KR191	KR181	KR171	KR161	KR151	KR141	KR131	KR121	KR111	KR101	KR091	KR081	KR071	KR061	KR051	KR041	KR031	KR021	KR011	KR001	0010
24	LOGIC REG (L REG)	LRUB1	LR221	LR211	LR201	LR191	LR181	LR171	LR161	LR151	LR141	LR131	LR121	LR111	LR101	LR091	LR081	LR071	LR061	LR051	LR041	LR031	LR021	LR011	LR001	0011
47	PERIPHERAL ADDRESS REG (P REG)	PRUB1	PR221	PR211	PR201	PR191	PR181	PR171	PR161	PR151	PR141	PR131	PR121A	PR111	PR101	PR091	PR081C	PR071B	PR061B	PR051B	PR041B	PR031B	PR021B	PR011	PR001	0012
26	Q REGISTER	QRUB1	QR221	QR211	QR201	QR191	QR181	QR171	QR161	QR151	QR141	QR131	QR121	QR111	QR101	QR091	QR081	QR071	QR061	QR051	QR041	QR031	QR021	QR011	QR001	0013
28	X REGISTER	XRUB1	XR221	XR211	XR201	XR191	XR181	XR171	XR161	XR151	XR141	XR131	XR121	XR111	XR101	XR091	XR081	XR071	XR061	XR051	XR041	XR031	XR021	XR011	XR001	0014
45	Y REGISTER	YRUB1	Y221	Y211	Y201	Y191	Y181	Y171	Y161	Y151	Y141	Y131	Y121	Y111	Y101	Y091	Y081	Y071	Y061	Y051	Y041	Y031	Y021	Y011	Y001	0015
60	INTERNAL MATCH REG	MIUB1	MRI221	MRI211	MRI201	MRI191	MRI181	MRI171	MRI161	MRI151	MRI141	MRI131	MRI121	MRI111	MRI101	MRI091	MRI081	MRI071	MRI061	MRI051	MRI041	MRI031	MRI021	MRI011	MRI001	0016
60	EXTERNAL MATCH REG	MEUB1	MRE221	MRE211	MRE201	MRE191	MRE181	MRE171	MRE161	MRE151	MRE141	MRE131	MRE121	MRE111	MRE101	MRE091	MRE081	MRE071	MRE061	MRE051	MRE041	MRE031	MRE021	MRE011	MRE001	0017
5	INSTRUCTION REG	IRUB1	I221	I211	I201	I191	I181	I171	I161	I151	I141	I131	I121	I111	I101	I091	I081	I071	I061	I051	I041	I031	I021	I011	I001	0020
20	ADDRESS STORAGE REG	ASRUB1									AS141	AS131	AS121	AS111	AS101	AS091	AS081	AS071	AS061	AS051	AS041	AS031	AS021	AS011	AS001	0021
74	SPECIAL CONTROL GROUP NO. 3	CG3UB1											IASWS	DMR1	INHPE	DCM1	F108R1	CPDS70	CPDS60	CPDS50	CPDS40	CPDS30	CPDS20	CPDS10	CPDS00	0033

* EXCEPTIONS NOTED ABOVE LEAD DESIGNATIONS.

CC ACCESSIBLE SIGNAL PROCESSOR LOCATIONS FOR WRITE OPERATIONS

FS	TITLE	GATE LEAD	CCDR BIT POSITIONS FOR CC WRITE IN CONTROL LOCATIONS																						CCAR ADDR IN OCT
			22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
65	SPECIAL CONTROL GROUP NO.1	CCCG11	RIMS	RINHE	SIMS SINHE	RECM	R1EHO	R1ES1	S1ES1	RNSQ	RISQ	REIR	RPSQ RPR23	RINT	RASXS	RSXS	SSXS	RASPS	SASPS	RNNM	SNNM	RD1V	SD1V	RACT	SACT	0022
66	SPECIAL CONTROL GROUP NO.2	CCCG21																	RPR	SPR	SFF5	SFF4	SFF3	SFF2	SFF1	0023
60	MATCH CONTROL ACTIVE SP - NOTE 1	CCMCA1												SMCE1	SMCE0	SMPE2	SMPE1	SMPE0	SMCV	SMCO	SMCI1	SMCI0	SMPI2	SMPI1	SMPI0	0026
64	MATCH CONTROL STANDBY SP - NOTE 1	CCMCS1										SMCV	SMCO	SMCI1	SMCI0	SMPI2	SMPI1	SMPI0			SMCE1	SMCE0	SMPE2	SMPE1	SMPE0	0026
61	CALL STORE BUS CONTROL	CCCSBC1				RTBL1	STBL1	RTBL0	STBL0	RCCBT	SCCBT	RCCBA	SCCBA	RCCB0	SCCB0	ROL3	SOL3	RMRC	SMRC	RCBT	SCBT	RCBA	SCBA	RCB0	SCB0	0027
62	PERIPHERAL BUS CONT	CCPBC						ROL2	SOL2	ROL1	SOL1	RSCBB	SSCBB	RSCBA	SSCBA	RPBMB	SPBMB	RPBMA	SPBMA	RCDMB	SCDMB	RCDMA	SCDMA	RCPDB	SCPDB	0030
63	CALL STORE ERROR SUM	REEC	SEE NOTE 2																							0024
70	SP ERROR SUMMARY ACTIVE SP	CCESG1														RRCS0	RMUS	RCAM	RPER		RMEI RME	RPEE	RPEI	RCSEE	RCSEI	0031
70	SP ERROR SUMMARY STANDBY SP	CCESG1														RRCS0	RMUS	RCAM	RPER		RMEI RME	RPEI	RPEE	RCSEI	RCSEE	0031
5	INSTRUCTION REG	CCIR1	SI22	SI21	SI20	SI19	SI18	SI17	SI16	SI15	SI14	SI13	SI12	SI11	SI10	SI09	SI08	SI07	SI06	SI05	SI04	SI03	SI02	SI01	SI00	0020
74	SPECIAL CONTROL GROUP NO. 3	CCCG31											SIASWS	SDMR	SINHPE		SF10BR	CPDS7	CPDS6	CPDS5	CPDS4	CPDS3	CPDS2	CPDS1	CPDS0	0033

NOTES:

1. THE MATCH CONTROL CIRCUIT INCORPORATES SINGLE-TO-DOUBLE RAIL CONVERSION.
2. A CC REQUEST FOR A WRITE OPERATION IN THIS GROUP WILL RESET THE COUNTER AND THE OVERFLOW F/F. THIS IS DONE INDEPENDENTLY OF THE CCDR DATA FIELD.
3. THE OPERATIONAL REGISTERS ARE WRITTEN INTO BY CC VIA THE MASKEL BUS. THE CCDR AND THE REGISTERS HAVE A BIT-BY-BIT CORRESPONDENCE.

SECTION 13

NO. 1A ESS PROCESSOR

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NO. 1A ESS PROGRAM/CALL STORE ADDRESS RANGE

ADDRESS	INFO BLK	K CODE 256K STORE	K CODE 64K STORE	ADDRESS	INFO BLK	K CODE 256K STORE	K CODE 64K STORE	ADDRESS	INFO BLK	K CODE 256K STORE	K CODE 64K STORE
00000000 00177777	0	0	0	02600000 02777777	13	10	13	05400000 05577777	26	24	26
00200000 00377777	1	0	1	03000000 03177777	14	14	14	05600000 05777777	27	24	27
00400000 00577777	2	0	2	03200000 03377777	15	14	15	06000000 06177777	30	30	30
00600000 00777777	3	0	3	03400000 03577777	16	14	16	06200000 06377777	31	30	31
01000000 01177777	4	4	4	03600000 03777777	17	14	17	06400000 06577777	32	30	32
01200000 01377777	5	4	5	04000000 04177777	20	20	20	06600000 06777777	33	30	33
01400000 01577777	6	4	6	04200000 04377777	21	20	21	07000000 07177777	34	34	34
01600000 01777777	7	4	7	04400000 04577777	22	20	22	07200000 07377777	35	34	35
02000000 02177777	10	10	10	04600000 04777777	23	20	23	07400000 07577777	36	34	36
02200000 02377777	11	10	11	05000000 05177777	24	24	24	07600000 07777777	37	34	37
02400000 02577777	12	10	12	0520000C 05377777	25	24	25				

NOTE:
Program stone starts at K code 20 (ADR 4000000) for Generic 1AE6 and earlier

REPT: LEV @ ADR MFNUM = MAINT FILE MICON = INT CTRL

LV = INT D0 = SR DATA D1 = FR DATA 1 D2 = FR DATA 2 D3 = 0

PIDENT ACTION TAKEN

DATA: C-LEVEL

1	IN1FR	IN1GR	IN1JR	IN1KR	IN1LR	IN1XR
2	IN1YR	IN1ZR	IN1BR	IN1CAR	IN1ILA	IN1SCA
3	IN1SDA	IN1SPA	IN1CSC	IN1INS	IN1MSR	IN1MMR
4	IN1MIO	ST1MEO	IN1CMO	IN1MI1	ST1ME1	IN1CM1
5	ST1MIO	IN1MEO	ST1CMO	ST1MI1	IN1ME1	ST1CM1
6	ST1SCA	ST1SDA	ST1SPA	ST1BR		

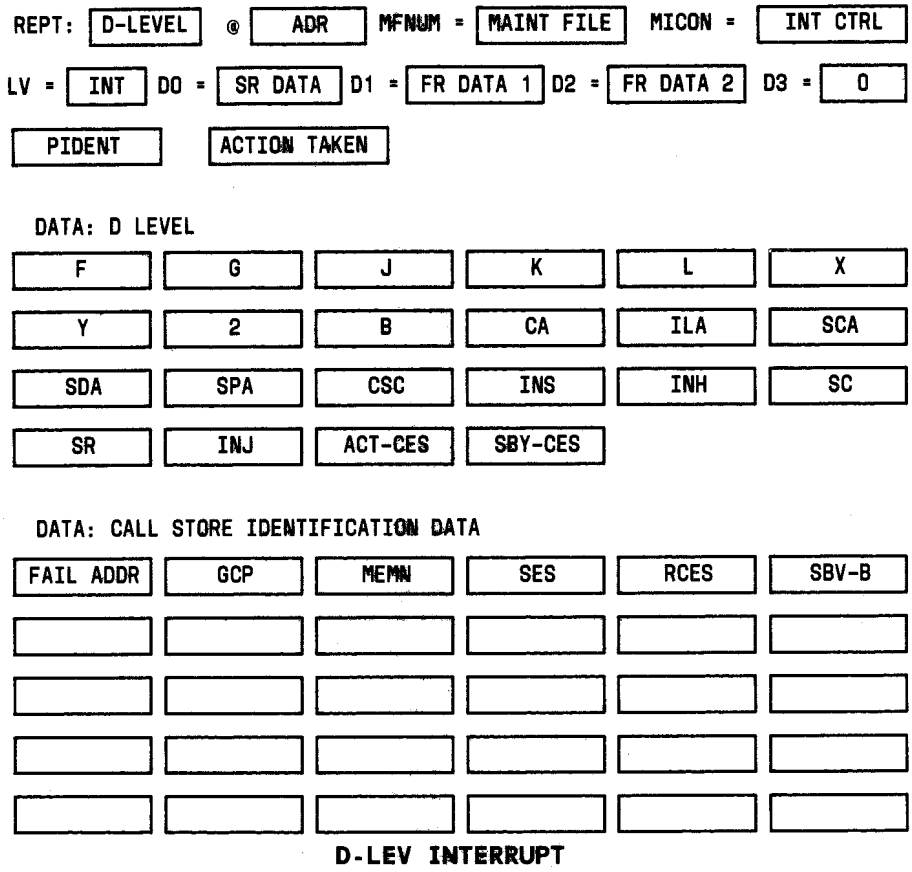
DATA: ACTIVE CC REGISTERS

1	AC1LR	AC1LRS	AC1FR	AC1FRS	AC1GR	AC1GRS
2	AC1KR	AC1KRS	AC1XR	AC1XRS	AC1YR	AC1YRS
3	AC1ZR	AC1ZRS	AC1JR	AC1JRS	AC1ER	AC1PRM
4	AC1PRL	AC1RR	AC1SR	AC1BCO	AC1MIO	AC1MEO
5	AC1CMO	AC1BC1	AC1MI1	AC1ME1	AC1CM1	AC1MMR
6	AC1MSR	AC1MOR	AC1M1R	AC1MCP	AC1MCO	AC1MCD
7	AC1CES	AC1ILA	AC1ILR	AC1INH	AC1INJ	AC1INS
8	AC1BCS	AC1PES	AC1PCR	AC1CSC	AC1PSC	AC1MDF
9	AC1DE	AC1SC	AC1LPA	AC1UPA	AC1ABK	AC1SVG
10	AC1AAS	AC1AMB	AC1AMC	AC1RIG	AC1RQG	AC1ARR
11	AC1AWF	AC1EVG	AC1AMA	AC1AWS	AC1EBG	AC1VRG

DATA: STANDBY CC REGISTERS

1	ST1LR	ST1LRS	ST1FR	ST1FRS	ST1GR	ST1GRS
2	ST1KR	ST1KRS	ST1XR	ST1XRS	ST1YR	ST1YRS
3	ST1ZR	ST1ZRS	ST1JR	ST1JRS	ST1ER	ST1PRM
4	ST1PRL	ST1RR	ST1SR	ST1BCO	ST1MIO	ST1MCO
5	ST1CMO	ST1BC1	ST1MI1	ST1ME1	ST1CM1	ST1MMR
6	ST1MSR	ST1MOR	ST1M1R	ST1MCP	ST1MCO	ST1MCD
7	ST1CES	ST1ILA	ST1ILA	ST1INH	ST1INJ	ST1INS
8	ST1BCS	ST1PES	ST1PCR	ST1CSC	ST1PSC	ST1MDF
9	ST1DE	ST1SC	ST1LPA	ST1UPA	ST1ABK	ST1SVG
10	ST1AAS	ST1AMB	ST1AMC	ST1RIG	ST1RQG	ST1ARR
11	ST1AWF	ST1EVG	ST1AMA	ST1AWS	ST1EBG	ST1VRG

C-LEV INTERRUPT



D-LEV INTERRUPT

REPT: E-LEVEL @ ADR MFNUM = MAINT FILE MICON = INT CTRL

LV = INT D0 = SR DATA D1 = FR DATA 1 D2 = FR DATA 2 D3 = 0

PIDENT ACTION TAKEN

DATA: E LEVEL

F	G	J	K	L	X
Y	2	B	CA	ILA	SCA
SDA	SPA	CSC	INS	INH	SC
SR	INJ	ACT-CES	SBY-CES		

DATA: PROGRAM STORE IDENTIFICATION DATA

FAIL ADDR	GCP	MEMN	SES	RCES	ABL
ABR	SBY-B	SABL	SABR		

E-LEV INTERRUPT

Section 14

GENERAL

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HEXIDECIMAL - DECIMAL CONVERSION

HEX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
2	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
3	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
4	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79
5	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
6	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111
7	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127
8	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143
9	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159
A	160	161	162	163	164	165	166	167	168	169	170	171	712	173	174	175
B	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191
C	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207
D	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223
E	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239
F	240	241	242	243	244	245	256	247	248	249	250	251	252	253	254	255

OCTAL - DECIMAL INTEGER CONVERSION TABLE

	0	1	2	3	4	5	6	7
0000	0000	0001	0002	0003	0004	0005	0006	0007
0010	0008	0009	0010	0011	0012	0013	0014	0015
0020	0016	0017	0018	0019	0020	0021	0022	0023
0030	0024	0025	0026	0027	0028	0029	0030	0031
0040	0032	0033	0034	0035	0036	0037	0038	0039
0050	0040	0041	0042	0043	0044	0045	0046	0047
0060	0048	0049	0050	0051	0052	0053	0054	0055
0070	0056	0057	0058	0059	0060	0061	0062	0063
0100	0064	0065	0066	0067	0068	0069	0070	0071
0110	0072	0073	0074	0075	0076	0077	0078	0079
0120	0080	0081	0082	0083	0084	0085	0086	0087
0130	0088	0089	0090	0091	0092	0093	0094	0095
0140	0096	0097	0098	0099	0100	0101	0102	0103
0150	0104	0105	0106	0107	0108	0109	0110	0111
0160	0112	0113	0114	0115	0116	0117	0118	0119
0170	0120	0121	0122	0123	0124	0125	0126	0127
0200	0128	0129	0130	0131	0132	0133	0134	0135
0210	0136	0137	0138	0139	0140	0141	0142	0143
0220	0144	0145	0146	0147	0148	0149	0150	0151
0230	0152	0153	0154	0155	0156	0157	0158	0159
0240	0160	0161	0162	0163	0164	0165	0166	0167
0250	0168	0169	0170	0171	0172	0173	0174	0175
0260	0176	0177	0178	0179	0180	0181	0182	0183
0270	0184	0185	0186	0187	0188	0189	0190	0191
0300	0192	0193	0194	0195	0196	0197	0198	0199
0310	0200	0201	0202	0203	0204	0205	0206	0207
0320	0208	0209	0210	0211	0212	0213	0214	0215
0330	0216	0217	0218	0219	0220	0221	0222	0223
0340	0224	0225	0226	0227	0228	0229	0230	0231
0350	0232	0233	0234	0235	0236	0237	0238	0239
0360	0240	0241	0242	0243	0244	0245	0246	0247
0370	0248	0249	0250	0251	0252	0253	0254	0255

	0	1	2	3	4	5	6	7
0400	0256	0257	0258	0259	0260	0261	0262	0263
0410	0264	0265	0266	0267	0268	0269	0270	0271
0420	0272	0273	0274	0275	0276	0277	0278	0279
0430	0280	0281	0282	0283	0284	0285	0286	0287
0440	0288	0289	0290	0291	0292	0293	0294	0295
0450	0296	0297	0298	0299	0300	0301	0302	0303
0460	0304	0305	0306	0307	0308	0309	0310	0311
0470	0312	0313	0314	0415	0316	0317	0318	0319
0500	0320	0321	0322	0323	0324	0325	0326	0327
0510	0328	0329	0330	0331	0332	0333	0334	0335
0520	0336	0337	0338	0339	0340	0341	0342	0343
0530	0344	0345	0346	0347	0348	0349	0350	0351
0540	0352	0353	0354	0355	0356	0357	0358	0359
0550	0360	0361	0362	0363	0364	0365	0366	0367
0560	0368	0369	0370	0371	0372	0373	0374	0375
0570	0376	0377	0378	0379	0380	0381	0382	0383
0600	0384	0385	0386	0387	0388	0389	0390	0391
0610	0392	0393	0394	0395	0396	0397	0398	0399
0620	0400	0401	0402	0403	0404	0405	0406	0407
0630	0408	0409	0410	0411	0412	0413	0414	0415
0640	0416	0417	0418	0419	0420	0421	0422	0423
0650	0424	0425	0426	0427	0428	0429	0430	0431
0660	0432	0433	0434	0435	0436	0437	0438	0439
0670	0440	0441	0442	0443	0444	0445	0446	0447
0700	0448	0449	0450	0451	0452	0453	0454	0455
0710	0456	0457	0458	0459	0460	0461	0462	0463
0720	0464	0465	0466	0467	0468	0469	0470	0471
0730	0472	0473	0474	0475	0476	0477	0478	0479
0740	0480	0481	0482	0483	0484	0485	0486	0487
0750	0488	0489	0490	0491	0492	0493	0494	0495
0760	0496	0497	0498	0499	0500	0501	0502	0503
0770	0504	0505	0506	0507	0508	0509	0510	0511

OCTAL - DECIMAL INTEGER CONVERSION TABLE

	0	1	2	3	4	5	6	7
1000	0512	0513	0514	0515	0516	0517	0518	0519
1010	0520	0521	0522	0523	0524	0525	0526	0527
1020	0528	0529	0530	0531	0532	0533	0534	0535
1030	0536	0537	0538	0539	0540	0541	0542	0543
1040	0544	0545	0546	0547	0548	0549	0550	0551
1050	0552	0553	0554	0555	0556	0557	0558	0559
1060	0560	0561	0562	0563	0564	0565	0566	0567
1070	0568	0569	0570	0571	0572	0573	0574	0575
1100	0576	0577	0578	0579	0580	0581	0582	0583
1110	0584	0585	0586	0587	0588	0589	0590	0591
1120	0592	0593	0594	0595	0596	0597	0598	0599
1130	0600	0601	0602	0603	0604	0605	0606	0607
1140	0608	0609	0610	0611	0612	0613	0604	0615
1150	0616	0617	0618	0619	0620	0621	0622	0623
1160	0624	0625	0626	0627	0628	0629	0630	0631
1170	0632	0633	0634	0635	0636	0637	0638	0639
1200	0640	0641	0642	0643	0644	0645	0646	0647
1210	0648	0649	0650	0651	0652	0653	0654	0655
1220	0656	0657	0658	0659	0660	0661	0662	0663
1230	0664	0665	0666	0667	0668	0669	0670	0671
1240	0672	0673	0674	0675	0676	0677	0678	0679
1250	0680	0681	0682	0683	0684	0685	0686	0687
1260	0688	0689	0690	0691	0692	0693	0694	0695
1270	0696	0697	0698	0699	0700	0701	0702	0703
1300	0704	0705	0706	0707	0708	0709	0710	0711
1310	0712	0713	0714	0715	0716	0717	0718	0719
1320	0720	0721	0722	0723	0724	0725	0726	0727
1330	0728	0729	0730	0731	0732	0733	0734	0735
1340	0736	0737	0738	0739	0740	0741	0742	0743
1350	0744	0745	0746	0747	0748	0749	0750	0751
1360	0752	0753	0754	0755	0756	0757	0758	0759
1370	0760	0761	0762	0763	0764	0765	0766	0767

	0	1	2	3	4	5	6	7
1400	0768	0769	0770	0771	0772	0773	0774	0775
1410	0776	0777	0778	0779	0780	0781	0782	0783
1420	0784	0785	0786	0787	0788	0789	0790	0791
1430	0792	0793	0794	0795	0796	0797	0798	0799
1440	0800	0801	0802	0803	0804	0805	0806	0807
1450	0808	0809	0810	0811	0812	0813	0814	0815
1460	0816	0817	0818	0819	0820	0821	0822	0823
1470	0824	0825	0826	0827	0828	0829	0830	0831
1500	0832	0833	0834	0835	0836	0837	0838	0839
1510	0840	0841	0842	0843	0844	0845	0846	0847
1520	0848	0849	0850	0851	0852	0853	0854	0855
1530	0856	0857	0858	0859	0860	0861	0862	0863
1540	0864	0865	0866	0867	0868	0869	0870	0871
1550	0872	0873	0874	0875	0876	0877	0878	0879
1560	0880	0881	0882	0883	0884	0885	0886	0887
1570	0888	0889	0890	0891	0892	0893	0894	0895
1600	0896	0897	0898	0899	0900	0901	0902	0903
1610	0904	0905	0906	0907	0908	0909	0910	0911
1620	0912	0913	0914	0915	0916	0917	0918	0919
1630	0920	0921	0922	0923	0924	0925	0926	0927
1640	0928	0929	0930	0931	0932	0933	0934	0935
1650	0936	0937	0938	0939	0940	0941	0942	0943
1660	0944	0945	0946	0947	0948	0949	0950	0951
1670	0952	0953	0954	0955	0956	0957	0958	0959
1700	0960	0961	0962	0963	0964	0965	0966	0967
1710	0968	0969	0970	0971	0972	0973	0974	0975
1720	0976	0977	0978	0979	0980	0981	0982	0983
1730	0984	0985	0986	0987	0988	0989	0990	0991
1740	0992	0993	0994	0995	0996	0997	0998	0999
1750	1000	1001	1002	1003	1004	1005	1006	1007
1760	1008	1009	1010	1011	1012	1013	1014	1015
1770	1016	1017	1018	1019	1020	1021	1022	1023

UNIT TYPES AND UNIT TYPE NUMBERS

No. 1A ESS

Unit Type No.	Unit Type
0	Ground Cross Detector
1	Peripheral Unit-Pseudo Unit Type
2	Coded Enable Peripheral Unit Bus- Pseudo Unit Type
3	Not Used in No. 1A ESS
4	Not Used in No. 1A ESS
5	Master Scanner
6	Central Pulse Distributor
7	Not Used in No. 1A ESS
8	Trunk and Line Test Circuit
9	Line Scanner, LLN 16-31 (LSC)
10	Line Switch Controller, LLN 16-31 (LSW)
11	Line Junctor Switch Controller, LLN 16-31 (LJSW)
12	Line Scanner, LLN 00-15 (LSC)
13	Line Switch Controller, LLN 00-15 (LSW)
14	Line Junctor Switch Controller, LLN 00-15 (LJSW)
15	Trunk Junctor Switch Controller
16	Trunk Switch Controller
17	Junctor Scanner
18	Junctor Signal Distributor
19	Universal Trunk Scanner
20	Universal Trunk Signal Distributor
21	Miscellaneous Trunk Frame - Signal Distributor (Miscellaneous or Supplementary)
22	Unassigned
23	Recorded Announcement Frame
24	Office Alarm Circuit
25	Not Used in No. 1A ESS
26	Ringing and Tone Frame
27	Unassigned
28	Power Distributing Frame
29	Centrex Data Link
30	Not Used in No. 1A ESS
31	Unassigned
32	Miscellaneous Power Frame
33	Miscellaneous Frame
34	Miscellaneous Building Alarm - Major
35	Miscellaneous Building Alarm - Minor
36	Route Transfer Key
37	PBX Key
38	Emergency Manual Line Circuit
39	Multiline Service Observing
40	Carrier Group Alarm
41	Miscellaneous Toll Alarm - Major
42	Miscellaneous Toll Alarm - Minor
43	Miscellaneous Service Alarm - Minor
44	Miscellaneous Special Alarm - Major
45	Miscellaneous Special Alarm - Minor
46	Network Management (NMGT)

UNIT TYPES AND UNIT TYPE NUMBERS

No. 1A ESS

Unit Type No.	Unit Type
47	Trunk Make Busy Keys
48	AC Distributing Circuit
49	Toll Miscellaneous Panel
50	Automatic Identified Outward Dialing (AIOD)
51	Member No. 0 - Precut/Postcut Lamp for Cutover Signaling Circuit
52	Not Used in No. 1A ESS
53	Automatic Transmission Measuring System (ATMS)
54	Terminal Make Busy Keys (MLH)
55	Queuing for Trunks and Lines
56	Dynamic Overload Control Transmitter (DOCX)
57	Data Terminals (CCISDT)
58	Data Terminals (CCTSDT)
61	Peripheral Unit Controller (PUC)
62	Cutover Test Lines
63	Used by MSN Translator for MEMN >127
66	Scanner Answer Bus
67	Scanner Row
68	Supplementary Signal Distributor
96	Peripheral Unit - (Pseudo Unty)
97	Coded Enable PUB - (Pseudo Unty)
98	CPD Enable Address Bus (Pseudo Unty)
99	PU Enable Address Bus (Pseudo Unty)
100	Scanner Answer Bus (Pseudo Unty)
101	Scanner Row (Pseudo Unty)
102	SSD (Pseudo Unty)
107	Common Processor Panel
108	Maintenance Control Display
109	System Status Logic
110	Remote Access Interface Ckt
111	Power Distribution Frame
112	Peripheral Unit Bus
113	Unassigned
114	Auxiliary Unit Bus
115	Call Store Bus
116	Program Store Bus
117	I/O Unit Selector
118	Data Link Controller
119	Tape Unit Controller
120	Data Unit Selector
121	Processor Peripheral-Interface
122	File Store
123	Call Store
124	Program Store
125	Central Control
126	Reserved for Growth
127	Not to Be Used

#1A ESS UNIT TYPES & UNIT TYPE NUMBERS

NUMBER	UNIT TYPE (ACRONYM)
50	Automatic Identified Outward Dialing (AIOD)
55	Automatic Queue for Trunks and Lines (AQTL)
114	Auxiliary Unit Bus
123	Call Store
115	Call Store Bus
40	Carrier Group Alarm (CGA)
125	Central Control
6	Central Pulse Distributor (CPD)
64	CPD Enable Address Bus
29	Centrex Data Link Frame (CDLF)
2	Coded Enable Peripheral Unit Bus
23	Common Systems Recorded Announcement Frame (CSRAF)
118	Data Link Controller
57	Data Terminals (CCISDT)
58	Data Terminals (CCTSDT)
120	Data Unit Selector
38	Emergency Manual Line Circuit (EML)
122	File Store
0	Ground Cross Detector (GCD)
21	HILO Misc Trk Supplementary Signal Distributor (HMTSD)
19	HILO Universal Trunk Scanner (HUTSC)
20	HILO Universal Trunk Signal Distributor (HUTSD)
117	Input/Output Unit Selector
17	Junctor Scanner (JSC)
18	Junctor Signal Distributor (JSD)
48	LEN Contactor List (LENLST)
11	Line Junctor Switch Controller, LLN 16-31 (LJSW)
14	Line Junctor Switch Controller, LLN 00-15 (LJSW)
9	Line Scanner, LLN 16-31 (LSC)
12	Line Scanner, LLN 00-15 (LSC)
10	Line Switch Controller, LLN 16-31 (LSW)
13	Line Switch Controller, LLN 00-15 (LSW)
8	Manual Trunk Test Circuit (MTT)
5	Master Scanner (MS)
34	Miscellaneous Building Alarm - Major (MBAMJ)
35	Miscellaneous Building Alarm - Minor (MBAMN)
33	Miscellaneous Frame (MF)
32	Miscellaneous Power Frame (MPF)
43	Miscellaneous Service Alarm - Minor (SRVALM)
44	Miscellaneous Special Alarm - Major (SPLAMJ)
45	Miscellaneous Special Alarm - Minor (SPLAMN)
41	Miscellaneous Toll Alarm - Major (TOLLMJ)
42	Miscellaneous Toll Alarm - Minor (TOLLMN)
39	Multi-line Service Observing (SERVOB)

#1A ESS UNIT TYPES & UNIT TYPE NUMBERS

NUMBER	UNIT TYPE (ACRONYM)
46	Network Management, MEMN = 0, (NMGT)
56	Ntwk Mgmt Receiver Attachment Delay Report, MEMN = 1, (RADR)
56	Ntwk Mgmt Indicator Circuit, MEMN = 2, (NMGTIN)
56	Ntwk Mgmt Maintenance, MEMN = 3, (NMGTMT)
56	Ntwk Mgmt MC3 Office Codes, MEMN = 4, (DOCMG)
56	Ntwk Mgmt MC1 and MC2 Office Codes, MEMN = 5, (DOCMC)
56	Ntwk Mgmt DOC Signal Acknowledgment, MEMN = 6-9, (DOCACK)
56	Ntwk Mgmt Dynamic Overload Control Signals, MEMN = 10-17
56	Ntwk Mgmt HILO RADR, MEMN = 16, (HRADR)
39	Number 6 PBX Service Observing (SERVOB)
24	Office Alarm Circuit (OFFALM)
1	Peripheral Unit
112	Peripheral Unit Bus
61	Peripheral Unit Controller (PUCDCT)
61	Peripheral Unit Controller (PUCDL)
65	Peripheral Unit Enable Address Bus
54	Position Make Busy Key (PMBKEY)
111	Power Conversion Distributing Frame
28	Power Distributing Frame (PDF)
121	Processor - Peripheral Interface
124	Program Store
116	Program Store Bus
23	Recorded Announcement Frame (RECANN)
37	Remote Make Busy and Stop Hunt Keys (PBXKEY)
53	Remote Office Test Line (ROTL/ROTLIT)
26	Ringing and Tone Plant (RG TN)
36	Route Transfer Keys (RTKEY)
66	Scanner Answer Bus
67	Scanner Row
51	Special Applique for Remote SD Operation (SPCAPL)
21	Supplementary Signal Distributor (MTF SD/CMT SD)
68	Supplementary Signal Distributor
8	Supplementary Trunk Test Panel, MEMN > 0, (STTP/STT)
119	Tape Unit Controller
49	Toll Miscellaneous Panel (TMP)
8	Trunk and Line Test Panel, MEMN = 0, (TLTP)
15	Trunk Junctor Switch Controller (TJSW)
47	Trunk Make Busy Key (TMBKEY)
16	Trunk Switch Controller (TSW)
19	Universal Trunk Scanner (UTSC/MUTSC)
20	Universal Trunk Signal Distributor (UTSD/MUTSD)

TABLE OF UNIT TYPES AND UNIT TYPE NUMBERS
NO. 1 ESS 2-WIRE

Unit Type No.	Unit Type
0	Traffic Data Sender (TDS) Mem. NO. 000, Ground Cross Detector (GCD) Mem. NO. 001 (Built in MSN Tran. Only)
1	CC
2	PS
3	CS
4	Signal Processor (Comm A)
5	Master Scanner
6	CPD
7	MCC Control and Display
8	MCC Line and Trunk Panel (MEMN=0), or Supplementary Trunk Test Circuit (MEMN > 0)
9	AMA Recorder
10	TTY TR Unit
11	Memory Card Writer
12	Line Scanner
13	Line Switch Controller
14	Line Junctor Switch Controller
15	Trunk Junctor Switch Controller
16	Trunk Switch Controller
17	Junctor Scanner
18	Junctor Signal Distributor
19	Universal Trunk Scanner
20	Universal Trunk Signal Distributor
21	Misc Trunk Frame - Signal Distributor (Miscellaneous or Supplementary)
22	Unassigned
23	Recorded Announcement Frame
24	Office Alarm Circuit
25	Signal Processor (Comm A) Call Store
26	Ringing and Tone Frame
27	Unassigned
28	Power Distributing Frame
29	Centrex Data Link
30	Service Link Network
31	Unassigned
32	Miscellaneous Power Frame
33	Miscellaneous Frame

TABLE OF UNIT TYPES AND UNIT TYPE NUMBERS
NO. 1 ESS 2-WIRE

Unit Type No.	Unit Type
34	Miscellaneous Building Alarm - Major
35	Miscellaneous Building Alarm - Minor
36	Route Transfer Keys
37	PBX Keys
38	Emergency Manual Line Circuit
39	Multiline Service Observing (MEMN = 0 - 3) or No. 6 PBX SO (MEMN > 3)
40	Carrier Group Alarm
41	Miscellaneous Toll Alarm - Major
42	Miscellaneous Toll Alarm - Minor
43	Miscellaneous Service Alarm - Minor
44	Miscellaneous Special Alarm - Major
45	Miscellaneous Special Alarm - Minor
46	Network Management (NMGT)
47	Trunk Make-Busy Keys
48	Contactor List
49	Toll Miscellaneous Panel
50	Automatic Identified Outward Dialing
51	Member No. 0 - Precut/Postcut Lamp for Cutover Member No. 1 - Calls Waiting and CAMA Suspension Signaling Circuit
52	Data Link Circuit
53	Automatic Transmission Measuring System (ATMS)
54	Terminal Make-Busy Keys (MLH)
55	Queuing for Trunks and Lines
56	Dynamic Overload Control Transmitter (DOCX)
57	Data Terminal Frame (DTF)
58	Data Terminal (DTRM)
59	Unassigned
60	Processor Interface Unit (PI)
62	Cutover Test Lines
63	Unassigned

1ATS

PAGING, TRANSLATIONS,
RESIDENT PROGRAMS
MEMORY LOCATION

SYMBOLIC = SY7DSTAT ADDRESS = 2200 REL 0

BIT

0	TDA on FS1
1	" on FS0
2	" on core
3	PERIPHERAL PDA on FS1
4	" " on FS0
5	" " on core
6	PROCESSOR PDA on FS1
7	" " on FS0
8	" " on core
9	PERIPHERAL PROGRAMS on FS1
10	" " on FS0
11	" " on core
12	FS1 is paged
13	FS0 is paged
14	Not Used
15 - 23	Reinitialization Code = 462

If system fails write symbolic address SY7DSTAT to the information desired, and interrupt with a soft A.

EXAMPLES:

Input:

REL 0

SET 2200 = 46277774 No TDA
= 46222222 Everything on FS0
= 46211111 Everything on FS1

COMMON ESS WORD FORMATS

CGN - Console Group Number

22 — 7	6 — 5	4 — 2	1 — 0
	FR	LINK	CSI

CPDN - Central Pulse Distributor Number

22 — 14	13 — 11	10 — 8	7 — 5	4 — 3	2	0
	GROUP	ROW	COL	PAIR	CPD	HALF

DLN - Data Link Number

22 — 5	4 — 3	2 — 0
	FR	LINK

ENABLE Information

22 — 20	19 — 17	16 — 15	14	13 — 11	10	9 — 0
GROUP	ROW	COL	PUB	PAIR	CPD	

JCN - Junctor Circuit Number

22 — 13	12 — 8	7	6 — 3	2 — 1	0
	FRAME	BAY	HMP-1	VG	CKT

COMMON ESS WORD FORMATS

DCT - Peripheral Equipment Number (PTW)

22	21	20	19	18	17	16	15	10	9	8	1	0
1	1	0	A	0	0	0	B		C	D		0

A = DCT Frame Indicator (= 1)
B = Frame Number/2
C = DCT Frame Half
D = Trunk Circuit Number

DCT - Trunk Circuit Number (TCN)

22	15	14	9	8	7	0
		A		B	C	

DCT - Trunk Scanner Number (TSN)

22	16	15	10	9	8	1	0
		A		B	C		D

DCT - Trunk Distributor Number (TDN)

22	17	16	11	10	9	2	1	0
		A		B	C		0	0

A = Frame Number/2
B = DCT Frame Half
C = Trunk Circuit Number
D = Scan Point

COMMON ESS WORD FORMATS

JNN - Junctor Network Number

1024 Network

22 14	13 10	9 8	7 6	5 3	2 0
	LLN	JSF	GRID	SWITCH 1	LEVEL

Switch 1 = Stage 1 switch

2048 Network

22 15	14 11	10 8	7 6	5 3	2 0
	LLN	JSF	GRID	SWITCH 1	LEVEL

Switch 1 = Stage 1 switch

JSN - Junctor Scanner Number

22 14	13 9	8	7 4	3 2	1	0
	FRAME	BAY	HMP-1	VF	CKT	PT

LEN (4:1) - Line Equipment Number

22 17	16 13	12 10	9	8 6	5 4	3 0
	LLN	LSF	BAY	CONCENTRATOR	SWITCH 1	LEVEL

Switch 0 = Stage 0 switch

COMMON ESS WORD FORMATS

LEN (2:1) - Line Equipment Number

22 17	16 13	12 10	9	8 6	5 2	1 0
	LLN	LSF	BAY	CONCENTRATOR	SWITCH 0 *	LEVEL

Switch 0 = Stage 0 switch
* Bit 4 indicates frame: 0 = Home; 1 = Mate

MTDN - Miscellaneous Trunk Distributor Number

22 18	17 10	9	8 2	1 0
	FRAME	BAY	INCREMENT	FIELD

SCN - Scanner

22 16	15 10	9 4	3 0
	SCANNER	ROW	ABP

TCN - Trunk Circuit Number

22 16	15 8	7	6 3	2 1	0
	FRAME	BAY	HMP-1	VF	CKT

COMMON ESS WORD FORMATS

TDN - Trunk Distributor Number

22 18	17 10	9	8 5	4 3	2	1 0
	FRAME	BAY	HMP-1	VF	CKT	PT

TNN - Trunk Network Number

22 15	14 11	10 8	7 6	5 3	2 0
	TLN	TSF	GRID	SWITCH	LEVEL

UTCN (2-Wire) - Universal Trunk Circuit Number

22	21	20 17	16	15 9	8	7 4	3 2	1	0
1	PTS		MATE	FRAME	BAY	PLATE	FILE	CKT	

UTCN (HILO) - Universal Trunk Circuit Number

22	21	20 16	15 10	9	8 1	0
1	PTS		FRAME/2	BAY	CIRCUIT NUMBER	

PTS = Circuits per unit

ALI/TR - ALARM AND LINE INTERFACE/TRANSMIT-RECEIVE

	15	14	13	12	11 ... 5	4	3	2 ... 0
	1	0	0	1		MOD	TR	BRD

BRD ≤ 4, TR = 0 ALI, TR = 1 TR

ALNK - A LINK

	15	14	13	12	11 10	9 ... 6	5	4 ... 0
	1	1	1	0		SWITCH	MOD	LEVEL

BUS - METALLIC BUS

	15	14	13	12	11 ... 7	6	5 4	3	2 ... 0
	1	0	0	0		MOD	GROUP	SW	LEVEL

DL - DATA LINK

	15	14	13	12	11 ... 1	0
	1	1	0	0		SIDE

ELS - ELECTRONIC LINE SEGREGATOR

	15	14	13	12	11 ... 1	0
	0	1	1	1		MOD

REMOTE SWITCHING SYSTEM (RSS)
EQUIPMENT IDENTIFICATION FIELDS

FO - FANOUT

	15	14	13	12	11 — 7	6	5	4 — 1	0
	1	0	1	0		MOD	SIDE	BRD	B

B = 0 NON-USC, B = 1 USC

GSA - GROUND START APPLIQUE

	15	14	13	12	11 — 7	6	5 — 4	3 — 0
	0	1	1	0		MOD	GRP	GSN

JCTR - JUNCTOR

	15	14	13	12	11	10	9	8	7 — 4	3 — 0
	0	0	1	0		B	PD	MOD	SW	LV

MPC - MEMORY OR MICROPROCESSOR
MEM - MEMORY

	15	14	13	12	11 — 6	5	4	3	2 — 0
	1	0	1	1		0	SIDE	0	BRD

PRCC - MICROPROCESSOR

	15	14	13	12	11 — 6	5	4	3	2	1	0
	1	0	1	1		1	SIDE	0	0	0	PROC

PA - POWER ALARM

	15	14	13	12	11	10	9 7	6	5 0
	1	1	1	1		ALT		MOD	PAN

ALT = 1 for ALIT
= 0 for rest of board

REN - REMOTE EQUIPMENT NUMBER
LREN (4:1) - LINE REN

	15	14	13	12	11	10	9 6	5 3	2 0
	0	0	0	1	MOD	0	CONC	SW	LV

CREN (1:1) - CHANNEL REN

	15	14	13	12	11	10	9 7	6 4	3 2	1 0
	0	0	0	1	MOD	1		CONC	SW	LV

ROH: CONC = 111
SW = 10

RLT - REMOTE LINE TEST

	15	14	13	12	11 2	1 0
	1	1	0	1		BRD

RSRD - REMOTE SCAN AND REMOTE DISTRIBUTOR
RSN - REMOTE SCANNER NUMBER

	15	14	13	12	11 9	8	7	6 5	4 0
	0	1	0	1		0	MOD	BRD	SPN

RDN - REMOTE DISTRIBUTOR NUMBER

	15	14	13	12	11 9	8	7	6 5	4 0
	0	1	0	1		1	MOD	BRD	DPN

TONE/TOUCH-TONE® (STAND-ALONE CIRCUIT)

	15	14	13	12	11	10	9	8	7	6	5 4	3	2 0
	0	1	0	0	MOD	1	0	1	1	0	CONC	SW	LV

USC - UNIVERSAL SERVICE CIRCUIT

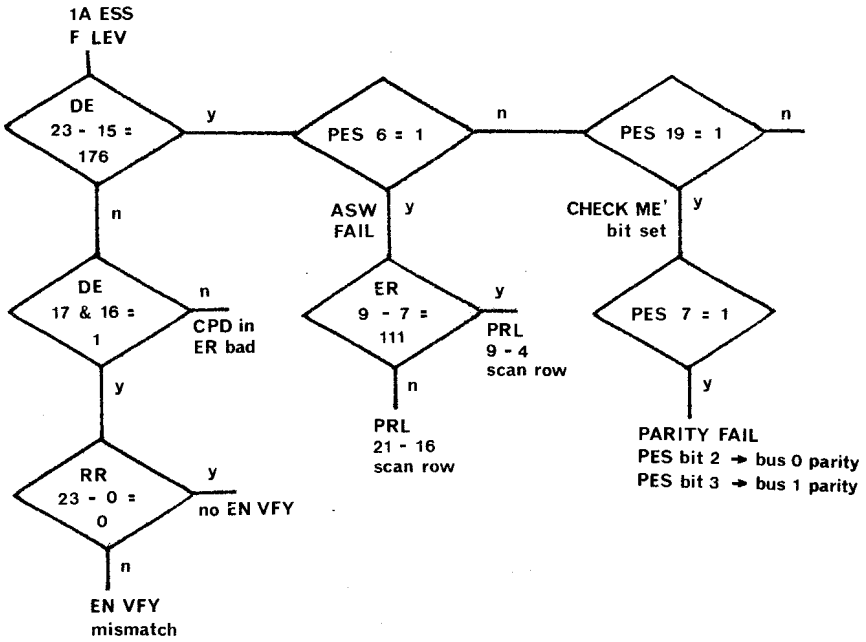
	15	14	13	12	11 5	4	3 2	1	0
	0	0	1	1		MOD	GRP	SW	LV

PEL - PHYSICAL EQUIPMENT LOCATION
(Unlike the preceeding data layouts that indicate the logical circuit identification, this layout identifies where the circuit is physically located on the frame.)

	15	14	13 7	6 0
	0	MOD	LEVEL	POSITION

LEVEL = Height, in inches from the base (7, 28, 36, 44, 52, 60, 70, or 78)
POSITION = Circuit pack displacement, in half inches, from left of frame (0 through 70)

F LEV



F	G	J	K	L	X
Y	Z	B	CAR	ILA	SCA
SDA	SPA	CSC	INS	INH	SC
SR	INJ	PES	PSC	DE	RR
ER	PRM	PRL	[L]	[PES]	[PSC]
[DE]	[RR]	[ER]	[PRM]	[PRL]	[INS]
[CSC]	[INH]	ULR	RFLC00	RFLC01	RFLC02
RFLC03	RFLC04	RFLC05	RFLC06	RFLC07	

[ ] = STANDBY CC REGISTERS

DE

23	17	16	15	0
	R1	R0	CPD	

GOOD = 176

ER

23	22 20	19 17	16 14	13 10	9 7	6	5	4 0
	GROUP	ROW	COL	CPD	PU XLAT			

EXPECT ASW= 1
EXPECT ENV= 1

RR

23 16	15 8	7 0
7 COLUMN 0	7 ROW 0	7 GROUP 0

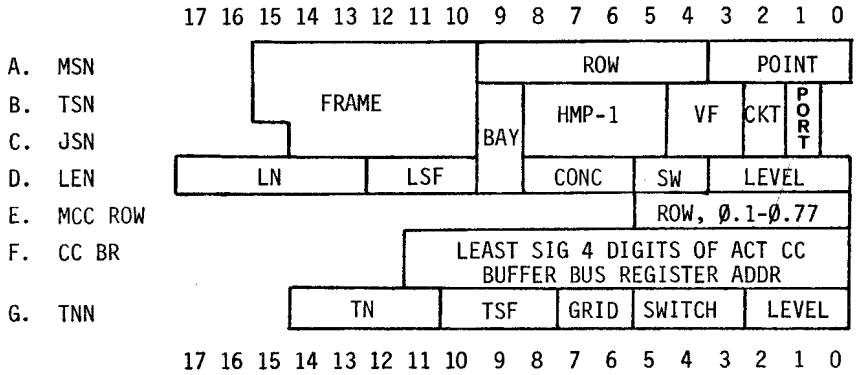
MASTER CONTROL CENTER SCAN POINT DISPLAY

MCC data insert key assignment for using the MCC Binary Display to display a Scanner Row, MCC Matrix Row, CC Buffer Bus Register, or Scan Points associated with a TNN.

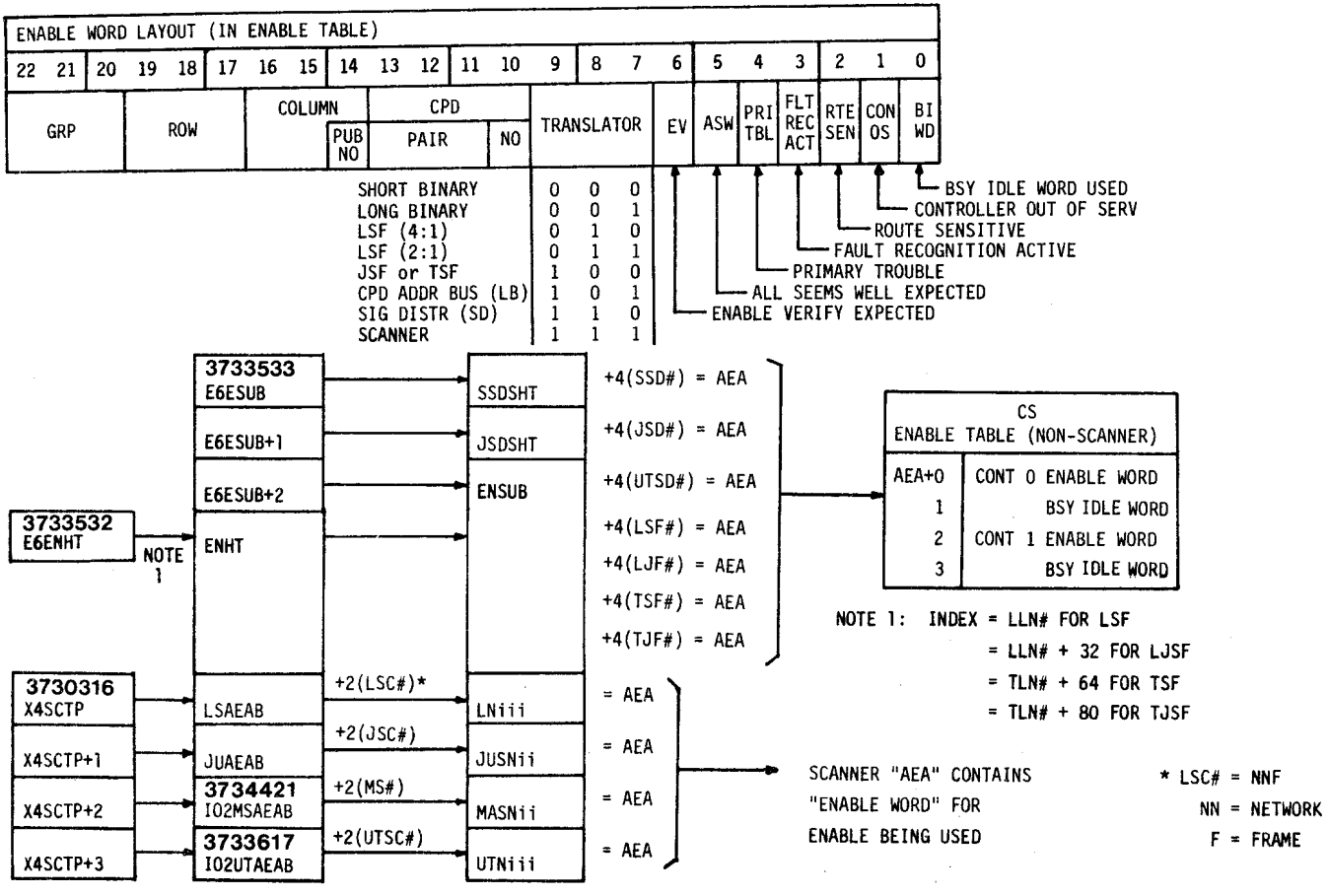
Step 1. Indicate type of display using data insert keys.

	KEY -	20	19	18
A.	Master Scanner Row	0	0	0
B.	Universal Trunk Scanner Row	0	0	1
C.	Junctor Scanner Row	0	1	0
D.	Line Scanner Row	0	1	1
E.	MCC Matrix Row	1	0	0
F.	CC Buffer Bus Register	1	0	1
G.	Scan Points Associated with TNN (Supervisory points right-adjusted, directed next, then fast)	1	1	0

Step 2. Identify row, register, or TNN on DATA INSERT keys 0 - 17.



Step 3. Operate the Scan Point key for display. Program MCMP updates the display at a 1 second rate. If any of the data checks made by MCMP fails, the display and the Scan Point key are extinguished. For some failures, the CD01 message is also printed


ENABLE WORD LAYOUT (IN ENABLE TABLE)
22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
GRP
ROW
COLUMN
PUB NO
CPD
PAIR
NO
TRANSLATOR
EV
ASW
PRI TBL
FLT REC ACT
RTE SEN
CON OS
BI WD
SHORT BINARY 0 0 0
LONG BINARY 0 0 1
LSF (4:1) 0 1 0
LSF (2:1) 0 1 1
JSF or TSF 1 0 0
CPD ADDR BUS (LB) 1 0 1
SIG DISTR (SD) 1 1 0
SCANNER 1 1 1
BSY IDLE WORD USED
CONTROLLER OUT OF SERV
ROUTE SENSITIVE
FAULT RECOGNITION ACTIVE
PRIMARY TROUBLE
ALL SEEMS WELL EXPECTED
ENABLE VERIFY EXPECTED
3733533 E6ESUB
E6ESUB+1
E6ESUB+2
3733532 E6ENHT
NOTE 1
ENHT
SSDSHT
JSDSHT
ENSUB
+4(SSD#) = AEA
+4(JSD#) = AEA
+4(UTSD#) = AEA
+4(LSF#) = AEA
+4(LJF#) = AEA
+4(TSF#) = AEA
+4(TJF#) = AEA
CS
ENABLE TABLE (NON-SCANNER)
AEA+0 CONT 0 ENABLE WORD
1 BSY IDLE WORD
2 CONT 1 ENABLE WORD
3 BSY IDLE WORD
NOTE 1: INDEX = LLN# FOR LSF
= LLN# + 32 FOR LJSF
= TLN# + 64 FOR TSF
= TLN# + 80 FOR TJSF
3730316 X4SCTP
X4SCTP+1
X4SCTP+2
X4SCTP+3
LSAEAB
JUAEAB
3734421 IO2MSAEAB
3733617 IO2UTAEAB
+2(LSC#)*
+2(JSC#)
+2(MS#)
+2(UTSC#)
LNiii
JUSNii
MASNii
UTNiii
= AEA
= AEA
= AEA
= AEA
SCANNER "AEA" CONTAINS "ENABLE WORD" FOR ENABLE BEING USED
* LSC# = NNF
NN = NETWORK
F = FRAME

DF	SCAN POINT
0	CONTROLLER IDLE WHILE IN TPA
1	CONTROLLER BUSY (ENABLED) WHILE IN TPA

AR	BR	DR	AP	SCAN POINTS
0	0	0	1	REGISTERS CLEAR
1	1	1	1	REGISTERS LOADED INCOMPLETE PATH
1	1	1	0	REGISTERS LOADED COMPLETE PATH
1	0	1	1	B REGISTER UNLOADED INCOMPLETE PATH
0	1	1	1	A REGISTER UNLOADED INCOMPLETE PATH
1	1	0	1	D REGISTER UNLOADED INCOMPLETE PATH

DIAGNOSTIC BUS SCAN POINTS

NO. 1A ESS SHORT INSTRUCTION ENCODING

INSTR	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FILL	0	0	0	0	0	0	0	0	DON'T CARE															
SZ	0	0	D1		0	0	0	1	*	C	D1													
S	0	0	D2		0	0	1	R1			D2													
CW	0	0	D3		0	1	0				D3													
C	0	0			0	1	1																	
AW	0	0			1	0	0																	
A	0	0			1	0	1																	
LW	0	0			1	1	0																	
L	0	0			1	1	1																	
LWA	0	0	1	1	Ri						SIZE/DISP									AMT ROTATE L				
LA	0	1	0	0																ADDRESS				
SA	0	1	0	1																				
IF:T	1	0	T1		Cd			Rc		T	T1, T2, T3													
IF:T	1	1			BIT #				CO	T														
LW(LX)	1	1	T2		1	1	0	R1		0	T1, T2													
T(TX)	1	1	T3		1	1	1	0	0	J	T	T1, T2, T3												
EXC	1	1			1	1	1	0	1	0	*	T1, T3												
PUSH	1	1			1	1	1	1	0	*	*	T1, T3												
H	1	1	0	0	1	1	0	R2			1	R1			C	±	AMT					Ri		
Q(QC)	1	1	1	0	1	1	0				1													
QS(QSC)	1	1	1	1	1	1	0				1													
SAVR	1	1	0	0	1	1	1	0	1	1	*	J	Z	Y	X	K	G	F	L	*	*	*	*	*
RESR	1	1	0	1	1	1	1	0	1	1	*													
POP	1	1	0	0	1	1	1	1	1	0	*	Ri			*	*	*	*	*	*	*	*	*	*
GBN	1	1	0	0	1	1	1	1	1	1	0	*	*	*	*	*	*	*	*	*	*	*	*	*
GBNHJ	1	1	0	0	1	1	1	1	1	1	1	*	*	*	*	*	*	*	*	*	*	*	*	*
STALL	1	1	0	1	1	1	1	1	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
TI	1	1	1	±	1	1	1	1	1	J	T	RELATIVE ADDRESS												
D1			0	0								DATA/ADDRESS												
D2			0	1						±		Ri			INCR									
D3			1	0								SIZE/DISP								*	*	Ri		
T1			0	±								RELATIVE ADDRESS												
T2			1	0								VECTOR ADDRESS												
T3			1	1								Rt			N	IJ	±		RELATIVE ADDRESS					
INSTR	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

COMBINATIONS OF CONTROL FLIP-FLOPS

	AZ	AU	LZ	LU	GT	GE	LT	LE
S	0	0	0	0	0	0	1	0
H	1	0	1	0	0	0	0	1
S	1	1		1		0		1
H	1	0		0		1		0
S				1		1		1
H				1		1		1

CONTROL FLIP-FLOPS
- S = SIGN FLIP-FLOP
- H = HOMOGENEITY FLIP-FLOP

CONDITION CODES
- AZ = ARITHMETIC ZERO
- AU = ARITHMETIC UNZERO
- LZ = LOGICAL ZERO
- LU = LOGICAL UNZERO
- GT = GREATER THAN ZERO
- GE = GREATER THAN OR EQUAL TO ZERO
- LT = LESS THAN ZERO
- LE = LESS THAN OR EQUAL TO ZERO

NO. 1A ESS LONG INSTRUCTION ENCODING

INSTR	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	
IF(T):ALPHA	0	1	1	0	0	T				A		Cd			R1			ALPHA							DA1
ALPHA	0	1	1	0	1	0	DA	W	C	S		R2													DA2
L(LW)CF/F	0	1	1	0	1	0		S		W		1	1	1	0	0	0	0	0	0					
H/Q:ALPHA	0	1	1	0	1	1	0	0	C	P	HQ	R1			R2			ALPHA							DA3
IF:T(IA)	0	1	1	0	1	1	0	1	0	0	TA	Cd			R1										DA1
IF:T(I)	0	1	1	0	1	1	0	1	0	1	V	Cd			Rb						R				DA2
T(I)	0	1	1	0	1	1	0	1	1	0	0	*	*	*	*	*	*	I	J	T					DA1
IF:T(I) CF/F	0	1	1	0	1	1	0	1	1	0	1	Cd			Rb										
F/Z:T(I)	0	1	1	0	1	1	0	1	1	1	Z	R2			R1										
LA	0	1	1	0	1	1	1	0	0	A		R1			AMT					P					DA2
SA	0	1	1	0	1	1	1	0	1	S										E					
LWA	0	1	1	0	1	1	1	1	0	W															
L(LW)	0	1	1	0	1	1	1	1	1	0	0	0	W	*	R1			C	A		*	Ri			DA4
S	0	1	1	0	1	1	1	1	1	0	0	1	0	I											
PUSH	0	1	1	0	1	1	1	1	1	0	0	1	1	*	*	*	*	*	*	*	R				DA1
SD	0	1	1	0	1	1	1	1	1	0	1	0	0	E	±	INCR									
SSD	0	1	1	0	1	1	1	1	1	0	1	0	1												
EXC	0	1	1	0	1	1	1	1	1	1	0	*	*	*	*	*	*	*	ASW		R				
SEARCH	0	1	1	0	1	1	1	1	1	1	1	Cd			R1			*	*	*	*				DA2
IR(M/W)	0	1	1	1	0	0	1	*																	
I(M/W)R	0	1	1	1	0	1	0	*	W	A		R1			PC	PL	D	U	Op	Sz					P1-P8
OR(M/W)	0	1	1	1	0	1	1	0		S					*										
O(M/W)R	0	1	1	1	0	1	1	1		W					*										
LK(U/X)I	0	1	1	1	0	0	0	0	0	1	1	0	0	*	PC	*	*	Zp	ASW		XU				DA2
ML	0	1	1	1	1	0	0	0	0	0	0	BG	*	IP	*	IS	IK	W	R	M	C				DA1
MS	0	1	1	1	1	0	0	0	0	0	1		I2	I1	IE										
GCP	0	1	1	1	1	0	0	0	0	1	1	*	*	*	*	*	*	*	*	*	*				

DA1	±	DATA/REL DATA/ADDRESS/REL ADDRESS																							
DA2				SD						±	DATA/REL DATA/ADDR/REL ADDR/VECT ADDR														
DA3	*	*	*	±	AMT					±	DATA/REL DATA/ADDR/REL ADDR														
DA4	MASK																								

INSTR	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

ENCODING	Ri	R1/R2	Rb	Rc	Rt	Cd	ALPHA
000	null	L	B	CF/F	T	LZ	L(W)
001	F	F	F	F	F	LU	A(W)
010	G	G	G	G	G	AZ	C(W)
011	K	K	K	K	K	AU	P(W)
100	X	X	X	X	X	GE	U(W)
101	Y	Y	Y	Y	Y	LE	X(W)
110	Z	Z	Z	Z	Z	GT	S(S)[1]
111	J	J	J	J	J	LT	S(S)[2]

CODE	MOD
00	NULL
01	A
10	S
11	W

[1] With product masking
[2] With insertion masking

Reference: HB 263, Section 1.4A

NO. 1A ESS SHORT AND LONG ORDER DECODING

MASKING	BITS (SHORT), LONG ORDER (13 12 10 9 5) 23 22 20 19 15									
SIZE 1 THROUGH 8 DISP 23 OR LESS	0	SIZE-1			DISP					
SIZE 9 THROUGH 16 DISP 15 OR LESS	1	SIZE-9			0	DISP				
SIZE 17 THROUGH 24 DISP 7 OR LESS	1	SIZE-17			1	0	DISP			
MASK LR = 0	0	0	0	0	1	1	0	0	0	
MASK = LR	0	0	0	0	1	1	0	0	1	
NO MASKING	0	0	0	0	1	1	0	1	0	

SIZE AND DISPL VALUE

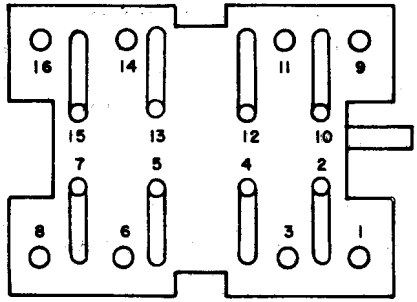
ADD-ONE, SAVE, WRITE

A +1 to Ri after instruction execution
S Ri set equal to data/addr field after instr execution
W Ri set equal to data/addr field + Ri after instr exec

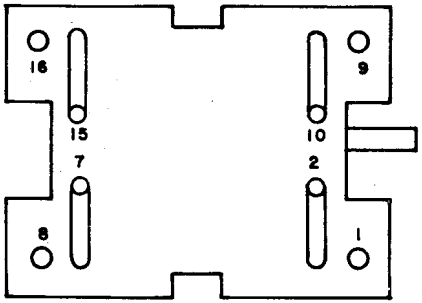
ENCODING	0	1
CO	LZ	LU
E		insertion mask
N	stack pop after xfer	no stack pop after xfer
Op		opcode
PC		parity check
PL		product masking
S	store	store secure
U		unit type
W	memory order	word order
XU	LKXI	LKUI
Z	F:Z	Z:T
Zp		zero upper bits of PR

TERMINAL ARRANGEMENTS
TYPE I FERROD SENSORS

WIRING END VIEWS

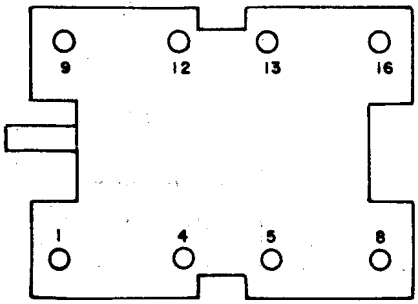


TYPE IB, IC, ID

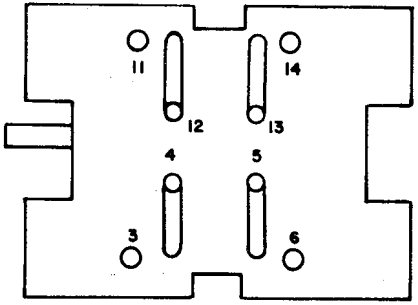


TYPE IE

EQUIPMENT END VIEWS



TYPE IB, IC, ID



TYPE IE

TYPES OF SCANNERS USING TYPE 1 THROUGH 5 FERRODS

TYPE OF SCANNER	FERROD SENSOR ASSEMBLY	MATRIX SIZE	LOCATION	FUNCTION
Line (4 to 1)	1B	16 by 32 (512)	Line Switching Frame (4 to 1), home and mate	Detection of call origination by customer (off-hook)
Line (2 to 1)		16 by 32 (512)	*Line Switching Frame (2 to 1)	
Junctor	1C	16 by 32 (512)	*Junctor Frame	Supervision of intraoffice calls
Universal Trunk	1C and 1D	16 by 32 (512)	*Universal Trunk Frame	Supervision of interoffice calls
Master	1D	16 by 32 (512)	Master Scanner Frame	Monitoring of points within the electronic central office for various purposes such as routine tests, trouble diagnosis, administration, and other requirements.
	1E	16 by 64 (1024)		

* For each pair of mate and home frames, the control for both 512-point matrixes are located on the home frame.

OPERATING CHARACTERISTICS OF TYPE 1 THROUGH 5 FERRODS

TYPE OF FERROD	TYPE OF FERROD ASSY	USED IN	MAX REST EXT TO FERROD	MIN EXT LEAK-AGE REST	REST PER CONTROL WINDING ±10%	NON-OPERATE CURRENT (1 READOUT) (ma)	OPERATE CURRENT (0 READOUT) (ma)
Type 1	1B*	Line Scanners (Loop-Start)	2800	10,000	660	5.5	10.0
Type 2		Line Scanners (Loop-Start, Ground Start, or No-Test Vertical	1800**	10,000	660	5.5	10.0
Type 3	1C	Junctor and Universal Trunk Scanners	1900	10,000	19	9.0	18.0
Type 4	1D	Universal Trunk and Master Scanners	10,700	30,000	35	1.8	3.9
Type 5	1E	Master Scanners	10,700	30,000	35	1.8	3.9

* Each 1B ferrod sensor assembly holds one type 1 and one type 2 ferrod. Both ferrods are arranged for loop-start use. The type 2 ferrod can be converted to ground-start use by changing wire straps on the equipment side of the assembly.

** The ground-start ferrod operates with a ground potential of ±10 volts.

† All resistances are in ohms.

OPERATING CHARACTERISTICS OF MINIATURE TYPE FERRODS

TYPE OF FERROD	USED IN	MAX RESt EXT TO FERROD	MIN EXT LEAKAGE RESt	RESt PER CONTROL WINDING ± 10%	NON-OPERATE CURRENT (1 READOUT)	OPERATE CURRENT (0 READOUT)
					(ma)	(ma)
2A	Line Scanner (Loop-Start)	2800	10000	685	5.5	10
	Ground-Start or Test Vertical)	1800*	10000	685	5.5	10
2B	Miniature Universal Trunk Scanner (Line Side of Trunk)	1900	10000	19	9.0	18.0
	Combined Miscellaneous Trunk Master Scanner (Line Side of Trunk)					
	Combined Miscellaneous Trunk Master Scanner (Trunk Side & Directed Scan Points)	6200		40	3.0	6.0

* The ground-start ferrod operates with a ground potential of ±10 volts.

† All Resistances are in ohms.

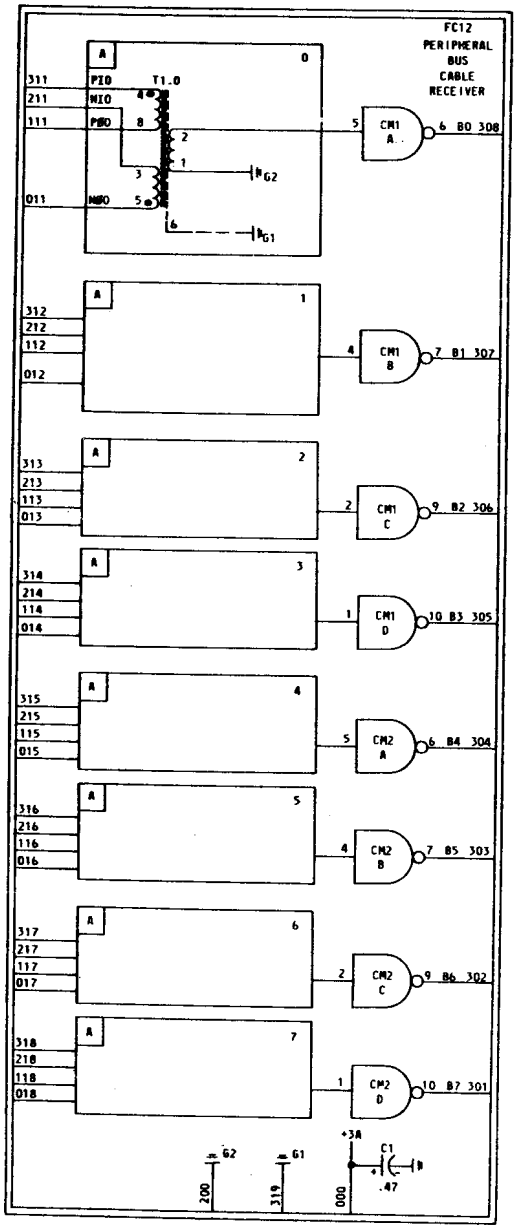
TOUCH-TONE® FREQUENCIES

LOW BAND	HIGH BAND 1209	1336	1477	1633
697	1	2	3	
770	4	5	6	
852	7	8	9	
941		0		

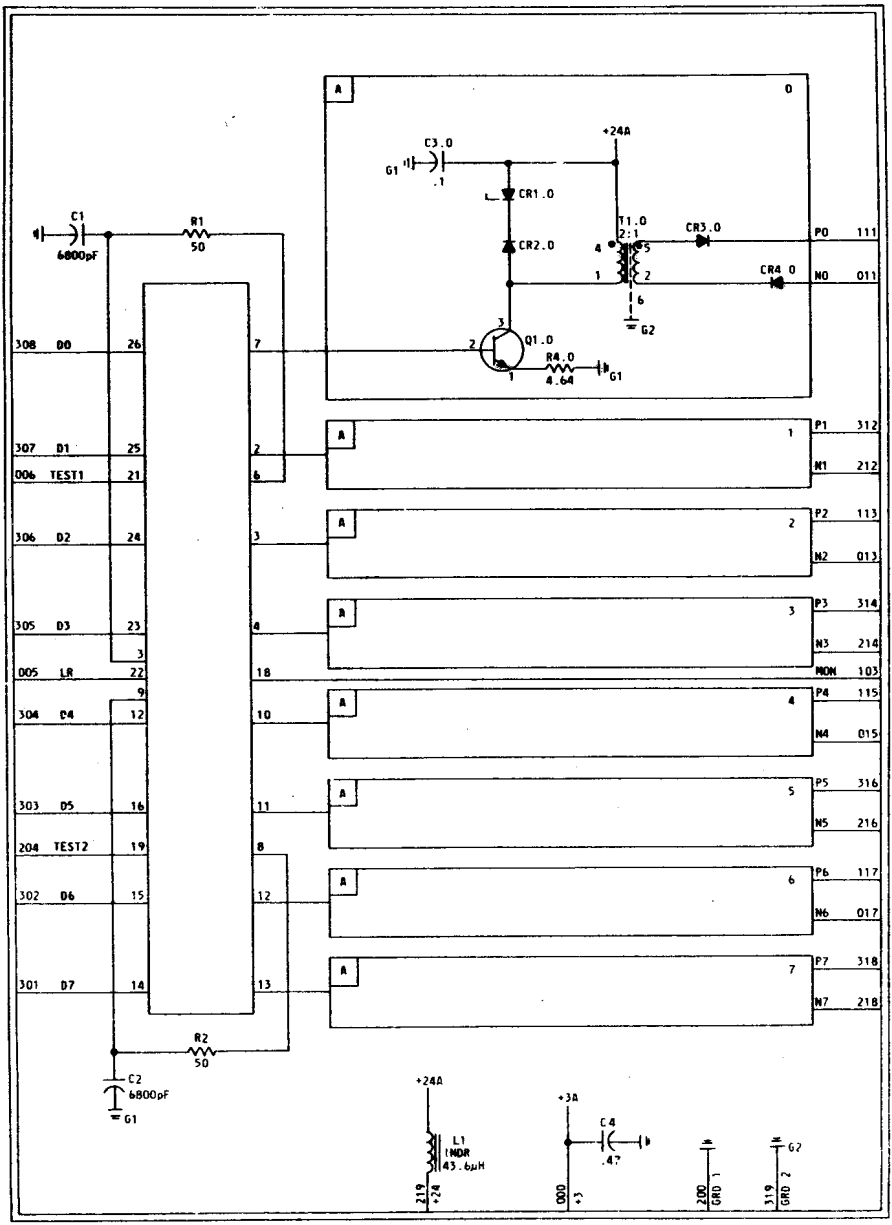
INTEROFFICE FREQUENCY SIGNALS (MF)

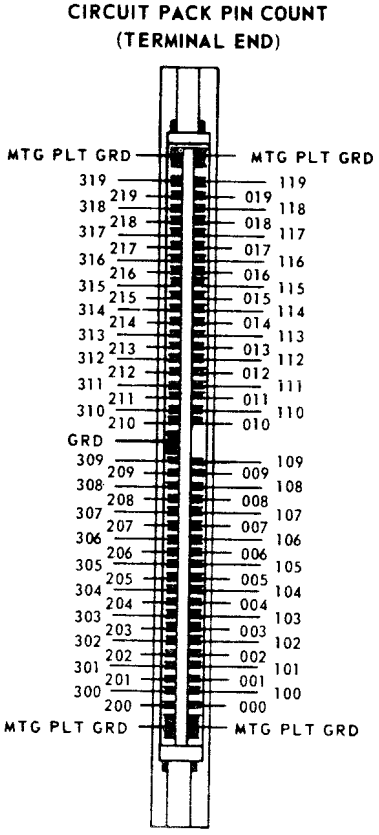
Hz	700	900	1100	1300	1500
900	1				
1100	2	3			
1300	4	5	6		
1500	7	8	9	0	
1700					START

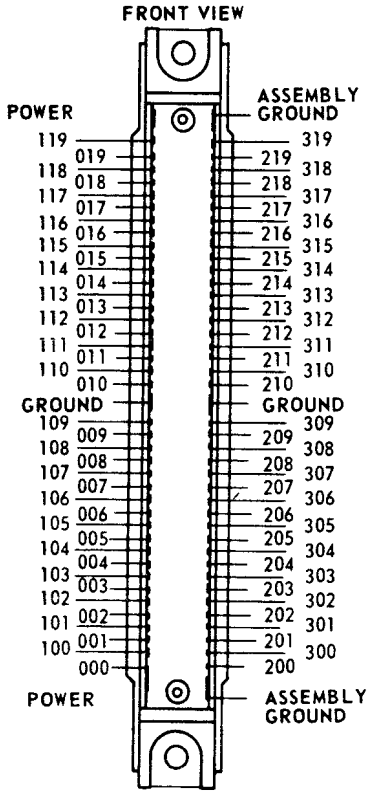
PERIPHERAL BUS CABLE RECEIVER, FC12

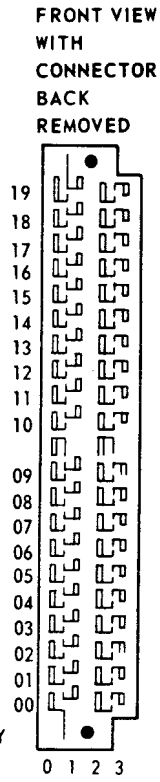


PERIPHERAL BUS CABLE DRIVER, FC13



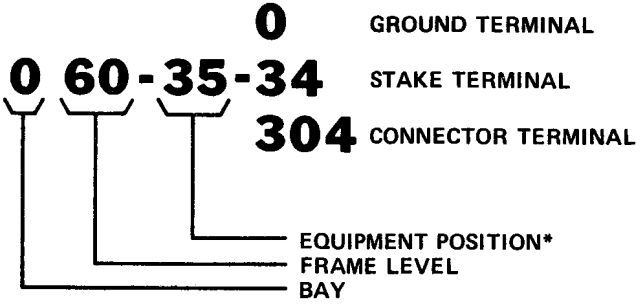






82 PIN CONNECTOR

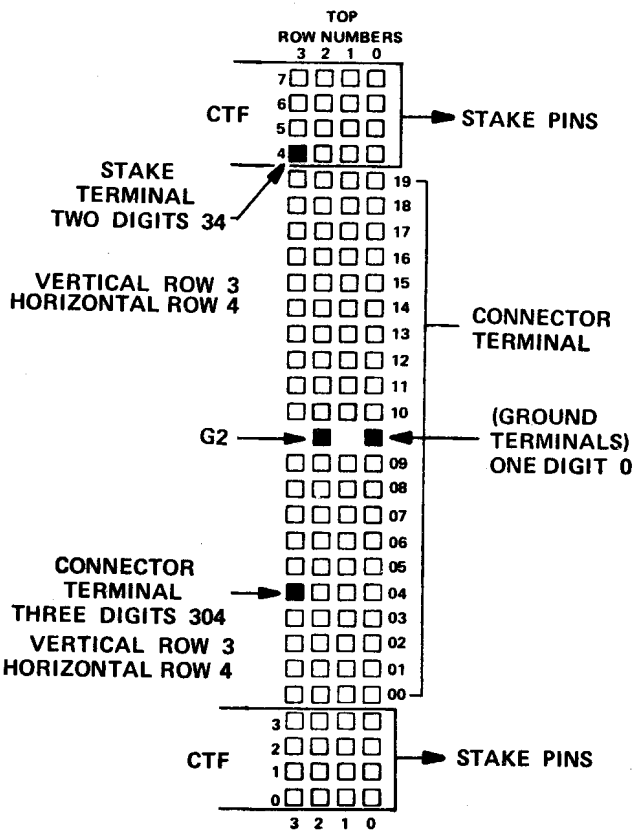
947 CONNECTOR LAYOUT



EQUIPMENT LOCATION

* EQUIPMENT POSITIONS 00 - 44 – 2'2" BAY

EQUIPMENT POSITIONS 00 - 70 – 3'3" BAY



BASICS OF BASIC ELECTRICITY

TERM	UNIT	SYMBOLS DC	SYMBOLS AC	DC FORMULAS SERIES	DC FORMULAS PARALLEL	AC FORMULAS SERIES	AC FORMULAS PARALLEL
CHARGE	COULOMB	Q	Q	*1 COULOMB=6.28 x 10^{18} ELECTRONS			
CURRENT	AMPERE	I_T I_1 I_2 I_3 etc I_{LP} I_{CP}	I_T I_R I_L I_C	$I_T = I_1 = I_2 = I_3$ * $I = \frac{E}{R}$	$I_T = I_1 + I_2 + I_3$	$I_T = I_R = I_L = I_C$ * $I_T = \frac{E_T}{Z}$ $I_R = \frac{E_R}{R}$ $I_L = \frac{E_L}{X_L}$ $I_C = \frac{E_C}{X_C}$	$I_T = \sqrt{I_R^2 + I_L^2}$ $I_T = \sqrt{I_R^2 + I_C^2}$ $I_{LP} = I_L - I_C$ $I_{CP} = I_C - I_L$
VOLTAGE (EMF)	VOLT	E_T E_1 E_2 E_3 etc E_{LS} E_{CS}	E_T E_R E_L E_C	$E_T = E_1 + E_2 + E_3$ * $E = IR$	$E_T = E_1 = E_2 = E_3$	$E_T = \sqrt{E_R^2 + E_L^2}$ $E_T = \sqrt{E_R^2 + E_C^2}$ $E_{LS} = E_L - E_C$ $E_{CS} = E_C - E_L$ * $E_T = I_T Z$; $E_R = I_R R$ $E_L = I_L X_L$; $E_C = I_C X_C$	$E_T = E_R = E_L = E_C$ *
CONDUCTANCE	MHO	G_T G_1 G_2 etc		* $G = \frac{1}{R}$	$G_T = \frac{1}{R_T}$ $G_T = G_1 + G_2 + G_3$ $G = \frac{1}{E}$		
RESISTANCE	OHM	R_T R_1 R_2 R_3	R	$R_T = R_1 + R_2 + R_3$ * $R = \frac{E}{I}$	$R_T = \frac{1}{G_T}$ $R_T = \frac{G_T}{T_T}$ $R_T = \frac{R_1 R_2}{R_1 + R_2}$ $R = \frac{1}{G}$	* $R = \frac{E_R}{I_R}$	
POWER	WATT	P_T P_1 P_2 P_3	AP TP PF	*$P = EI$ $P = IR \times I$ $P = E \times E/R$ $P_T = P_1 + P_2 + P_3$ $P_T = E_T I_T$		* AP = APPARENT POWER $AP = E_T I_T$ TP = TRUE POWER $TP = E_R I_R$ PF = POWER FACTOR = $\frac{TP}{AP}$	
FREQUENCY	CPS		f			* $f = \frac{1}{T}$; $f = \frac{X_L}{2\pi L}$; $f = \frac{1}{2\pi C X_C}$	
PERIOD	SECOND		T			* $T = \frac{1}{f}$	
PHASE DIFFERENCE	DEGREES		θ			$\sin\theta = \frac{E_L}{E_T}$ OR $\frac{X_L}{Z}$ $\sin\theta = \frac{E_C}{E_T}$ OR $\frac{X_C}{Z}$	$\sin\theta = \frac{I_L}{I_T}$ OR $\frac{Z}{X_L}$ $\sin\theta = \frac{I_C}{I_T}$ OR $\frac{Z}{X_C}$
INDUCTANCE	HENRY	L_T L_1 L_2	L_T L_1 L_2	M=0 $L_T = L_1 + L_2$ M AIDING $L_T = L_1 + L_2 + 2M$ M OPPOSING $L_T = L_1 + L_2 - 2M$	M=0 $L_T = \frac{L_1 L_2}{L_1 + L_2}$	* $L = \frac{X_L}{2\pi f}$	
MUTUAL INDUCTANCE	HENRY	M	M	* $M = k\sqrt{L_1 L_2}$ k = COEFFICIENT OF COUPLING			
INDUCTIVE REACTANCE	OHM		X_L X_{LS}			$X_{LS} = X_L - X_C$ * $X_L = 2\pi f L$ $X_L = \frac{E_L}{I_L}$	
CAPACITANCE	FARAD	C_T C_1 C_2	C_T C_1 C_2	$\frac{1}{C_T} = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}$ $C_T = \frac{C_1 C_2}{C_1 + C_2}$	$C_T = C_1 + C_2 + C_3$	* $C = \frac{1}{2\pi f X_C}$	
CAPACITIVE REACTANCE	OHM		X_C X_{CS}			$X_{CS} = X_C - X_L$ * $X_C = \frac{1}{2\pi f C}$ $X_C = \frac{E_C}{I_C}$	
IMPEDANCE	OHM		Z			$Z = \sqrt{R^2 + X_L^2}$ $Z = \sqrt{R^2 + X_C^2}$ $Z = \sqrt{R^2 + X_{LS}^2}$ $Z = \sqrt{R^2 + X_{CS}^2}$	* $Z = \frac{E_T}{I_T}$

* FORMULA GOOD FOR BOTH SERIES AND PARALLEL

ELECTRONIC COMPONENTS

RESISTORS - COMPOSITION OR WIRE WOUND

RADIAL	AXIAL	
BODY A	BAND A	INDICATES FIRST SIGNIFICANT FIG.
END B	BAND B	INDICATES SECOND SIGNIFICANT FIG.
BAND C (OR DOT)	BAND C	INDICATES MULTIPLYING VALUE
		INDICATES MULTIPLYING VALUE
BAND D	BAND D	INDICATES TOLERANCE IN PERCENT
NOTE:	BAND E	INDICATES FAILURE RATE

1. DOUBLE WIDTH BAND SIGNIFIES LOW POWER FIXED, WIRE WOUND RESISTOR.
2. BAND E, WHEN USED ON COMPOSITION RESISTORS INDICATES PERCENT FAILURE PER 1,000 HOURS. THIS IS A (MIL) MILITARY STANDARD.

COLOR	SIGNIFICANCE OF FIRST TWO DIGITS	MULTIPLIER (SEE NOTE 4)	TOLERANCE (SEE NOTE 3)	FAILURE RATE (SEE NOTE 2)
BLACK	0	1		
BROWN	1	10		1.0
RED	2	100		0.1
ORANGE	3	1,000		0.01
YELLOW	4	10,000		0.001
GREEN	5	100,000		
BLUE	6	1,000,000		
VIOLET	7	10,000,000		
GRAY	8	100,000,000		
WHITE	9	1,000,000,000		SOLDERABLE
GOLD		0.1	±5%	
SILVER		0.01	±10%	
NO COLOR			±20%	

NOTE 3 SEE TABLE A FOR TOLERANCES OF KS-SPEC COMPOSITION RESISTORS

NOTE 4 THE MULTIPLIER IS THE FACTOR BY WHICH THE FIRST TWO DIGITS SHALL BE MULTIPLIED TO OBTAIN THE NOMINAL RESISTANCE IN OHMS.

TABLE - A
POWER RATING AND TOLERANCE ON KS - SPEC RESISTORS

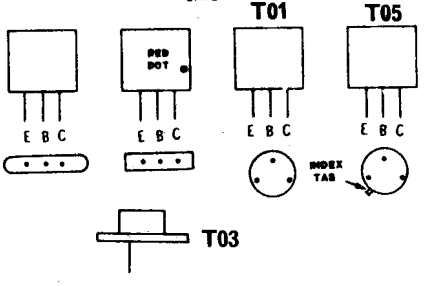
TYPE	POWER RATING IN WATTS
KS - 13490	½
KS - 13491	1
KS - 13492	2

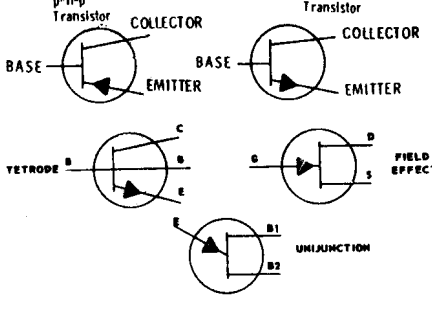
LIST NO.	INITIAL MFR. TOLERANCE	AFTER SHOP INSTALLATION OR SHELF AGING	LONG TERM OPER. TOLERANCE NOTE 5
L1	± 5%	-6 TO +11%	-20 TO +30%
L2	±10%	-13 TO +16%	-25 TO +35%
L3	±20%	-23 TO +26%	-35 TO +45%

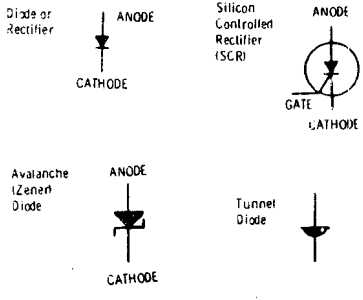
NOTE 5 THE TOLERANCES IN THIS COLUMN SHOULD BE NOTED BEFORE REPLACEMENT OF RESISTORS IN NON CRITICAL PATHS

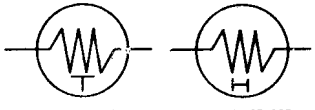
E - EMITTER
B - BASE
C - COLLECTOR

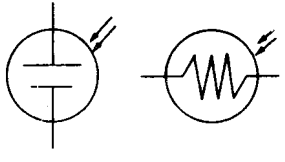
S - SOURCE
D - DRAIN
G - GATE





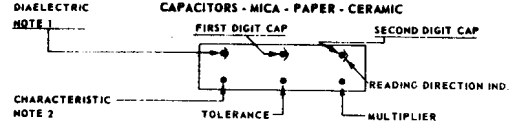




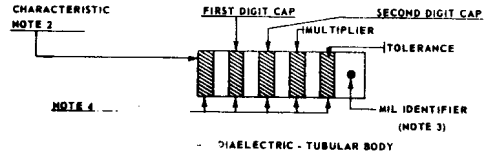


NOTE: REFER TO HANDBOOK 9 SECTION 333 FOR CARE AND HANDLING OF ALL SEMICONDUCTOR DEVICES AND PIG TAIL APPARATUS.

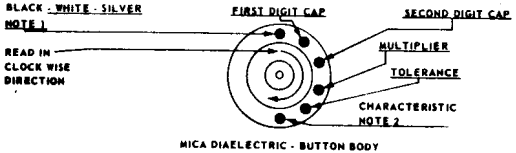
CAPACITORS - MICA - PAPER - CERAMIC



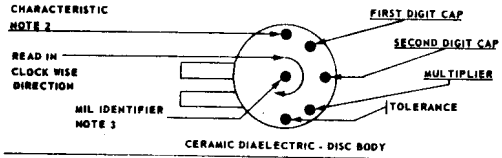
MICA OR PAPER DIAELECTRIC FLAT BODY



DIAELECTRIC - TUBULAR BODY



MICA DIAELECTRIC - BUTTON BODY



CERAMIC DIAELECTRIC - DISC BODY

NOTES

1. SILVER INDICATES PAPER: BLACK INDICATES MICA (MIL): WHITE INDICATES MICA (RETMA).
2. THE CHARACTERISTIC IS A DESIGN FACTOR CONSIDERATION AND IS THEREFORE NOT INCLUDED IN TABLE A OR B.
3. WHEN SPOTS ARE USED, A BLACK SPOT IS APPLIED ON THE OPPOSITE SIDE.
4. COLORED BANDS OR SPOTS MAY BE USED.

TABLE-A-CAPACITORS
MICA OR PAPER DIAELECTRIC

COLOR	SIGNIFICANCE OF FIRST TWO DIGITS	MULTIPLIER (SEE NOTE 1)	TOLERANCE
BLACK	0	1	±20%
BROWN	1	10	
RED	2	100	±2%
ORANGE	3	1000	
YELLOW	4		
GREEN	5		
BLUE	6		
VIOLET	7		
GRAY	8		
WHITE	9		
GOLD		0.1	±5%
SILVER		0.01	±10%

NOTE 1: THE MULTIPLIER IS THE FACTOR BY WHICH THE FIRST TWO DIGITS SHALL BE MULTIPLIED TO OBTAIN THE NOMINAL CAPACITANCE IN MICROMICROFARADS. (MMF).

SYMBOL	NAME	POWER OF TEN
M	MEGA	10^{6}
K	KILO	10^{3}
m	MILLI	10^{-3}
μ	MICRO	10^{-6}
$\mu\mu$	MICRO-MICRO	10^{-12}

TABLE-B-CAPACITORS
CERAMIC-DIAELECTRIC

COLOR	SIGNIFICANCE OF FIRST TWO DIGITS	MULTIPLIER (SEE NOTE 2)	TOLERANCE NOM. CAPACITANCE	
			10MMF OR LESS	OVER 10 MMF
			PERCENT	
BLACK	0	1	±2.0	±20
BROWN	1	10	±0.1	±1
RED	2	100		±2
ORANGE	3	1,000		±3
YELLOW	4	10,000		
GREEN	5	100,000	±0.5	±5
BLUE	6			
VIOLET	7			
GRAY	8	0.01	±0.25	
WHITE	9	0.1	±1.0	±10

NOTE 2: THE MULTIPLIER IS THE FACTOR BY WHICH THE FIRST TWO DIGITS SHALL BE MULTIPLIED TO OBTAIN THE NOMINAL CAPACITANCE IN MICROMICROFARADS (MMF).