PM Technical Reference Manual

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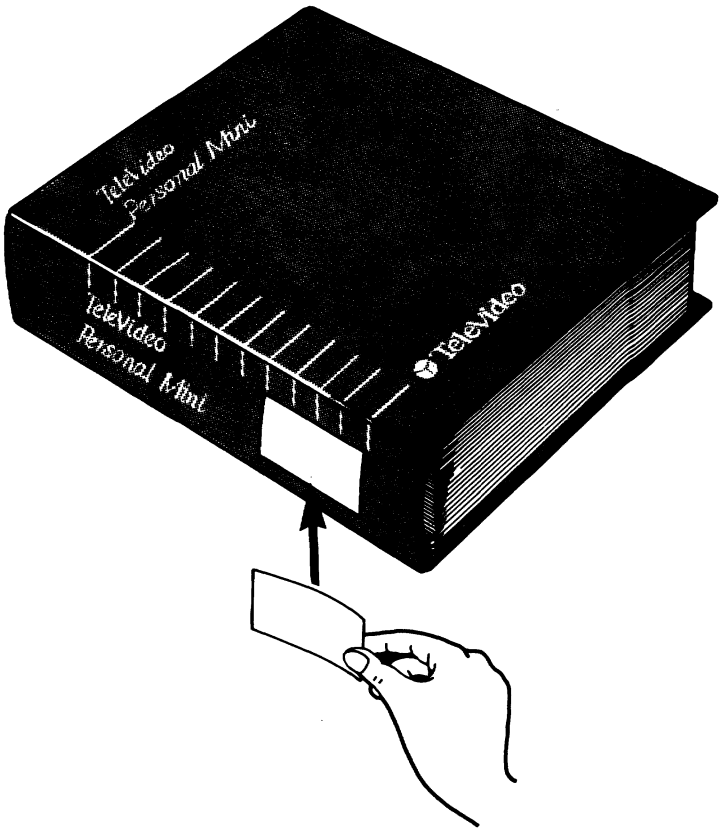

PM
Technical Reference Manual

TeleVideo Part Number 127611-00 Rev. A

February 1985

TeleVideo Systems, Inc.

Personal Mini Technical Reference

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Personal Mini Technical Reference

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PREFACE

The Personal Mini Technical Reference Manual is intended for use by the programmer, engineer, dealer, and end user. The manual provides an overview of the hardware and a more in-depth view of the hardware programming. The systems covered include the PM/16, PM/16T, and PM/4T. The latter two systems feature an integral backup tape drive for backing up the hard disk, hence the 'T' suffix in their names.

The manual has five chapters and three appendices which are described here. **Chapter 1, Unit Overview,** describes the features of the Personal Mini and provides the physical, environmental, power, memory, and storage specifications. The workstation cable requirements and a general description of each major assembly are also described. At the end of the chapter is a list of references that provide additional information about the components discussed in this manual.

Chapter 2, Hardware Functions, details the operations of the following components: the CPU (16-bit), Z80A (8-bit processor), main memory, hard disk controller, and the tape backup drive.

Chapter 3, Hardware Programming, contains the information a programmer needs to interface with the system hardware, such as I/O addresses and command codes.

Chapter 4, Interface, details the pin-outs and signals for the internal and external connectors.

Appendix A, Jumper Configurations, describes the jumper configurations on the main CPU board and tape drive interface board.

Appendix B, Self Diagnostics, describes the diagnostics that are performed by the Personal Mini upon initialization.

Appendix C, Logic Diagrams, contains the logic diagrams of the main CPU board, Winchester disk controller board, and tape drive interface board.

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1. UNIT OVERVIEW

The Personal Mini (PM) is a high performance, network system, capable of interfacing with the IBM PC, most IBM compatible computers, and the TeleVideo TS 1605 and TPC II systems. The Personal Mini is available in three configurations:

* PM/16 - Manages eight workstations and contains a 40 megabyte hard disk drive. The system can be expanded to sixteen workstations with the PM Expansion Unit and its eight additional ports. The Expansion Unit also provides 40 megabytes of additional hard disk storage.

* PM/16T - Manages eight workstations. The system contains an intelligent interface tape backup drive and a 40 megabyte hard disk. It too can be expanded to sixteen workstations with the PM Expansion Unit.

* PM/4T - Manages four workstations and contains an intelligent interface tape backup drive to backup its 20 megabyte hard disk.

The hard disk in the PM/16 and the PM Expansion Unit can be backed up onto tape with the TS 806C Tape Drive Unit. The unit is available from TeleVideo and includes the necessary software.

The Personal Mini is configured as a star network, with RS-422 ports and a simple, low overhead protocol. Table 1-1 lists many of the outstanding features of the systems.

Table 1-1
PM Features

	PM/4T	PM/16	PM/16T
Maximum # of Users	12	16	16
CPU	80186 & Z80A	80186 & Z80A	80186 & Z80A
RAM	256-512K	256-512K	512K
Floppy Drive	360K	720K	360K
Hard Disk Drive	20M	44.5M	44.5M
Tape Drive	20M	-	20M

All PM systems use the InfoShare operating system, which offers four levels of security, as well as many other advanced features for handling business, engineering, and programming needs. Also, all of the systems can be expanded to one megabyte of main memory.

This chapter lists the unit specifications, briefly describes the main assemblies, and provides a list of technical references.

The specifications are divided into five sections:

* Physical Specifications
* Environmental Specifications
* Power Requirements
* Memory and Storage
* Workstation Cables

PHYSICAL SPECIFICATIONS

Height:	7.25 in (18.4 cm)
Width:	17.50 in (44.4 cm)
Depth:	16.88 in (42.8 cm)

Weight:

PM/16:

Net:	36.5 lbs (18.1 kg)
Shipping:	50.0 lbs (22.8 kg)

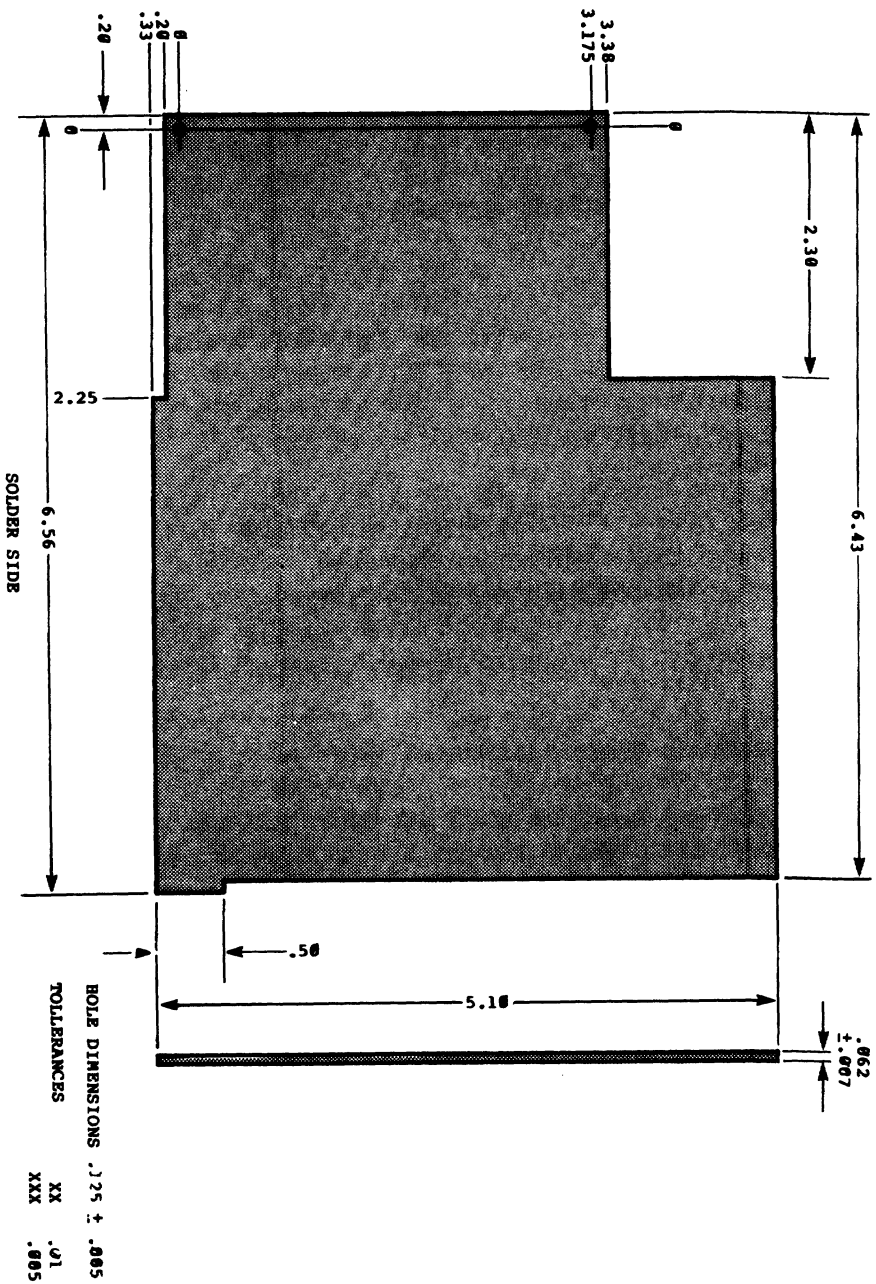
PM/4T, PM/16T:

Net:	41.5 lbs (18.8 kg)
Shipping:	55.0 lbs (24.9 kg)

Expansion Board Dimensions

Expansion boards can be installed in the expansion board slots X1 and X2. The board dimensions are illustrated in Figure 1-1.

Figure 1-1
Expansion Board Dimensions



ENVIRONMENTAL SPECIFICATIONS

Temperature:

Operating:	15 to 35 degrees Celsius 59 to 95 degrees Fahrenheit
Non-operating:	-25 to 60 degrees Celsius 13 to 140 degrees Fahrenheit

Relative Humidity (non-condensing):

Operating:	20-80%
Transit:	5-95%

Heat Output:

PM/16	221.8 BTU/hr 55.9 kg-calories
Peak	235.5 BTU/hr 59.2 kg-calories
PM/16T & PM/4T	552.7 BTU/hr 139.3 kg-calories

Altitude:

Operating:	10,000 ft. (max)
Transit:	50,000 ft. (max)

POWER REQUIREMENTS

AC Power:

Voltage:	115/230 Vac +/-10%
Frequency:	50/60 Hz
Regulation:	1% max

Current (RMS):

115Vac	1.50 ampere
230Vac	.75 ampere

Power Consumption:

115Vac	2 ampere
230Vac	1 ampere

Start Current:

115Vac	1.87 ampere
230Vac	0.94 ampere

DC Power:

PM/16:

Voltage	Current	Regulation (20%-100%)	Power Consumption
+5	7.0a	3% max	35 watts
+12	2.0a	5% max	24 watts
-12	0.5a	5% max	6 watts

+12V peak (300 ms)	6 ampere
+5V cross regulation	1% max

PM/4T and PM/16T:

Voltage	Current	Regulation (20%-100%)	Power Consumption
+5	12.0a	3% max	60 watts
+12	8.0a	5% max	96 watts
-12	0.5a	5% max	6 watts

+5V Cross regulation (20%-100%)	1% max

MEMORY AND STORAGE

Main Memory:

PM/4T, PM/16	64Kx1 RAM	256 Kbytes
Expansion	64Kx1 RAM	512 Kbytes
PM/16T	64Kx1 RAM	512 Kbytes
Option	256Kx1 RAM	512 Kbytes
Option	256Kx1 RAM	1 Mbyte

Z80A Static RAM:

All systems	2Kx8 RAM	32 Kbytes
Option	8Kx8 RAM	64 Kbytes
Option	8Kx8 RAM	128 Kbytes

Hard Disk:

PM/4T:	
Formatted	20 Mbytes
PM/16 and PM/16T:	
Formatted	44.5 Mbytes
Unformatted	53.0 Mbytes

Floppy Disk:

PM/16:	
Formatted	720 Kbytes
Unformatted	1 Mbyte
TPI (tracks per inch)	96
PM/4T and PM/16T:	
Formatted	320 Kbytes
Unformatted	500 Kbytes
TPI (tracks per inch)	48

Tape Backup:

Formatted	20 Mbytes
Unformatted	21 Mbytes
Tape speed (nominal)	90 ips
Data density (nominal)	7772 bpi

WORKSTATION CABLES

Maximum Distance Between Workstation and PM:

450 feet using shielded, twisted-pair cable.

6000 feet using Optic Data Systems ODS214/215 fiber optics modem and duplex fiber cables.

MAJOR ASSEMBLIES

Main CPU Board

The main CPU board contains the 16-bit CPU functions, 8-bit processor functions, main memory, and all interface signals going to the connectors and the floppy disk.

Winchester Disk Controller Board

The controller board controls the internal hard disk drive.

Hard Disk Assembly

PM/16 and PM/16T:

The hard disk is a random-access Winchester assembly with eight recording surfaces and a 44.5 megabyte storage capacity.

PM/4T:

The hard disk is a random-access Winchester assembly with four recording surfaces and a 20 megabyte storage capacity.

Floppy Disk Assembly

PM/16:

The floppy disk drive is a 5 1/4-inch quad-density, double-sided assembly with a 720 Kbyte capacity. This 96 TPI drive has read/write capabilities but the write function is not software supported. This drive is used to up-load the system. The drive can load programs recorded at 48 TPI in PC-DOS format.

PM/4T and PM/16T:
The floppy disk drive is a 5 1/4-inch double-density, double-sided assembly with a 320 Kbyte capacity. This 48 TPI drive is a logical (read and write) drive for PC-DOS formatted diskettes.

Interface

The interface is made up of twenty-one interface connectors located on the main CPU board, back panel, front panel, and tape controller board.

Tape Backup:

The tape backup drive has an intelligent interface allowing it to directly access main memory. The intelligent tape adaptor is installed in one of the expansion slots and controls the Streaming Tape Drive through a standard QIC-02 intelligent interface board.

TECHNICAL REFERENCES

The following publications contain technical data related to the Personal Mini:

* Intel Microprocessor and Peripheral Handbook (Intel)

* Zilog Data Book (Zilog)

* MOS Microprocessor Data Manual (Signetics)

* Synertek Data Catalog (Synertek)

* Storage Management Products Handbook (Western Digital)

2. HARDWARE FUNCTIONS

The Personal Mini contains two processors: an Intel 80186 to handle the 16-bit operations, and a Zilog Z80A to handle the 8-bit operations. Both have access to main memory.

The system architecture is designed so that the two processors remain isolated in normal operation with main memory and the interrupts as their only link.

This chapter describes the functions of the unit. The functions described are the 80186 CPU, main memory, Winchester disk controller, Z80A, and tape backup. Figure 2-1 shows the functional block diagram of the unit.

80186 CPU FUNCTIONS

The 80186 CPU (see Figure 2-2) is a 16-bit microprocessor that controls the 16-bit interfaces, system interrupts, and EPROM. The 80186 has sixteen data lines, twenty address lines, and an 8 MHz system clock that is developed from a 16 MHz crystal. The following main board 16-bit interfaces are controlled by the 80186.

* DUART - console and serial printer ports
* Parallel printer port
* Floppy disk controller
* Hard disk interface

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Figure 2-1
System Functions

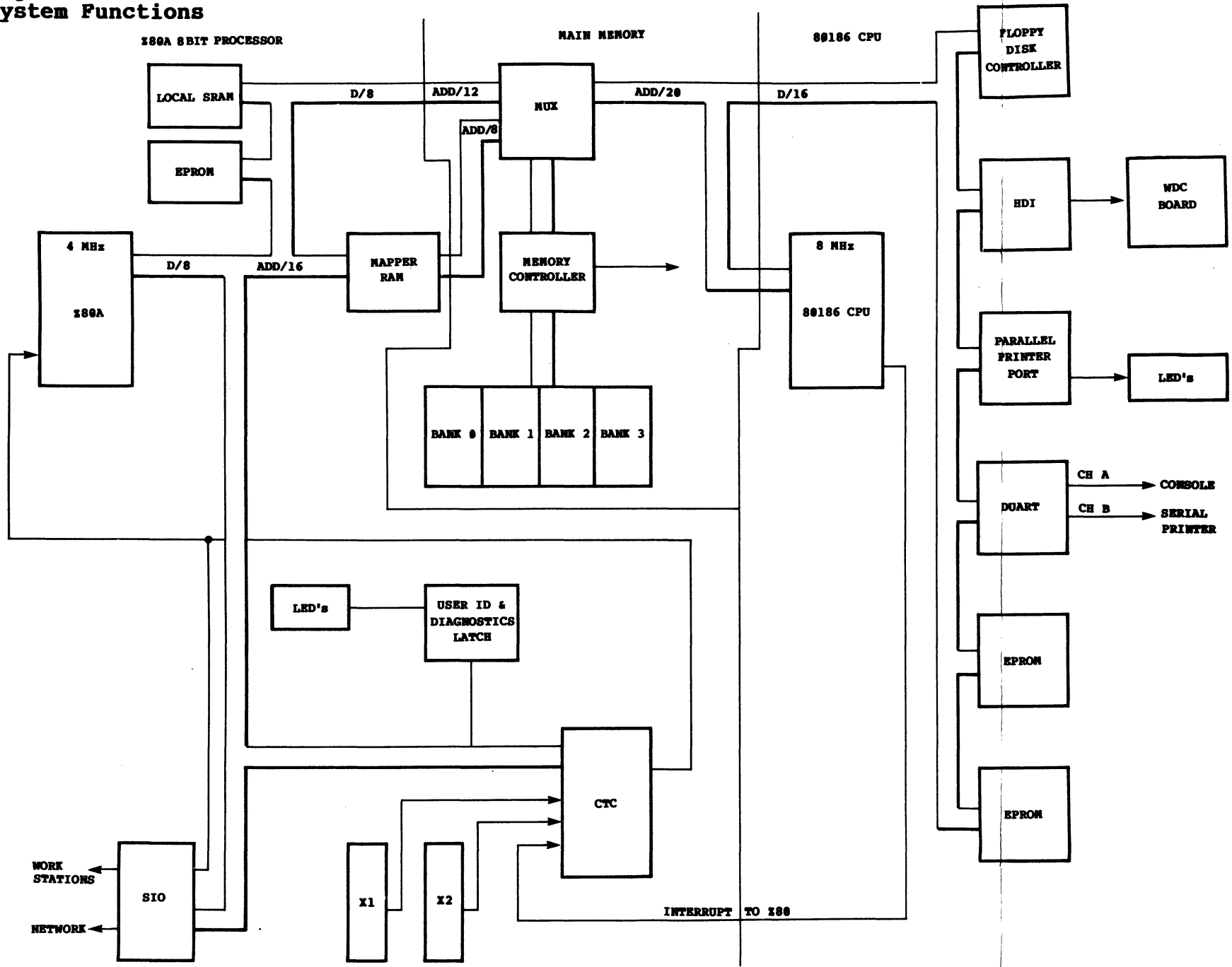
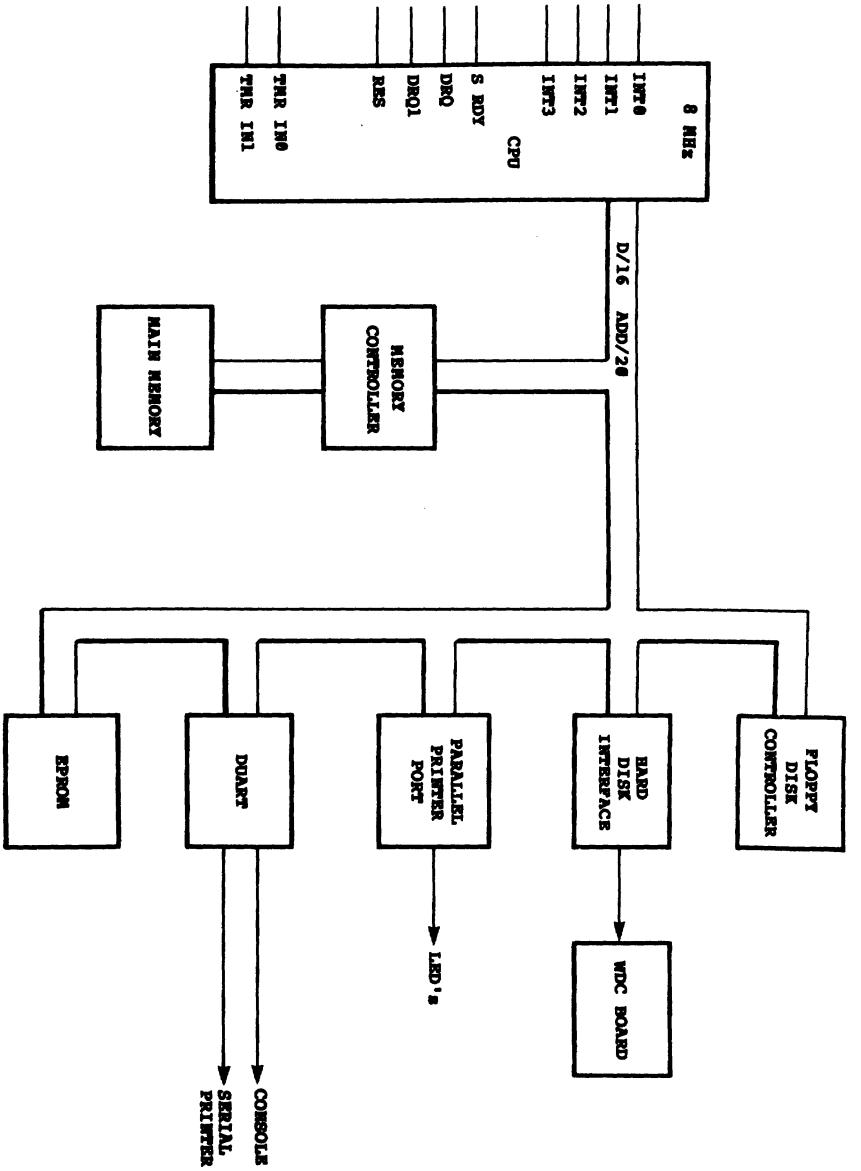


Figure 2-2
80186 CPU Section



DUART (Console and Serial Printer)

The 2681 DUART (see Figure 2-3) controls both the system console port and the serial printer port. This device has programmable, internal baud rate generators derived from a 3.6864 MHz crystal, and provides handshaking signals on the general purpose IP0-IP6 input lines and the general purpose OP0-OP7 output lines.

The DUART has two DCE serial RS-232C I/O channels with channel A as the system console port and channel B as the serial printer port. The channels can be reconfigured to a DTE port by the installation of a special cable. They can also be converted for reverse channel protocol by changing the E11 and E15 jumpers (see Appendix A).

The system console port is the system service port that provides keyboard input.

The serial printer port can be configured by the jumpers for two functions. The default configuration sets it as a serial printer port but it can be changed to allow use by a diagnostics console (see Appendix A). This allows access to the Z80A independent of the 80186 CPU operations. This function is not software supported.

PARALLEL PRINTER PORT

The parallel printer port (see Figure 2-4) allows for the use of a parallel data input printer. This section is made up of a parallel printer and interrupt latch (U50), printer data latch (U61), and printer control and diagnostics latch (U56).

Figure 2-3
DUART

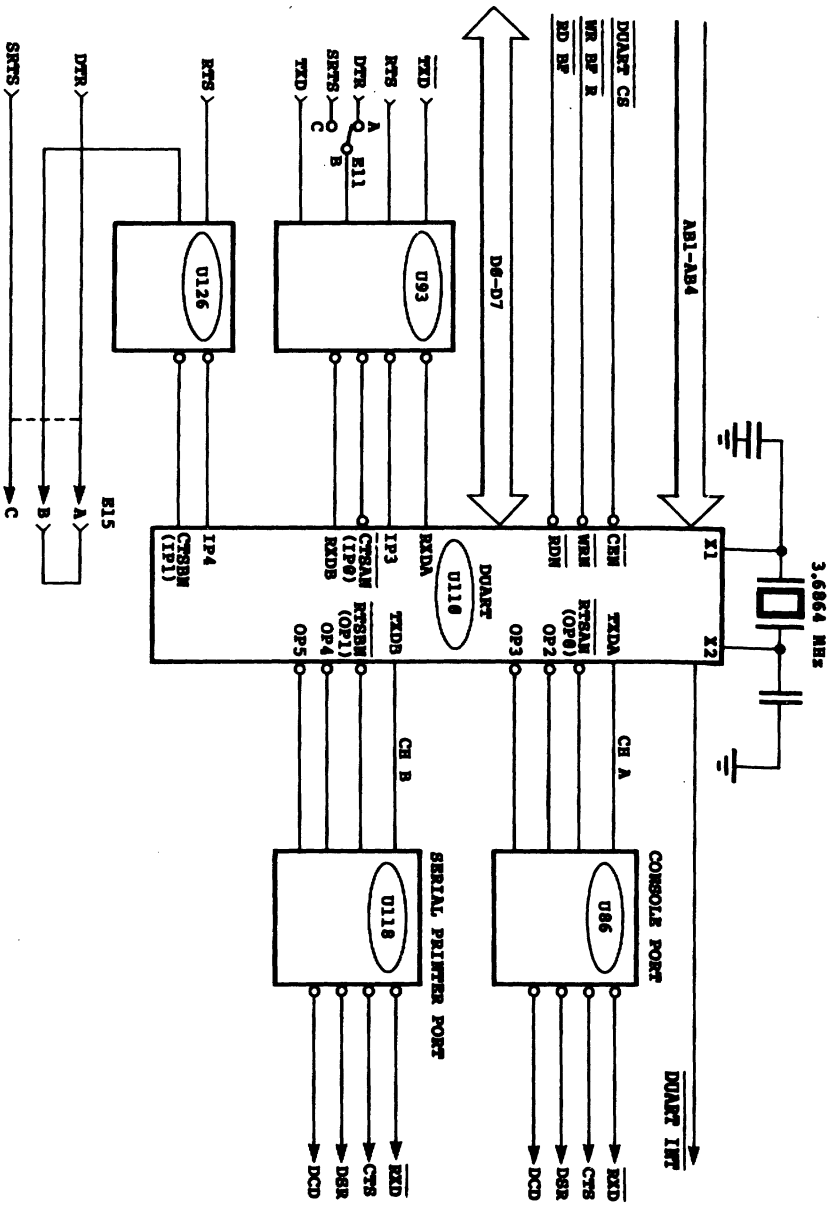
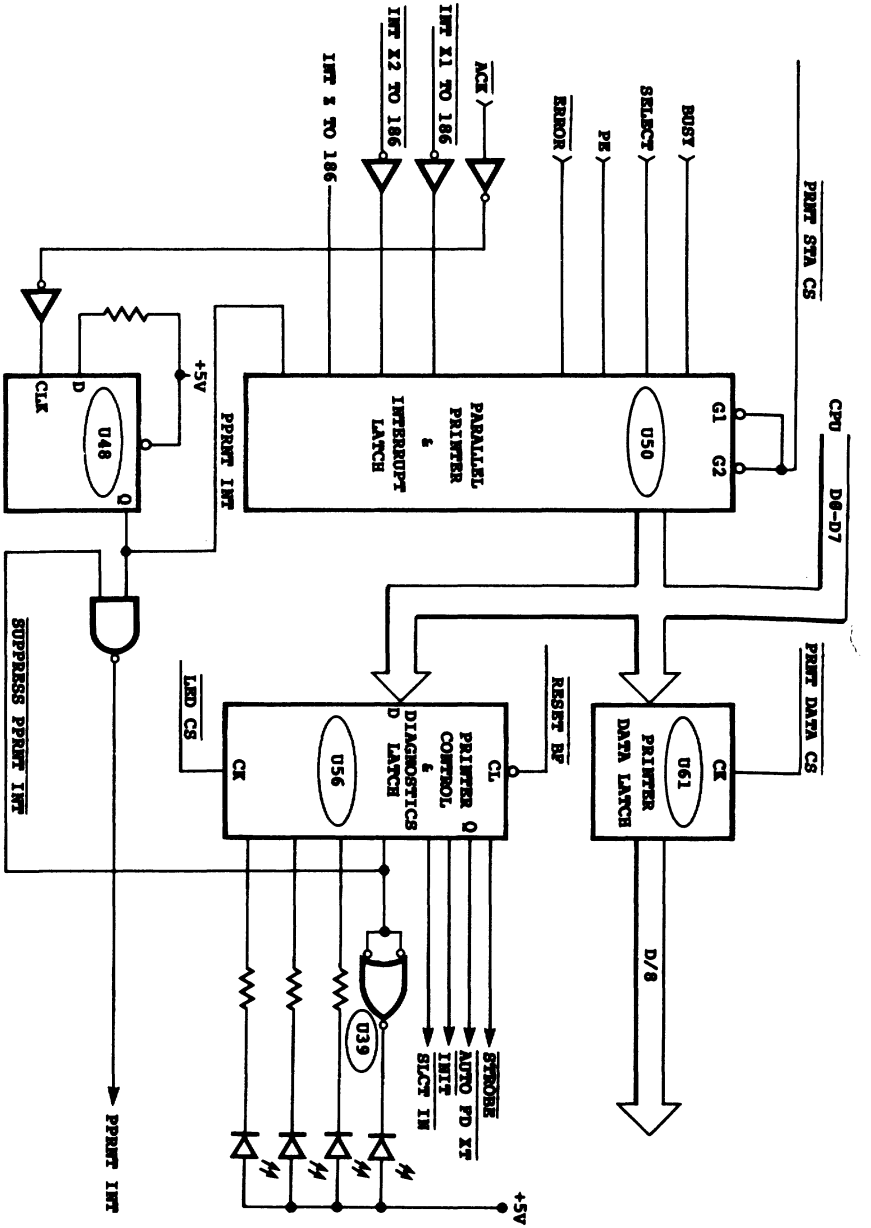


Figure 2-4
Parallel Printer Port



The parallel printer and interrupt latch receives control signals from the parallel printer and four interrupt signals. These interrupt signals are the INT Z TO 186, -INT X1 TO 186, -INT X2 TO 186, and a software programmable PPRNT INT signal that is not used in the default configuration. Data bits D0-D7 are passed by the latch to the 80186 data bus.

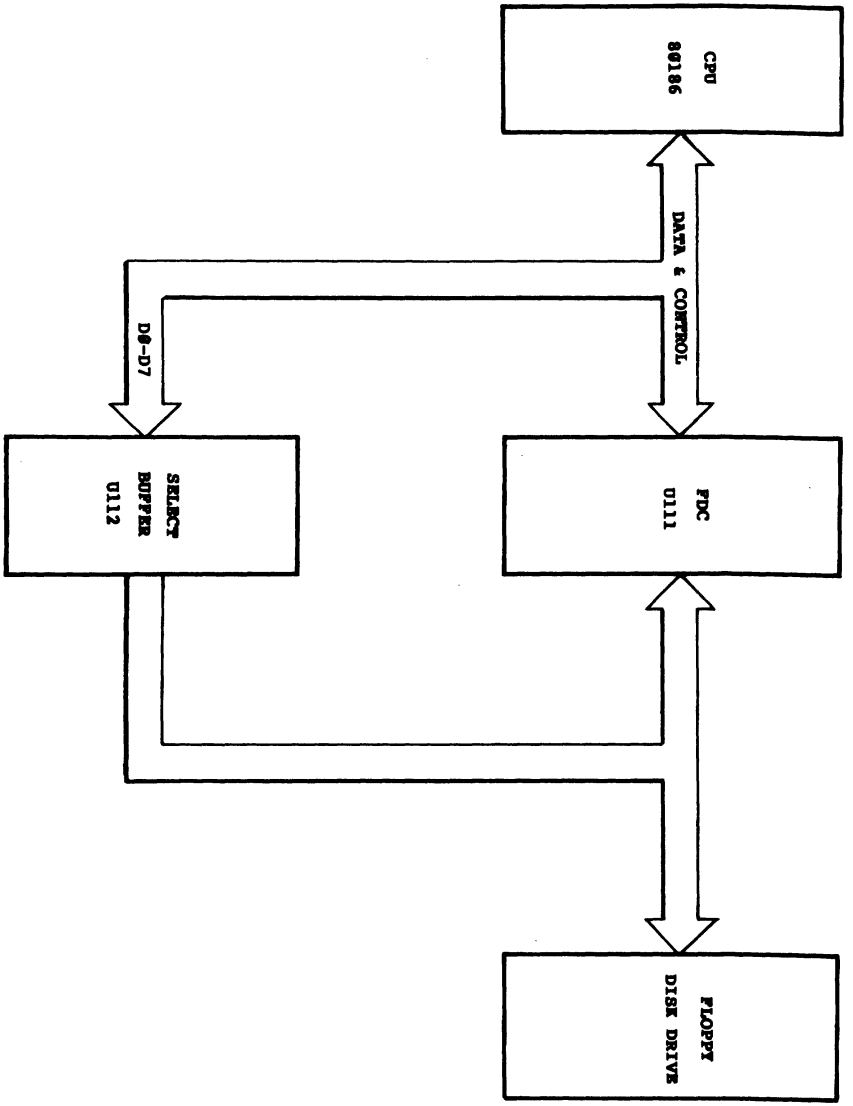
The printer control and diagnostics latch strobes parallel data to the printer and controls the 80186 diagnostic LED's. This latch provides the parallel printer control signals. The most important is the -STROBE signal which strobes the parallel data bits to the printer.

FLOPPY DISK CONTROLLER

The floppy disk controller is a Western Digital WD1770 (see Figure 2-5). It contains internal registers to accept high-level commands from the 80186. The controller interface to the 80186 consists of an 8-bit, bidirectional, data access bus for the transfer of status, data, and commands. All 80186 communication with the drive occurs through these lines. The controller contains an internal digital data separator, digital phase lock loop circuit, and write precompensation.

The drive select buffer (U112) controls floppy disk drive selection, motor on, and side selection.

Figure 2-5
Floppy Disk Controller



HARD DISK INTERFACE

The hard disk interface (see Figure 2-6) includes the Winchester disk controller Board, which is discussed later in this chapter. The interface provides data and control lines from the 80186 to the WDC board.

The hard disk data buffer (U53) holds data for transfer to the WDC board or the 80186.

The control buffer (U54) transfers the control signals to the WDC board.

SYSTEM INTERRUPTS

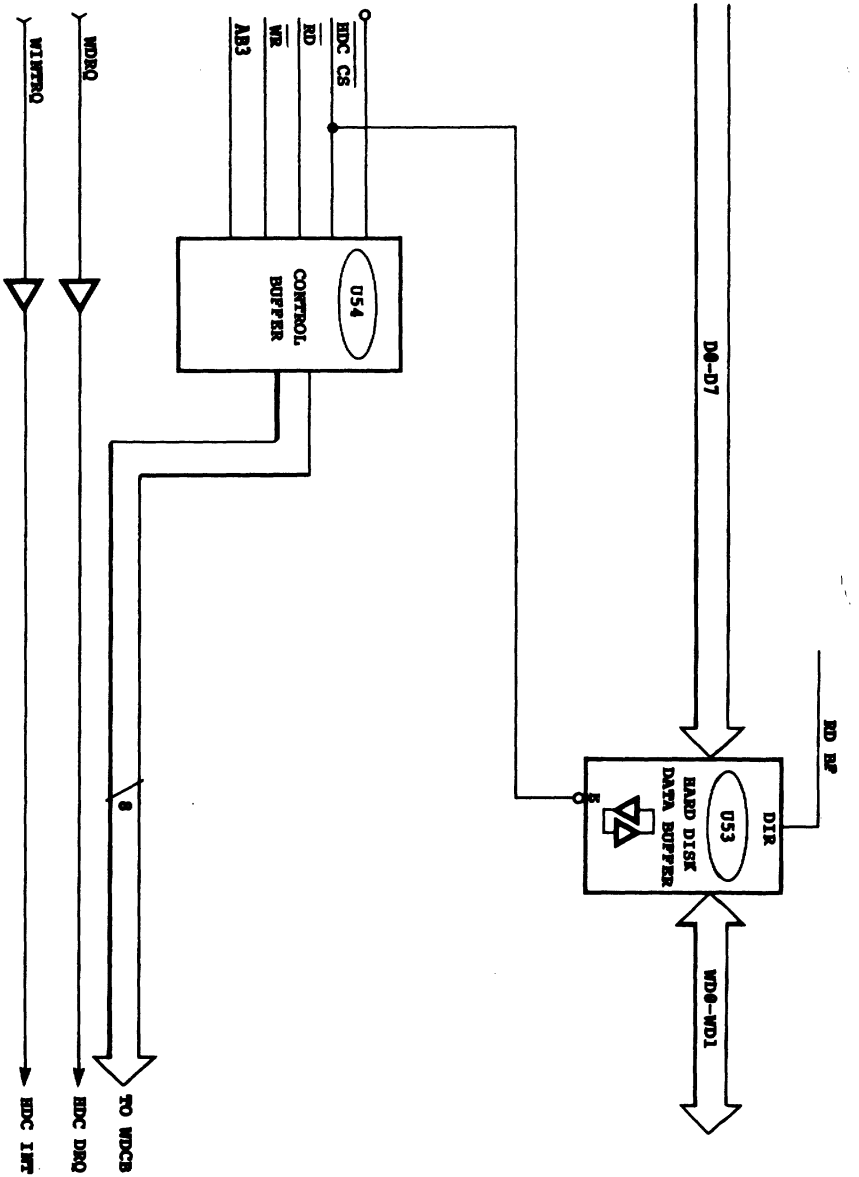
The 80186 has four interrupt inputs: INT 0, INT 1, INT 2, and INT 3. All interrupts are maskable and are prioritized. The interrupts are described according to their priority with the highest priority listed first.

INT 0 is the DUART interrupt. It is activated when either the system console or serial printer has completed a command function and is ready for another command.

INT 1 receives one of four interrupts on this input. They are PPRNT INT, INT Z TO 186, -INT X1 TO 186, and -INT X2 TO 186. When this interrupt input is active, the 80186 polls the Parallel Printer and Interrupt Latch (U50) to find out which interrupt is active. This latch also holds error signals from the parallel printer.

INT 2 is the hard disk controller interrupt. It is activated to let the 80186 know that the previous command has been completed.

Figure 2-6
Hard Disk Interface



INT 3 is the floppy disk interrupt. The drive activates the signal to inform the 80186 CPU that the previous command has been completed and that a new drive command can be issued.

MAIN MEMORY

Main memory (see Figure 2-7) is a two-port memory that is equally addressable by the 80186 and the Z80A. The intelligent interface tape backup can also directly access main memory on the 8-bit bus but does not have access to the memory mappers. The 80186 and Z80A can both access up to one megabyte of memory. The main memory contains a memory MUX, memory controller, and memory banks.

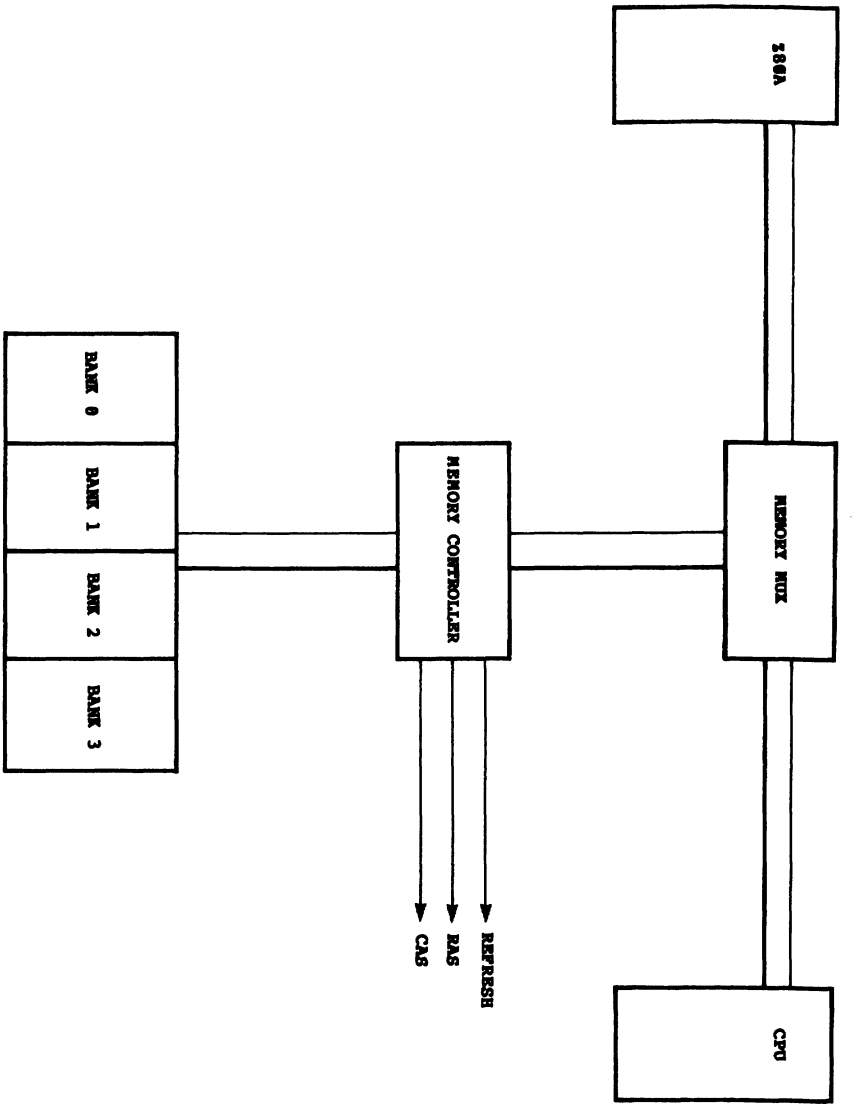
Memory MUX

The memory MUX (U9) is an R-S flip-flop that enables either the 80186 or Z80A to address main memory. The MUX is set or reset by the memory controller (U96) MUX/PCLK signal.

Memory Controller

The 8207 memory controller is configured as a dual-port controller. Port A holds the 80186 CPU address lines and port B holds the Z80A address lines. The controller arbitrates the processor requests and directs data to or from the appropriate port. A priority system reassigns priorities based on past history. Requests are internally queued.

Figure 2-7
Main Memory Section



The memory controller limits the number of functions performed by main memory at any time to one event. The controller may be addressing for the Z80A or the 80186, or performing a refresh cycle.

At power-up, parallel data bits from the parallel data register (U144 & U145) are sent to the PDI input. This input programs the controller's jumper selectable options.

Refresh requests are generated internally for the dynamic RAM's. This frees the processors from this function. The controller provides RAS (row) and CAS (column) signals for each of four possible memory banks allowing it to access one megabyte of memory.

The memory-locking feature gives each processor uninterrupted access to a portion of the memory. This allows one processor to complete its data processing before the other processor can access that area.

Memory Banks

If the system contains a memory expansion board, the memory controller divides the memory into four banks. The main memory contains 64Kx1 dynamic RAM chips to provide 256 Kbytes of main memory. The memory expansion board provides another 256 Kbytes of memory expanding it to 512 Kbytes. The 256 kbyte configuration is basic for the PM/4T and PM/16 units, and the 512 Kbyte configuration is basic for the PM/16T unit. Another option is the use of 256Kx1 dynamic RAM chips to provide either 512 Kbytes or 1 Mbyte of main memory.

Each bank has its own RAS (row) and CAS (column) lines to strobe the address. The RAS and CAS are selected by the decoding of the program bits RB1 and RB2, and bank input bits BS0 and BS1. Twenty address lines are required to address one megabyte of memory.

The signals from the high and low byte write enable are decoded by the Write Enable Decoder (U49).

WINCHESTER DISK CONTROLLER

The Winchester disk controller board (see Figure 2-8) provides the main controller function for the Winchester disk drive(s).

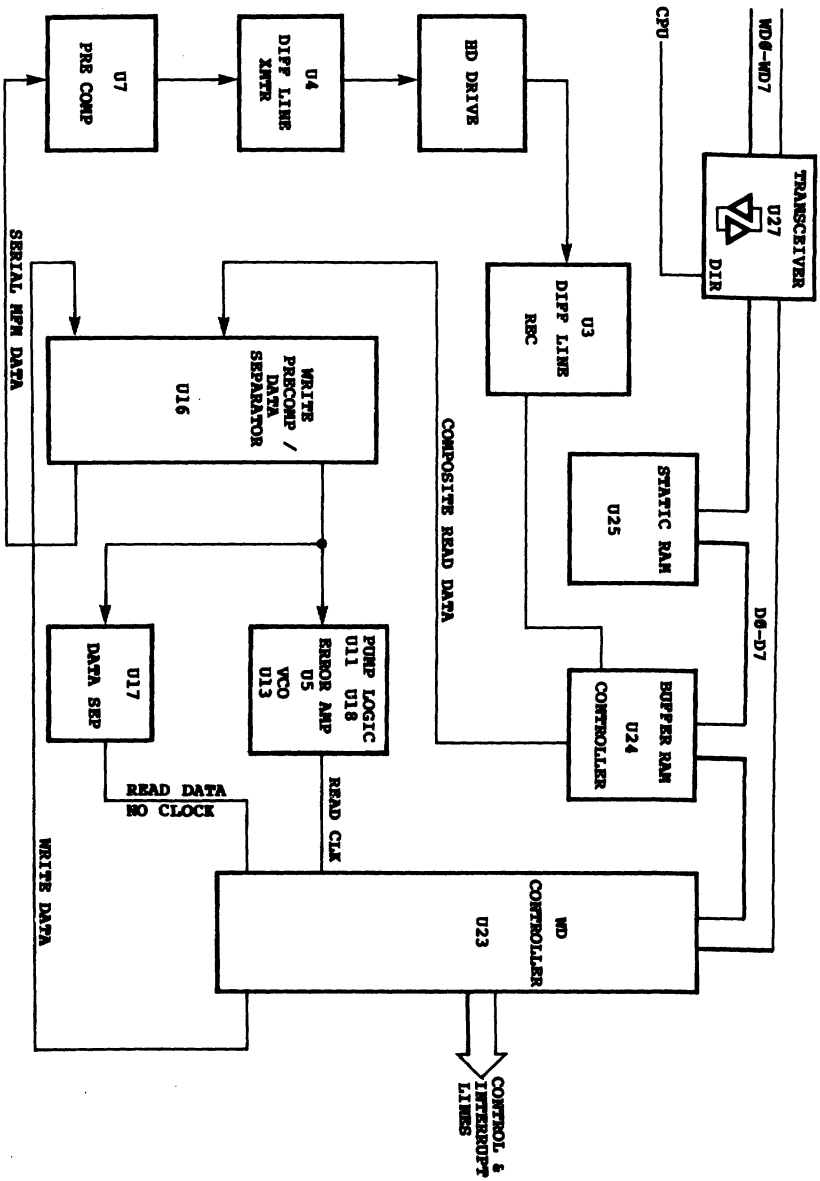
The WD controller (U23) can handle up to four disk drives and provides all control and data handling functions needed to interface the system with a disk drive.

The controller interfaces the host through a bi-directional transceiver (U27), which is controlled at its DIR input by the 80186. The data bus goes to the controller (U23), buffer RAM Controller (U24), and static RAM (U25).

The static RAM is controlled by the RAM buffer controller and stores one sector of read or write data.

The RAM buffer controller controls the RAM sector data and the head and drive select lines. It also controls the interface between the static RAM and the controller.

Figure 2-8
Winchester Disk Controller



The write precompensator/data separator (U16) provides the write precompensation logic and data separator control logic that sends a synthesized read clock and read data to the controller.

The controller board receives commands from the 80186 CPU, initiates the commands, and sends status signals to the CPU.

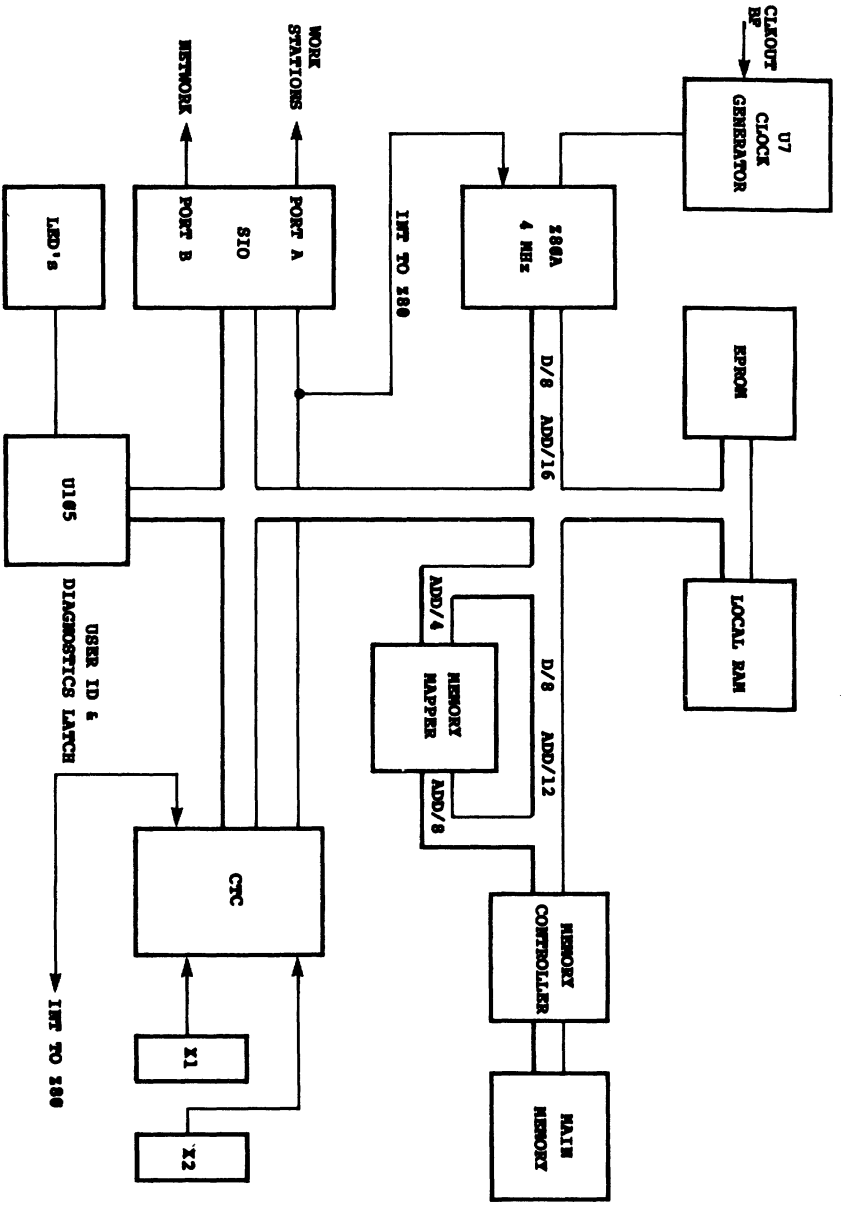
During a read operation, composite read data (serial) is received by the differential line receiver (U3) from the hard disk. This data is passed to the buffer RAM Controller.

During a write operation, data is sent from the write precompensator/data separator to the precompensator, and then to the differential line transmitter (U4) for transmittal to the hard disk.

8-BIT NETWORKING FUNCTIONS

The Z80A 8-bit processor (see Figure 2-9) controls the 8-bit functions that include networking, expansion cards, and 8-bit diagnostics. The processor runs on a 4 MHz clock generated by the clock generator (U7) from the CPU CLKOUT BF signal. The processor has eight data lines and sixteen address lines. The functional areas of the processor are local memory, memory mapping, SIO and work stations, CTC, and expansion slots.

Figure 2-9
Z80A 8-Bit Section



Local Memory

The local memory (see Figure 2-10) has a 4-kbyte EPROM and 4 Kbytes of static RAM, expandable to 16 Kbytes. The EPROM performs the 8-bit initialization and diagnostics. The static memory polls the workstations for a service request since interrupts are not used for the workstations.

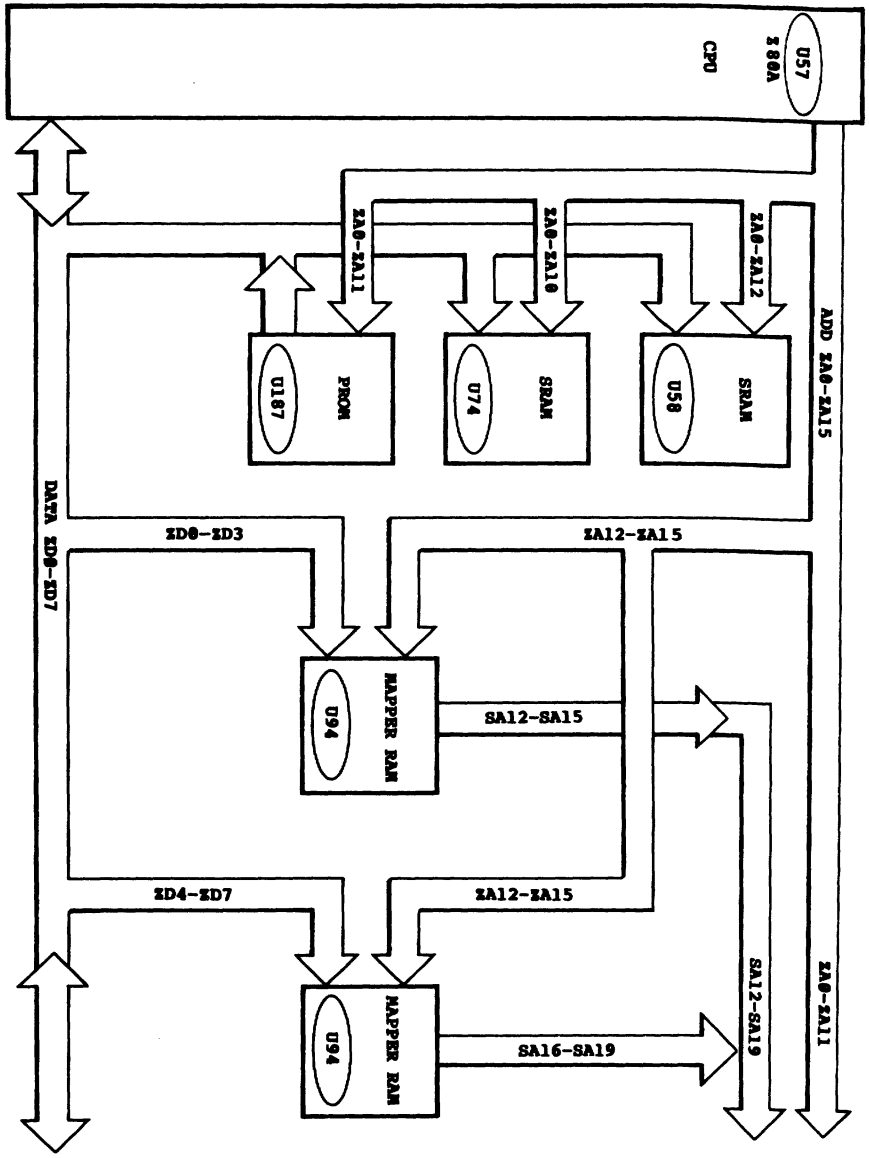
Memory Mapping

The Z80A has sixteen address lines which allow it to access up to 64 Kbytes of memory. The PM can have up to 1 Mbyte of memory. This means that, in order to access 1 Mbyte of memory, twenty address lines are needed. Address bus bits 0-11 go to the memory controller while bus bits 12-15 go to the memory mapping RAM's (U94 and U97), which are decoded into eight address lines (bus bits 12-19). These eight address lines go to the memory controller to produce a 20-bit address bus.

Serial I/O And Workstations

The Serial I/O (SIO) contains two RS-422 ports with port A as the workstation port and port B as the daisy-chain network port. Port B also allows for direct access to the Z80A by a diagnostic console. A jumper configuration change (see Appendix A) is required for this. The SIO 800 KHz baud rate is generated by the clock generator (U7) which also generates the 800 KHz receive clock to the workstations.

Figure 2-10
Local Memory



Port A sends out the TXDA signal to select the one workstation out of the possible sixteen that is latched in the user ID and diagnostics latch (U105). This latch output is also used for diagnostics at power-up. When the diagnostics have been completed, it latches the binary-coded user select address. The ZLK MEM line locks the memory area that the Z80A is using. This allows the processor to complete its operation before the memory area is accessed. The INHIBIT BUS RQ signal is used to establish the priority of the expansion cards or the workstations. The -Z PROM OFF signal allows the EPROM memory area to be masked off.

Counter-Timer Circuit

The CTC (Counter-Timer Circuit) is a four channel device of which only three are currently being used. The CTC is used as an interrupt controller to control and prioritize the following interrupts, which are listed from the highest to lowest in priority:

-INT 186 TO Z
-INT X1 TO Z
-INT X2 TO Z

In response to an interrupt signal, the CTC issues an interrupt to the Z80A CPU, which in turn interrupts the 80186. The 80186 determines the source of the interrupt by reading the internal registers of the CTC.

Expansion Slots

There are two expansion card slots mounted on the main board. Slots X1 (P8) and X2 (P7) are used for system expansion including the intelligent interface tape backup. An expansion card may contain its own DMA controller for direct access to main memory. The expansion card must be 8-bit to access the 8-bit Z80A bus. On power-up, the processor checks bits 1 and 2 of the buffer (U62) to determine if the slots are occupied. For more information on the expansion slots, refer to Chapter 3.

TAPE BACKUP

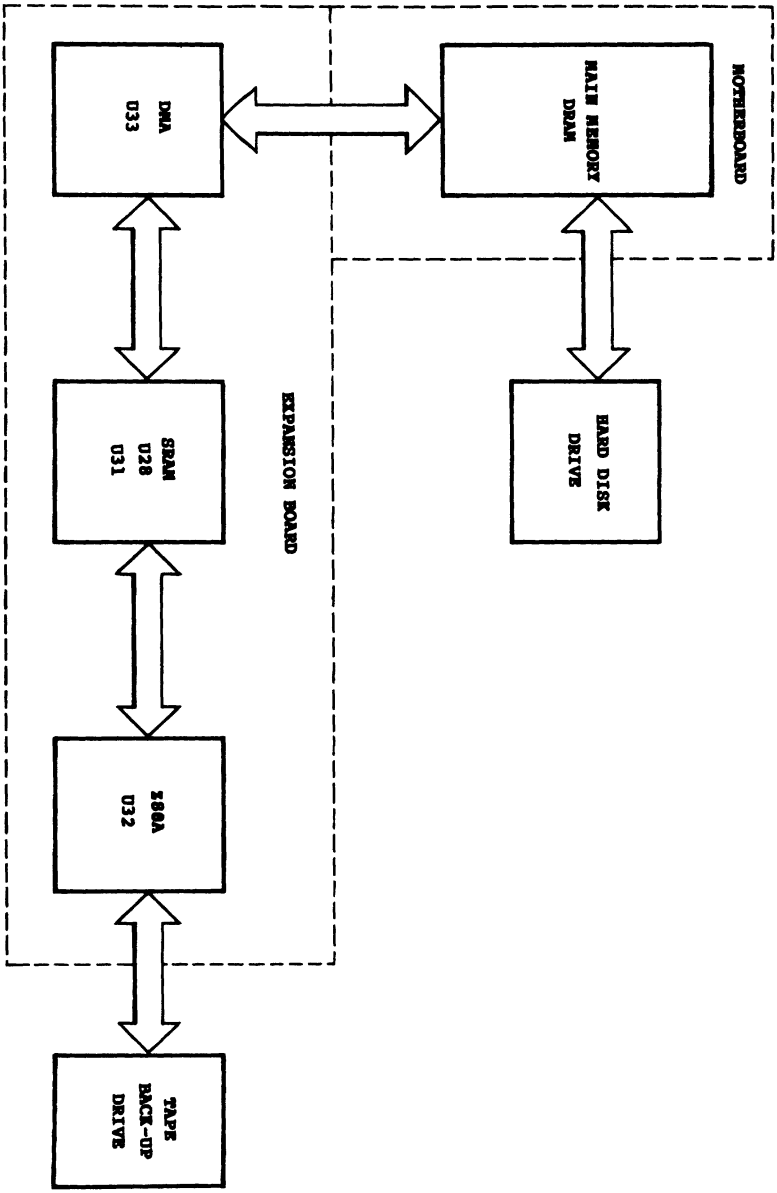
The tape backup (see Figure 2-11) has an intelligent interface that can access the main memory on the 8-bit processor bus. The tape expansion board can be installed in either the X1 or X2 expansion slot but there are jumper requirements (see Appendix A). The tape backup has a storage capacity of 20 Mbytes. The tape expansion board has a DMA and a processor control section.

The local memory is made up of 8 Kbytes of EPROM with a 4 kbyte option, and 4 Kbytes of static RAM with an 8-kbyte or 16-kbyte option.

Tape Operation

The 80186 moves data from the hard disk to main memory on the main board. This occurs during the CPU operating cycle.

Figure 2-11
Tape Backup



The DMA requests the 8-bit data bus from the two processors on the main board, and when acknowledged, accesses the bus. All 8-bit functions occur during the Z80A operating cycle. The DMA fetches the data memory address and moves the data to the local static RAM. The DMA continues this process to keep the RAM full as long as there is data in main memory for the tape backup.

The Z80A on the tape expansion board provides the local intelligence to access the main memory and communicate with the 80186 microprocessor. It controls the tape drive interface and runs on a 4-MHz clock. The processor moves data from the static RAM to the tape drive in the streaming mode.

The DMA and processor run concurrent operations to keep the RAM buffer full to maintain the streaming of the tape.

3. HARDWARE PROGRAMMING

This chapter provides the programmer with the information necessary to interface with the system hardware. Included in the chapter are discussions on I/O port addresses, coding tables, command codes, and registers for the 80186, Z80A, and the tape expansion card.

80186 MICROPROCESSOR

The 80186 is a 16-bit internal and external HMOS microprocessor device with a 20-bit address bus. The 80186 performs all DMA transfers to the floppy and hard disk drives, and handles interrupts from the Z80A 8-bit processor and from peripheral devices. This microprocessor is also responsible for performing diagnostics on the 16-bit side of the system at system initialization. For complete information on the 80186, refer to the **Intel iAPX 86/88, 186/188 User's Manual.**

80186 Interrupts

The interrupt lines INT0 through INT3 on the 80186 provide four prioritized levels of interrupts to service hardware requirements, with INT0 having the highest priority. The interrupt levels are shown in Table 3-1.

To properly service interrupts, the system software must program the interrupt control registers of the 80186 into the fully-nested mode (non-cascade, non-iRMX operation). All interrupts are maskable.

Interrupts from the 80186 are applied on a SETI line to the reset pin of a set-reset flip-flop. The acknowledgement from the Z80A 8-bit side or from an expansion card returns the flip-flop to the set state. A system reset also places the flip-flop into the set state.

Table 3-1
80186 Interrupt Priorities

Level	Input	Device
0	INT0	Serial printer or console port.
1	INT1	Parallel printer, Z80 microprocessor, expansion card slot 1, or expansion card slot 2.
2	INT2	Winchester hard disk controller board.
3	INT3	Floppy disk controller board.

To determine which device is sending an interrupt on INT1, the 80186 polls bits 4 through 7 of the parallel printer and interrupt status buffer at address %0120. Refer to Figure 3-1 for the bit assignments to the buffer.

Figure 3-1
Parallel Printer and Status Buffer (%0120)

```
Bit   7   6   5   4
      |   |   |   |
      |   |   |   0 = Parallel printer
      |   |   |       interrupt
      |   |   |   1 = Normal input
      |   |   |
      |   |   0 = Normal input
      |   |   1 = Z80 interrupt
      |   |
      |   0 = Normal input
      |   1 = Expansion card slot 1
      |       interrupt
      |
      0 = Normal input
      1 = Expansion card slot 2 interrupt
```

80186 Read-Only Memory

Standard read-only memory for the 80186 processor is organized as 4K x 16 bits in two chips, optionally expandable to 8K x 16 bits. Standard ROM is located in address space %FE000 through %FFFFF. The size of the ROM is contained in the firmware itself, thus eliminating the need to change jumpers or switch settings with a change in ROM.

The UCS pin of the 80186 decodes the memory address of the ROM devices. After system reset, the UMCS register must be initialized to the ROM block size and programmed with one wait for the ROM devices.

80186 I/O Port Selection

System I/O port selection is performed through the six peripheral chip select lines PCS0 through PCS5 of the 80186. The lines are controlled through the PACS register and the MPCS register. These registers set the programmable base address (PBA) of the peripherals and specify whether the peripherals are mapped into memory or I/O space. Both registers must be accessed to activate the peripheral chip select lines.

The PACS register defines the starting address of the peripheral chip select block. Refer to Table 3-2 for the bit assignments to the register.

Table 3-2
PACS Register

Bits	Function
15 - 6	Correspond to bits 19 through 10 of the 20-bit programmable base address (PBA) of the peripheral chip-select block.
5 - 3	Set to 1.
2 - 0	Specify the READY mode and the wait states, and are encoded as follows: Bits 2 1 0 0 0 0 = Zero wait states, external RDY also used. 0 0 1 = One wait state inserted, external RDY also used.

Table 3-2 continued

Bits	Function
2 - 0	Bits 2 1 0 0 1 0 = Two wait states inserted, external RDY also used. 0 1 1 = Three wait states inserted, external RDY also used. 1 0 0 = Zero wait states, external RDY ignored. 1 0 1 = One wait state inserted, external RDY ignored. 1 1 0 = Two wait states inserted, external RDY ignored. 1 1 1 = Three wait states inserted, external RDY ignored.

Table 3-3 shows the address range of each peripheral chip select with respect to the PBA contained in the PACS register.

Table 3-3
PCS Address Ranges

PCS Line	Active Between Locations
PCS0	PBA - PBA+127
PCS1	PBA+128 - PBA+255
PCS2	PBA+256 - PBA+383
PCS3	PBA+384 - PBA+511
PCS4	PBA+512 - PBA+639
PCS5	PBA+640 - PBA+767

The MPCS register controls the mode of operation for the peripheral chip select lines. Refer to Table 3-4 for the bit assignments. Bit 6 of this register determines whether the selects are mapped into memory or I/O space. A one for this bit maps the peripherals into memory space. A zero maps the peripherals into I/O space.

Table 3-4
MPCS Register

Bits	Function
15	Set to 1.
14 - 8	Define the size of the memory block. Only one bit can be set at a time.

Bits 14 - 8	Total Block Size	Individual Select Size
0000001	8K	2K
0000010	16K	4K
0000100	32K	8K
0001000	64K	16K
0010000	128K	32K
0100000	256K	64K
1000000	512K	128K

7	Set to 1.
6	If 0, the peripherals are mapped into memory space. If 1, the periherals are mapped into I/O space.

Table 3-4 continued

Bits	Function
5 - 3	Set to 1.
2 - 0	Specify the READY mode. Refer to Table 3-3 for the coding.

The I/O port addresses for the 16-bit processor are listed in Table 3-5. The port addresses assume that the programmable base address of the PACS register is zero, that the relocation register is in the default %20FF, and that the ports are I/O mapped. This arrangement assures that the I/O space for the internal control register block is located outside of the low order address space.

Table 3-5
80186 I/O Port Addresses

Address	Function
%0000	Printer Control/Diagnostic Indicators Latch Select
%0004	Reset FDC
%0008	Release FDC Reset
%000C	Reset HDC
%0010	Release HDC Reset
%0014	Reset Z80
%0018	Release Z80 Reset
%0020	Printer Data Latch Select
%0040	Floppy Disk Drive Control Latch
%0060	Printer Interrupt Acknowledge
%0080 - %009E	DUART Device Registers

Table 3-5 continued

Address	Function
%0120	Parallel Printer and Interrupt Status Buffer Select
%0180 - %018E	Floppy Disk Controller Device Registers
%0200 - %020E	Winchester Disk Controller Board Registers
%0280	Spare 6
%0290	Spare 7
%02A0	Set Interrupt 80186 to Z80
%02B0	Set Interrupt 80186 to Expansion Card 1
%02C0	Set Interrupt 80186 to Expansion Card 2
%02D0	Interrupt Acknowledge 80186 to Z80
%02E0	Interrupt Acknowledge 80186 to Expansion Card 1
%02F0	Interrupt Acknowledge 80186 to Expansion Card 2
%FF00 - %FFFE	80186 Internal Registers

Z80 MICROPROCESSOR

The task of interfacing with the workstations is performed by the 8-bit side of the motherboard with a Z80A CPU running at 4 MHz.

Z80 Interrupts

Interrupts from the Z80A SIO and Z80A CTC are daisy-chained to the Z80A CPU, with the SIO device having the highest priority. Other interrupts are generated at timer inputs 1 through 3 of the CTC. These interrupts are listed in Table 3-6.

Table 3-6
Z80A Interrupts

Timer Channel	Function
1	Interrupt from 80186 to Z80A CPU
2	Interrupt from expansion slot 1 to Z80A
3	Interrupt from expansion slot 2 to Z80A CPU

The timer channel is loaded with a count of 1; an incoming interrupt decrements this count to 0 to generate a CTC interrupt. The expansion cards can also directly interrupt the 80186, as previously described in Table 3-3. Interrupt acknowledge signals to these devices are sent through the Z80A CPU I/O ports at the addresses listed in Table 3-7.

Interrupts are sent from the Z80A CPU to the 80186 through the Z80A CPU port address %06.

Z80 Read-Only Memory

The 8-bit processor ROM occupies the lower 4 Kbytes of Z80A CPU address space from %0000 through %0FFF. The section also has a local RAM area in the upper Z80A CPU space from %F000 through %FFFF.

Standard local memory is expandable with one or two 8K x 8 static RAM devices to begin local RAM at %E000 or %C000.

Z80A I/O Ports

Table 3-7 lists the I/O port addresses for the 8-bit processor section.

Table 3-7
Z80A I/O Port Addresses

Address	Function
%00	Interrupt Acknowledge Z80A CPU to 80186
%02	Interrupt Acknowledge Z80A CPU to Expansion Slot 1
%04	Interrupt Acknowledge Z80A CPU to Expansion Slot 2
%06	Interrupt Z80A CPU to 80186
%08	Configure Z80A Buffer Select
%0A	Spare 5
%0C	Set User ID and Misc. Latch Enable
%0E	Set Memory Map Enable
%10 - %13	Z80A CTC Internal Registers
%20 - %23	Z80A SIO Internal Registers
%60 - %FF	Expansion Card I/O

The first four bits of the set user ID and misc latch at address %0C select one of the sixteen workstation channels for input. The latch is sequenced as follows:

Bit 3	Bit 2	Bit 1	Bit 0	User No.
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4

This continues in binary sequence up to workstation sixteen:

Bit 3	Bit 2	Bit 1	Bit 0	User No.
1	1	1	1	16

Bits 0 through 3 of this latch are also used to light the diagnostic LED indicators 1 through 4. These indicators are lit when the bits are low.

The functions of bits 4 through 7 of the latch are listed in Table 3-8.

Table 3-8
Set User ID and Misc Latch
(%0C)

Bit	Function
4	Network Transmit Enable - Enables transmission on the RS-422 network channel to allow communications between multiple PM systems.
5	8-Bit Processor Main Memory Locking - activates the main memory locking feature of the 16-bit processor section.
6	Inhibit Bus Request - Inhibits a bus request from an expansion card when the cards and the Z80A CPU simultaneously request the section data and address busses.
7	Disable 8-Bit Processor ROM - Frees the address space normally used by the ROM for memory mapping.

When writing to a portion of this latch, care must be taken to preserve the remaining bit values.

The configure Z80A buffer select is read at address %08. The bit assignments for the buffer are listed in Figure 3-2.

Figure 3-2
Configure Z80A Buffer Select
(%08)

```
Bits
7  6  5  4  3  2  1  0
|  |  |  |  |  |  |  |
|  |  |  |  |  |  |  1 = Normal operation
|  |  |  |  |  |  1 = No expansion card in
|  |  |  |  |  |     slot 1
|  |  |  |  |  |  0 = Expansion card
|  |  |  |  |  |     present in slot 1
|  |  |  |  |  1 = No expansion card in
|  |  |  |  |     slot 2
|  |  |  |  |  0 = Expansion card present
|  |  |  |  |     in slot 2
|  |  |  |  Spare for expansion cards
|  |  |  Spare for expansion cards
|  |  Spare for expansion cards
|  Spare for expansion cards
Not used
```

Z80A Processor Section Reset

The 8-bit processor section is reset at 80186 I/O port address %0014. This reset includes the expansion card slots. After reset, the 8-bit processor section must be software released at 80186 I/O port address %0018 to begin operation. After release, the Z80A CPU executes a self-diagnostic test as described in Appendix C.

MAIN MEMORY

Main memory is contained in 64K x 1 dynamic RAM devices. Standard memory is 256 Kbytes, expandable to 512 Kbytes with an add-on board, and to 1 Mbyte with 256K x 1 dynamic RAM devices. This area can be accessed by either the 16-bit processor or the 8-bit processor sections under control of the dual port RAM controller. When the 8-bit section, including an 8-bit expansion card, accesses main memory, the 20-bit address for the controller is produced through a mapper in the 8-bit section. Generation of this mapped address is described later in this section.

Dual Port RAM Controller

Main memory is controlled through an Intel 8207 Advanced Dynamic RAM Controller device. This device provides independent access to main memory by each processor section on a last-access-served-first priority scheme. The 8207 generates all control signals for memory, including programmable refresh and data transfer acknowledge. A detailed description of the 8207 is contained in the **Intel Microsystem Components Handbook, Volume I.**

Port A of the 8207 is connected to the 16-bit processor. This port runs in the slow-cycle, synchronous, status interface mode of the controller. There are no wait states for a normal memory access with 150 nanosecond RAM devices.

Port B of the 8207 services the 8-bit processor and expansion card bus. Port B runs in the slow-cycle, asynchronous, command interface mode of the controller. One wait state is required for a normal memory read and two wait states for an normal memory write.

If one port attempts to access the memory while the other port is active, the port attempting the access must wait from 1 to 5 wait states for 80186 memory cycles (125 nanoseconds/wait), or 3 to 5 wait states for Z80A memory cycles (250 nanoseconds/wait). Longer wait states are necessary if the controller is refreshing memory during a simultaneous request.

Address lines from each processor are multiplexed to a single set of lines for the 8207. Address bit 0 selects the high or low byte during the access along with high byte enable lines -BHE for the 80186, or -ZRBH for the Z80A. Jumper options finalize the memory selection, as described under Memory Organization below.

The 8207 is programmed through a hardware initialization shift register during system reset. Table 3-9 lists these default states.

Table 3-9
Default Initialization of the Memory Controller

Bit	Set/Function
0	Low. Non-ECC mode.
1	Low. Port A set asynchronous.
2	Low. Port B set synchronous.
3	High. Slow cycle iAPX 86 mode.
4	High. Slow (150 nanoseconds) RAM.
5/6	Low. RAS and CAS to banks as selected by bank select inputs to memory controller:

(BS1)	(BS0)	Utilization
0	0	RAS0/CAS0 to Bank 0
0	1	RAS1/CAS1 to Bank 1
1	0	RAS2/CAS2 to Bank 2
1	1	RAS3/CAS3 to Bank 3

7/8/9	Low. One refresh each 15.6 microseconds, no frequency deviation. Optionally, bit 9 is tied high to give one refresh every 7.8 microseconds with no frequency deviation for some 256K RAM devices. Jumpers are required as listed in Appendix B.
10	Low. Memory cycle is not extended.
11	Low. Fast (8 MHz) 80186 clock.
12	Low. In priority contention, the most-recently used port is selected.
13	Low. Test mode is not selected.
14/15	Low. Reserved.

Memory Organization

Main memory occupies the address space from %00000 through %3FFFF in the standard 256 Kbyte memory version, from %00000 through %7FFFF in the 512 Kbyte option version, and from %00000 through the lower boundary of system ROM in the 1 megabyte system. With standard 8 Kbyte ROM, this boundary is at %FE000. When changed, the new size of ROM and the number of wait states must be programmed into the UMCS register of the 80186.

Referring to Table 3-9, bits 5 and 6 of the initialization register set up the bank interleaving feature of the 8207. Interleaving overlaps the start of the next RAM access cycle with the RAM precharge period of the previous cycle. This feature optimizes memory bandwidth for the PM system.

For systems with 256 Kbytes of memory, banks 0 and 1 are selected using address line R1 to input BS0 of the 8207. For 512 Kbyte memories made up of 64 Kbyte devices, address lines R1 and R18 are tied to controller inputs BS0 and BS1, with all four banks of memory selected. When 256 Kbyte devices are used, only bank 0 is selected with no bank interleaving. The 1 megabyte memory uses interleaving in banks 0 and 1 with the address lines utilized as for the 256 Kbyte configuration. Physical selection of these memory configurations is accomplished with jumper options as listed in Appendix B.

Some 256 Kbyte dynamic RAM devices require a refresh every 7.8 microseconds, accomplished by setting the PD9 bit of the 8207 high as listed in Table 3-9.

Memory Locking

A memory-locking feature of the 8207 prevents access to a portion of memory by either processor section. This feature may be used to allow one side to complete processing a block of data before allowing the other section to access the area. The lock feature is multiplexed between the two processor sections; when port A (80186) is selected, the lock feature originates at port A, and when port B (Z80A CPU) is selected, the lock originates at port B.

To use the lock feature, the 80186 must execute a lock prefix instruction and assert the -LOCK line to the 8207. When the Z80A asserts a lock, it writes a 1 to bit 5 of the set user ID latch on the 8-bit side, which is transferred through an address buffer to the lock input of the 8207. Refer to the schematic diagrams and to the 8-bit I/O port listing in Table 3-7. Expansion cards may use lock in a similar manner to the Z80A.

Z80A CPU Main Memory Mapping

Memory mapping, using two high-speed bipolar RAM devices, is used to translate the 16-bit Z80A CPU address into a 20-bit address for main memory. The upper four address bits, on lines ZA15 through ZA12, address the mapper RAM to produce main memory upper address lines SA19 through SA12. The lower Z80A CPU address lines, ZA11 through ZA0 address main memory as SA11 through SA0.

Using memory mapping, any 4 Kbyte segment of main memory can be addressed by loading the upper eight bits of its address into the mapper RAM. Using the four address bits to mapper RAM, up to sixteen such segments can be stored for mapping. For example, if the Z80A CPU wishes to address the 4 Kbyte area from %2E000 through %2EFFF of main memory, it loads the value %2E into mapper RAM. If the mapper RAM location chosen for this segment is the one addressed, the upper four address bits would be:

ZA15	ZA14	ZA13	ZA12
0	0	1	1

Then the Z80A CPU would produce %3000 through %3FFF to access %2E000 through %2EFFF. Any other mapper RAM location could have been chosen to map this address, with a corresponding change in the Z80A CPU address to mapper RAM.

Due to possible conflicts between 8-bit processor ROM, local memory, and mapper RAM, several cautions must be observed with mapped addresses:

* The area between %0000 and %0FFF must not be used unless the 8-bit processor ROM is mapped off.

* The area between %C000 and %FFFF must not be used if the local RAM consists of two 8K x 8 devices.

* The area between %E000 and %FFFF must not be used if the local RAM consists of one 8K x 8 device.

* The area between %F000 and %FFFF must never be used because it is always occupied by local RAM and cannot be mapped off.

The system determines the areas of 8-bit processor ROM and local memory during power-up and reset, and automatically inhibits mapper RAM access.

Mapper RAM is located at Z80A CPU I/O port %2E. Load the mapper address into bits 4 through 7 of register B of the Z80A CPU, using bits 12 through 15 for the address. Next, put the map data out using register A, address %2E. Because the RAM devices invert the data, the data to be written must be in complemented form.

EXPANSION CARD SLOTS

The PM system can accommodate two 8-bit or 16-bit expansion cards in the x1 and x2 slots on the main board. The expansion cards can be intelligent or slave to the Z80A microprocessor.

A slave expansion card decodes its address and responds with -XIORQ and -XRD for a read request, and -XIORQ and -XWR for a write request. Hardware timing must conform to the Z80A family timing, with an extra delay due to card buffers. If the card requires wait states, the expansion card must assert the signal -XZ WAIT. There are no provisions for slave expansion card DMA; however, an expansion card can contain its own DMA controller for independent operations. Refer to Table 3-7 for the expansion card I/O port assignments.

Only intelligent cards can access main memory. The data bus for the expansion cards is either 8-bit on lines XD7 through XD0, or 16-bit on lines XD15 through XD0. To use a 16-bit data bus, the expansion card sets the XBYTE line low; the default assumes an 8-bit data bus.

If a 16-bit address is provided to main memory from an expansion card, it uses the address bus from the 8-bit processor section through its own lines XZA15 through XZA0 and the memory mapper by setting the XUSEMAP line high. If the expansion card provides a 20-bit address, it accesses main memory on lines XSA19 through XSA12, and lines XZA11 through XZA0. Use of the memory map is assumed; if the expansion card provides a 20-bit address to main memory, it must disable the map by setting its XUSEMAP signal low.

Because some data and address bus lines, and control lines -ZMREQ, -ZIORQ, -ZRD, and -ZWR, are shared by the Z80A CPU and the expansion card, the card must request the buses from the Z80A CPU before each operation. The Z80A CPU can override this request by setting bit 6 of the set user ID and miscellaneous latch low.

To use the buses, the expansion card sets its line -INT X TO Z low and waits for the -BUS AK return signal from the Z80A CPU. Expansion slot 1 has the higher priority, by virtue of its daisy-chained position. Expansion card devices do not have to be in the Z80A family, but the Z80A rules for bus request and acknowledge must be observed. An expansion card can use the lock feature of the 16-bit processor section in the same manner as the 8-bit processor section. The expansion card lock signal is -XLOCK.

System Facilities for Expansion Cards

After power-on or reset, and its self-diagnostics, the Z80A CPU checks bits 1 and 2 of the configure Z80A buffer to determine if expansion cards are installed (refer to Figure 3-2). These bits are generated on the expansion card, and are active low to indicate card presence. Next, the CPU reads a configuration port on the expansion card to determine the card's identification. This port is intended to be configured in a DIP switch or with jumpers, and is read as an I/O port. Bits 3 through 6 of the configure Z80A buffer are available for general purpose signals. These signals must be of the open-collector type.

Timer channels 0 and 1 of the 80186 are directly useable by the expansion cards. These channels are clocked at 1.6 MHz.

PARALLEL PORT

The parallel port has three ports for data transfer and control. Table 3-10 and Figures 3-3 and 3-4 give their addresses and bit assignments.

Table 3-10
Data Output Port
(%0020)

Bit	Signal	Pin Num.
0	Data 0	2
1	Data 1	3
2	Data 2	4
3	Data 3	5
4	Data 4	6
5	Data 5	7
6	Data 6	8
7	Data 7	9

Figure 3-3
Control Signal Input Port
(%0120)

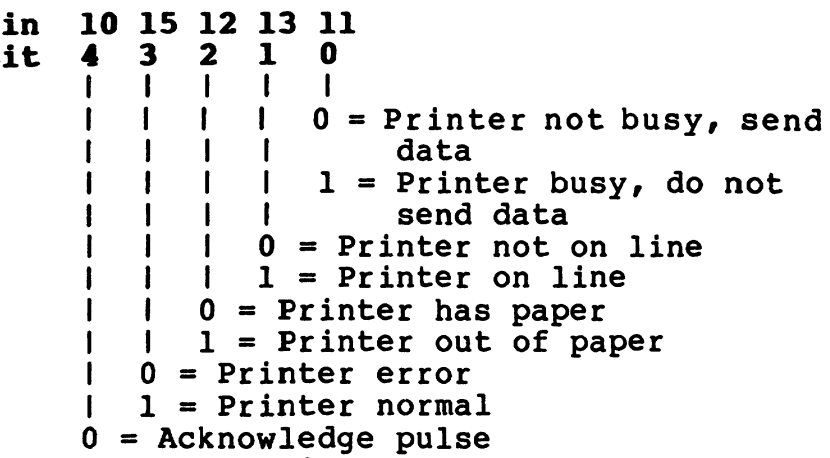


Figure 3-4
Output Control Port
(%0000)

```
Pin   10 17 16 14 1
Bit   4  3  2  1  0
      |  |  |  |  |
      |  |  |  |  0 = Normal setting
      |  |  |  |  1 = Pulse bit to 1 to
      |  |  |  |      send data to the
      |  |  |  |      printer
      |  |  |  0 = Normal setting
      |  |  |  1 = Auto line feed after
      |  |  |      carriage return
      |  |  0 = Pulse bit must be set low for
      |  |      at least 50 microseconds to
      |  |      initialize the printer
      |  |  1 = Normal setting
      |  0 = Normal setting
      |  1 = Allows printer to read output
      0 = Printer interrupt disabled
      1 = INT1 interrupt enabled on printer
          acknowledge signal pulse
```

SERIAL AND SYSTEM CONSOLE PORTS

The serial port and the system console port are controlled through the DUART chip and its two independent, asynchronous channels. Channel A controls the console port, and channel B the serial port. Both ports are configured DCE and can be programmed from 50 to 9600 baud. Parity checking, character lengths of from 5 to 8 bits, and eight interrupt masking conditions are also supported.

The independent channels are programmed by initializing the appropriate channel registers. Table 3-11 lists the DUART registers and their addresses.

Table 3-11
DUART Register Addresses

Address	Register
%0080	MR1A: Mode Register 1
%0090	MR1B: Mode Register 1
%0080	MR2A: Mode Register 2
%0090	MR2B: Mode Register 2
%0082	CSRA: Clock Select Register
%0092	CSRB: Clock Select Register
%0084	CRA: Command Register
%0094	CRB: Command Register
%0082	SRA: Status Register
%0092	SRB: Status Register
%009A	OPRC: Output Port Configuration Register
%0088	ACR: Auxiliary Control Register
%0088	IPCR: Input Port Change Register
%008A	ISR: Interrupt Status Register
%008A	IMR: Interrupt Mask Register
%008C & %008E	CTUR/CTLR: Counter/Time Register

Mode Register 1 - MR1A & MR1B

The format of the asynchronous data communications is specified through the Channel A Mode Register 1 (MR1A) for the console port and the Channel B Mode Register 1 (MR1B) for the serial port. The bit definitions for both registers are identical and are listed in Table 3-12.

Table 3-12
Mode Register 1
MR1A & MR1B

Bit	Assignment
0	Bits per character
1	Bits per character
2	Parity type select
3	Parity mode select
4	Parity mode select
5	Error mode select
6	Receiver interrupt
7	Receiver request-to-send control

Bits 0 & 1 These bits set the number of bits in each transmitted or received serial character. They are encoded as follows:

Bit 0	Bit 1	Character Length
0	0	5
1	0	6
0	1	7
1	1	8

Bit 2 This bit designates whether the parity number will be even or odd.

Bit 2	Parity Number
0	Even
1	Odd

Bits 3 & 4 — These bits enable the parity check.

Bit 3	Bit 4	Parity Check
0	0	Parity enabled
1	0	Force parity
0	1	Parity disabled
1	1	Multiple drop mode

Bit 5 — This bit sets the operating mode of the status bits to either character-by-character status or an accumulation of the status for all characters since the last reset error command (block).

Bit 5	Error Mode
0	Character-by-character
1	Block

Bit 6 — This bit selects either the receiver ready status or the FIFO full status to be used for 80186 interrupts.

Bit 6	Interrupt Select
0	Receiver ready status
1	FIFO full status

Bit 7 — This bit controls the deactivation of the request to send signal (RTSAN) on the OP0 output to prevent an overrun in the receiver.

Bit 7	Assignment
0	Active RTSAN output
1	Deactivate

Clock Select Registers - CSRA & CSRB

The DUART provides each channel with a programmable baud rate generator capable of taking the clock input and dividing it by any divisor from 1 to 65,535. The output frequency of the baud rate generator is sixteen times the baud rate. Channel A Clock Select Register (CSRA) sets the baud rate for the console port, and Channel B Clock Select Register (CSRB) sets the baud rate for the serial port.

Table 3-13 lists the bit assignments for bits 4 through 7 of the CSRA. These bits set the baud rate for the channel receiver.

Table 3-13
CSRA

				Baud Rates	
7	**6**	**5**	**4**	**ACR(7) = 0**	**ACR(7) = 1**
0	0	0	0	50	75
0	0	0	1	110	110
0	0	1	0	134.5	134.5
0	0	1	1	200	150
0	1	0	0	300	300
0	1	0	1	600	600
0	1	1	0	1200	1200
0	1	1	1	1050	2000
1	0	0	0	2400	2400
1	0	0	1	4800	4800
1	0	1	0	7200	1800
1	0	1	1	9600	9600
1	1	0	1	Timer	Timer
1	1	1	0	IP4-16X	IP4-16X
1	1	1	1	IP4-1X	IP4-1X

NOTE: IP4 refers to a general purpose input line on the DUART.

Bit 7 of the Auxiliary Control Register selects which of the two sets of baud rates the baud rate generator is to generate.

The definitions for bits 0 through 3 of the CSRA for the channel A transmitter are identical to bits 4 through 7, with the following exceptions:

Bits				**Baud Rates**	
0	**1**	**2**	**3**	**ACR(7) = 0**	**ACR(7) = 1**
1	1	1	0	IP3-16X	IP3-16X
1	1	1	1	IP3-1X	IP3-1X

The definitions of bits 4 through 7 for CSRB, which set the baud rate for the channel B receiver, are identical to the corresponding bits in the CSRA register, with the following exceptions:

Bits				**Baud Rates**	
4	**5**	**6**	**7**	**ACR(7) = 0**	**ACR(7) = 1**
1	1	1	0	IP6-16X	IP6-16X
1	1	1	1	IP6-1X	IP6-1X

The definitions of bits 0 through 3, which set the baud rate for the channel B transmitter, are identical to bits 4 through 7, with the following exceptions:

Bits				Baud Rates	
0	1	2	3	ACR(7) = 0	ACR(7) = 1
1	1	1	0	IP6-16X	IP6-16X
1	1	1	1	IP6-1X	IP6-1X

Interrupt Status Register - ISR

This register provides the status of all potential interrupt sources. If a bit in the ISR is set at "1" and the corresponding bit in the IMR register is also a "1", the interrupt line INTRN goes low, generating an interrupt. Refer to Table 3-14 for the register bit assignments.

Table 3-14
Interrupt Status Register

Bit	Description
0	The function of this bit is identical to bit 2 of the SRA register.
1	Channel A Receiver Receiver Ready or FIFO Full - The function of this bit is programmed by bit 6 in MR1A. If programmed as receiver ready, it indicates that a character has been received in channel B. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO, causing the FIFO to become full.
2	Channel A Change in Break - This bit goes to 1 when the Channel A receiver detects the beginning or the end of a received break.
3	Counter Ready - In the counter mode, this bit is set when the counter reaches terminal count. In the timer mode, this bit is set once each cycle of the square wave.

Table 3-14 continued

Bit	Description
4	Channel B Transmitter Ready - The function of this bit is identical to bit 2 of the SRB register.
5	Channel B Receiver Ready or FIFO Full - The function of this bit is identical to bit 1, with the exception that it operates on channel B.
6	Channel B Change in Break - The function of this bit is identical to bit 2, with the exception that it operates on Channel B.
7	This bit goes to 1 when a change of state occurs on input line IP3.

Command Registers - CRA & CRB

The CRA register provides commands to the console port on channel A. The CRB register provides commands to the serial port on channel B. The bit assignments to both registers are identical and are listed in Table 3-15.

Table 3-15
Command Register

Bit			Description
0			Enable Channel Receiver - Enables operation of the channel receiver.
1			Disable Channel Receiver - A 1 for this bit immediately terminates the operation of the receiver.
2			Enable Channel Transmitter - Enables operation of the channel transmitter.
3			Disable Channel Transmitter - Set this bit to 1 to terminate transmitter operation and reset the TxRDY and TxEMT status bits.
6	5	4	
0	0	0	No command.
0	0	1	Reset MR pointer - Causes the channel A MR pointer to point to MR1.
0	1	0	Reset receiver - Resets the channel receiver as if a hardware reset had been applied.
0	1	1	Reset transmitter - Resets the channel transmitter as if a hardware reset had been applied.
1	0	0	Reset error status - Resets error bits 4 through 7 of the status register.

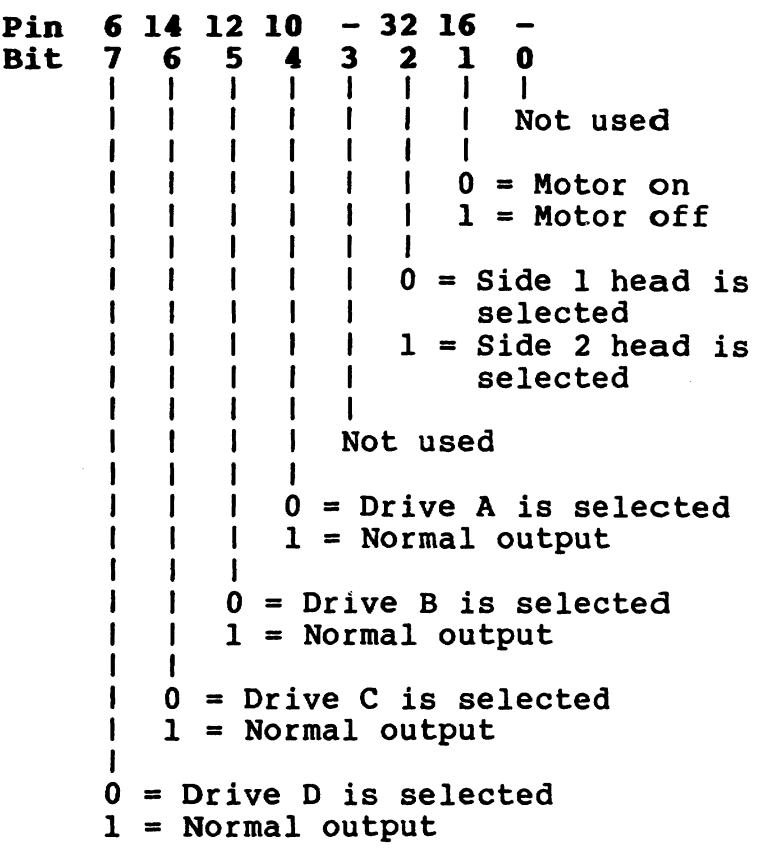
Table 3-15 continued

Bit			Description
6	5	4	
1	0	1	Reset channel break change interrupt - Changes bit 2 in the interrupt status register to 0.
1	1	0	Start break - Forces the TXDA output low.
1	1	1	Stop break - Causes the TXDA line to go high within two bit times. TXDA will remain high for one bit time before the next character, if any, is transmitted.

FLOPPY DISK CONTROLLER

A Western Digital WD1770 controller generates the floppy disk control signals for the PM system. For complete information on the controller, refer to the **Storage Management Products Handbook** from Western Digital. Additional control signals are generated by the 80186 through the latch at address %0040. The 80186 must program this latch as part of a floppy disk access. Refer to Figure 3-5 for the latch bit assignments.

Figure 3-5
Floppy Disk Control Latch



The FDC has four registers accessible to the 80186. The registers and their addresses are listed in Table 3-16.

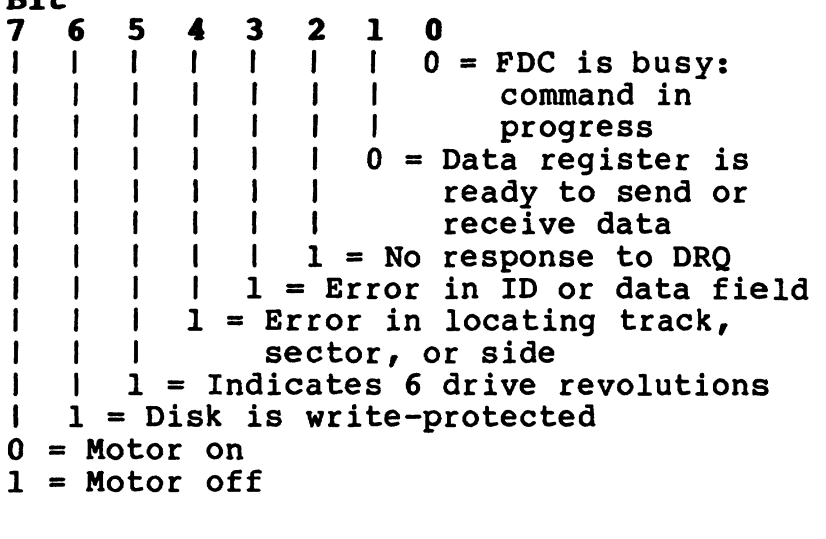
Table 3-16
FDC Register Addresses

Address	Register
%0180	Status and Command Registers
%0181	Track Register
%0182	Sector Register
%0183	Data Register

Status Register

The status register provides the 80186 with status information on the previously executed command and is accessible only when the R/W input is high. Refer to Figure 3-6 for the bit assignments to this register.

Figure 3-6
Status Register



Command Register

The command register holds the command currently being executed and is accessible only when the R/W input is low.

The WD1770 is capable of executing 11 commands. All commands are initiated by the 80186 with a byte transfer on lines D0 through D7. The commands are listed in Table 3-17. Table 3-18 contains a flag summary.

Table 3-17
FDC Commands

Command	Bit 7	6	5	4	3	2	1	0
Restore	0	0	0	0	h	V	r1	r0
Seek	0	0	0	1	h	V	r1	r0
Step	0	0	1	u	h	V	r1	r0
Step-in	0	1	0	u	h	V	r1	r0
Step-out	0	1	1	u	h	V	r1	r0
Read Sector	1	0	0	m	h	E	0	0
Write Sector	1	0	1	m	h	E	P	a0
Read Address	1	1	0	0	h	E	0	0
Read Track	1	1	1	0	h	E	0	0
Write Track	1	1	1	1	h	E	P	0
Force Interrupt	1	1	0	1	I3	I2	I1	I0

Table 3-18
Flag Summary

h = Motor On Flag (Bit 3)
h = 0, Enable spin-up sequence
h = 1, Disable spin-up sequence

Table 3-18 continued
Flag Summary

V = Verify Flag (Bit 2)
V = 0, No verify
V = 1, Verify on destination track

r1, r0 = Stepping Rate (Bits 1,0)

r1	r2	
0	0	= 6 ms
0	1	= 12 ms
1	0	= 20 ms
1	1	= 30 ms

u = Update Flag (Bit 4)
u = 0, No update
u = 1, Update track sector

m = Multiple Sector Flag (Bit 4)
m = 0, Single sector
m = 1, Multiple sector

a0 = Data address mark (Bit 0)
a0 = 0, Write normal data mark
a0 = 1, Write deleted data mark

E = 30ms Settling Delay (Bit 2)
E = 0, No delay
E = 1, Add 30ms delay

P = Write Precompensation (Bit 1)
P = 0, Enable write precomp
P = 1, Disable write precomp

I3 - I0 = Interrupt Condition (Bit 3-0)
I0 = 1, Don't care
I1 = 1, Don't care
I2 = 1, Interrupt on index pulse
I3 = 1, Immediate interrupt
I3 - I0 = 0, Terminate without interrupt

The FDC commands are described in the following pages.

SEEK: In response to this command, the FDC updates the track register as it issues stepping pulses. This continues until the contents of the track register and the data register are equal. This assumes that the data register is holding the location of the desired track number.

STEP: In response to this command, the FDC steps the disk drive with one stepping pulse. The direction of the step is the same as the previous step command.

STEP-IN: In response to this command, the FDC steps the drive towards track 76, and increments the track register by 1.

STEP-OUT: In response to this command, the FDC steps the drive towards track 0, and decrements the track register by 1.

READ SECTOR: In response to this command, the busy bit is set, and when the correct ID field is encountered, a sector is read from disk.

READ ADDRESS: In response to this command, the busy bit is set and the next ID field is read from disk.

READ TRACK: In response to this command, the head is loaded and the busy bit is set. reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse.

WRITE SECTOR: In response to this command, the busy bit is set, and when the correct ID field is encountered, a sector is transferred to disk.

FORCE INTERRUPT: This command can be loaded into the command register at any time. It is generally used to stop a multiple sector read or write command.

Track Register

This 8-bit register holds the number of the current head position. The register is incremented with each step-in command and decremented with every step-out command. During read and write operations, this register is compared with the track number in the ID field on the disk itself.

Sector Register

This 8-bit register holds the address of the desired sector. During read and write operations, the contents of this register are compared with the sector number in the ID field on the disk.

Data Register

This 8-byte register is used as a holding register for the byte of data being either written to or read from disk.

WINCHESTER DISK CONTROLLER BOARD

The Winchester disk controller board contains a WD1010-05 Winchester disk controller device to perform executive control over disk operations. To command the board, the system addresses a set of task file registers in the WD1010-05 with the I/O port address of each of the individual registers. Table 3-19 is a list of the individual registers, along with their I/O port addresses for the PM system.

Table 3-19
WD1010-05 Registers

Address	Read	Write
%0200	System Access	System Access
%0202	Error Flags	Write Precomp Cylinder
%0204	Sector Count	Sector Count
%020C	Sector Number	Sector Number
%0208	Cylinder Low	Cylinder Low
%020A	Cylinder High	Cylinder High
%020C	Sector/Drive/Head	Sector/Drive/Head
%020E	Status Register	Command Register

A detailed description of the WD1010-05 device is given in the **1984 Storage Management Products Handbook** from Western Digital.

Task File Register Functions

For a typical operation, the task file registers are written to, or read for status, and a command is given to the command register. The WD1010-05 then tri-states the address bus and executes the command. At the end of the operation, the task file is again opened to the system.

Error Register

Contains error flags for bad block detect, CRC data field, ID not found, aborted command, TK0000 error, and data address mark error. During read operations, the error register is read after the data is read out of buffer RAM, that is, after the byte count goes to zero. The error register bit assignments are listed in Table 3-20.

Table 3-20
Error Register

Bit	Description
0	Set during a read sector command if the address mark is not found after the proper sector ID is read.
1	Set only by the restore command. It indicates that the head is not positioned over track 000 after 1024 stepping pulses.
2	Set if a command was issued while the status register shows a drive fault (bit 5), or command disable (bit 6) condition. This bit is also set if an undefined command is issued.
4	Set when the desired cylinder, head, sector, or size parameter cannot be found after 8 revolutions of the disk. This bit is also set if a cyclic redundancy check error has occurred.
5	Not used. Forced to 0.

Table 3-20 continued

Bit	Description
6	Set if a data field CRC error has occurred or the data mark address has not been found.
7	Set if an ID field has been encountered that contains a bad block mark (used for bad sector mapping).

Write Precomp Register

Defines the starting cylinder number at which reduced write current (RWC) begins. This value is in the range 0 to 255, and is internally multiplied by four to obtain the actual cylinder.

Sector Count Register

Contains the number of sectors that are to be transferred to buffer RAM. Because this is a decrementing function, all zeros are written for a 256-sector transfer and a 1 is written for a 1 sector transfer.

Sector Number Register

Contains the starting sector of a transfer in the range 0 to 255. This register is incremented with every transfer.

Cylinder Number Low Register

Least significant 8 bits of the starting cylinder number in the range 0 to 1023.

Cylinder Number High Register

Carries the most significant bits of the starting cylinder number as bits 0(8) and 1(9). The other bits of this register are unused.

Sector/Drive/Head Register

Contains the sector size, drive number, and head number parameters for the operation:

```
Bits
7  6  5  4  3  2  1  0
|  |  |  |  |  |  |  |
|  |  |  |  |  0  0  0 = Select head 0
|  |  |  |  |  0  0  1 = Select head 1
|  |  |  |  |  0  1  0 = Select head 2
|  |  |  |  |  0  1  1 = Select head 3
|  |  |  |  |  1  0  0 = Select head 4
|  |  |  |  |  1  0  1 = Select head 5
|  |  |  |  |  1  1  0 = Select head 6
|  |  |  |  |  1  1  1 = Select head 7
|  |  |  |  |
|  |  |  0  0 = Select drive 1
|  |  |  0  1 = Select drive 2
|  |  |  1  0 = Select drive 3
|  |  |  1  1 = Select drive 4
|  |  |
|  0  0 = Sector size 256
|  0  1 = Sector size 512
|  1  0 = Sector size 1024
|  1  1 = Sector size 128
|  = Extension bit
```

Bit 7 is an extension bit that extends the data field by 7 bytes when ECC codes are used. When set to 1, CRC is not appended to the end of the data field; the data field becomes sector size + 7 bytes long.

The SDH byte written into the ID field is different than the SDH register contents. The recorded SDH byte does not have the drive number and contains a bad block in bit 7.

Status Register

Contains status bits for device busy, device ready, write fault (same as WF line), seek complete (same as SC line), data request (same as BDRQ line), command in progress, and error register flags set. The status register bit assignments are listed in Table 3-21.

Table 3-21
Status Register

Bit	Description
0	Set whenever any bits in the error register are set. This bit is reset when a new command is written into the command register.
1	Set when a command is being executed.
3	Set when the sector buffer should be loaded or read (depending on the command). It is reset upon completion of the operation.
4	Set during a seek, and reset when the head settling time has expired.
5	Indicates a fault condition at the drive when set. An interrupt is generated when this bit is set.
6	Must be set for commands to execute.

Table 3-21 continued

Bit	Description
7	Set whenever the disk is being accessed. Do not load commands into the command register when this bit is set. It is reset at the end of all commands except the read sector command. This bit is reset after the sector buffer is filled on the read sector command.

Command Register

This write-only register loads the desired command. A command begins to execute immediately upon loading. Do not load this register while bits 1 or 7 are set in the status register.

The command set consists of six commands: restore, seek, read, write sector, scan ID, and write format. Prior to loading a command, the task file registers must be set with the proper parameters. Except for the command register, the task file registers can be loaded in any order.

RESTORE - Restore heads. The restore command is usually used on a power-up condition. The head is stepped back to track 000. If, after 1024 stepping pulses, the head is not over track 000, bit 1 of the error flag is set. The head settling time determines the stepping rate. The rate entered into the rate field of the restore command is stored in an internal register and used in future commands with implied seeks (the default stepping rate is 7.5 ms.)

SEEK - For seek operations between multiple drives. Since all commands feature an implied seek, the seek command is primarily used for overlap seek operations on multiple drives. The rate field step rate is used and then stored in an internal register for future use.

Table 3-22
Command Register Format

Command	7	6	5	4	3	2	1	0
Restore	0	0	0	1	R3	R2	R1	R0
Seek	0	1	1	1	R3	R2	R1	R0
Read sector	0	0	1	0	I	M	0	0
Write sector	0	0	1	1	0	M	0	0
Scan ID	0	1	0	0	0	0	0	0
Write format	0	1	0	1	0	0	0	0

Note:
a. R0 through R3 is the rate field:

R3	R2	R1	R0	
0	0	0	0	= approx. 35 microseconds
0	0	0	1	= 0.5 milliseconds
0	0	1	0	= 1.0 milliseconds
0	0	1	1	= 1.5 milliseconds
0	1	0	0	= 2.0 milliseconds
0	1	0	1	= 2.5 milliseconds
0	1	1	0	= 3.0 milliseconds
0	1	1	1	= 3.5 milliseconds
1	0	0	0	= 4.0 milliseconds
1	0	0	1	= 4.5 milliseconds
1	0	1	0	= 5.0 milliseconds
1	0	1	1	= 5.5 milliseconds
1	1	0	0	= 6.0 milliseconds
1	1	0	1	= 6.5 milliseconds
1	1	1	0	= 7.0 milliseconds
1	1	1	1	= 7.5 milliseconds

b. M is the multiple sector flag:
   0 = Transfer 1 sector
   1 = Transfer multiple sectors

c. When limited RAM buffer size does not allow multiple sector operations, M must be set to 0.

d. I is the interrupt enable:

   0 = Set interrupt when bit 3 of the status register is set (sector buffer is ready to be loaded or read)

   1 = Set interrupt upon completion of the command

   The value is calculated by comparing the contents of the cylinder high/low registers to the cylinder position number stored internally. After all steps have been issued, the command is terminated.

READ SECTOR - Transfers one or more sectors to disk. The following programming sequence should be used with the read sector command:

1. Check the status of the Busy bit (bit 7) of the status register until a reset condition is found.

2. Write to the task file registers with the transfer parameters:

Precomp reg	= Desired precomp start track/4
Sector count	= 1
Sector number	= Sector number to read
Cylinder high/low	= Desired cylinder number
SDH	= Desired sector size, drive number, and head number

3. Send the read sector command to the command register.

4. Delay 1 or 2 NOP instructions.

5. Check the status of the Busy bit (bit 7) of the status register until a reset condition is found.

6. Read the data buffer (total number of bytes is equal to the sector size).

7. Read the status register and check the error bit (bit 0).

8. If the error bit is set, read the error register for error information.

WRITE SECTOR - Writes one or more sectors to disk. The following programming sequence should be used with the write command:

1. Check the status of the Busy bit (bit 7) of the status register until a reset condition is found.

2. Write to the task file registers with the transfer parameters:

Precomp reg	= Desired precomp start track/4
Sector count	= 1
Sector number	= Sector number to write
Cylinder high/low	= Desired cylinder number
SDH	= Desired sector size, drive number, and head number

3. Send the write command to the command register.

4. Write a sector of data to the data buffer.

5. Delay 1 or 2 NOP instructions.

6. Check the status of the Busy bit Register (bit 7) of the status register until a reset condition is found.

7. Re-read the status register and check the error bit (bit 0).

8. If the error bit is set, read the error register for error information.

SCAN ID - Updates the head, sector size, sector number, and cylinder registers. The internal cylinder position is also updated. This operation is used for multiple drives for an implied seek.

WRITE FORMAT - Used to format a single track using the task file and sector buffer. The sector buffer is used for additional parameter information instead of sector data. The following programming sequence should be used with the write format command:

1. Check the status of the Busy bit (bit 7) of the status register until a reset condition is found.

2. Write to the task file registers with the transfer parameters:

   Precomp reg = Desired precomp start track/4
   Sector count = Number of sectors to be formatted
   Sector number = Number of bytes minus three to be used for Gap 1 and Gap 3. Gap 3 is determined as follows:

   Gap 3 = 2 * M * S + K + E

   where:
   M = motor speed variation (.03 for +-3%)
   S = sector length in bytes
   K = 25 for an interleave factor of 1
   K = 0 for any other interleave factor
   E = 7 if the sector is to be extended

   Cylinder high/low = Desired cylinder number
   SDH = Desired sector size, drive number, and head number (set extension = 0)

3. Send the write format command to the command register.

4. Fill the interleave table in the sector buffer. Each sector to be formatted requires a 2-byte sequence. The first byte indicates whether a bad block mark is to be recorded in the sector's ID field. An 80H indicates a bad block mark for that sector; a 00H is normal. The second byte indicates the logical sector number to be recorded. Using this scheme, sectors can be recorded in any interleave factor desired. The remaining memory in the sector buffer can be filled with any value (but must be filled with one sector size worth of data).

5. Delay 1 or 2 NOP instructions.

6. Check the status of the Busy bit (bit 7) of the status register until a reset condition is found.

7. Re-read the status register and check the error bit (bit 0).

8. If the error bit is set, read the error register for error information.

TAPE INTERFACE CARD

The Tape Interface Card is designed to interface the PM system with the Tape Storage Unit.

The card contains a Z80A microprocessor running at 4 MHz, an 8 Kbyte PROM, and 4 Kbytes of static RAM, optionally expandable to 16 Kbytes. The size of RAM was chosen to provide enough buffer area for streaming operations to the tape drive. Underrun or overrun of the buffer area will severely slow down the streaming operation of the drive.

The tape interface card can be installed in either the x1 or x2 expansion slot of the PM system. Several jumpers on the card, however, must be set according to the slot in which the board is installed. For the correct jumper settings, refer to Appendix A.

Tape Card Interrupts

Handshaking protocol between the Z80A on the tape card and the two processors on the PM main system board is performed by several interrupt lines. The addresses to the interrupts are listed in Table 3-23.

Table 3-23
Tape Card Interrupt Addresses

Address	Function
%C0	Set interrupt Z80A on card to PM's Z80A
%C8	Set interrupt Z80A on card to 80186

Table 3-23 continued

Address	Function
%D0	Interrupt acknowledge from card's Z80A to 80186
%D8	Interrupt acknowledge from card's Z80A to PM's Z80A

Interrupts from the PM main board to the tape interface card are sent through the addresses listed in Table 3-24. Note that the port addresses differ depending on the slot in which the card is installed.

Table 3-24
Main Board Interrupts to the Tape Card

Address	Function
%02	Interrupt acknowledge from the PM Z80A to the tape interface card if in slot x1.
%04	Interrupt acknowledge from the PM Z80A to the tape interface card if in slot x2.
%002E0	Interrupt acknowledge from the 80186 to the tape interface card if in slot x1.
%002F0	Interrupt acknowledge from the 80186 to the tape interface card if in slot x2.
%088	Interrupt signal from the PM Z80A to the tape interface card if in slot x1.
%0D8	Interrupt signal from the PM Z80A to the tape interface card if in slot x2.

Table 3-24 continued

Address	Function
%02B0	Interrupt signal from the 80186 to the tape interface card if in slot x1.
%02C0	Interrupt signal from the 80186 to the tape interface card if in slot x2.

Local Memory Space

The local memory space on the interface board consists of an 8 Kbyte EPROM and 4 Kbytes static RAM, expandable to 16 Kbytes. Refer to Figure 3-7 for a map of the local memory space.

Figure 3-7
Tape Card Local Memory Space Map

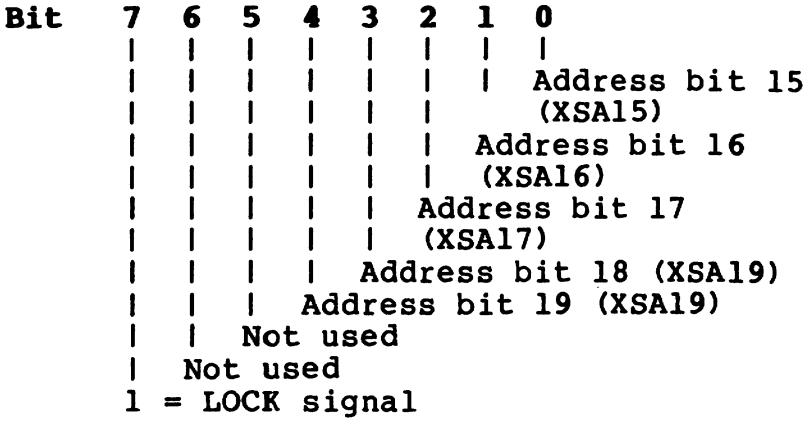
A15	A14	A13	A12	A11	Range	Memory
0	0	0	0	x	0000H	Start of EPROM
					1FFFH	End of EPROM
0	1	x	x	x	4000H	Start of static RAM
					4FFFH	End of 4K static RAM
					5FFFH	End of 8K static RAM
					7FFFH	End of 16K static RAM
1	x	x	x	x	8000H-FFFFH	PM main memory

Main Memory Addressing

The Z80A and the DMA chip on the tape interface card can access the PM main memory by executing a bus request to the Z80A on the PM board. A bus request is automatically asserted whenever the address space accessed falls between 8000H and FFFFH. To avoid blocking out the PM Z80A for too long, the transfer should be performed in the DMA byte mode.

The 20-bit address bus on the tape interface card is designed to bypass the memory mapper on the PM main board and directly access the main memory. Bits 0 through 14 of the bus are identical to address bits 0 through 14 on the PM board. Bits 15 through 19 are generated from a latch at address %E0 called the High Address Register. Refer to Figure 3-8 for the bit assignments to the register.

Figure 3-8
High Address Register
(%E0)



When bit 0 of the register (XSA15) is set to 1, the card accesses main memory. When set to 0, the card accesses local RAM.

Bit 7 of the register generates the LOCK signal. When set to 1, the 80186 is locked out of the main memory.

Configuration Facility

At power-on or reset of the PM system, the Z80A on the main system board inspects the expansion slots to determine if an expansion board is installed. It does this by reading the 'ANY 1' and 'ANY 2' signals. A low on the line indicates the presence of a card. If a board is installed, the Z80A needs to determine its ID by inspecting the XD4 through XD0 bits on the PM interface data bus.

The ID of the Tape Interface Card is given below:

XD Bits	4	3	2	1	0
ID	0	0	0	1	0

CTC Counter/Timer

Table 3-25 lists the CTC channel assignments and their addresses.

Table 3-25
CTC Channel Assignments

Channel	Address	Function
0	%00	Bus-request-time-out timer (timer mode)
1	%01	General purpose counter/timer
2	%02	Time-out interrupt (counter mode)
3	%03	Interrupt from PM main board to tape card's Z80A

NOTE: These ports are accessible only by the card's Z80A.

Channel 0 of the CTC on the Tape Interface Card is used as a bus-request-time-out timer. Channel 2 of the CTC is used to generate an interrupt to notify the CPU once time-out has occurred. This scheme resolves any possibility of a hang-up in the bus-request cycle. Channel 0 must be programmed in the timer mode, and channel 2 in the counter mode.

Channel 1 is a general purpose counter/timer. Channel 3 is used to generate an interrupt to the card's Z80A when either the PM's Z80A or 80186 wants to interrupt the card.

DMA Transfers

The DMA chip on the tape interface board transfers data between local memory and the main memory on the PM main system board. The upper limit of the size of a DMA transfer is 32 Kbytes, which corresponds to the 32-Kbyte boundary of the address space.

To maintain the high pace of data transfer required by streaming tape, the card's Z80A transfers data between local memory and the tape drive in the block I/O instruction. Transfer of data between the local memory and the PM main memory should be performed by the card's DMA chip in 'BYTE MODE'. This prevents the possibility of shutting-off other operations external to the card. If desired, the block transfer mode can be used if the PM Z80A and the 80186 do not need to access main memory, or when both of them can wait for the card's DMA chip to complete a block transfer.

Tape Drive Interface

The tape interface card contains three I/O ports that interface with the tape drive itself. These ports provide control, data, and status information, and are accessible only to the card's Z80A.

The Write Control latch at address %42 generates three of the four control signals for the tape drive unit. Figure 3-9 lists the bit assignments.

Figure 3-9
Write Control Latch
(%42)

```
Pin  -  32  30  28
Bit  3   2   1   0
     |   |   |   |
     |   |   |   0 = Places the drive in
     |   |   |       on-line status
     |   |   0 = Handshake control
     |   0 = Reset the tape drive
     1 = Bus request to PM system
```

The fourth control signal, -XFR, is generated by two D-type latches that are ORed together and clocked whenever a read from or write to tape command is issued. The signal controls the transfer timing.

Drive status information is obtained by reading the two latches at address %43. The first latch provides bits 0-3 of the drive status by reading back the control signals to the Write Command Latch. The second latch provides bits 4-7 from the control signal port from the drive. Together they make the 8-bit wide command status byte. Refer to Figure 3-10 for the bit assignments.

Figure 3-10
Drive Status Bit Assignments
(%43)

```
Pin   42  40  38  36   -   -   -   -
Bit    7   6   5   4   3   2   1   0
       |   |   |   |   |   |   |   |
       |   |   |   |   |   |   |   1 = Drive is
       |   |   |   |   |   |   |       on-line
       |   |   |   |   |   |   1 = Handshaking
       |   |   |   |   |   |       signal is
       |   |   |   |   |   |       active
       |   |   |   |   |   1 = Reset tape drive
       |   |   |   |   0 =  Bus request to PM
       |   |   |   |          system
       |   |   |   0 = Interrupt acknowledge
       |   |   0 = Drive ready for next
       |   |       command
       |   0 = Interrupt signal
       0 = Data direction: Read from tape
       1 = Data direction: Write to tape
```

Data Format

Data storage by the tape drive on the tape's four tracks involves the conversion of the data into a GCR format. Data is stored in blocks of 512 bytes, which after conversion, is 5120 bytes on tape. Refer to Table 3-26 for the conversion table.

Table 3-26
GRC Conversion Table

PM Data				Data on Tape				
D7/D3	D6/D2	D5/D1	D4/D0	G4	G3	G2	G1	G0
0	0	0	0	1	1	0	0	1
0	0	0	1	1	1	0	1	1
0	0	1	0	1	0	0	1	0
0	0	1	1	1	0	0	1	1
0	1	0	0	1	1	1	0	1
0	1	0	1	1	0	1	0	1
0	1	1	0	1	0	1	1	0
0	1	1	1	1	0	1	1	1
1	0	0	0	1	1	0	1	0
1	0	0	1	0	1	0	0	1
1	0	1	0	0	1	0	1	0
1	0	1	1	0	1	0	1	1
1	1	0	0	1	1	1	1	0
1	1	0	1	0	1	1	0	1
1	1	1	0	0	1	1	1	0
1	1	1	1	1	1	1	1	1

Data is recorded on tape with G4 first and G0 last.

Timing and address information is added by the drive to every block of data in the following sequence:

1. Sync
2. Mark
3. Control Byte
4. Data Block
5. CRC
6 Sync

SYNC - Designates both the beginning and the end of a data block and its related control signals. The signal is a magnetic flux at 60 times per minute at a density of 10,000frpi.

MARK - Indicates the header of a data block and takes on the following pattern. The MSB is on the left.

G4	G3	G2	G1	G0	G4	G3	G2	G1	G0
1	1	1	1	1	0	0	1	1	1

CONTROL BYTE - 8 bits before conversion and 10 bits on tape. The format of the byte before conversion is shown in Figure 3- 11.

Figure 3-11
Control Byte

```
Bits
7  6  5  4  3  2  1  0
|  |  |  |  |  |  |  |
|  |  |  |  |  |  |  Track Number (LSB)
|  |  |  |  |  |  Track Number
|  |  |  |  |  Track Number
|  |  |  |  Track Number
|  |  |  Track Number
|  |  Track Number (MSB)
|  1 =  End of track
1 = File Mark
```

Table 3-11 Continued

Bits	Description
7	Set to 1 to indicate a file mark, which divides data segments on tape.
6	Set to 1 in the last block of each track except for the last track.
5-0	Designates the current track number in binary.

BLOCK ADDRESS - Two bytes before conversion and 20 bits after conversion. The control block designates the block address, which starts at 0 for the first block on the tape. This is incremented block-by-block to generate a serial number for each block. On reaching FFFF, the address starts again at 0.

DATA BLOCK - 512 bytes before conversion and 5120 bytes after conversion.

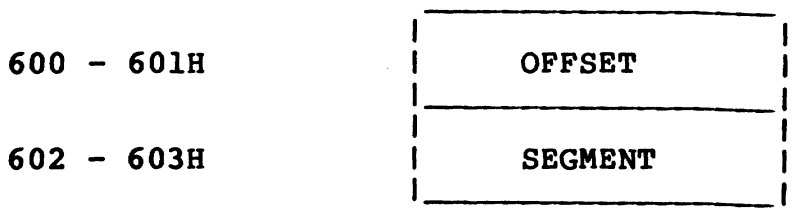
CRC - Ensures that the conversion process functioned properly by checking that every 16 bits of data before conversion resulted in 20 bits after conversion.

The IOCB

The Z80A on the tape card communicates with the 80186 through the IOCB (I/O Control Block). The IOCB is an area in main memory that is accessible to both processors and through which commands and status information based on the semaphore set/reset mechanism, are passed.

The pointer to the IOCB consists of four bytes. The first two bytes contain the segment value and the last two the offset. Refer to Figure 3-12.

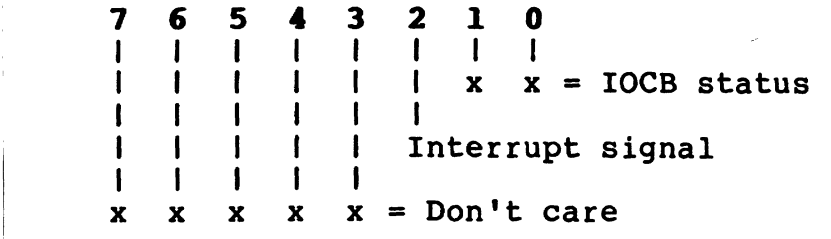
Figure 3-12
IOCB Pointer



To maintain the speed of the streaming tape, two IOCB's should be used. While one IOCB is being processed by the tape card, the 80186 can be setting up the second IOCB for execution by the tape drive.

One byte of the IOCB provides status information on and interrupt control for the tape drive. The byte is referred to as the **Status Code.** Refer to Figure 3-13 for the bit assignments to this byte.

Figure 3-13
Status Code



Bits	Description
0-1	The 80186 sets bits 0 and 1 to 0 when the IOCB is ready to be processed by the tape card. As the command is being executed, the tape card changes bit 1 to 1. At the completion of the command, the tape card changes both bits to 1 to signal the 80186 that it is ready for a new command.
2	If this bit is set to 0 by the 80186, the tape card will issue an interrupt at the completion of the command. If set to 1, no interrupt will be generated.
3-7	Don't care.

Tape Commands

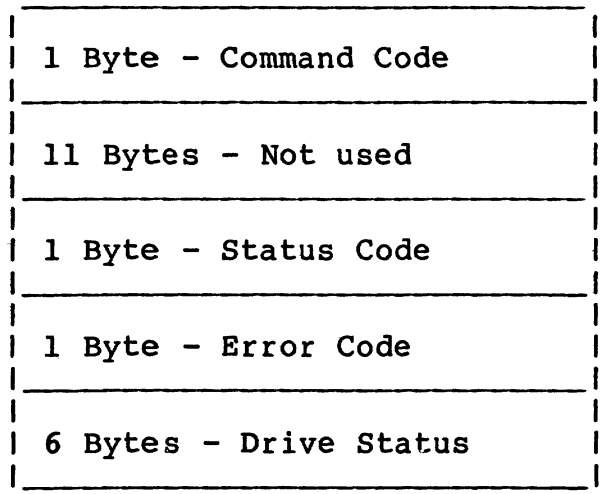
The tape drive can perform the following ten commands:

1. Reset the drive
2. Drive select (0 - 1)
3. Tape drive status
4. Rewind the tape
5. Erase the tape
6. Retension the tape
7. Write data to tape
8. Read data from tape
9. Write file mark
10. Read file mark

The IOCB structure for each command along with the command and error codes are discussed in the following pages.

RESET THE DRIVE - This command resets the tape expansion board.

IOCB Structure:



Command Code - contains the code of the command:

Bits	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	0

Status Code - contains information on the status of the tape drive. Refer to page 3.64 for details on this IOCB byte.

Error Code - If the drive experiences difficulty during the execution of the command, it signals the 80186 by setting one or more of the bits in this byte to 1. Specific information on the nature of the difficulty is obtained in the six bytes of the Drive Status section of the IOCB.

Drive Status - provides specific information on any problem that the tape drive may have experienced during the execution of a command. For the bit definitions to these six bytes, refer to the Drive Status command.

Error Conditions:

The following error conditions will cause the drive to reject the command.

1. Illegal Command - The command is issued while the tape drive is performing another operation.

2. Illegal Command - The command selects more than one drive.

3. Unselected Drive - The command selects a non-existing drive (i.e. drive 1 when the system has only one drive).

4. Fault - A system error exists.

DRIVE SELECT - This command selects the drive to perform a command. This command must be issued whenever the PM system is turned on or reset, even if the system has only one tape drive. The maximum number of tape drives that can be connected to a PM system is two.

NOTE: This command must not be issued while a read or write operation is in progress. The command should only be issued once the operation is completed and the tape is rewound.

When a drive is selected with this command and the cassette tape is properly loaded, the LED indicator on the front of the drive should light up.

IOCB Structure:

1 Byte - Command Code
1 Byte - Drive Number
10 Bytes - Not used
1 Byte - Status Code
1 Byte - Error Code
6 Bytes - Drive Status

Command Code - contains the code of the command:

Bits	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	1

Drive Number - designates the number of the desired drive. A 0 for this byte selects drive 0, and a 1 drive 1.

Status Code - contains information on the status of the tape drive. Refer to page 3.64 for details on this IOCB byte.

Error Code - If the drive experiences difficulty during the execution of the command, it signals the 80186 by setting one or more of the bits in this byte to 1. Specific information on the nature of the difficulty is obtained in the six bytes of the Drive Status section of the IOCB.

Drive Status - provides specific information on any problem that the tape drive may have experienced during the execution of a command. For the bit definitions to its six bytes, refer to the Drive Status command.

Error Conditions:

The following error conditions will cause the drive to reject the command.

1. Illegal Command - The command is issued while the tape drive is performing another operation.

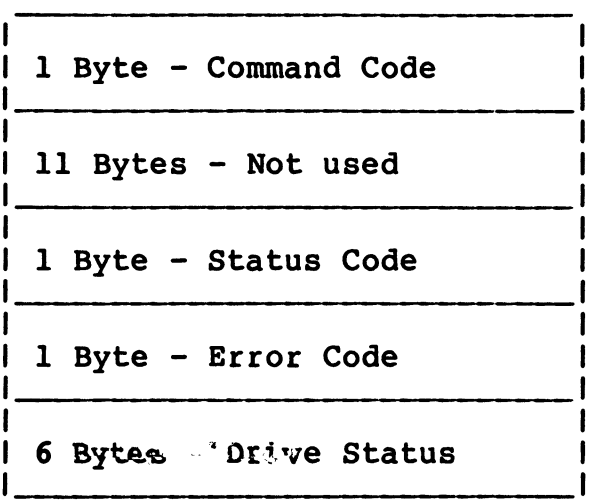
2. Illegal Command - The command selects more than one drive.

3. Unselected Drive - The command selects a non-existing drive (i.e. drive 1 when the system has only one drive).

4. Fault - A system error exists.

TAPE DRIVE STATUS - This command provides status and error information on the tape drive. The information is read from the six bytes of the Drive Status section of the IOCB.

IOCB Structure:



Command Code - contains the code of the command:

Bits	7	6	5	4	3	2	1	0
	1	1	0	0	0	0	0	1

Status Code - contains information on the status of the tape drive. Refer to page 3.64 for details on this IOCB byte.

Error Code - If the drive experiences difficulty during the execution of the command, it signals the 80186 by setting one or more of the bits in this byte to 1. Specific information on the nature of the difficulty is obtained in the six bytes of the Drive Status section of the IOCB.

Drive Status - provides specific information on problems that the tape drive may have experienced during the execution of a command. The bit definitions for the bytes are provided below.

Status Byte 0:

Table 3-27
Status Byte 0

Bits
7 6 5 4 3 2 1 0

```
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  1 = File Mark Detected
|  |  |  |  |  |  1 = Block Not Located
|  |  |  |  |  1 = Unrecoverable Data Error
|  |  |  |  1 = End of Media
|  |  |  1 = Write Protected Cassette
|  |  1 = Unselected Drive
|  1 = Cassette Not In Place
1 = Error Flag
```

Bit	Description
7	Set whenever one of the bits in this status byte is set. The bit is reset with a read status command.

Table 3-27 Continued

Bit	Description
6	Set when no drive is selected, or if the cassette is not loaded properly.
5	Set when a command is issued without a selected drive, or when a non-existing drive is selected.
4	Set when a command is issued without a selected drive. This bit is also set if the cassette is not properly loaded or is write protected.
3	Set when the BOT (Beginning of Tape) is detected during a write or read operation. The bit is reset with any one of the following commands: rewind the tape, retension the tape, and drive select.
2	Set when a write or read operation fails more than sixteen times on the same data block. The bit is reset with the read status command.
1	Indicates that a block address cannot be read after sixteen attempts. Reset the bit with a read status command.
0	Set when a file mark is detected during a read operation, and reset with a read status command.

Status Byte 1:

Table 3-28
Status Byte 1

```
Bits
7  6  5  4  3  2  1  0
|  |  |  |  |  |  |  |
|  |  |  |  |  |  |  1 = Power/On, Reset
|  |  |  |  |  |  1 = Fault
|  |  |  |  |  Not used
|  |  |  |  1 = Beginning Of Media
|  |  |  1 = Marginal Block Detected
|  |  1 = No Data Detected
|  1 = Illegal Command
1 = Error Flag
```

Bit	Description
7	Indicates that one or more of the bits in this status byte have been set. The bit is reset with a read status command.
6	Indicates that an illegal command has been issued, such as specifying more than one drive or issuing a drive select command during a write operation.
5	Set when a gap of 380 mm has been detected during a read operation.
4	Set when a write operation fails after more than eight attempts in the same block. The bit is also set after the drive has stored all of the received data.
3	Indicates that the tape is located on the BOT clear reader tape of Track 0.

Table 3-28 Continued

Bits	Description
2	Not used.
1	Set when a error occurs that is not related to a read or write operation. Sources of such errors include ROM, RAM, and the buffer.
0	Set whenever the Persoal Mini is turned on or reset. The bit is reset with the read status command.

Status Bytes 2 and 3: Data Error Counter:

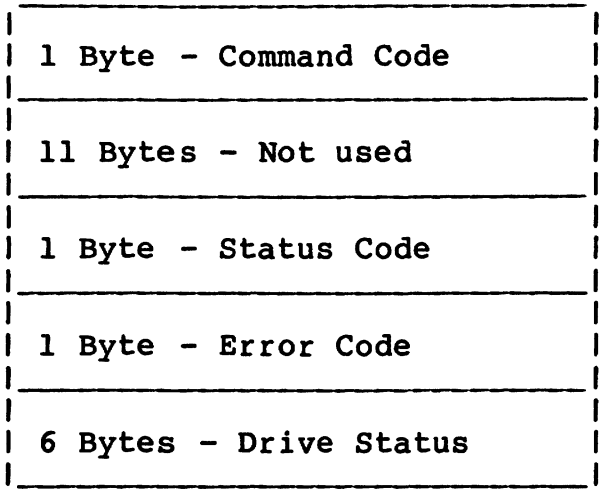
Status bytes 2 and 3 provide a 16-bit binary counter. Transferred to the system with the MSB first, the counter is incremented whenever an error is encountered during a read or write operation.

Status Bytes 4 and 5: Underrun/Overrun Counter:

Status bytes 4 and 5 also provide a 16-bit binary counter. Transferred to the system with the MSB first, the counter is incremented whenever there is an overrun of the buffer during a read operation, or an underrun during a write operation.

REWIND THE TAPE - This command rewinds the tape back to the BOT.

IOCB Structure:



Command Code - contains the code of the command:

Bits	7	6	5	4	3	2	1	0
	0	0	1	0	0	0	0	1

Status Code - contains information on the status of the tape drive. Refer to page 3.64 for details on this IOCB byte.

Error Code - If the drive experiences difficulty during the execution of the command, it signals the 80186 by setting one or more of the bits in this byte to 1. Specific information on the nature of the difficulty is obtained in the six bytes of the Drive Status section of the IOCB.

Drive Status - provides specific information on any problem that the tape drive may have experienced during the execution of a command. For the bit definitions to its six bytes, refer to the Drive Status command.

Error Conditions:

The tape drive will reject this command if any of the following conditions exist when the command is issued.

1. Unselected Drive - The drive select command was not issued.

2. Cassette Not In Place - The cassette is not properly loaded in the drive.

3. Fault - A system error exists.

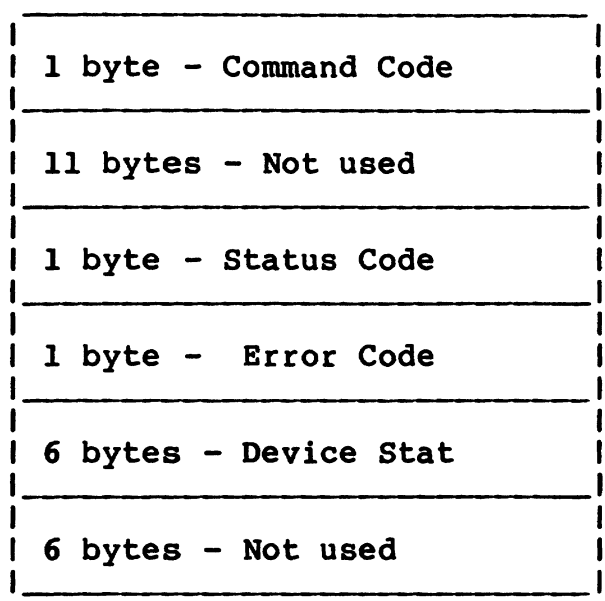
The tape drive will reject the command if any of the following conditions occur during its execution.

1. Cassette Not In Place - The cassette is ejected.

2. Fault - The drive is unable to start the tape.

ERASE THE TAPE - This command, which can be executed at any tape position, erases all of the data on the tape. At the completion of the command, the drive rewinds the tape back to the BOT.

IOCB Structure:



Command Code - contains the code of the command:

Bits	7	6	5	4	3	2	1	0
	0	0	1	0	0	0	1	0

Status Code - contains information on the status of the tape drive. Refer to page 3.64 for details on this IOCB byte.

Error Code - If the drive experiences difficulty during the execution of the command, it signals the 80186 by setting one or more of the bits in this byte to 1. Specific information on the nature of the difficulty is obtained in the six bytes of the Drive Status section of the IOCB.

Drive Status - provides specific information on any problem that the tape drive may have experienced during the execution of a command. For the bit definitions to its six bytes, refer to the Drive Status command.

Error Conditions:

The drive will reject this command if any of the following conditions exist at the time the command is issued.

1. Unselected Drive - The drive select command was not issued.

2. Cassette Not In Place - The cassette tape is not properly loaded in the drive.

3. Write Protected Cassette - The tape is write protected.

4. Illegal Command - A read operation is being performed.

5. Fault - A system error exists.

The drive will abort the command if any of the following conditions occur during the execution of the command.

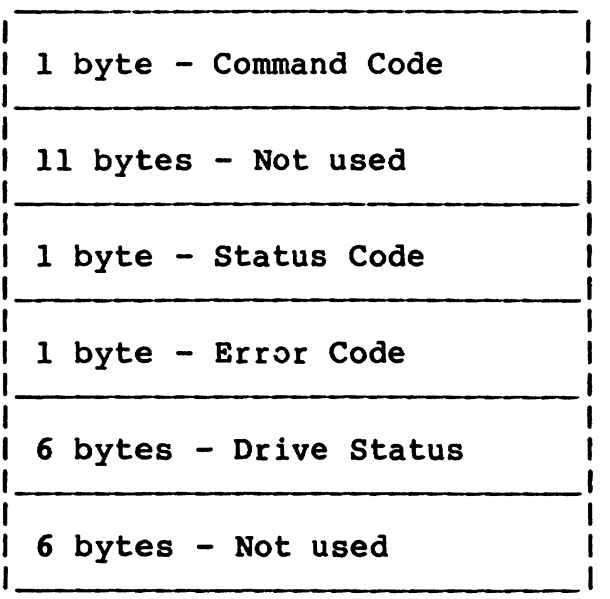
1. Cassette Not In Place - The cassette tape is ejected.

2. Fault, Timeout - The tape drive is unable to start the tape.

3. Fault, Drive Fault - The drive's erase head fails to operate properly.

RETENSION THE TAPE - This command, which can be run at any tape location, ensures that the tape is wound at the proper tension by running it to the EOT and then by rewinding back to the BOT.

IOCB Structure:



Command Code - contains the code of the command:

Bits	7	6	5	4	3	2	1	0
	0	0	1	0	0	1	0	0

Status Code - contains information on the status of the tape drive. Refer to page 3.64 for details on this IOCB byte.

Error Code - If the drive experiences difficulty during the execution of the command, it signals the 80186 by setting one or more of the bits in this byte to 1. Specific information on the nature of the difficulty is obtained in the six bytes of the Drive Status section of the IOCB.

Drive Status - provides specific information on any problem that the tape card may have experienced during the execution of a command. For the bit definitions to its six bytes, refer to the Drive Status command.

Error Conditions:

The following error conditions will cause the tape drive to reject the command.

1. Unselected Drive - The drive select command was not issued.

2. Cassette Not In Place - The cassette tape is not loaded properly.

3. Fault - A system error exists.

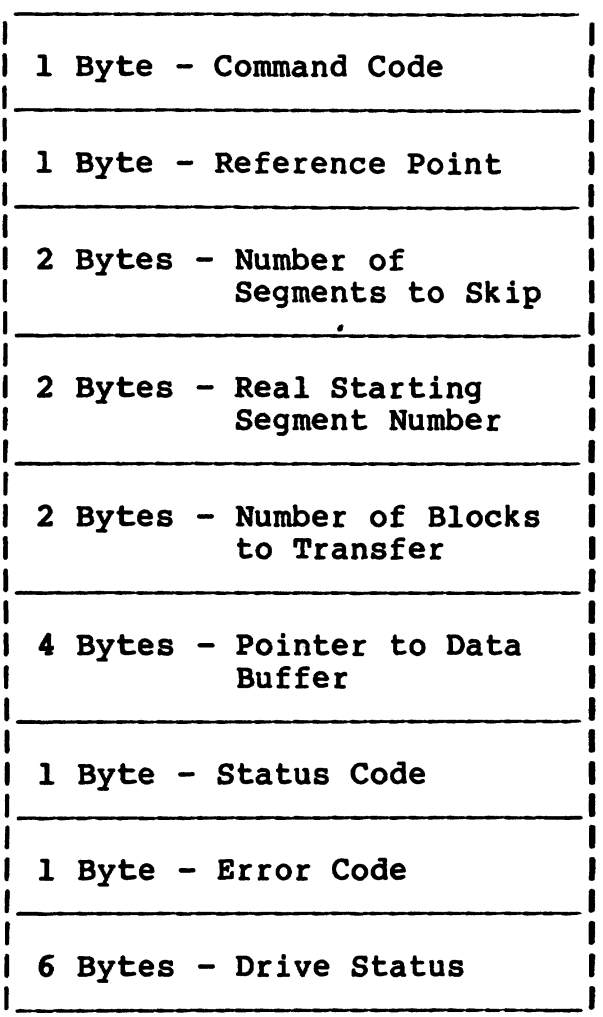
The following error conditions will cause the command to abort.

1. Unselected Drive - The cassette is ejected.

2. Fault, Timeout - The drive is unable to start the tape.

WRITE DATA TO TAPE - This command writes data from the hard disk onto the cassette tape, which consists of four tracks, numbered from 0 to 3.

IOCB Structure:



When the drive is writing data on track 0, it erases the old data prior to storing the new. It also checks to issue accurate data storage by performing a Read after Write Check error detection operation. If an error is detected, the write operation is retried up to sixteen times. The Data Error Counter in the Drive Status section of the IOCB is incremented every time an error is encountered.

Command Code - contains the code of the command:

Bits	7	6	5	4	3	2	1	0
	0	1	0	0	0	0	0	0

Reference Point - designates the starting point for the operation. If the drive is reset or if a new cassette is loaded, a 0 is written into this byte to indicate that the starting point is the BOT. Otherwise, the byte is written with a 1 to indicate the current tape position.

Number of Segments to Skip - specifies the number of segments the drive is to skip prior to performing the read operation.

Real Starting Segment Number - contains the actual number of segments the drive skipped prior to starting the write operation. The value here can be compared with the value in Number of Segments to Skip to insure that the drive is at the proper location.

Status Code - contains information on the status of the tape drive. Refer to page 3.64 for details on this IOCB byte.

Error Code - If the drive experiences difficulty during the execution of the command, it signals the 80186 by setting one or more of the bits in this byte to 1. Specific information on the nature of the difficulty is obtained in the six bytes of the Drive Status section of the IOCB.

Drive Status - provides specific information on any problem that the tape card may have experienced during the execution of a command. For the bit definitions to its six bytes, refer to the Drive Status command.

Number of Segments Skipped - contains the number of segments the drive skipped prior to starting the operation. The value of these two bytes can be checked against the two bytes in Number of Segments to Skip to ensure that the drive is located at the proper segment.

Error Conditions:

The tape drive will reject the command if any of the following error conditions exist.

1. Unselected Drive - The drive select command was not issued.

2. Cassette Not In Place - The tape cassette is not properly loaded.

3. Write Protected Cassette - The cassette is write protected.

4. Fault - A system error has occurred.

The following error conditions abort the execution of the command.

1. Cassette Not In Place - The cassette is ejected.

2. Fault, Timeout - The drive is unable to start the tape.

3. Marginal Block Detected - A rewrite operation is repeated more than eight times for the same block. To continue the write operation, issue the write command again.

4. Unrecoverable Data Error - A rewrite operation is repeated more than sixteen times to the same block. The occurrence of this error causes the drive to rewind the tape automatically.

5. End Of Media - The end of the tape is detected.

6. Fault, Drive Fault - The drive's erase head fails to operate during the write operation on Track 0.

All other commands can be executed during a write operation. The only exception is the erase the tape command which will only function on Track 0.

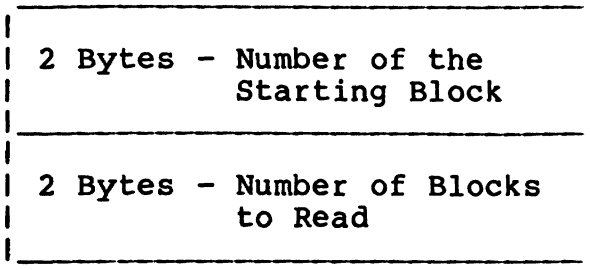
READ DATA FROM TAPE - This command reads data from the cassette and transfers it to the Personal Mini.

IOCB Structure:

The IOCB for this command consists of two parts: the main portion with its vector address at 600H, and a sub-IOCB with its vector address located in the main IOCB.

1 Byte - Command Code
1 Byte - Reference Point
2 Bytes - Number of Segments to Skip
4 Bytes - Pointer to Sub-IOCB
4 Bytes - Pointer to Data Buffer
1 Byte - Status Code
1 Byte - Error Code
6 Bytes - Drive Status
2 Bytes - Number of Blocks Transferred

Sub-IOCB



If an error is detected during the read operation, the operation can be retried up to sixteen times. The retry includes the block containing the error and two or more succeeding blocks, or until a gap of 35 inches is detected. The Data Error Counter is incremented every time a data error is detected.

Command Code - contains the code of the command:

Bits	7	6	5	4	3	2	1	0
	1	0	0	0	0	0	0	0

Reference Point - designates the starting point for the operation. If the drive is reset or if a new cassette is loaded, a 0 is written into this byte to indicate that the starting point is the BOT. Otherwise, the byte is written with 1 to indicate that the operation is to start at the current tape position.

Number of Segments to Skip - specifies the number of segments the drive is to skip prior to performing the read operation.

Pointer to IOCB - contains the address in main memory where the second portion of the IOCB is located.

Pointer to Data Buffer - contains the address in main memory where the data is to be transferred from the tape drive.

Status Code - contains information on the status of the tape drive. Refer to page 3.64 for details on this IOCB byte.

Error Code - If the drive experiences difficulty during the execution of the command, it signals the 80186 by setting one or more of the bits in this byte to 1. Specific information on the nature of the difficulty is obtained in the six bytes of the Drive Status section of the IOCB.

Drive Status - provides specific information on any problem that the tape card may have experienced during the execution of a command. For the bit definitions to its six bytes, refer to the Drive Status command.

Number of Blocks Transferred - contains the number of blocks of data transferred by the drive to the data buffer.

Number of the Starting Block - contains the address of the first block of data that the drive is to read from the tape.

Number of Blocks to Read - contains the number of blocks the drive is to read during the operation.

Error Conditions:

The drive will reject this command if any of the following error conditions exist at the time the command is issued.

1. Unselected Drive - The drive select command was not issued.

2. Cassette Not In Place - The cassette is not loaded properly in the drive.

3. Illegal Command - The drive is performing a write operation.

The drive will abort the command if any of the following error conditions occur during the execution of the command.

1. Cassette Not In Place - The cassette is ejected.

2. Fault, Timeout - The drive is unable to start the tape.

3. Unrecoverable Data Error - The drive fails to read a block of data without error after sixteen attempts.

4. No Data Detected - The drive detects a gap of 380 mm with no data.

5. No Data Detected, End Of Media - The drive encountered the BOT clear reader tape on the last track.

6. File Mark Detected - The drive detects a file mark.

7. Fault, BOT, EOT - The clear leader tape is detected before the last block from each track is read.

WRITE FILE MARK - This command writes a file mark to divide major segments of data on tape. If the file mark is being written on track 0, the erase head is activated causing the tracks to be erased before the file marks are written.

IOCB Structure:

1 Byte - Command Code
1 Byte - Reference Point
4 Bytes - Not used
2 Bytes - Number of Segments to Skip
4 Bytes - Not used
1 Byte - Status Code
1 Byte - Error Code
6 Bytes - Drive Status
2 Bytes - Number of Segments Skipped

Command Code - contains the code of the command:

Bits	7	6	5	4	3	2	1	0
	0	1	1	0	0	0	0	0

Reference Point - designates the starting point for the operation. If the drive is reset or a new cassette is loaded, this byte is written with 0 to indicate the BOT. Otherwise, the byte is written with 1 to indicate the current tape location.

Number of Segments to Skip - specifies the number of segments the drive is to skip prior to performing the read operation.

Status Code - contains information on the status of the tape drive. Refer to page 3.64 for details on this IOCB byte.

Error Code - If the drive experiences difficulty during the execution of the command, it signals the 80186 by setting one or more of the bits in this byte to 1. Specific information on the nature of the difficulty is obtained in the six bytes of the Drive Status section of the IOCB.

Drive Status - provides specific information on any problem that the tape card may have experienced during the execution of a command. For the bit definitions to the six bytes, refer to the Drive Status command.

Number of Segments Skipped - contains the number of segments the drive skipped prior to starting the operation. The value of these two bytes can be checked against the two bytes in Number of Segments to Skip to ensure that the drive is located at the proper segment.

Error Conditions:

The drive will reject the command if any of the following error conditions exist at the time the command is issued.

1. Unselected Drive - The drive select command was not issued.

2. Cassette Not In Place - The cassette is not properly loaded in the drive.

3. Write Protected Cassette - The cassette is write protected.

If any of the following error conditions occur during the execution of the command, the drive will abort the operation.

1. Cassette Not In Place - The cassette is ejected.

2. Fault, Timeout - The drive is unable to start the tape.

3. Marginal Block Detected - The drive is unable to write the file mark after eight attempts.

4. Unrecoverable Data Error - The drive is unable to write the file mark after sixteen attempts. If this error occurs, the drive will automatically rewind the tape.

5. End of Media - The drive encountered the BOT on the last track.

6. Drive Fault - The erase head on the drive failed to operate.

READ FILE MARK - This command runs the tape until it encounters a file mark.

IOCB Structure:

1 Byte - Command Code
1 Byte - Reference Point
4 Bytes - Not used
2 Bytes - Number of Segments to Skip
4 Bytes - Not used
1 Byte - Status Code
1 Byte - Error Code
6 Bytes - Drive Status
2 Bytes - Number of Segments Skipped

Command Code - contains the code of the command:

Bits	7	6	5	4	3	2	1	0
	1	0	1	0	0	0	0	0

Reference Point - designates the starting point for the operation. If the drive is reset or if a new cassette is loaded, this byte is written with 0 to indicate the BOT. Otherwise, the byte is written with 1 to indicate the current tape location.

Number of Segments to Skip - specifies the number of segments the drive is to skip prior to performing the read operation.

Status Code - contains information on the status of the tape drive. Refer to page 3.64 for details on this IOCB byte.

Error Code - If the drive experiences difficulty during the execution of the command, it signals the 80186 by setting one or more of the bits in this byte to 1. Specific information on the nature of the difficulty is obtained in the six bytes of the Drive Status section of the IOCB.

Drive Status - provides specific information on any problem that the tape card may have experienced during the execution of a command. For the bit definitions to its six bytes, refer to the Drive Status command.

Number of Segments Skipped - contains the number of segments the drive skipped prior to starting the operation. The value of these two bytes can be checked against the two bytes in Number of Segments to Skip to insure that the drive is located at the proper segment.

Error Conditions:

The drive will reject the command if any of the following conditions exist at the time the command is issued.

1. Unselected Drive - The drive select command was not issued.

2. Cassette Not In Place - The cassette is not properly loaded in the drive.

3. Illegal Command - The drive is performing a write operation.

4. Fault - A system error exists.

The drive will terminate the command if any of the following error conditions occur during its execution.

1. Cassette Not In Place - The cassette is ejected.

2. Fault, Timeout - The drive is unable to start the tape.

3. Unrecoverable Data Error - The drive fails to read the file mark after sixteen attempts. The drive responds to this error by rewinding the tape.

4. INTERFACE

This chapter describes the internal connector interfaces and external connector ports. These ports provide the means to expand or perform major internal functions while allowing external system expansion. This section is divided into internal and external interfaces.

There are two connectors located on the tape expansion board. P1 can be connected to either the X1 or X2 expansion slot. P2 is connected to the tape drive controller board. A second P2 connector, located on the main board, is the hard disk expansion connector.

INTERNAL INTERFACES

Table 4-1
Power Supply (P1)

Pin	Signal	Description
1	-12V	-12v supply
2	----	Polarization key
3	GND	Ground
4	+5V	+5v supply
5	+12V	+12v supply
6	GND	Ground
7	GND	Ground
8	+5V	+5v supply
9	GND	Ground
10	+5V	+5v supply

Table 4-2
Tape Drive Expansion Board (P2)

NOTE: This P2 connector is located on the Tape Drive Expansion Board and connects to the tape controller board found on the tape drive.

Pin	Signal	Description
2	---	No connection
4	---	No connection
6	---	No connection
8	---	No connection
10	HBP	Host bus odd parity
12	HB7	Host bus bit 7 (MSB)
14	HB6	Host bus bit 6
16	HB5	Host bus bit 5
18	HB4	Host bus bit 4
20	HB3	Host bus bit 3
22	HB2	Host bus bit 2
24	HB1	Host bus bit 1
26	HB0	Host bus bit 0 (LSB)
28	ONL	Online
30	REQ	Request
32	RST	Reset
34	XFR	Transfer
36	ACK	Acknowledge
38	RDY	Ready
40	EXC	Exception
42	DIR	Direction
44	---	No connection
46	---	No connection
48	---	No connection
50	---	No connection

All odd numbered pins are connected to ground.

Table 4-3
Expansion Card Slot (P7)

Pin	Signal	Description
A1	+5V	+5v supply
A2	+5V	+5v supply
A3	+12V	+12v supply
A4	-XWR	Write enable
A5	-XIORQ	I/O request
A6	-XRD	Read enable
A7	-XZ RESET	Expansion card reset
A8	X USE MAP	High, uses mapper Low, bypasses mapper
A9	-XRFSH	Expansion memory refresh
A10	X BYTE	High, 1 byte data bus Low, 2 byte data bus
A11	-XM1	Inverted Z80 M1 output
A12	XZ SYS CLK	4 MHz clock signal
A13	X CLK OUT	8 MHz clock signal
A14	SPARE 7	I/O write to address %0290
A15	SPARE 6	I/O write to address %0280
A16	SPARE 5	I/O write to address %0A
A17	XD 15	Data bit 15
A18	XD 14	Data bit 14
A19	XD 13	Data bit 13
A20	XD 12	Data bit 12
A21	XD 11	Data bit 11
A22	XD 10	Data bit 10
A23	XD 9	Data bit 9
A24	XD 8	Data bit 8
A25	SA 12	Address bit 12
A26	SA 13	Address bit 13
A27	SA 14	Address bit 14
A28	SA 15	Address bit 15
A29	SA 16	Address bit 16
A30	SA 17	Address bit 17
A31	SA 18	Address bit 18
A32	SA 19	Address bit 19

Table 4-3 continued

Pin	Signal	Description
B1	+5V	+5v supply
B2	+5V	+5v supply
B3	-12V	-12v supply
B4	-12V	-12v supply
B5	-ANY X2	X2 board installed
B6	-XMREQ	Memory request
B7	-X1 BUSAK	Expansion bus acknowledge
B8	-BUSAK OUT	Bus request from X2
B9	-INTA Z TO X1	Interrupt acknowledge
B10	GND	Ground
B11	XZ WAIT	Wait request
B12	GND	Ground
B13	-INT X2 TO 186	Interrupt request
B14	GND	Ground
B15	-INT X1 TO Z	Interrupt request to CTC
B16	GND	Ground
B17	-X1 BUSAK	Interrupt acknowledge from 80186
B18	GND	Ground
B19	-X BUS REQ	Interrupt request to CTC
B20	GND	Ground
B21	-X LOCK	Memory lock request
B22	GND	Ground
B23	-----	Not used
B24	GND	Ground
B25	-INT X2 TO Z	Interrupt request to Z80A
B26	GND	Ground
B27	TIMER 1	80186 timer output
B28	GND	Ground
B29	TIMER 0	80186 timer output

Table 4-3 continued

Pin	Signal	Description
B30	-INTA 186 TO X2	Interrupt acknowledge from 80186
B31	-INT 186 TO X2	Interrupt request to 80186
B32	-INTA X2 TO 186	Interrupt acknowledge to 80186
C1	+5V	+5v supply
C2	+5V	+5v supply
C3	+12V	+12v supply
C4	XD 0	Data bus bit 0
C5	XD 1	Bus bit 1
C6	XD 2	Data bus bit 2
C7	XD 3	Data bus bit 3
C8	XD 4	Data bus bit 4
C9	XD 5	Data bus bit 5
C10	XD 6	Data bus bit 6
C11	XD 7	Data bus bit 7
C12	SPARE 3	I/O read in bit 6 at address %08
C13	SPARE 2	I/O read in bit 5 at address %08
C14	SPARE 1	I/O read in bit 4 at address %08
C15	SPARE 0	I/O read in bit 3 at address %08
C16	-INTA Z TO X2	Interrupt acknowledge from Z80
C17	XZ 15	Address bit 15
C18	XZ 14	Address bit 14
C19	XZ 13	Address bit 13
C20	XZ 12	Address bit 12
C21	XZ 11	Address bit 11
C22	XZ 10	Address bit 10
C23	XZ 9	Address bit 9
C24	XZ 8	Address bit 8
C25	XZA 7	Address bit 7

Table 4-3 continued

Pin	Signal	Description
C26	XZA 6	Address bit 6
C27	XZA 5	Address bit 5
C28	XZA 4	Address bit 4
C29	XZA 3	Address bit 3
C30	XZA 2	Address bit 2
C31	XZA 1	Address bit 1
C32	XZA 0	Address bit 0

Table 4-4
Expansion Card Slot (P8)

Pin	Signal	Description
A1	+5V	+5v supply
A2	+5V	+5v supply
A3	+12V	+12v supply
A4	-XWR	Write enable
A5	-XIORQ	I/O request
A6	-XRD	Read enable
A7	-XZ RESET	Expansion card reset
A8	X USE MAP	High, uses mapper Low, bypasses mapper
A9	-XRFSH	Expansion memory refresh
A10	X BYTE	High, 1 byte data bus Low, 2 byte data bus
A11	-XM1	Inverted Z80 M1 output
A12	XZ SYS CLK	4 MHz clock signal
A13	X CLK OUT	8 MHz clock signal
A14	SPARE 7	I/O write to address %0290
A15	SPARE 6	I/O write to address %0280

Table 4-4 continued

Pin	Signal	Description
A16	SPARE 5	I/O write to address %0A
A17	XD 15	Data bit 15
A18	XD 14	Data bit 14
A19	XD 13	Data bit 13
A20	XD 12	Data bit 12
A21	XD 11	Data bit 11
A22	XD 10	Data bit 10
A23	XD 9	Data bit 9
A24	XD 8	Data bit 8
A25	SA 12	Address bit 12
A26	SA 13	Address bit 13
A27	SA 14	Address bit 14
A28	SA 15	Address bit 15
A29	SA 16	Address bit 16
A30	SA 17	Address bit 17
A31	SA 18	Address bit 18
A32	SA 19	Address bit 19
B1	+5V	+5v supply
B2	+5V	+5v supply
B3	-12V	-12v supply
B4	-12V	-12v supply
B5	-ANY X1	X1 board installed
B6	-XMREQ	Memory request
B7	-BUSAK IN	Daisy chain bus acknowledge
B8	--------	Not used
B9	INTA Z TO X1	Interrupt acknowledge
B10	GND	Ground
B11	XZ WAIT	Wait request
B12	GND	Ground
B13	-INT TO 186	Interrupt request
B14	GND	Ground
B15	-INT X1 TO Z	Interrupt request to CTC
B16	GND	Ground

Table 4-4 continued

Pin	Signal	Description
B17	X1 BUSAK	Expansion bus acknowledge
B18	GND	Ground
B19	-X BUS REQ	Bus request to Z80
B20	GND	Ground
B21	-X LOCK	Memory lock request
B22	GND	Ground
B23	------	Not used
B24	GND	Ground
B25	-INT X2 TO Z	Interrupt request to CTC
B26	GND	Ground
B27	TIMER 1	80186 timer output
B28	GND	Ground
B29	TIMER 0	80186 timer output
B30	-INTA 186 TO X1	Interrupt request to 80186
B31	-INT 186 TO X1	Interrupt request to 80186
B32	-INTA X1 TO 186	Interrupt acknowledge to 80186
C1	+5V	+5v supply
C2	+5V	+5v supply
C3	+12V	+12v supply
C4	XD 0	Data bit 0
C5	XD 1	Data bit 1
C6	XD 2	Data bit 2
C7	XD 3	Data bit 3
C8	XD 4	Data bit 4
C9	XD 5	Data bit 5
C10	XD 6	Data bit 6
C11	XD 7	Data bit 7
C12	SPARE 3	I/O read on bit 6 at address %08
C13	SPARE 2	I/O read on bit 5 at address %08

Table 4-4 continued

Pin	Signal	Description
C14	SPARE 1	I/O read on bit 4 at address %08
C15	SPARE 0	I/O read on bit 3 at address %08
C16	-INTA Z TO X2	Interrupt acknowledge from Z80
C17	XZ 15	Address bus bit 15
C18	XZ 14	Address bus bit 14
C19	XZ 13	Address bus bit 13
C20	XZ 12	Address bus bit 12
C21	XZ 11	Address bus bit 11
C22	XZ 10	Address bus bit 10
C23	XZ 9	Address bus bit 9
C24	XZ 8	Address bus bit 8
C25	XZA 7	Address bus bit 7
C26	XZA 6	Address bus bit 6
C27	XZA 5	Address bus bit 5
C28	XZA 4	Address bus bit 4
C29	XZA 3	Address bus bit 3
C30	XZA 2	Address bus bit 2
C31	XZA 1	Address bus bit 1
C32	XZA 0	Address bus bit 0

Table 4-5
Floppy Disk Drive (P9)

Pin	Signal	Description
1-4	---------	Not used
6	-DR SEL 3	Select drive 3
8	-INDEX	Index mark
10	-DR SEL 0	Select drive 0
12	-DR SEL 1	Select drive 1
14	-DR SEL 2	Select drive 2
16	-MOTOR ON	Start drive motor
18	-DIR	Low, stepping in High, stepping out

Table 4-5 continued

Pin	Signal	Description
20	-STEP	Step pulse
22	-COMP WR DATA	Composite write data
24	-WR EN	Write Enable
26	-TR 00	Head on track 00
28	-WR PROT	Write protect
30	-COMP RD DATA	Composite read data
32	-SIDE SELECT	Low, side 1 High, side 2

Table 4-6
Memory Expansion Board (P10)

Pin	Signal	Description
A1	RAMDO 7	Data output bit 7
A2	RAMDO 5	Data output bit 5
A3	RAMDO 3	Data output bit 3
A4	GND	Ground
A5	RAMDO 1	Data output bit 1
A6	-RAS 2	Bank 2 RAS
A7	-RAS 3	Bank 3 RAS
A8	-------	Not used
A9	RAMDI 1	Data input bit 1
A10	RAMDI 3	Data input bit 3
A11	+5V	+5v supply
A12	RAMDI 5	Data input bit 5
A13	RAMDI 7	Data input bit 7
A14	GND	Ground
A15	GND	Ground
A16	-CAS 1	Bank 1 CAS
A17	-RAS 1	Bank 1 RAS
A18	RAMA 8	Address bit 8
A19	RAMDI 9	Data input bit 9
A20	RAMDI 11	Data input bit 11
A21	+5V	+5v supply
A22	RAMDI 13	Data input bit 13

Table 4-6 continued

Pin	Signal	Description
A23	RAMDI 15	Data input bit 15
A24	GND	Ground
A25	RAMDO 15	Data output bit 15
A26	RAMDO 13	Data output bit 13
A27	RANDO 11	Data output bit 11
A28	AMDO 9	Data output bit 9
A29	RAMA 6	Address bit 6
A30	RAMA 0	Address bit 0
A31	RAMA 2	Address bit 2
A32	RAMA 1	Address bit 1
C1	RAMDO 6	Data output bit 6
C2	RAMDO 4	Data output bit 4
C3	RAMDO 2	Data output bit 2
C4	GND	Ground
C5	RAMDO 0	Data output bit 0
C6	-CAS 3	Bank 3 CAS
C7	-CAS 2	Bank 2 CAS
C8	--------	Not used
C9	RAMDI 0	Data input bit 0
C10	RAMDI 2	Data input bit 2
C11	+5V	+5v supply
C12	RAMDI 4	Data input bit 4
C13	RAMDI 6	Data input bit 6
C14	GND	Ground
C15	GND	Ground
C16	--------	Not used
C17	HIGH WR 2	High byte write enable 2
C18	LOW WR 2	Low byte write enable 2

Table 4-7
Hard Disk Controller (P21)

Pin	Signal	Description
1	WD 0	Data bus bit 0
3	WD 1	Data bus bit 1
5	WD 2	Data bus bit 2
7	WD 3	Data bus bit 3
9	WD 4	Data bus bit 4
11	WD 5	Data bus bit 5
13	WD 6	Data bus bit 6
15	WD 7	Data bus bit 7
17	WA 0	Address bus bit 0
19	WA 1	Address bus bit 1
21	WA 2	Address bus bit 2
23	-WCS	Controller chip select
25	-WWE	Write enable
27	-WRE	Read enable
29	----	Not used
31	----	Not used
33	8 MHZCK	8 megahertz clock
35	WINTRQ	Interrupt request
37	WDRQ	Data request
39	-WMR	Controller reset

All even-numbered pins are connected to ground.

Table 4-8
Hard Disk Expansion (P2) And Hard Disk Data (P22)

P22 Pin	P2 Pin	Signal	Description
1	1	MFMWR	Drive 4 write data
2	14	-MFMWR	Drive 4 write data
3	2	GND	Ground
4	15	GND	Ground
5	3	MFMRD	Drive 4 read data
6	16	-MFMRD	Drive 4 read data
7	4	MFMWR	Drive 3 write data
8	17	-MFMWR	Drive 3 write data
9	5	GND	Ground
10	18	GND	Ground
11	6	MFMRD	Drive 3 read data
12	19	-MFMRD	Drive 3 read data
13	7	MFMWR	Drive 2 write data
14	20	-MFMWR	Drive 2 write data
15	8	GND	Ground
16	21	GND	Ground
17	9	MFMRD	Drive 2 read data
18	22	-MFMRD	Drive 2 read data
19	10	GND	Ground
20	23	GND	Ground

Table 4-8
Parallel Printer Port (P3)

Pin	Signal	Description
1	-STROBE	Data strobe to printer
2	DATA 0	Data bus bit 0
3	DATA 1	Data bus bit 1
4	DATA 2	Data bus bit 2
5	DATA 3	Data bus bit 3
6	DATA 4	Data bus bit 4

Table 4-9 continued

Pin	Signal	Description
7	DATA 5	Data bus bit 5
8	DATA 6	Data bus bit 6
9	DATA 7	Data bus bit 7
10	-ACK	Printer ready to receive data
11	BUSY	Printer busy
12	PE	Paper empty
13	SELECT	Printer selected
14	-AUTO FD XT	Automatic feed
15	-ERROR	Error state
16	-INIT	Reset printer
17	-SLCTIN	Select to printer
18-25	GND	Ground

NOTE: The ground lines can be used as return lines.

Table 4-10
Console (P4) And Serial Printer (P5)
RS-232C Serial I/O

Pin	Signal	Description
1	GND	Ground
2	-TXD	Incoming serial data
3	-RXD	Outgoing serial data
4	RTS	Request to send
5	CTS	Clear to send
6	DSR	Data set ready
7	GND	Ground
8	DCD	Data carrier detect
9-18	----	Not used
19	SRTS	Secondary RTS
20	DTR	Data terminal ready (Busy, Buffer Control Signal)
21-25	----	Not used

Table 4-11
RS-422 Network Port (P6)

Pin	Signal	Description
1	GND	Ground
2	TXD	Data to system
3	RXD	Data to user
4	RTS	Ready to send
5	CTS	Clear to send
6	-TXC	Clock to system
7	-RXC	Clock from system
8	GND	Ground
9	-TXD	Data to system
10	-RXD	Data to user
11	-RTS	Ready to send
12	-CTS	Clear to send
13	TXC	Clock to system
14	RXC	Clock from system

Table 4-12
User Channels (P11-P18)

Pin	Signal	Description
1	GND	Ground
2	-TXD	Data to system
3	TXD	Data to system
4	-RXD	Data to user
5	RXD	Data to user
6	-RTS	Ready to send
7	RTS	Ready to send
8	-CTS	Clear to send
9	CTS	Clear to send
10	TXC	Clock to system
11	-TXC	Clock to system
12	RXC	Clock from system
13	-RXC	Clock from system
14*	-SDIAG	Manufacturing use only
15	GND	Ground
16	----	Not used

* Connector P11 only

Table 4-13
User Expansion (P19)

Pin	Signal	Description
1	----	Not used
2	GND	Ground
3	-RXC OUT	Clock from system
4	GND	Ground
5	RXD OUT	SDLC data from system
6	GND	Ground
7	TXD IN	SDLC data to system
8	-CTS OUT	Clear to send from system
9	-RTS IN	Ready to send to system
10	GND	Ground
11	-TXC IN	Clock to system
12	USER SEL 0	User select line 0
13	USER SEL 1	User select line 1
14	USER SEL 2	User select line 2
15	USER SEL 3	User select line 3
16	----	Not used

Table 4-14
Reset Button (P20)

Pin	Signal	Description
1	GND	Ground
2	RESET	Reset (normally open)
3	-----	Normally closed

APPENDIX A
JUMPER CONFIGURATIONS

Appendix A lists the jumper default configurations and describes the function of each jumper. The jumper configurations provide flexability in operation and are set up in a basic (default) configuration (see Tables A-1 and A-2).

A jumper plug connects the jumper pins but, in some instances, a trace on the motherboard is used. This appendix is divided into motherboard and tape expansion board sections. In the following description of the jumpers, three designations are used:

---	Jumper connection
<X>	Trace must be cut
< >	No connection

Table A-1
Jumper Default Configurations

Basic configuration:

Jumper	Connection	Jumper	Connection
E2	A---B	E14	B---C
E3	B---C	E15	A---B
E4	B---C	E16	A---B
E5	A---B	E17	B---C
E6	A< >B	E18	A---B
E7	A---B	E19	A---B
E8	A< >B	E20	A---B
E9	A---B	E21	A---B
E10	A---B	E22	A< >B

Table A-1 Continued

Jumper	Connection	Jumper	Connection
E11	A---B	E23	A---B
E12	B---C	E24	A---B
E13	A---B		

Tape configuration (modified basic configuration):

Jumper	Connection
E4	B---C
E14	A---B
E19	B---C

MOTHERBOARD

Memory Configurations

Thirty-two 64Kx1 dynamic RAM devices, 256 Kbytes total (default).

E3	A< >B	B---C
E4	A< >B	B---C
E12	A< >B	B---C
E13	A---B	B< >C
E14	A< >B	B---C
E19	A---B	B< >C

Sixty-four 64Kx1 dynamic RAM devices, 512 Kbytes total. This configuration is used in the PM/16M memory expansion model.

E3	A< >B	B---C
E4	A---B	B< >C
E12	A< >B	B---C
E13	A< >B	B---C
E14	A< >B	B---C
E19	A---B	B< >C

Sixteen 256Kx1 dynamic RAM devices, 512 Kbytes total.

E3	A< >B	B---C
E4	A---B	B< >C
E12	A< >B	B---C
E13	A---B	B< >C
E14	A---B	B< >C
E19	A< >B	B---C

Thirty-two 256Kx1 dynamic RAM devices, 1 megabyte total.

E3	A---B	B< >C
E4	A---B	B< >C
E12	A---B	B< >C
E13	A---B	B< >C
E14	A< >B	B---C
E19	A< >B	B---C

Two 2Kx8 static RAM devices (default).

E6	A< >B	
E7	A---B	B< >C
E9	A---B	B< >C
E10	A---B	B< >C

One 8Kx8 static RAM device.

E6	A---B	
E7	A< >B	B---C
E9	A< >B	B---C
E10	A< >B	B< >C

Two 8Kx8 static RAM devices.

E6	A< >B	
E7	A< >B	B---C
E9	A< >B	B---C
E10	A< >B	B---C

Parallel Data Bits

Sets the parallel data bits for the PDI input of the memory mapping RAM (U96).

Interval between refreshes is decreased by 0% (default).

```
E16     A---B     B< >C
E20       A---B B< >C
```

Interval between refreshes is decreased by 10%.

```
E16     A---B     B< >C
E20     A<X>B     B---C
```

Interval between refreshes is decreased by 20%.

```
E16     A<X>B     B---C
E20     A---B     B< >C
```

Interval between refreshes is decreased by 30%.

```
E16     A<X>B     B---C
E20     A<X>B     B---C
```

Fast RAM (default)

```
E17     A< >B     B---C
```

Slow RAM

```
E17     A---B     B<X>C
```

RAM cycle not extended (default).

```
E18     A---B     B< >C
```

RAM cycle is extended.

E18 A<X>B B---C

Network Channel Termination

Set this jumper to "terminated" if the Personal Mini is located at either end of the network cable. If the Personal Mini is located between two other Personal Mini systems, set the jumper to "not terminated."

Terminated (default)

E21 A---B
E23 A---B
E24 A---B

Not Terminated

E21 A<X>B
E23 A<X>B
E24 A<X>B

Normal DCE or Reverse Channel Protocol

E11 modifies the console interface and E15 modifies the serial printer interface. E11 and E15 allow connection to either the DTR (normal DCE) signal or SRTS (reverse channel protocol) signal.

Normal DCE (default)

E11 A---B B< >C
E15 A---B B< >C

Reverse Channel Protocol

E11 A<X>B B---C
E15 A< >B B---C

Z80A Reset

The reset signal may come from either the Z Reset Latch (U21) or the reset button on the front panel.

Z Reset Latch (default)

E2 A---B B< >C

Reset Button

E2 A< >B B---C

DR4 MFMWR

The E5 jumper must always remain connected.

CLKOUT BF

This jumper breaks the CLKOUT BF signal line to U54, which goes to a pin (P21-33) that is reserved for later use.

E8 A< >B

Serial Printer Port

The diagnostic console may be connected to the serial printer port.

Serial Printer (default)

E22 A< >B

Diagnostic Console

E22 A---B

TAPE EXPANSION BOARD

Seven jumpers on the tape expansion board are default-configured according to the expansion slot used for the tape drive (see Table A-2).

Table A-2
Tape Board Default Configuration

X1		X2	
Jumper	**Connection**	**Jumper**	**Connection**
J1	1---2	J1	2---3
J2	1---2	J2	2---3
J3	1---2	J3	2---3
J4	1---2	J4	1---2
J5	1---2	J5	1---2
J6	2---3	J6	2---3
J7	2---3	J7	1---2

X1 or X2 Configuration

JI, J2, J3, and J7 configure expansion slots X1 and X2.

X1 Slot (default)

J1	1---2	2< >3	-INTA Z TO X1
J2	1---2	2< >3	-INT X1 TO Z
J3	1---2	2< >3	Address decoder output which initializes U14 output for X1
J7	1< >2	2---3	-BUS ACK
J7	1---2	2< >3	If tape is in X1 and another card is in X2.

X2 Slot

J1	1< >2	2---3	-INTA Z TO X2
J2	1< >2	2---3	-INT X2 TO Z
J3	1< >2	2---3	Address decoder output which initializes U14 output for X2
J7	1---2	2< >3	-BUS ACK IN

EPROM Size

J4	1---2	2< >3	8 Kbytes (default)
J4	1< >2	2---3	4 Kbytes

Local Static RAM Size

4 Kbytes (default)

J5	1---2	2< >3
J6	1< >2	2---3

8 Kbytes or 16 Kbytes

J5	1< >2	2---3
J6	1---2	2< >3

APPENDIX B
SELF DIAGNOSTICS

The Personal Mini contains self-test diagnostics that are automatically run during system initialization. The PM/16 diagnostics are similar to the enhanced version in the PM/4T and PM/16T units. The main differences are the optional memory test and the tape diagnostics. The diagnostic LED indicators flash during the self-test to indicate an error.

When the diagnostics are successfully completed, the operating system is loaded.

The self diagnostics are divided into two sets. The first is for the EPROM which comes with the basic PM/16 unit, and the second is for the one that comes with the PM/4T and PM/16T units.

At power-on, the 16-bit CPU disables the interrupts and performs a system reset. All CPU diagnostic indicators are flashed once.

The 2681 DUART is now initialized allowing communication on the service terminal. The CPU (16-bit) diagnostics begin at this time.

BASIC UNIT (PM/16)

Memory Test

The memory test is performed by writing a pattern in main memory and then reading it back. The data patterns %FF, %00, and incrementing %00-%FF are repeated for the entire memory.

An error in the memory test causes the DS5 indicator to flash. The system halts testing and prints the error message:

MEMORY ERROR.....

Successful completion of the memory test turns off all indicators and the system moves to the next test.

Checksum

A checksum is then made on the system PROM to detect any alterations to the data stored in the PROM. An error in this test causes the DS6 indicator to flash. The system halts testing and prints the error message:

HASH TOTAL ERROR

Successful completion of the PROM test turns off the indicators and the system moves to the next test.

Memory Size

The size of the main memory is now displayed.

Interrupt Test

A software interrupt test is now performed on all interrupts. An error in the interrupt test displays one of the error messages:

NO INTERRUPT

INTERRUPT TEST ERROR

The system moves to the next test.

Timer Interrupt Test

The timer interrupt test checks the timer 0 and 2 interrupts. If an interrupt is not detected, then the following error message is displayed:

0 NO TIMER INTERRUPT

2 NO TIMER INTERRUPT

If any other interrupt is detected the following error message is displayed:

TIMER INTERRUPT TEST ERROR

Restore Test

After completion of the interrupt tests, the system resets the floppy disk controller and then the hard disk controller.

The Z80A is now released so that it can perform the 8-bit diagnostics. See the Z80A Checksum Test for the description of the 8-bit diagnostics.

A floppy disk restore and then a hard disk restore is performed. An error displays one of the following messages:

TOO MUCH TIME

FLOPPY DRIVE RESTORE ERROR

HARD DISK RESTORE ERROR

STATUS = XX

XX = Hex status code from hard disk controller.

System Boot

The system now displays the following message:

HIT ESC TO BOOT FROM THE FLOPPY DISK

If no answer is given within ten seconds, the system boots from the hard disk. If the user presses the <ESC> key, the system boots from the floppy disk.

For either a hard disk or a floppy disk boot, the system will load the boot record into memory. The operating system is then loaded and execution begins. An initial message is displayed to indicate the operating system.

Hard Disk Boot

Prior to the hard disk boot, a reset to the hard disk controller is performed. A restore is again performed to read the system information from the disk. Some of the possible error messages are:

BAD BOOT SECTOR .....RESET PLEASE

...READ ERROR...

HARD DISK SEEK ERROR

An error in the hard disk boot causes the DS7 indicator to flash.

Floppy Disk Boot

Prior to the floppy disk boot, a reset to the floppy controller is performed. A restore is again performed to read the system information from the disk. Some of the possible error messages are:

CHECK FLOPPY DISKETTE PLEASE

CONTROLLER ALWAYS BUSY, NO COMMAND ISSUED

...SEEK ERROR...

...NO DRQ...

...READ ERROR...

Z80A Checksum Test

A checksum test is made on the Z80A EPROM to detect any alterations to the stored data. If an error occurs, DS1 and DS2, and DS3 and DS4 indicators will flash alternately.

Static RAM

A static RAM test is performed using %00, %FF, %55, and %AA patterns. If an error occurs, DS2 will flash.

Dynamic RAM

A dynamic RAM test is performed and an error causes DS1 and DS2 to flash.

SIO Test

The SIO ports are initialized and an error causes DS1, DS2, DS3, and DS4 to flash %0F - %00.

System Loader

The Z80A CPM3 system loader is initialized by initializing the interrupt vectors and memory mapper. The Z80A now halts, waiting for an interrupt.

TAPE UNIT (PM/4T, PM/16T)

The tape unit contains its own Z80A processor and EPROM for diagnostics. When the 80186 CPU completes its tests, it releases the main board Z80A and the tape Z80A to perform their diagnostics. There are four diagnostic LED's located on the tape expansion board. The LED's light up to indicate the test being run and flash if there is an error. The LED indicators light up giving the binary-coded test sequence.

Optional Memory Test

An optional memory test can be performed. This test has a menu and takes several minutes, depending on the menu selections. If the Control "@" keys are not pressed then the timed period ends, bypassing this test. The DS5 indicator lights to indicate that this test is being run.

CPU Memory Test

The memory test is performed by writing a pattern in main memory and then reading it back. The data patterns %FF, %00, and incrementing %00-%FF are repeated for the entire memory.

An error in the memory test causes the DS5 indicator to flash. The system halts testing and displays the error message:

MEMORY ERROR.....

CPU Checksum

A checksum test is made on the system PROM to detect any alterations to the data stored. An error in this test causes the DS6 indicator to flash and the following error message is displayed.

HASH TOTAL ERROR

Memory Size

The size of the main memory is now displayed.

CPU Interrupt Test

A software interrupt test is now performed on all interrupts. An error displays one of the following messages:

NO INTERRUPT

INTERRUPT TEST ERROR

CPU Timer Interrupt Test

This test checks the timer 0 and timer 2 interrupts. If an interrupt is not detected, then one of the following error messages is displayed.

0 NO TIMER INTERRUPT

2 NO TIMER INTERRUPT

If any other interrupt is detected the following message is displayed.

TIMER INTERRUPT TEST ERROR

8-Bit Diagnostics

After completion of the interrupt tests, the system resets the floppy disk controller and then the hard disk controller.

The 80186 now releases the Z80A and any expansion cards to perform the 8-bit diagnostics.

Expansion Slot Configuration

The Z80A checks the expansion slots, and, if occupied, places their ID in memory at a preset location.

Z80A Checksum

A checksum test is made on the Z80 EPROM to detect any alterations to the stored data. The DS1 indicator is used and the following error message is displayed.

ERROR Z80 EPROM

Z80 Static RAM

A static RAM test is performed using %00. %FF, %55, and %AA patterns. If an error occurs, DS2 flashes and the following error message is displayed.

ERROR Z80 EPROM

Z80A Initial Status

The 80186 polls the Z80A for its initial status and waits for a reply. If the status contains an error, an error message is displayed. If there is no reply, the following message is displayed.

NO REPLY FROM PROCESSOR Z

Tape Configuration

The tape Z80A checks memory for its slot location, and, if not located, assumes it is located in slot 1. If not located, the following error message appears:

ERROR TAPE ID

Tape Checksum

A checksum is made on the tape EPROM to detect any alterations to the stored data. If an error occurs, the DS2 indicator flashes and the following error message appears.

ERROR TAPE CHECKSUM

Tape Static RAM

The local memory is tested using incrementing patterns %55, %AA, %FF, and %00. The DS1 and DS2 indicators are used and the following message is displayed:

ERROR TAPE LOCAL PROM

Tape Initial Status

The 80186 polls the initial status of the tape Z80A and waits for a reply. If the status contains an error, an error message is displayed. If there is no reply, the following message is displayed:

NO REPLY FROM PROCESSOR X

X = slot location

Z80 Dynamic RAM

A dynamic RAM test if performed and an error causes DS1 and DS2 to flash and the following error message is displayed:

ERROR Z80 LOCAL PROM

Z80 Memory Status

The 80186 polls the Z80A for its memory status and waits for a reply.

Tape Dynamic RAM

A dynamic RAM test is performed by the tape Z80A. The DS3 indicator is used and the following error message is displayed:

ERROR TAPE DYNAMIC RAM

DMA Local To Dynamic

The DMA transfers data from local memory to main memory and the DMA interrupt is set to indicate completion of data transfer. The DS1 and DS3 indicators are used and one of the following error messages is displayed:

ERROR TAPE DMA NO INTERRUPT

ERROR TAPE DMA LOCAL TO MAIN MEMORY

DMA Dynamic To Local

The DMA transfers data from main memory to the static memory and the DMA interrupt is set to indicate completion of data transfer. The DS2 and DS3 indicators are used and one of the following error messages is displayed:

ERROR TAPE DMA NO INTERRUPT

ERROR TAPE DMA MAIN TO LOCAL MEMORY

Tape Memory Status

The CPU polls the tape Z80 for its memory status and waits for a reply.

Z80 SIO

The SIO ports are initialized and an error causes DS3 to flash. The following error message is displayed:

ERROR Z80 SIO

Z80 Final Test Status

The CPU polls the Z80A for its final test status and waits for a reply.

Tape CTC

The CTC is set up to generate the timer mode of channel 0 and the counter mode of channel 2. It then signals the main Z80 to block its access to main memory for a short period. The DS1, DS2, and DS3 indicators are used and one of the following error messages is displayed:

ERROR CTC 0, NO INTERRUPT

ERROR CTC 2, NO INTERRUPT

Tape Reset

A tape reset is performed and the status is checked. If an error occurs, one of the following error messages is displayed:

ERROR TAPE RESET

TAPE CARTRIDGE NOT INSTALLED

Tape Motion

If the tape is installed in the unit, a rewind operation is performed. If an error occurs, the following error message is displayed:

ERROR TAPE BOOT

Tape Final Test Status

The CPU polls the tape Z80 for its final test status and waits for a reply.

Optional Tape Diagnostics

To request the optional tape diagnostics, type in a question mark when the escape message is displayed on the screen. A rewind operation is performed prior to each read or write operation. When an error occurs, an error message and the status of the tape controller are displayed. Table B-1 lists the LED's the PM will light up for a given problem. The tape status bits are defined in Table B-2 and the tape extended status bits are defined in Table B-3. Table B-4 lists the hex complementary status bits.

Bit 7 is the most significent bit and bit 0 is the least significent bit. The controller status is displayed as follows:

STATUS = NN XX XX XX XX XX XX

NN = Sequence number of the test as defined by the binary coded indicators.

XX = Tape controller status from byte 0 - 5 in complementary hex.

Table B-1
Sequence Number And Error Message

Sequence Number*	Error Message
8	Tape Cartridge Not Installed
8	Tape Is Write Protected
B	Error Tape Write
A	Error Tape Read
0	Aborting, No Tape Unit
0	Main Z80 Failed Test
0	No Reply From Processor Z
0	No Reply From Processor 1
0	No Reply From Processor 2

* Sequence number in hex.

Table B-2
Tape Status Bits

Byte 0

Bit	Description
0	File mark detected
1	Block not found
2	Unrecoverable data error
3	End of Tape (media)
4	Tape is write protected
5	Tape not online
6	Tape cartridge not installed
7	Status bit set in byte 0

Table B-2 continued
Tape Status Bits

Byte 1

Bit	Description
0	Power on or reset occurred
1	Fault (ROM, RAM, or buffer)
2	Bus parity error (command or data output)
3	Beginning of tape (media)
4	Marginal block detected during write retry
5	No data detected
6	Illegal command sent to tape controller
7	Status bit set in byte 1

Byte 2

MSB — Data error counter

Byte 3

LSB — Data error counter

The data error counter is incremented when a block has to be rewritten or a read retry has been made.

Byte 4

MSB — Underrun/Overrun counter

Byte 5

LSB — Underrun/Overrun counter

	This counter is incremented when data to the tape controller is not sent fast enough to enable the tape to stream. It is also incremented if data is not accepted fast enough to enable the tape to stream.

Table B-3
Tape Extended Status Bits

Byte 0

Bit	Description
0	Not used
1	Erase current not detected during an erase or write command
2	Clear reader tape is detected before BOT/EOT during a write.
3	Timeout (command execution)
4	Repositioning Error
5	Tape controller buffer error
6	Tape controller RAM error
7	Tape controller ROM error

Byte 1

0	Tape drive 0 selected
1	Tape drive 1 selected
2 - 7	No tape drive selected

Byte 2

0 - 1	00 Track 0 01 Track 1 10 Track 2 11 Track 3
2 - 7	No track selected

Table B-3 continued

Byte 3

Bit	Description
MSB	Current block number (binary)

Byte 4

LSB	Current block number

Table B-4
Hex Complementary Status Bits

	Bits							
Count	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
7F	0	1	1	1	1	1	1	1
BF	1	0	1	1	1	1	1	1
DF	1	1	0	1	1	1	1	1
EF	1	1	1	0	1	1	1	1
F7	1	1	1	1	0	1	1	1
FB	1	1	1	1	1	0	1	1
FD	1	1	1	1	1	1	0	1
FE	1	1	1	1	1	1	1	0

NOTE: True = 0, False = 1

System Loader

The Z80A CPM3 system loader is initialized by initializing the interrupt vectors and memory mapper. The main Z80 now halts and waits for an interrupt.

Restore Test

A floppy disk restore and then a hard disk restore are performed. An error will display one of the following messages:

TOO MUCH TIME

FLOPPY DRIVE RESTORE ERROR

HARD DISK RESTORE ERROR

STATUS = XX

XX = Hex status code as listed in Table B-5.

Table B-5
Drive Hex Status Code

Floppy Disk

Hex	Bit	Description
80	7	Motor on
40	6	Write protected
20	5	Type I commands: Spin up sequence completed, 6 rev. Type II - II commands: 0 = Data mark 1 = Deleted data mark
10	4	Record not found
08	3	CRC error: ID field error if bits 3 and 4 are set Data field error if not set

Table B-5 continued

Hex	Bit	Description
04	2	Type I command: Track 00 indicator Type II - III commands: Lost data
02	1	Type I command: Index Type II - III commands: Data request
01	0	Busy

Type I Commands

Restore
Seek
Step
Step-in
Step-out

Type II Commands

Read Sector
Write Sector

Type III Commands

Read Address
Read Track
Write Track

Table B-5 continued

Hard Disk

Hex	Bit	Description
80	7	Bad block detected
40	6	CRC data field error
20	5	...Reserved... (not used)
10	4	ID not found
08	3	...Reserved... (not used)
04	2	Command aborted
02	1	Track 000 error
01	0	Data address mark not found

Hard Disk Commands

Restore
Seek
Read Sector
Write Sector
Scan ID
Write Format

Boot

The System now displays the following message:

HIT ESC TO BOOT FROM FLOPPY

If no answer is given within a short period of time, the system boots from the hard disk. If the user presses the <ESC> key, the system boots from the floppy disk.

For either a hard disk boot or a floppy disk boot, the system loads the boot record into memory. The operating system is then loaded and execution begins. An initial message is displayed to indicate the operating system.

Hard Disk Boot

Prior to the hard disk boot, a reset to the hard disk controller is performed. A restore is again performed to read the system information from the disk. Some of the possible error messages:

BAD BOOT.....RESET PLEASE

...READ ERROR...

HARD DISK SEEK ERROR

An error in the hard disk boot causes DS7 to flash.

Floppy Disk Boot

Prior to the floppy disk boot, a reset is performed. A restore is again performed to read the system information from the disk. Some of the error messages are:

CHECK FLOPPY DISKETTE PLEASE

CONTROLLER ALWAYS BUSY, NO COMMAND ISSUED

...SEEK ERROR...

...NO DRQ...

...READ ERROR...

APPENDIX C
LOGIC DIAGRAMS

This section contains the logic diagrams of the Personal Mini. They are:

* Personal Mini (motherboard)
* Winchester disk controller board
* Tape expansion board

NAMES OF CONNECTORS:

P1: DC POWER (10P MOLEX WAFER)
P10: 16Ø8 MEM EXTENSION (64P DIN-TYPE, 2 ROWS)
P9: FLOPPY DISK (34P STR HDR)
P21: HARD DISK HOST INTERFACE (4ØP STR HDR)
P22: HARD DISK DATA DR 2/3/4 (2ØP STR HDR)
P2: HARD DISK DATA DR 2/3/4 EXTERNAL (25P DB-TYPE)
P6: RS422 NETWORK (15P DB-TYPE)
P3: PARALLEL PRINTER (25P DB-TYPE)
P20: RESET BUTTON (3P MOLEX WAFER)
P5: SERIAL PRINTER (25P DB-TYPE)
P4: CONSOLE (25P DB-TYPE)
P11 - P18 : 8 USER CHANNELS (16P STR HDR)
P19: EXTRA USER CHANNELS (16P STR HDR)
P8: OPTIONAL CARD X1 SLOT (96P DIN TYPE, 3 ROWS)
P7: OPTIONAL CARD X2 SLOT (96P DIN TYPE, 3 ROWS)

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE VALUED IN OHMS AND ARE 1/4 WATT ±5%.
2. ALL CAPACITORS ARE VALUED IN µf. 16 VDC AND ARE ±20%.

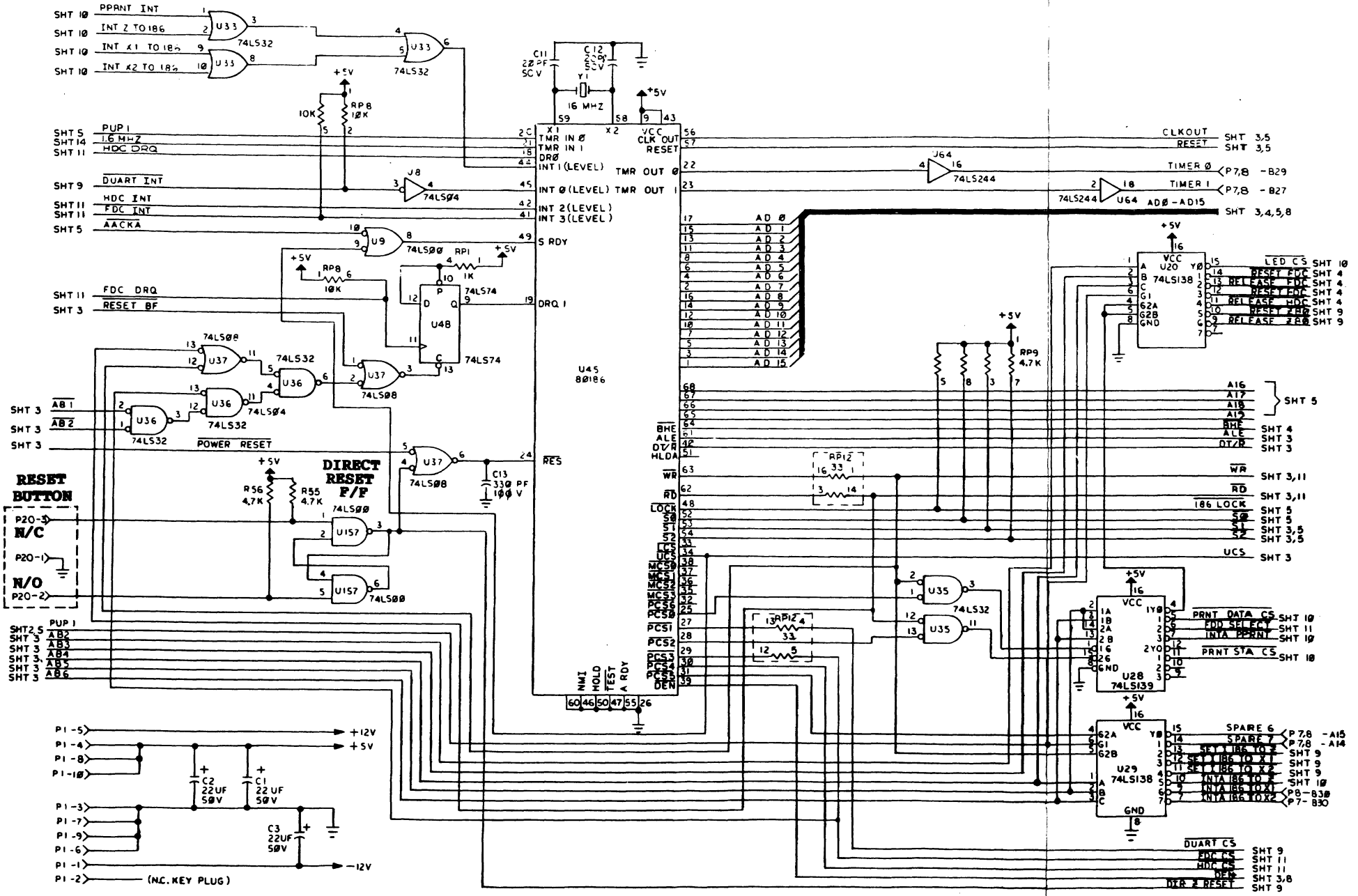
NOTES ON JUMPERS:

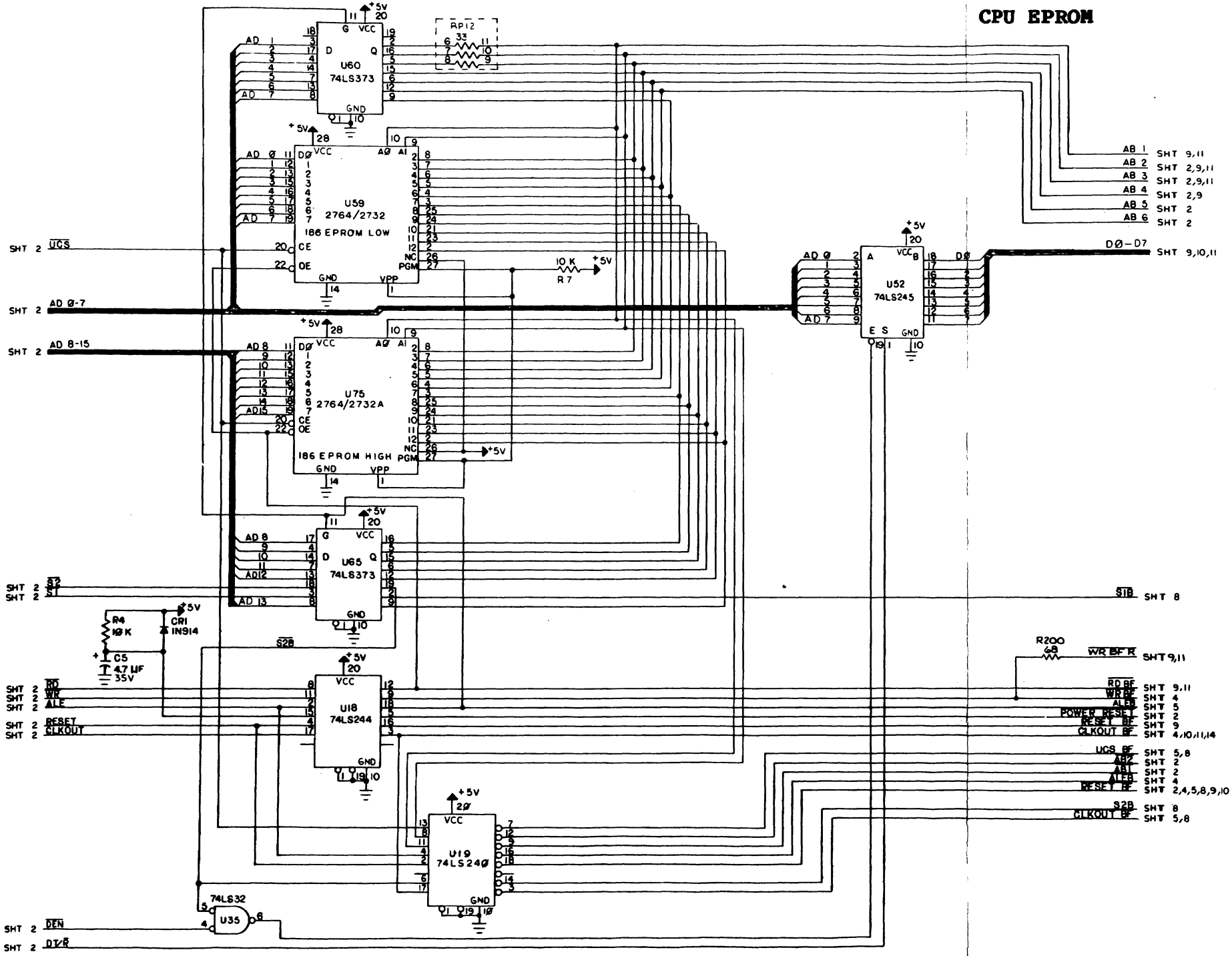
A) STANDARD MOUNTING OF JUMPERS:

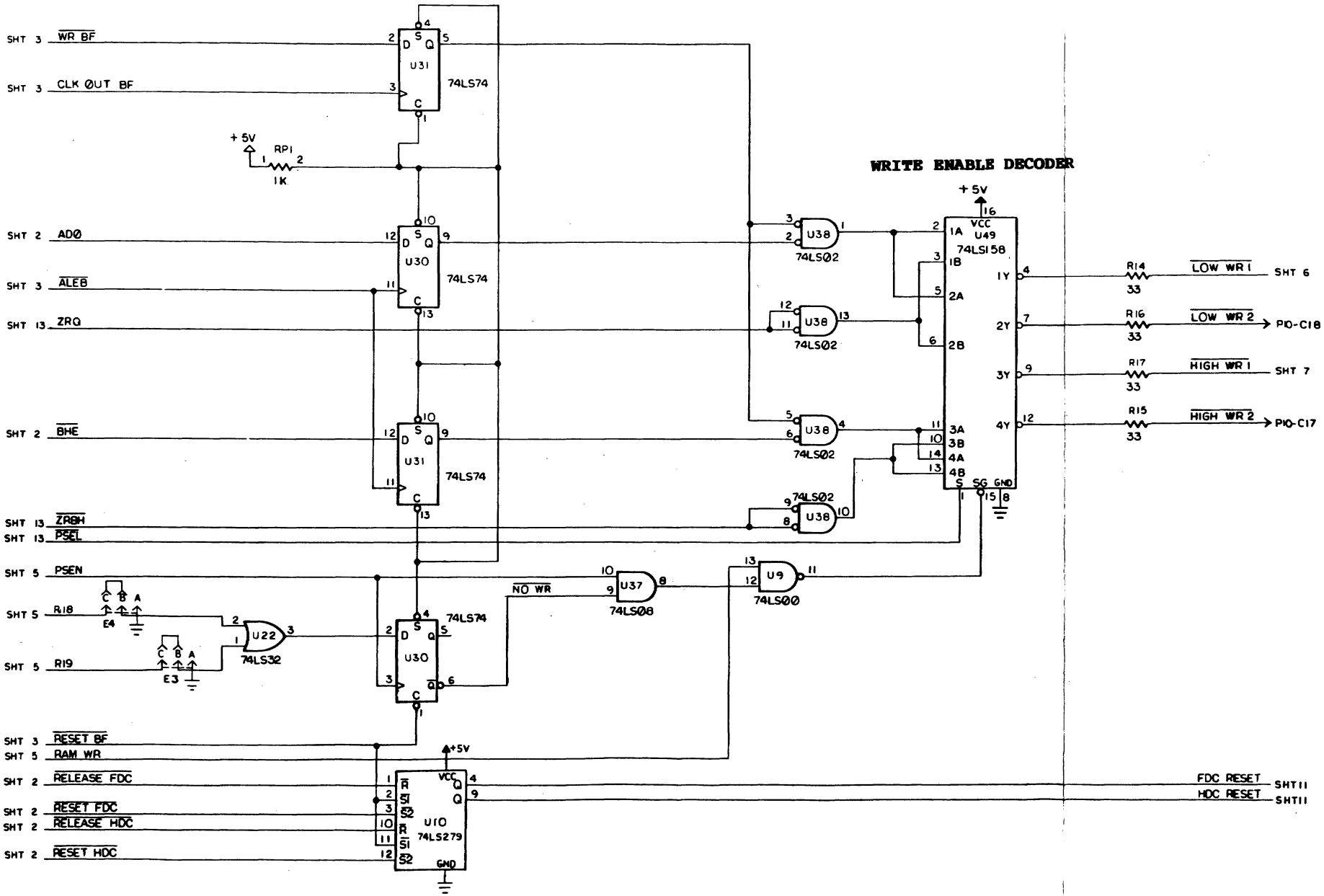
E14 B-C	E6 (PARK ON PIN B)
E13 A-B	E7 A-B
E12 B-C	E9 A-B
E4 B-C	E10 A-B
E3 B-C	
E19 A-B	
E2 A-B	
E15 A-B	

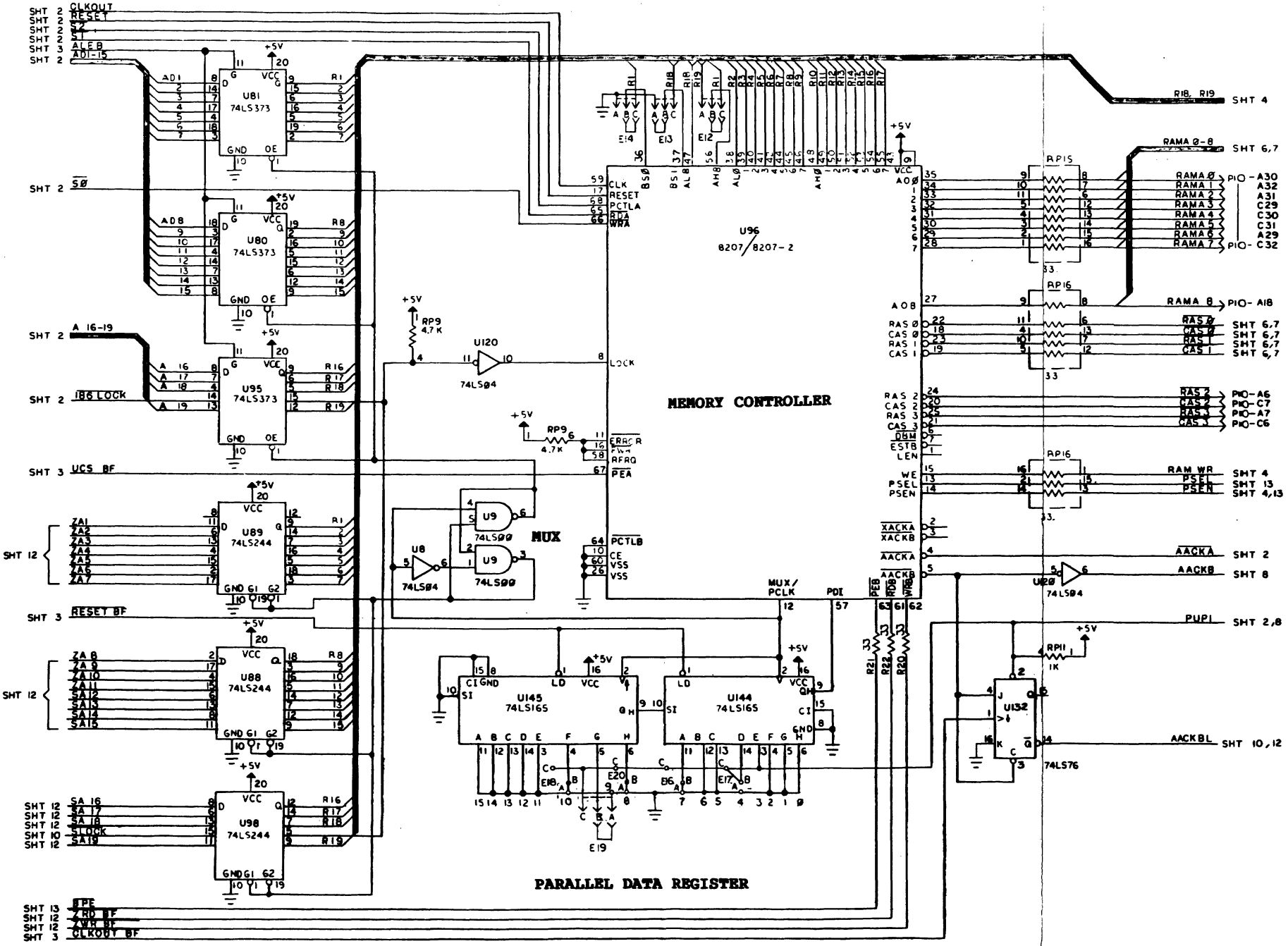
B) OPTIONAL MOUNTING OF JUMPERS:

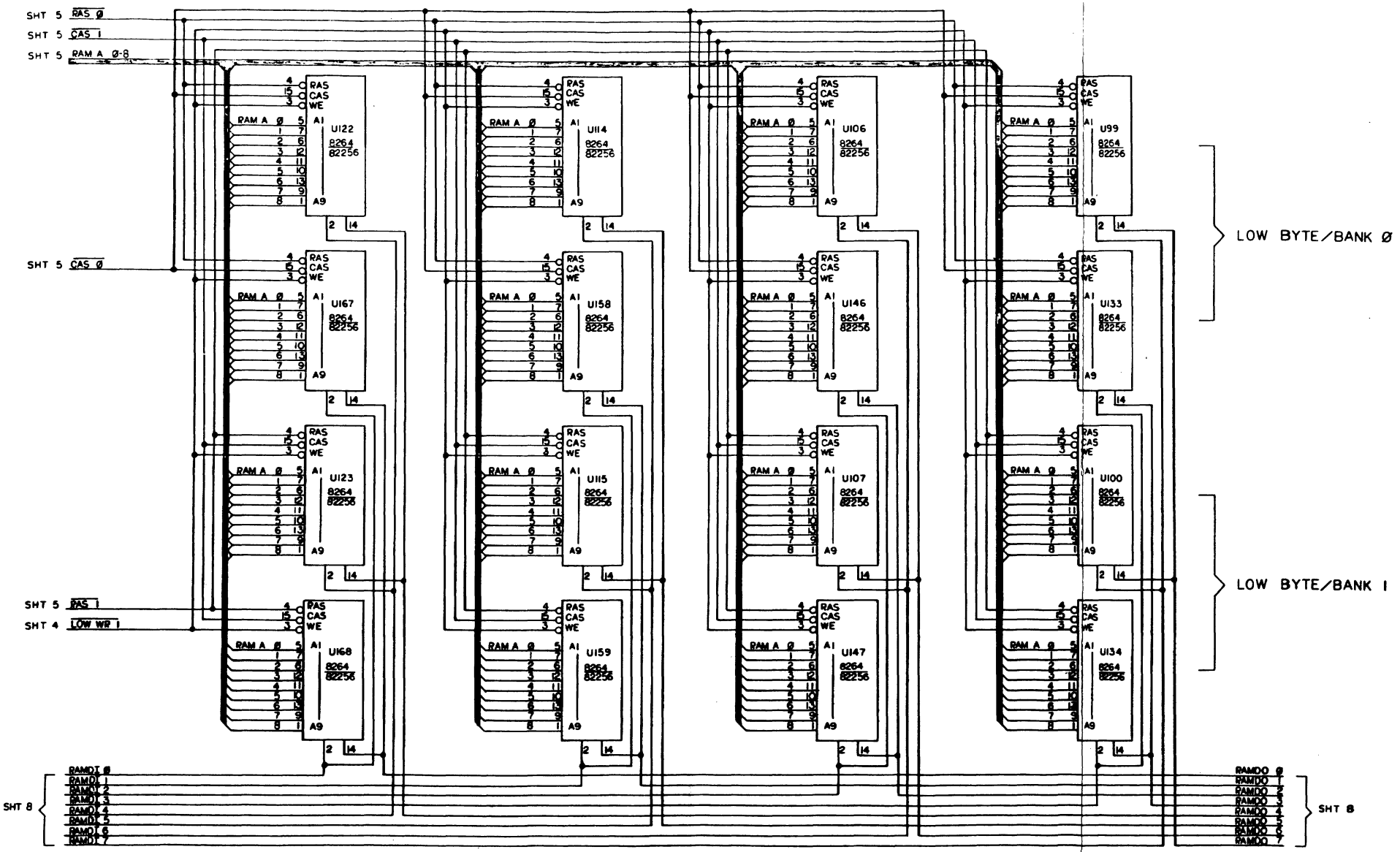
① 512K OF 64K DRAMS: E14(A-B), E13(A-B), E12(B-C), E4(A-B), E3(B-C), E19(A-B)
② 512K OF 256K DRAMS: E14(A-B), E13(A-B), E12(B-C), E4(A-B), E3(B-C), E19(B-C)
③ 1M OF 256K DRAMS: E14(B-C), E13(A-B), E12(A-B), E4(A-B), E3(A-B), E19(B-C)
④ REVERSE CHANNEL ON SERIAL PRINTER: E15(B-C)
⑤ Z8Ø DIAGNOSTICS CONSOLE: E22(A-B)
⑥ DIRECT RESET Z8Ø THROUGH RESET BUTTON: E28-C
⑦ TWO 2KX8 SRAM'S E6 (PARK ON PIN B), E7 (A-B), E9 (A-B), E10 (A-B)
⑧ ONE 8KX8 SRAM'S E6 (A-B), E7 (B-C), E9 (B-C), E10 (PARK ON PIN C)
⑨ TWO 8KX8 SRAM'S E6 (PARK ON PIN B), E7 (B-C), E9 (B-C), E10 (B-C)

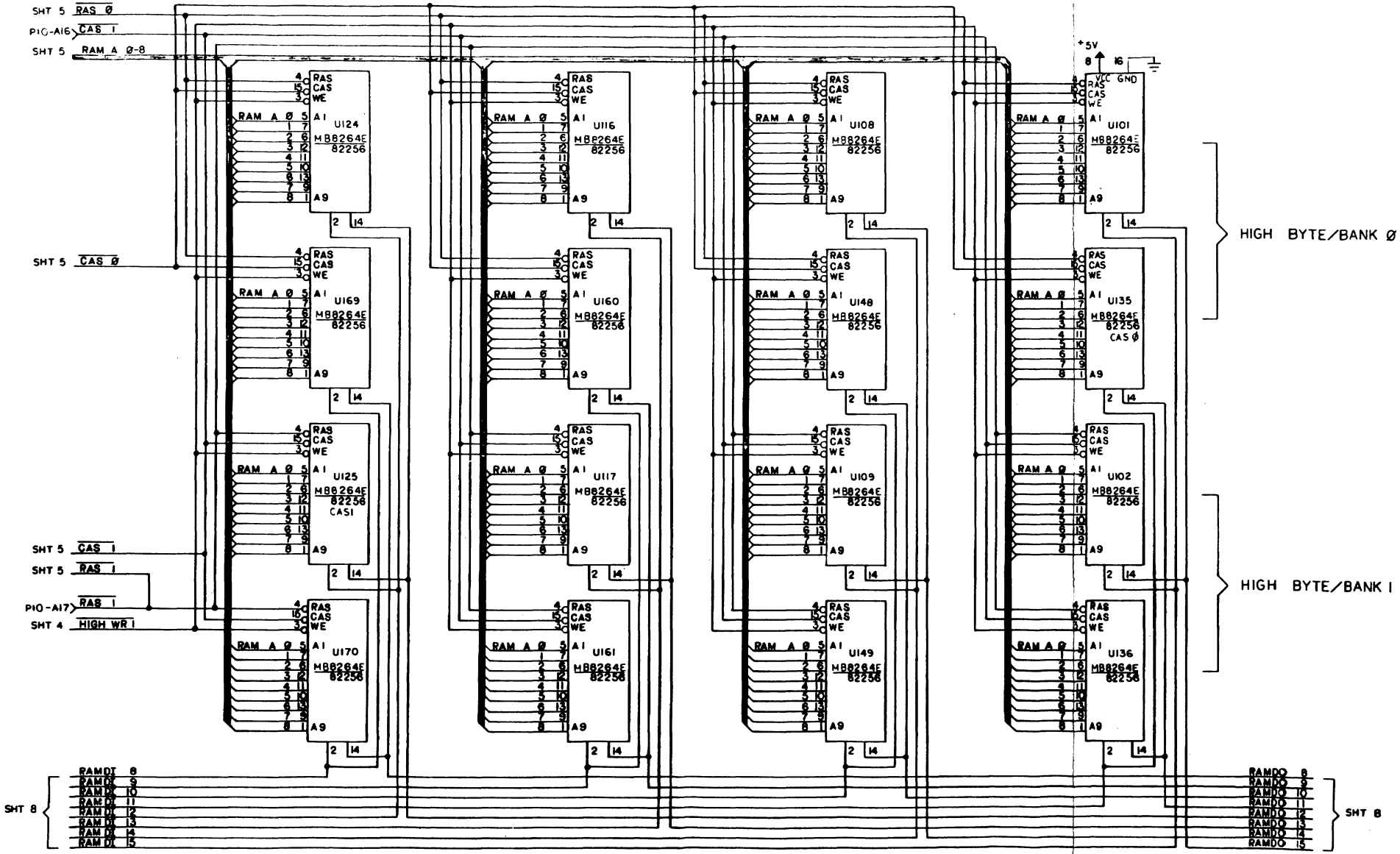

SHT 10 PPRNT INT
SHT 10 INT 2 TO 186
SHT 10 INT X1 TO 186
SHT 10 INT X2 TO 186
U33
74LS32
+5V
10K
RP8 10K
SHT 5 PUP 1
SHT 14 1.6 MHZ
SHT 11 HDC DRQ
SHT 9 DUART INT
SHT 11 HDC INT
SHT 11 FDC INT
SHT 5 AACKA
U8
74LS04
C11 22 PF 5CV
C12 22 PF 5CV
Y1
16 MHZ
X1
X2
VCC
CLK OUT
RESET
TMR IN 0
TMR IN 1
DRQ0
INT 1 (LEVEL)
INT 0 (LEVEL)
TMR OUT 0
TMR OUT 1
INT 2 (LEVEL)
INT 3 (LEVEL)
S RDY
DRQ 1
U45
80186
U9
74LS00
RP1 1K
RP8 10K
SHT 11 FDC DRQ
SHT 3 RESET BF
U48
74LS74
U37
74LS08
U36
74LS32
74LS04
SHT 3 AB1
SHT 3 AB2
SHT 3 POWER RESET
RESET BUTTON
P20-3 N/C
P20-1
N/O
P20-2
DIRECT RESET F/F
R56 4.7K
R55 4.7K
U157
74LS00
C13 330 PF 100 V
RES
NMI
HOLD
TEST
A RDY
J64
74LS244
CLKOUT SHT 3,5
RESET SHT 3,5
TIMER 0 P7,8 -B29
TIMER 1 P7,8 -B27
AD0 - AD15 SHT 3,4,5,8
RP9 4.7K
A16 A17 A18 A19 SHT 5
BHE SHT 4
ALE SHT 3
DT/R SHT 3
WR SHT 3,11
RD SHT 3,11
186 LOCK SHT 5
S0 SHT 5
S1 SHT 3,5
S2 SHT 3,5
UCS SHT 3
RP12 33
RP13 33
U35
74LS32
U20
74LS138
LED CS SHT 10
RESET FDC SHT 4
RELEASE FDC SHT 4
RESET HDC SHT 4
RELEASE HDC SHT 4
RESET 2 RS SHT 9
RELEASE 2 RS SHT 9
U28
74LS139
PRNT DATA CS SHT 10
FDD SELECT SHT 11
INTA PRNT SHT 10
PRNT STA CS SHT 10
U29
74LS138
SPARE 6 P7,8 -A15
SPARE 7 P7,8 -A14
SET 186 TO X2 SHT 9
SET 186 TO X1 SHT 9
SET 186 TO X2 SHT 9
INTA 186 TO X1 SHT 10
INTA 186 TO X2 P8-830
P7-830
DUART CS SHT 9
FDC CS SHT 11
HDC CS SHT 11
DEN SHT 3,8
DIR 2 RESET SHT 9
P1-5 +12V
P1-4 +5V
P1-8
P1-10
P1-3
P1-7
P1-9
P1-6
P1-1 -12V
P1-2 (N.C. KEY PLUG)
C2 22UF 50V
C1 22 UF 50V
C3 22UF 50V

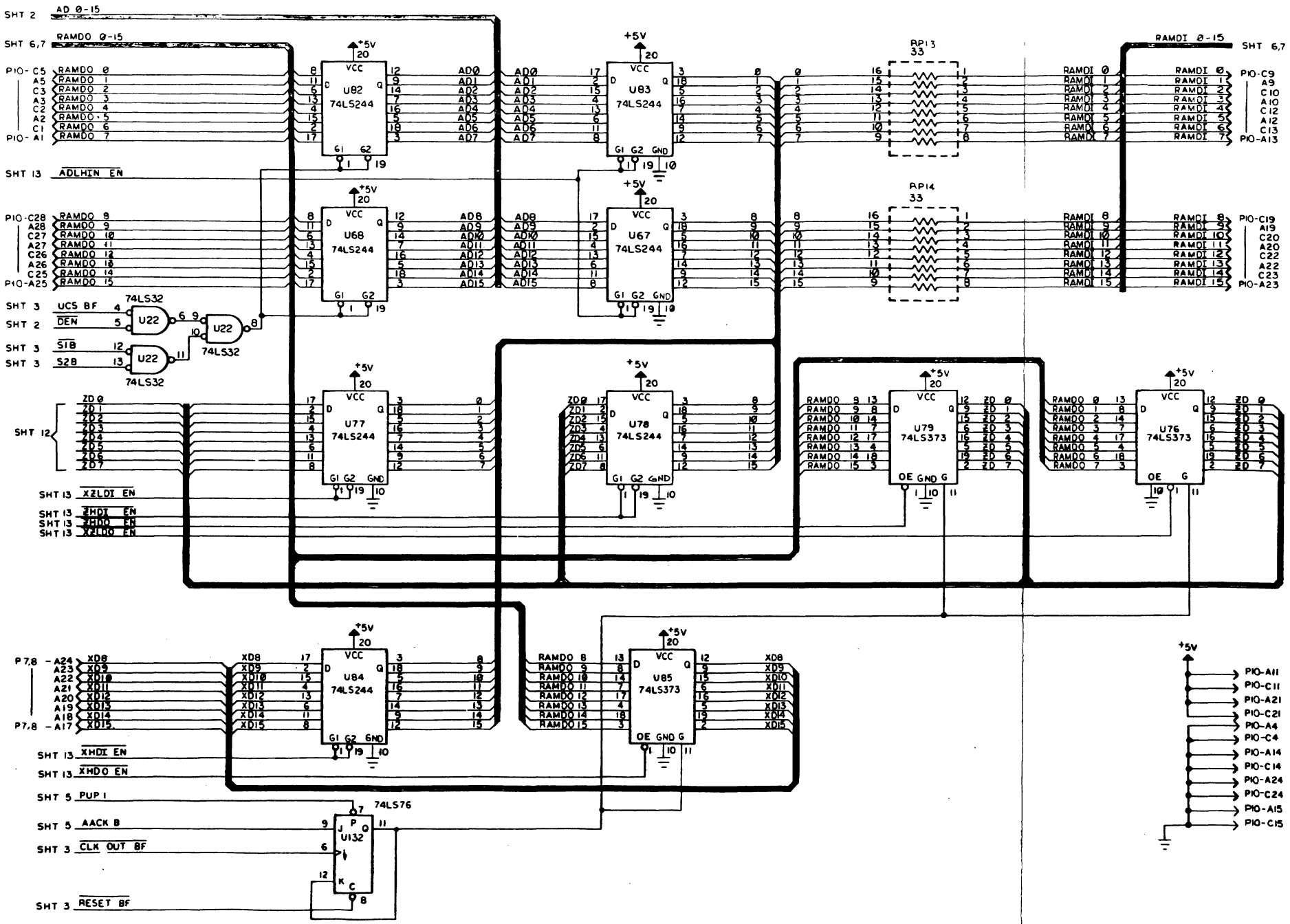

CPU EPROM
U60
74LS373
RP12
33
U59
2764/2732
186 EPROM LOW
U75
2764/2732A
186 EPROM HIGH
10 K
R7
U52
74LS245
U65
74LS373
R4
10 K
CR1
IN914
C5
4.7 UF
35V
U18
74LS244
U19
74LS240
74LS32
U35
R200
68
SHT 2 UCS
SHT 2 AD 0-7
SHT 2 AD 8-15
SHT 2 S2
SHT 2 S1
SHT 2 S0
SHT 2 RD
SHT 2 WR
SHT 2 ALE
SHT 2 RESET
SHT 2 CLKOUT
SHT 2 DEN
SHT 2 DT/R
AB 1 SHT 9,11
AB 2 SHT 2,9,11
AB 3 SHT 2,9,11
AB 4 SHT 2,9
AB 5 SHT 2
AB 6 SHT 2
D0-D7 SHT 9,10,11
STB SHT 8
WR BF R SHT 9,11
RD BF SHT 9,11
WR BF SHT 4
ALE BF SHT 5
POWER RESET SHT 2
RESET BF SHT 9
CLKOUT BF SHT 4,10,11,14
UCS BF SHT 5,8
AB2 SHT 2
AB1 SHT 2
ALE BF SHT 4
RESET BF SHT 2,4,5,8,9,10
S2B SHT 8
CLKOUT BF SHT 5,8

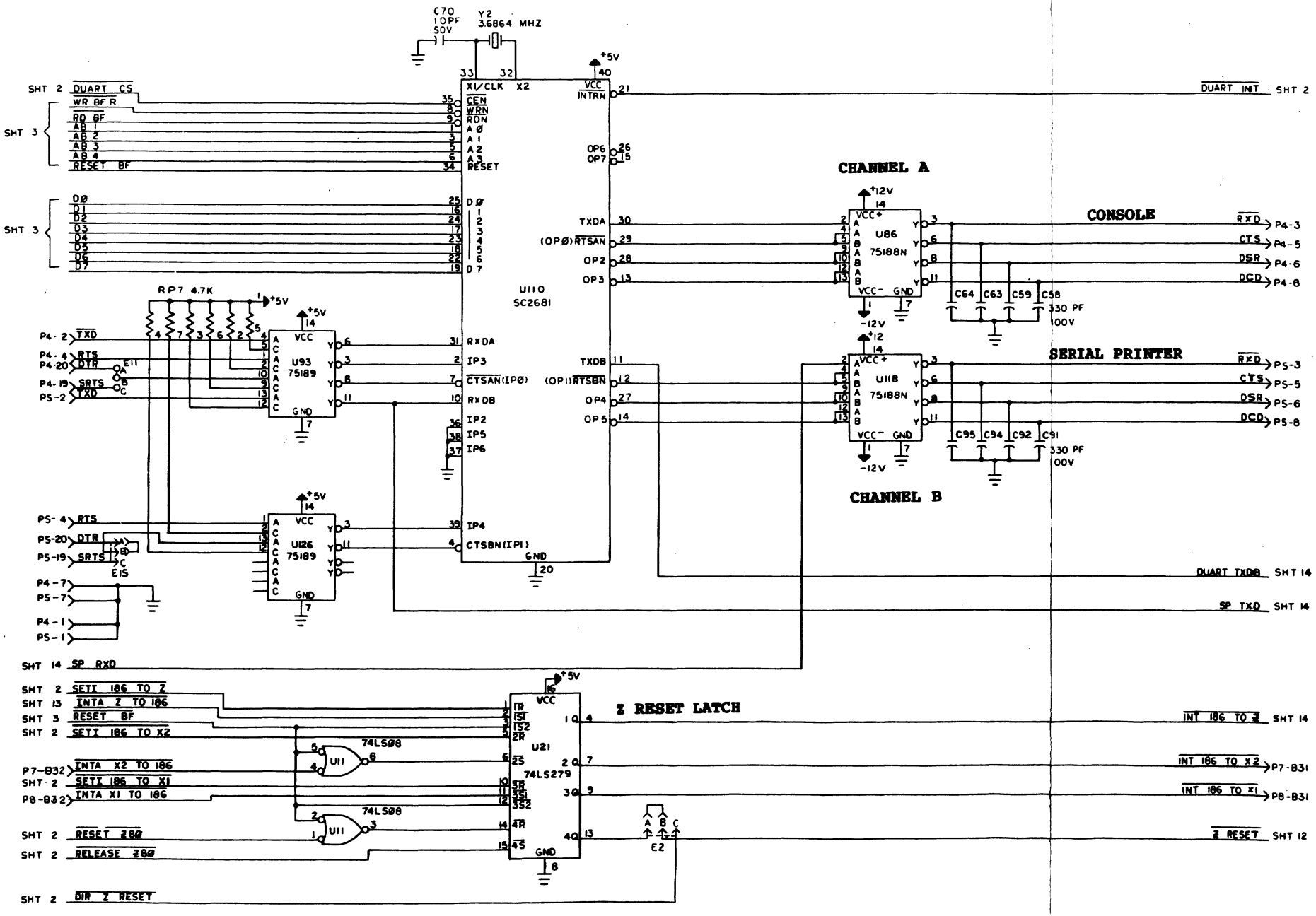

WRITE ENABLE DECODER
SHT 3 WR BF
SHT 3 CLK ØUT BF
+5V
RP1
1K
U31
74LS74
SHT 2 ADØ
SHT 3 ALEB
SHT 13 ZRQ
U30
SHT 2 BHE
SHT 13 ZRBH
SHT 13 PSEL
SHT 5 PSEN
SHT 5 R18
SHT 5 R19
E4
E3
U22
74LS32
NO WR
U37
74LSØ8
U9
74LSØØ
U38
74LSØ2
U49
74LS158
1A
1B
2A
2B
3A
3B
4A
4B
1Y
2Y
3Y
4Y
SG
GND
R14
R16
R17
R15
33
LOW WR 1
LOW WR 2
HIGH WR 1
HIGH WR 2
SHT 6
P10-C18
SHT 7
P10-C17
SHT 3 RESET BF
SHT 5 RAM WR
SHT 2 RELEASE FDC
SHT 2 RESET FDC
SHT 2 RELEASE HDC
SHT 2 RESET HDC
U10
74LS279
FDC RESET
HDC RESET
SHT11
SHT11

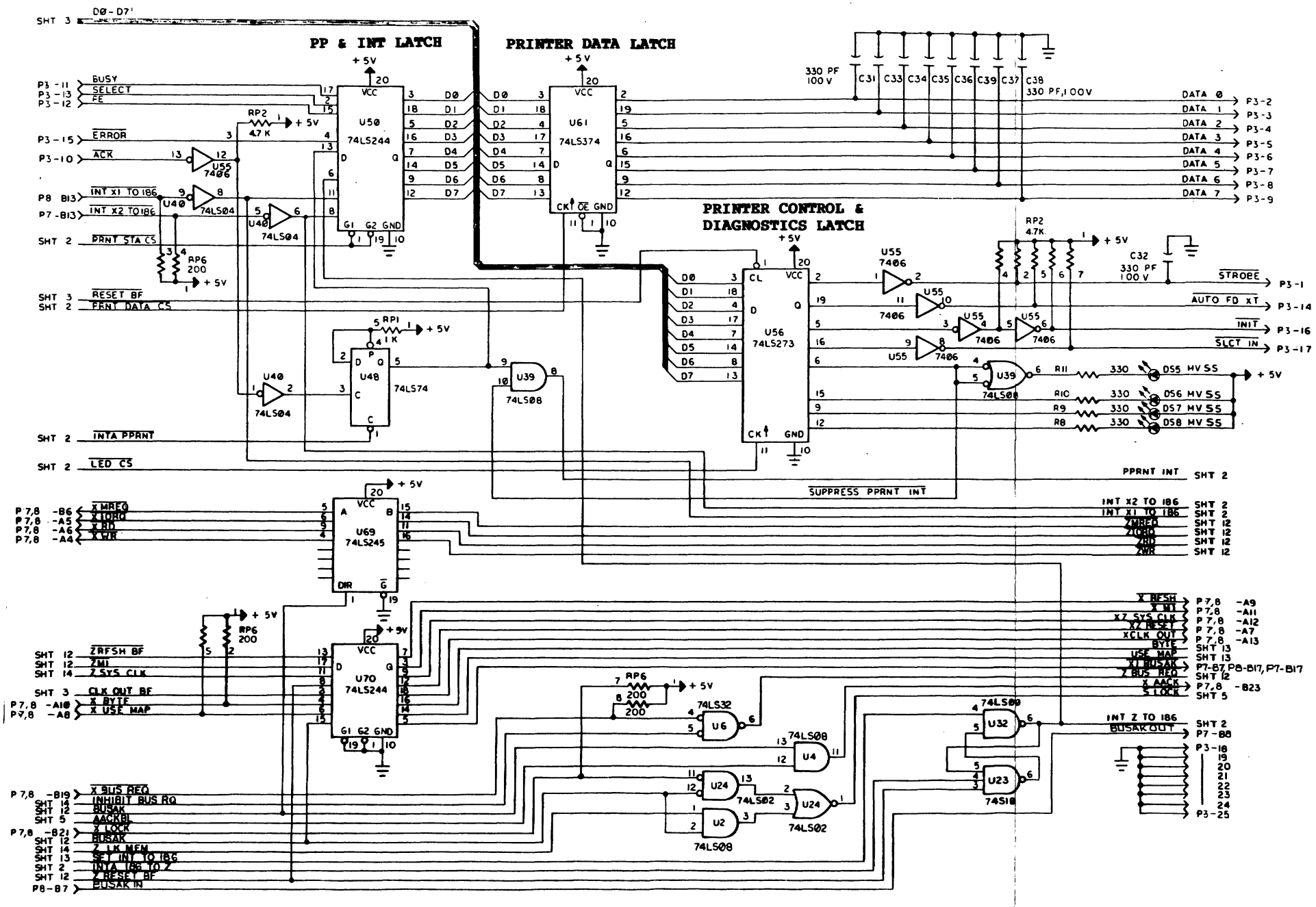

MEMORY CONTROLLER
U96
8207/8207-2
PARALLEL DATA REGISTER
MUX
U81
74LS373
U80
74LS373
U95
74LS373
U89
74LS244
U88
74LS244
U98
74LS244
U120
74LS04
U8
74LS04
U9
74LS00
U145
74LS165
U144
74LS165
U132
74LS76
U20
74LS04
RP9
4.7K
RP16
RP15
RP11
1K
E14
E13
E12
E19
E18
E20
E16
E17
R21
R22
R20
+5V
CLKOUT
RESET
ALEB
AD1-15
SØ
A 16-19
IBG LOCK
UCS BF
RESET BF
SA 16
SA 17
SA 18
SLOCK
SA19
BPE
RD BF
WR BF
CLKOUT BF
RAMA Ø-8
RAMA Ø
RAMA 1
RAMA 2
RAMA 3
RAMA 4
RAMA 5
RAMA 6
RAMA 7
RAMA 8
PIO-A30
A32
A31
C29
C30
C31
A29
PIO-C32
PIO-A18
RAS Ø
CAS Ø
RAS 1
CAS 1
RAS 2
CAS 2
RAS 3
CAS 3
PIO-A6
PIO-C7
PIO-A7
PIO-C6
RAM WR
PSEL
PSEN
AACKA
AACKB
AACKBL
PUPI
LOCK
PCTLB
MUX/PCLK
PDI
SHT 2
SHT 3
SHT 4
SHT 6,7
SHT 13
SHT 4,13
SHT 2,8
SHT 10,12
SHT 12

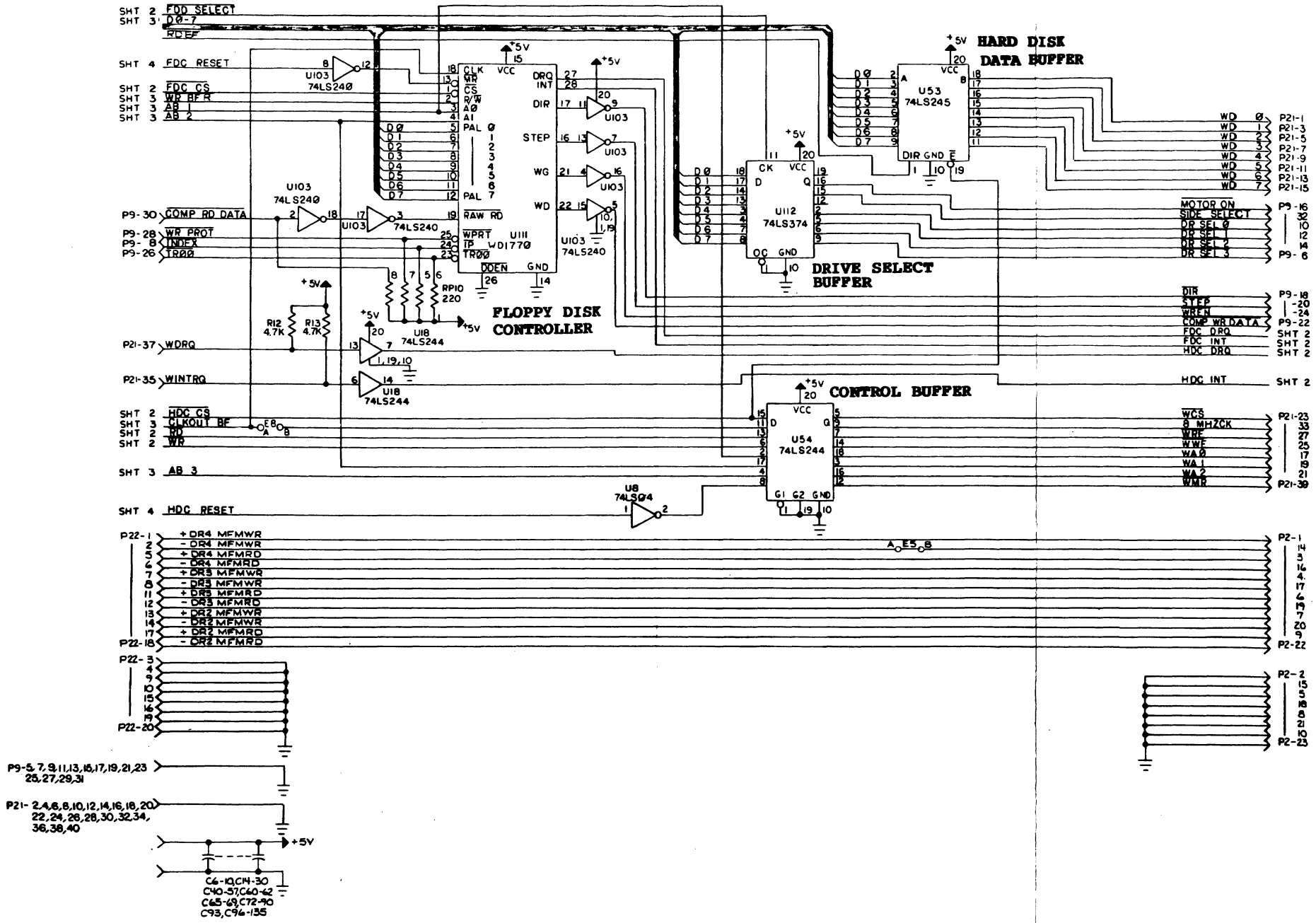

SHT 5 RAS Ø
SHT 5 CAS 1
SHT 5 RAM A Ø-8
SHT 5 CAS Ø
SHT 5 RAS 1
SHT 4 LOW WR 1
SHT 8
SHT 8
RAMDI Ø
RAMDI 1
RAMDI 2
RAMDI 3
RAMDI 4
RAMDI 5
RAMDI 6
RAMDI 7
RAMDO Ø
RAMDO 1
RAMDO 2
RAMDO 3
RAMDO 4
RAMDO 5
RAMDO 6
RAMDO 7
RAS
CAS
WE
RAM A Ø
A1
A9
U122
U114
U106
U99
U167
U158
U146
U133
U123
U115
U107
U100
U168
U159
U147
U134
8264
82256
LOW BYTE/BANK Ø
LOW BYTE/BANK 1

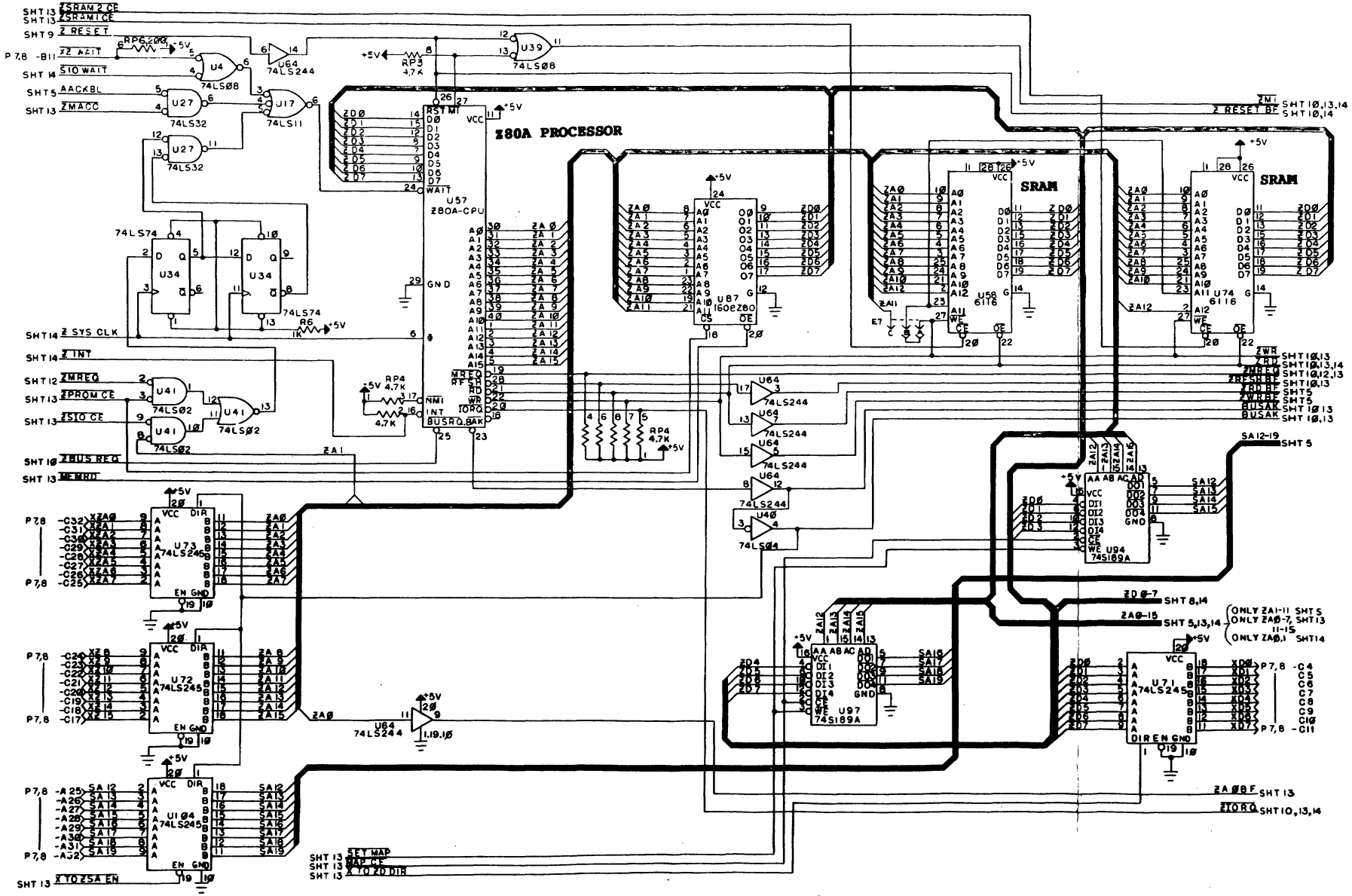

SHT 5 RAS Ø
P10-A16 CAS I
SHT 5 RAM A Ø-8
SHT 5 CAS Ø
SHT 5 CAS I
SHT 5 RAS I
P10-A17 RAS I
SHT 4 HIGH WR I
+5V
VCC GND
U124
U116
U108
U101
U169
U160
U148
U135
U125
U117
U109
U102
U170
U161
U149
U136
MB8264E 82256
CAS I
CAS Ø
HIGH BYTE/BANK Ø
HIGH BYTE/BANK I
SHT 8
RAMDI 8
RAMDI 9
RAMDI 10
RAMDI 11
RAMDI 12
RAMDI 13
RAMDI 14
RAMDI 15
RAMDO 8
RAMDO 9
RAMDO 10
RAMDO 11
RAMDO 12
RAMDO 13
RAMDO 14
RAMDO 15
SHT 8

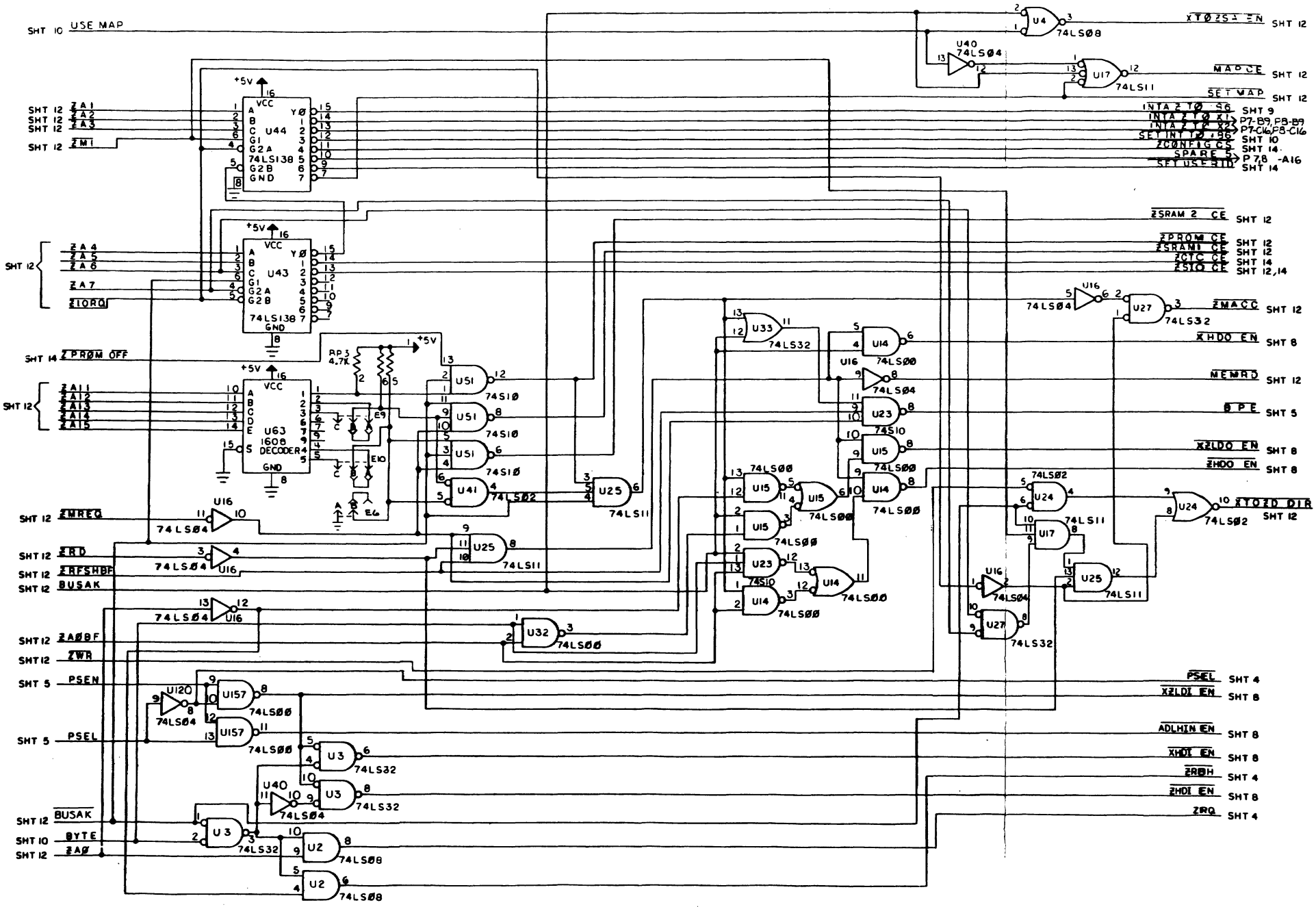

SHT 2 AD 0-15
SHT 6,7 RAMDO 0-15
RAMDI 0-15 SHT 6,7
U82 74LS244
U83 74LS244
U68 74LS244
U67 74LS244
U77 74LS244
U78 74LS244
U84 74LS244
U85 74LS373
U79 74LS373
U76 74LS373
RP13 33
RP14 33
74LS32
74LS76
U132
+5V
SHT 13 ADLHIN EN
SHT 3 UCS BF
SHT 2 DEN
SHT 3 S1B
SHT 3 S2B
SHT 12
SHT 13 XZLDI EN
SHT 13 ZHDI EN
SHT 13 ZHDO EN
SHT 13 XZLDO EN
P7,8 -A17
SHT 13 XHDI EN
SHT 13 XHDO EN
SHT 5 PUP I
SHT 5 AACK B
SHT 3 CLK OUT BF
SHT 3 RESET BF
PIO-C5
PIO-A1
PIO-C28
PIO-A25
PIO-C9
PIO-A13
PIO-C19
PIO-A23
PIO-A11
PIO-C11
PIO-A21
PIO-C21
PIO-A4
PIO-C4
PIO-A14
PIO-C14
PIO-A24
PIO-C24
PIO-A15
PIO-C15

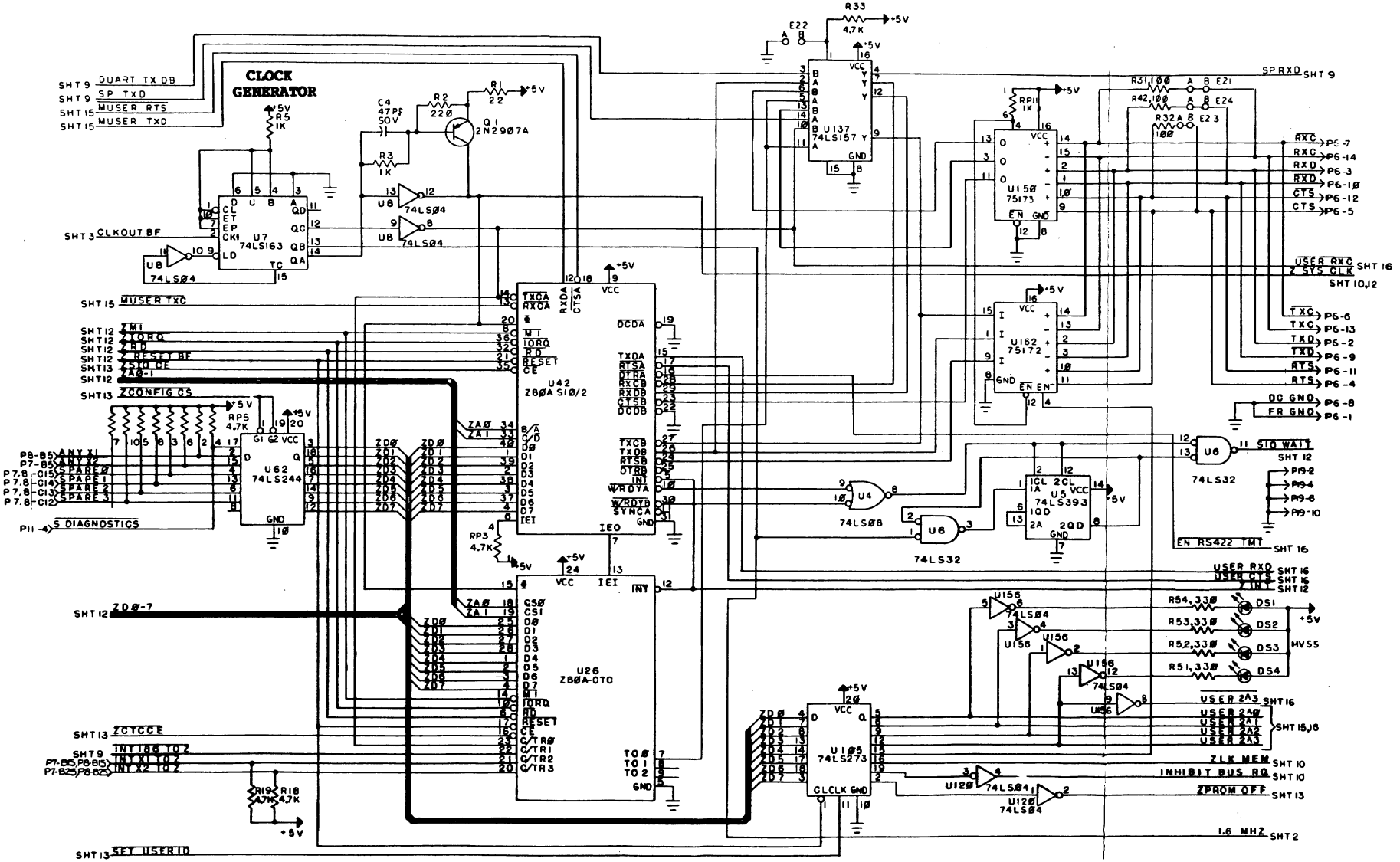

C70 10PF 50V
Y2 3.6864 MHZ
U110 SC2681
CHANNEL A
CONSOLE
U86 75188N
CHANNEL B
SERIAL PRINTER
U118 75188N
U93 75189
U126 75189
RP7 4.7K
C64 C63 C59 C58 330 PF 100V
C95 C94 C92 C91 330 PF 100V
DUART INT SHT 2
DUART TXDB SHT 14
SP TXD SHT 14
SP RXD SHT 14
Z RESET LATCH
U21 74LS279
74LS08
INT 186 TO Z SHT 14
INT 186 TO X2 P7-B31
INT 186 TO X1 P8-B31
Z RESET SHT 12
DIR Z RESET

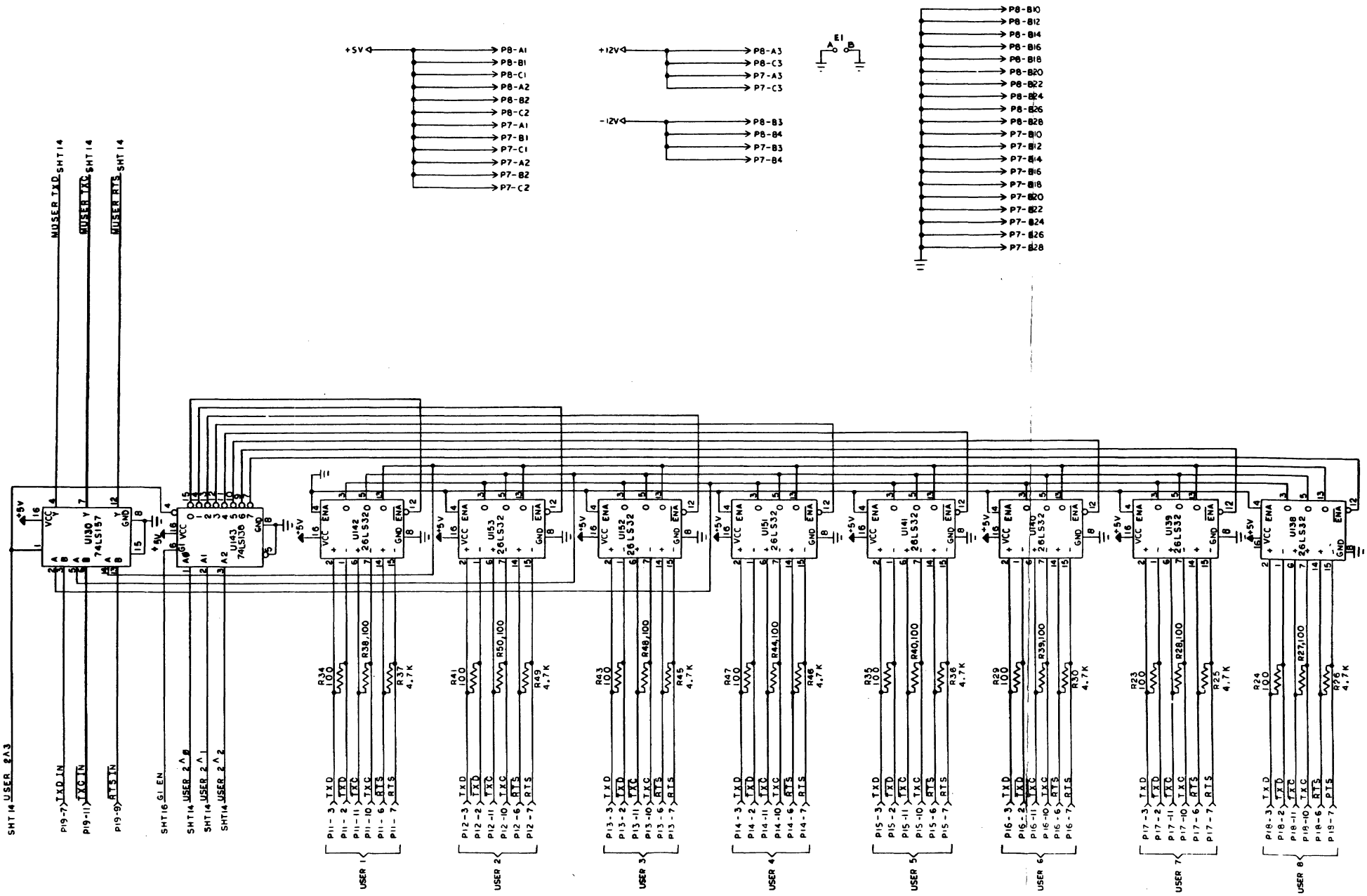

PP & INT LATCH
PRINTER DATA LATCH
PRINTER CONTROL & DIAGNOSTICS LATCH
U50 74LS244
U61 74LS374
U56 74LS273
U69 74LS245
U70 74LS244
U48 74LS74
U55 7406
U39 74LS08
U40 74LS04
U24 74LS02
U6 74LS32
U4 74LS08
U2 74LS08
U32 74LS00
U23 74S10
RP2 4.7K
RP1 1K
RP6 200
C31 C33 C34 C35 C36 C39 C37 C38 330 PF, 100V
C32 330 PF 100 V
DS5 MV SS
DS6 MV SS
DS7 MV SS
DS8 MV SS
R11 330
R10 330
R9 330
R8 330
+5V
BUSY
SELECT
FE
ERROR
ACK
INT X1 TO 186
INT X2 TO 186
PRNT STA CS
RESET BF
PRNT DATA CS
INTA PPRNT
LED CS
SUPPRESS PPRNT INT
PPRNT INT
STROBE
AUTO FD XT
INIT
SLCT IN
DATA 0
DATA 1
DATA 2
DATA 3
DATA 4
DATA 5
DATA 6
DATA 7
X MREQ
X IORQ
X RD
X WR
ZRFSH BF
ZMI
Z SYS CLK
CLK OUT BF
X BYTE
X USE MAP
X BUS REQ
INHIBIT BUS RQ
BUSAK
AACKBI
Z LOCK
BUSAK
Z LK MEM
SET INT TO 186
INTA 186 TO Z
Z RESET BF
BUSAK IN
INT Z TO 186
BUSAK OUT

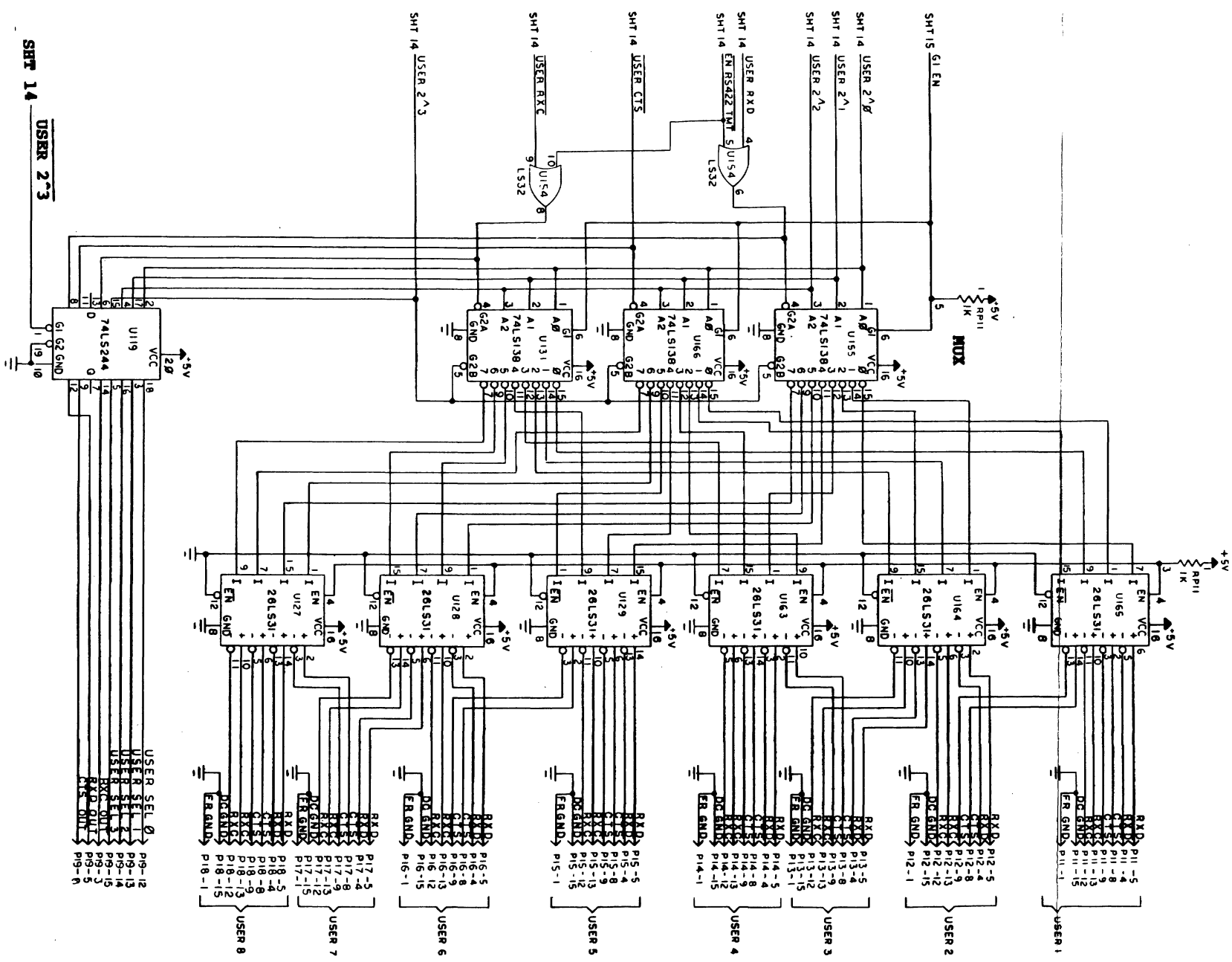

FLOPPY DISK CONTROLLER
HARD DISK DATA BUFFER
DRIVE SELECT BUFFER
CONTROL BUFFER
U111 WD1770
U112 74LS374
U53 74LS245
U54 74LS244
U103 74LS240
U18 74LS244
U8 74LS04
RP10 220
R12 4.7K
R13 4.7K
FDD SELECT
DD-7
RDEF
FDC RESET
FDC CS
WR BFR
AB 1
AB 2
COMP RD DATA
WR PROT
INDEX
TR00
WDRQ
WINTRQ
HDC CS
CLKOUT BF
RD
WR
AB 3
HDC RESET
+DR4 MFMWR
-DR4 MFMWR
+DR4 MFMRD
-DR4 MFMRD
+DR3 MFMWR
-DR3 MFMWR
+DR3 MFMRD
-DR3 MFMRD
+DR2 MFMWR
-DR2 MFMWR
+DR2 MFMRD
-DR2 MFMRD
MOTOR ON
SIDE SELECT
DR SEL 0
DR SEL 1
DR SEL 2
DR SEL 3
DIR
STEP
WREN
COMP WR DATA
FDC DRQ
FDC INT
HDC DRQ
HDC INT
WCS
8 MHZCK
WRE
WWE
WA0
WA1
WA2
WMR
P9-5,7,9,11,13,15,17,19,21,23 25,27,29,31
P21-2,4,6,8,10,12,14,16,18,20 22,24,26,28,30,32,34, 36,38,40
+5V
C6-10,C14-30
C40-57,C60-62
C65-69,C72-90
C93,C94-135

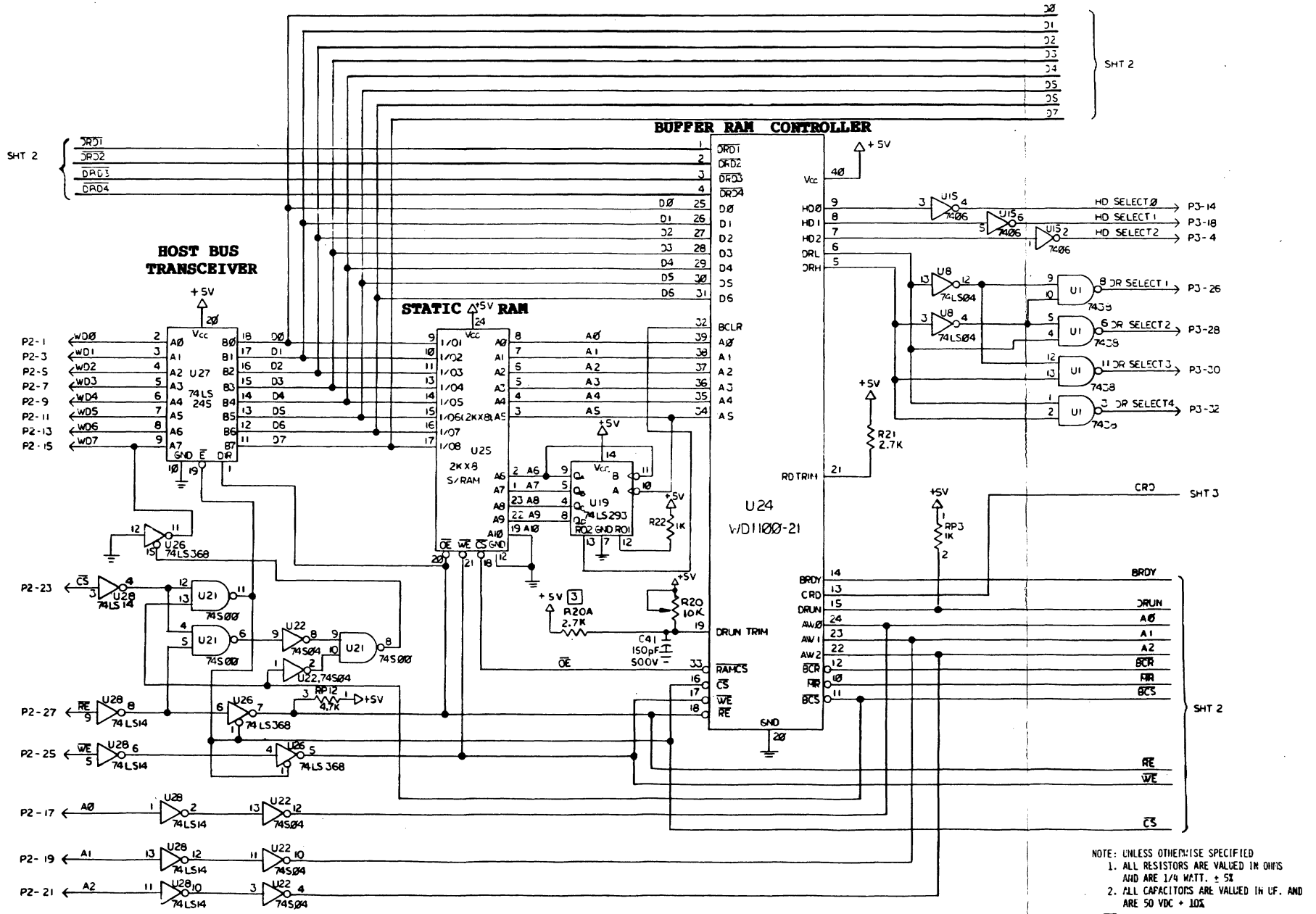

Z80A PROCESSOR
SRAM
SRAM
74LS74
74LS74
74LS32
74LS32
74LS11
74LS08
74LS08
74LS244
74LS02
74LS02
74LS02
74LS245
74LS245
74LS245
74LS244
74LS244
74LS244
74LS244
74LS04
74LS244
74LS245
74LS189A
74LS189A
6116
6116
RP6 200
RP3 4.7K
RP4 4.7K
RP4 4.7K
1K
4.7K
SHT 13 ZSRAM2 CE
SHT 13 ZSRAM1 CE
SHT 9 Z RESET
P 7,8 -B11 XZ WAIT
SHT 14 STO WAIT
SHT 5 AACKBL
SHT 13 ZMACC
SHT 14 Z SYS CLK
SHT 14 Z INT
SHT 12 ZMREQ
SHT 13 ZPROM CE
SHT 13 ZSIO CE
SHT 10 ZBUS REQ
SHT 13 MEMRD
ZA1
ZA0
P 7,8 -C32 XZA0
-C31 XZA1
-C30 XZA2
-C29 XZA3
-C28 XZA4
-C27 XZA5
-C26 XZA6
-C25 XZA7
P 7,8 -C24 XZA8
-C23 XZA9
-C22 XZA10
-C21 XZA11
-C20 XZA12
-C19 XZA13
-C18 XZA14
-C17 XZA15
P 7,8 -A25 SA12
-A26 SA13
-A27 SA14
-A28 SA15
-A29 SA17
-A30 SA18
-A31 SA19
-AJ2 SA16
SHT 13 XTOZSA EN
SHT 13 SET MAP
SHT 13 MAP CE
SHT 13 X TO ZD DIR
ZMI SHT 10,13,14
Z RESET BF SHT 10,14
ZWR SHT 10,13
ZRD SHT 10,13,14
ZMREQ SHT 10,12,13
ZREFRH BF SHT 10,13
ZRD BF SHT 5
ZWR BF SHT 5
BUSAK SHT 10 13
BUSAK SHT 10,13
SA12-19 SHT 5
ZD 0-7 SHT 8,14
ZA 0-15 SHT 5,13,14
ONLY ZA1-11 SHT 5
ONLY ZA0-7, SHT 13
11-15
ONLY ZA0,1 SHT 14
ZA 0 BF SHT 13
ZIORQ SHT 10,13,14
P 7,8 -C4
-C5
-C6
-C7
-C8
-C9
-C10
-C11

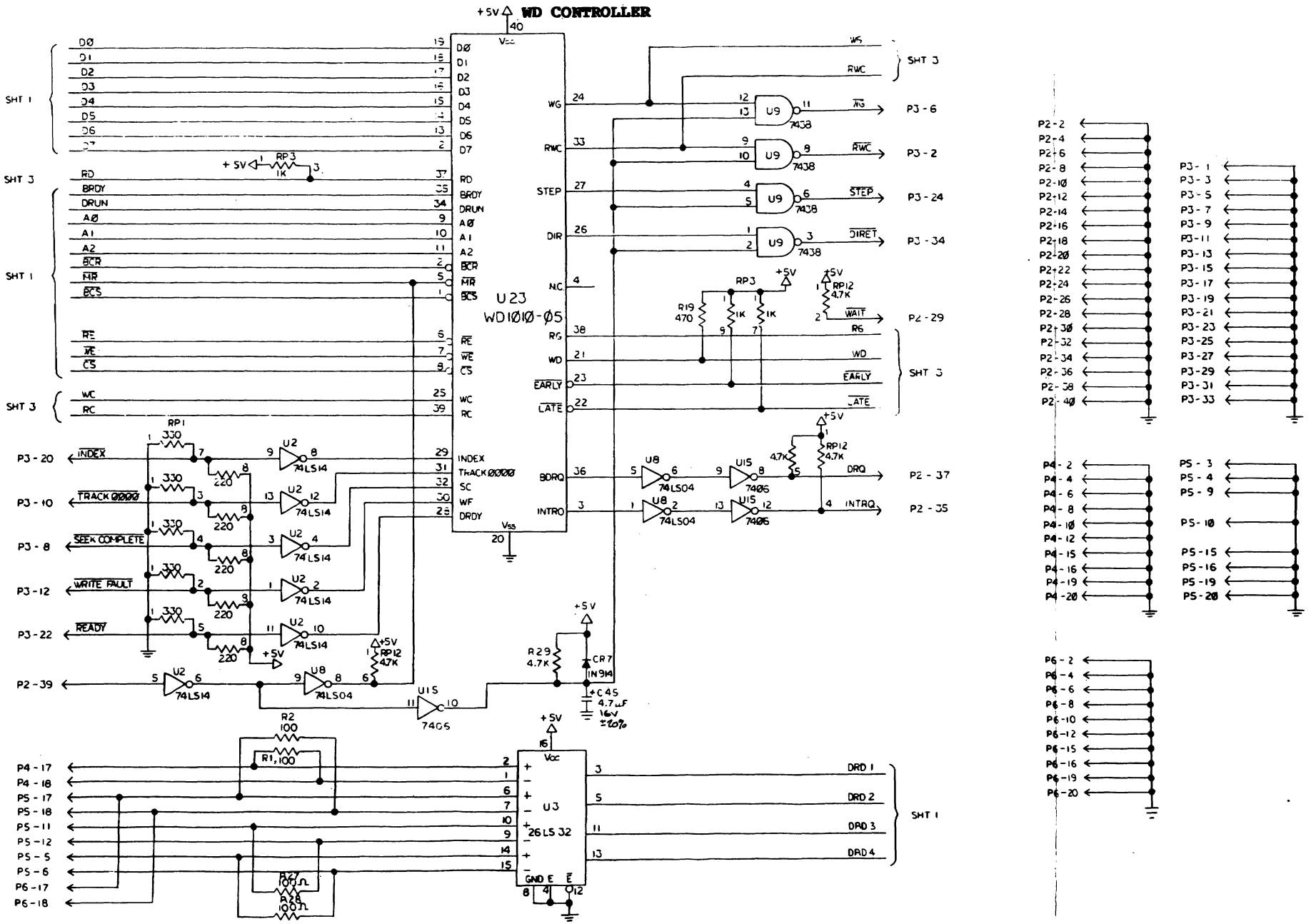

SHT 10 USE MAP
SHT 12 ZA1
SHT 12 ZA2
SHT 12 ZA3
SHT 12 ZM1
U44 74LS138
SHT 12 ZA4
ZA5
ZA6
ZA7
ZIORQ
U43 74LS138
SHT 14 ZPROM OFF
SHT 12 ZA11
ZA12
ZA13
ZA14
ZA15
U63 1608 DECODER
RP3 4.7K
E9
E10
E6
SHT 12 ZMREQ
ZRD
ZRFSHBF
BUSAK
ZA0BF
ZWR
SHT 5 PSEN
SHT 5 PSEL
SHT 12 BUSAK
SHT 10 BYTE
SHT 12 ZA0
U4 74LS08
U40 74LS04
U17 74LS11
XT0ZS1 EN SHT 12
MAPCE SHT 12
SETMAP SHT 12
INTA2T0 S6 SHT 9
INTA2T0 X1 P7-B9, P8-B9
INTA2T0 X2 P7-C16, P8-C16
SETINT2 S6 SHT 10
ZCONFIGCS SHT 14
SPARE 5 P7,8 -A16
SETUSERID SHT 14
ZSRAM2 CE SHT 12
ZPROM CE SHT 12
ZSRAM1 CE SHT 12
ZCYC CE SHT 14
ZSIO CE SHT 12,14
U27 74LS32
ZMACC SHT 12
XHDO EN SHT 8
MEMRD SHT 12
BPE SHT 5
XZLDO EN SHT 8
ZHDO EN SHT 8
U24 74LS02
XTOZD DIR SHT 12
PSEL SHT 4
XZLDI EN SHT 8
ADLHIN EN SHT 8
XHDI EN SHT 8
ZA0H SHT 4
ZHDI EN SHT 8
ZRQ SHT 4

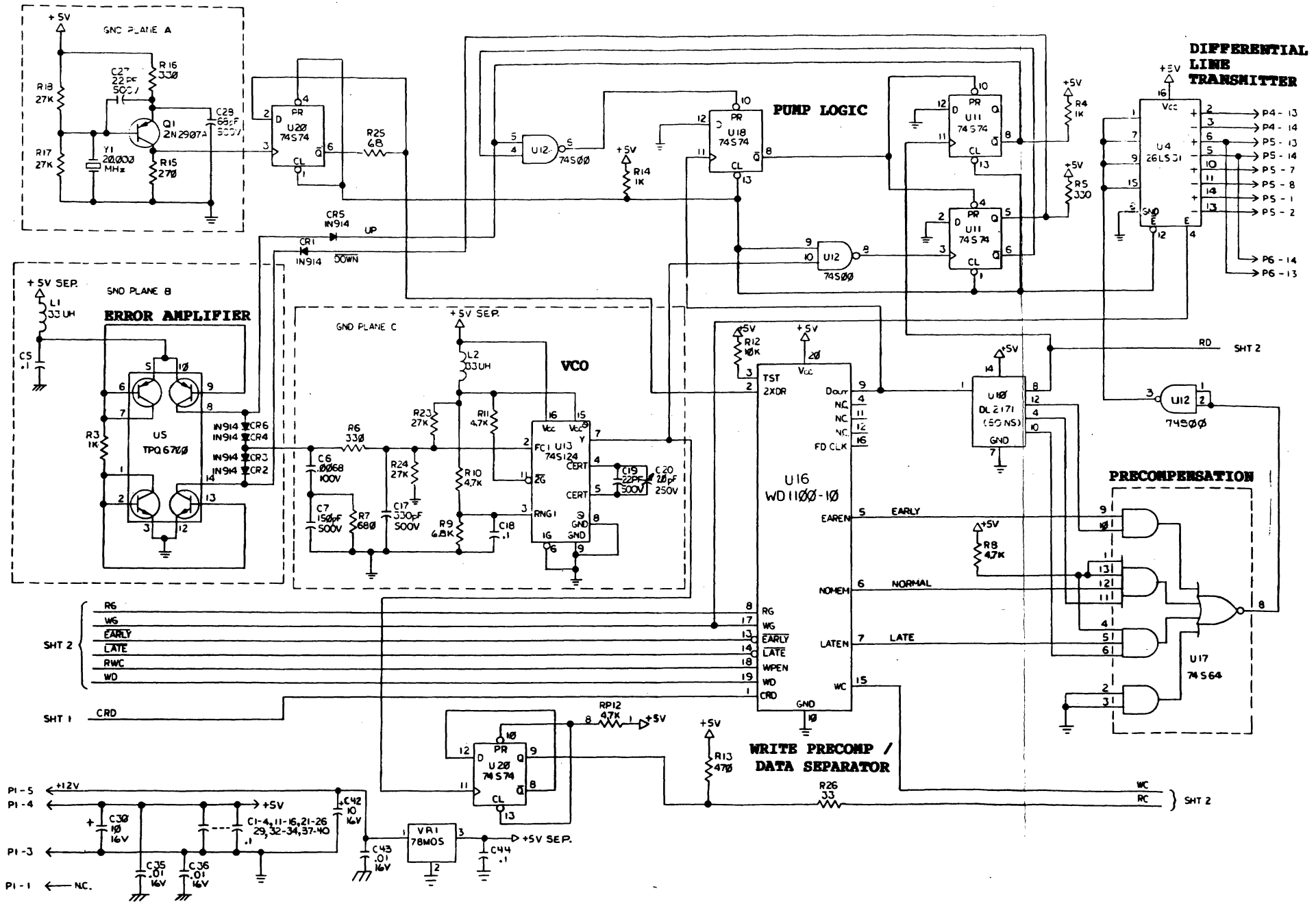

CLOCK GENERATOR
U42 Z80A SIO/2
U26 Z80A-CTC
U62 74LS244
U7 74LS163
U137 74LS157
U150 75173
U162 75172
U105 74LS273
U5 74LS393
74LS32
74LS08
74LS04
74LS244
74LS273
74LS163
74LS157
74LS393
SP RXD SHT 9
DUART TX DB
SP TXD
MUSER RTS
MUSER TXD
MUSER TXC
CLKOUT BF
ZCONFIG CS
S DIAGNOSTICS
ZD0-7
ZCTCCE
SET USERID
SIO WAIT
EN RS422 TMT
USER RXD
USER CTS
ZINT
USER 2A3
ZLK MEM
INHIBIT BUS RQ
ZPROM OFF
1.6 MHZ
DS1
DS2
DS3
DS4
RXC
RXD
CTS
TXC
TXD
RTS
DC GND
FR GND


+5V
P8-A1
P8-B1
P8-C1
P8-A2
P8-B2
P8-C2
P7-A1
P7-B1
P7-C1
P7-A2
P7-B2
P7-C2
+12V
P8-A3
P8-C3
P7-A3
P7-C3
-12V
P8-B3
P8-B4
P7-B3
P7-B4
E1
P8-B10
P8-B12
P8-B14
P8-B16
P8-B18
P8-B20
P8-B22
P8-B24
P8-B26
P8-B28
P7-B10
P7-B12
P7-B14
P7-B16
P7-B18
P7-B20
P7-B22
P7-B24
P7-B26
P7-B28
NUSER TXD SHT14
NUSER TXC SHT14
NUSER RTS SHT14
U130 74LS157
U143 74LS30
SHT14 USER 2^0
SHT14 USER 2^1
SHT14 USER 2^2
SHT16 GI EN
P19-7 TXD IN
P19-11 TXC IN
P19-9 RTS IN
U142 26LS32
U153 26LS32
U152 26LS32
U151 26LS32
U141 26LS32
U140 26LS32
U139 26LS32
U138 26LS32
R34 100
R38,100
R37 4.7K
R41 100
R50,100
R49 4.7K
R43 100
R48,100
R45 4.7K
R47 100
R44,100
R46 4.7K
R35 100
R40,100
R36 4.7K
R29 100
R39,100
R30 4.7K
R23 100
R28,100
R25 4.7K
R24 100
R27,100
R26 4.7K
USER 1
USER 2
USER 3
USER 4
USER 5
USER 6
USER 7
USER 8


SHT 14 USER 2^3
MUX
USER 1
USER 2
USER 3
USER 4
USER 5
USER 6
USER 7
USER 8
USER SEL Ø
USER SEL 1
USER SEL 2
USER SEL 3
RXD OUT
CTS OUT


BUFFER RAM CONTROLLER
HOST BUS TRANSCEIVER
STATIC RAM
U24
WD1100-21
U27 74LS 245
U25 2K X 8 S/RAM
U19 74LS293
SHT 2
SHT 3
HD SELECT0
HD SELECT1
HD SELECT2
DR SELECT1
DR SELECT2
DR SELECT3
DR SELECT4
R21 2.7K
R22 1K
R20 10K
R20A 2.7K
RP3 1K
RP12 4.7K
C41 150pF 500V
+5V
GND
DRUN TRIM
RDTRIM
BRDY
CRD
DRUN
RAMCS
NOTE: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE VALUED IN OHMS AND ARE 1/4 WATT. ± 5%
2. ALL CAPACITORS ARE VALUED IN UF. AND ARE 50 VDC + 10%
3 R20A IS USED WITHOUT R20. R20 IS USED ONLY WHEN R20A IS NOT USED BY ENGRG CHANGE ORDER.


WD CONTROLLER
U23
WD1010-05
DIFFERENTIAL LINE RECEIVER
SHT 1
SHT 3
P3 - 20
P3 - 10
P3 - 8
P3 - 12
P3 - 22
P2 - 39
P2 - 29
P2 - 37
P2 - 35
P3 - 6
P3 - 2
P3 - 24
P3 - 34
INDEX
TRACK 0000
SEEK COMPLETE
WRITE FAULT
READY
WAIT
DRQ
INTRQ
U3
26LS32
DRD 1
DRD 2
DRD 3
DRD 4


DIFFERENTIAL LINE TRANSMITTER
PUMP LOGIC
ERROR AMPLIFIER
VCO
PRECOMPENSATION
WRITE PRECOMP / DATA SEPARATOR
GND PLANE A
GND PLANE B
GND PLANE C
+5V SEP.
UP
DOWN
CR5 IN914
CR1 IN914
U20 74S74
U18 74S74
U11 74S74
U12 74S00
U4 26LS31
U16 WD1100-10
U13 74S124
U10 DL2171 (50 NS)
U17 74S64
VR1 78M05
Q1 2N2907A
Y1 20.000 MHz
L1 33 UH
L2 33UH
RD
SHT 2
SHT 1
CRD
RG
WG
EARLY
LATE
RWC
WD
WC
RC
EAREN
NOMEM
LATEN
WPEN
P4 - 13
P4 - 14
P5 - 13
P5 - 14
P5 - 7
P5 - 8
P5 - 1
P5 - 2
P6 - 14
P6 - 13
P1 - 5 +12V
P1 - 4
P1 - 3
P1 - 1 NC.

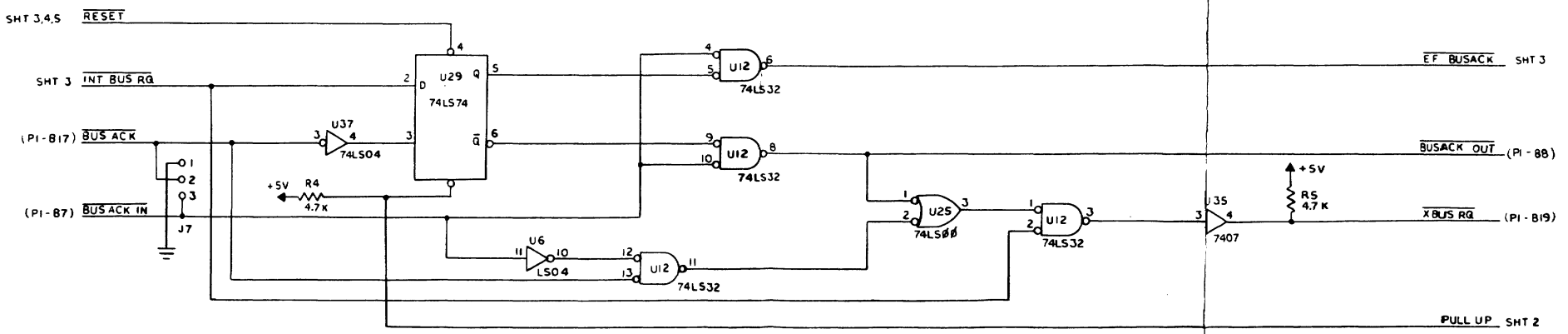
NOTES : UNLESS OTHERWISE SPECIFIED

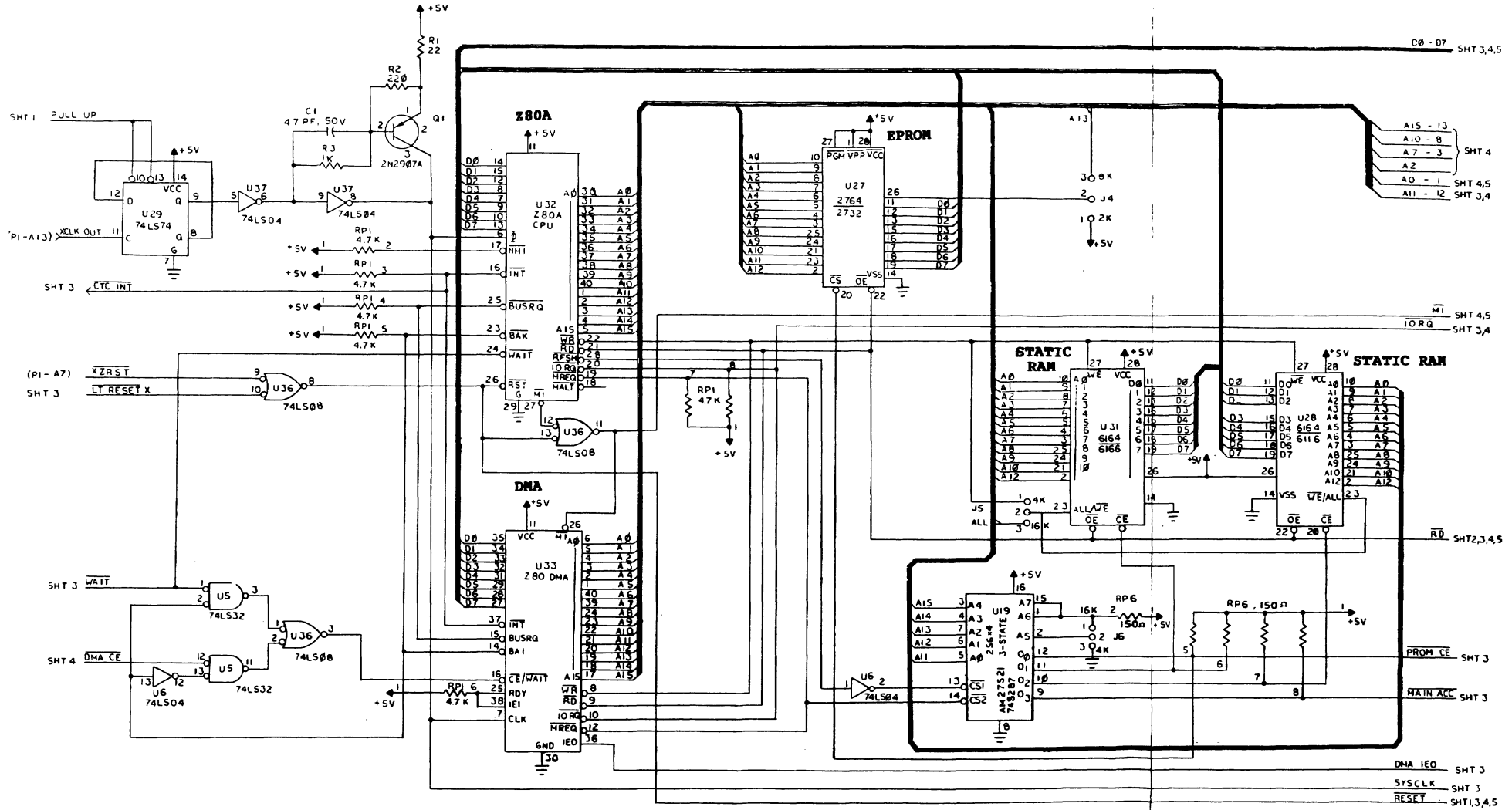
1. STANDARD MOUNTING OF JUMPERS (CARD INSTALLED ON X1 EXP SLOT, SRAM SIZE 4K EPROM SIZE 8K)
   - J1 (1,2) J7 (2,3)
   - J2 (1,2)
   - J3 (1,2)
   - J4 (2,3)
   - J5 (1,2)
   - J6 (2,3)

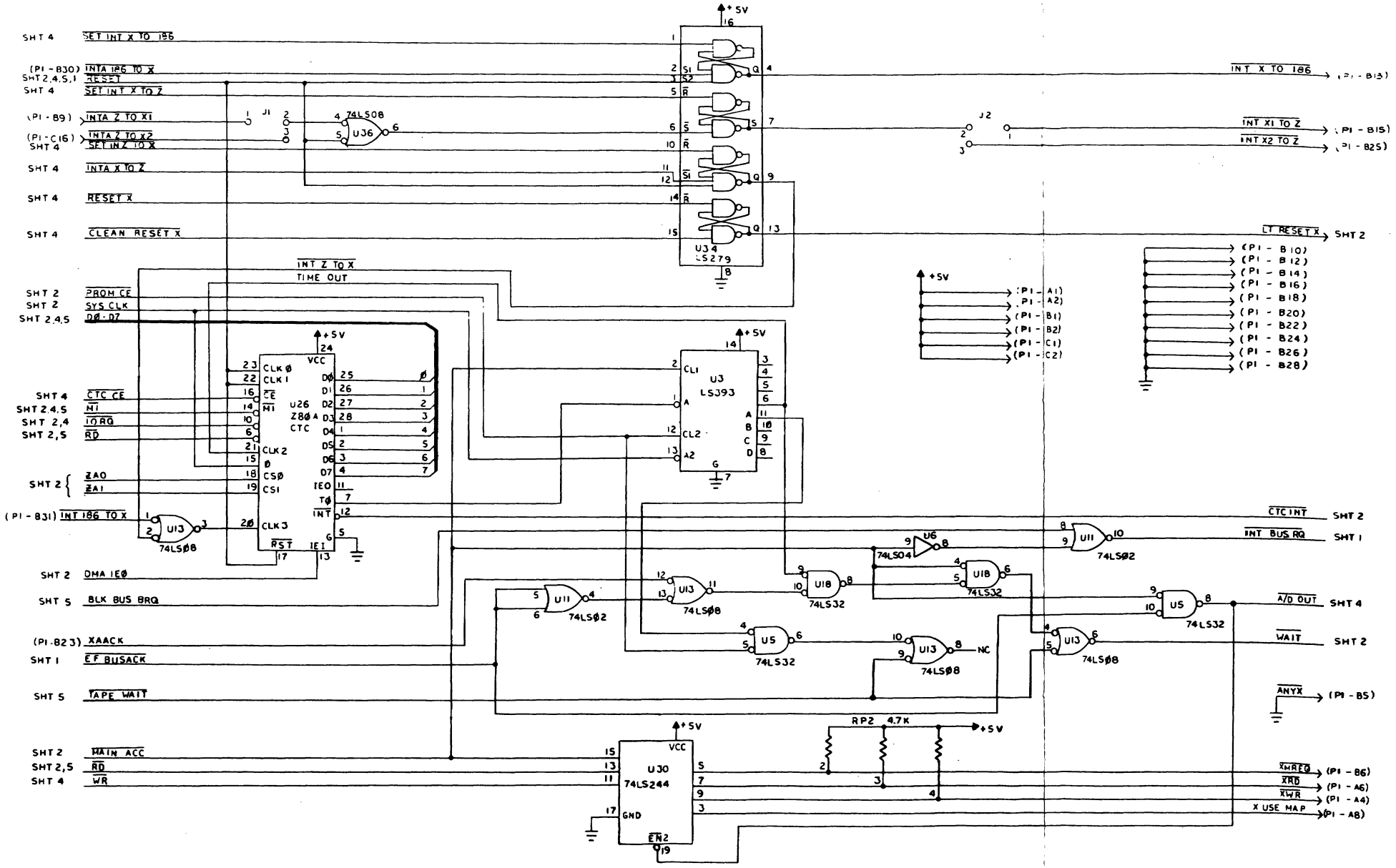
2. OPTIONAL MOUNTING OF JUMPERS
   - INSTALLED ON X2 EXP SLOT : J1(2,3) J2(2,3) J3(2,3)
   - EPROM SIZE 4K : J4 (1,2)
   - SRAM SIZE 16K : J5 (2,3) . J6 (1,2)
   - WHEN TAPE CARD IS INSTALLED ON X1 SLOT AND SOME CARD IS INSTALLED ON X2 SLOT OR WHEN THE TAPE CARD IS INSTALLED ON X2 SLOT: J7(1,2)

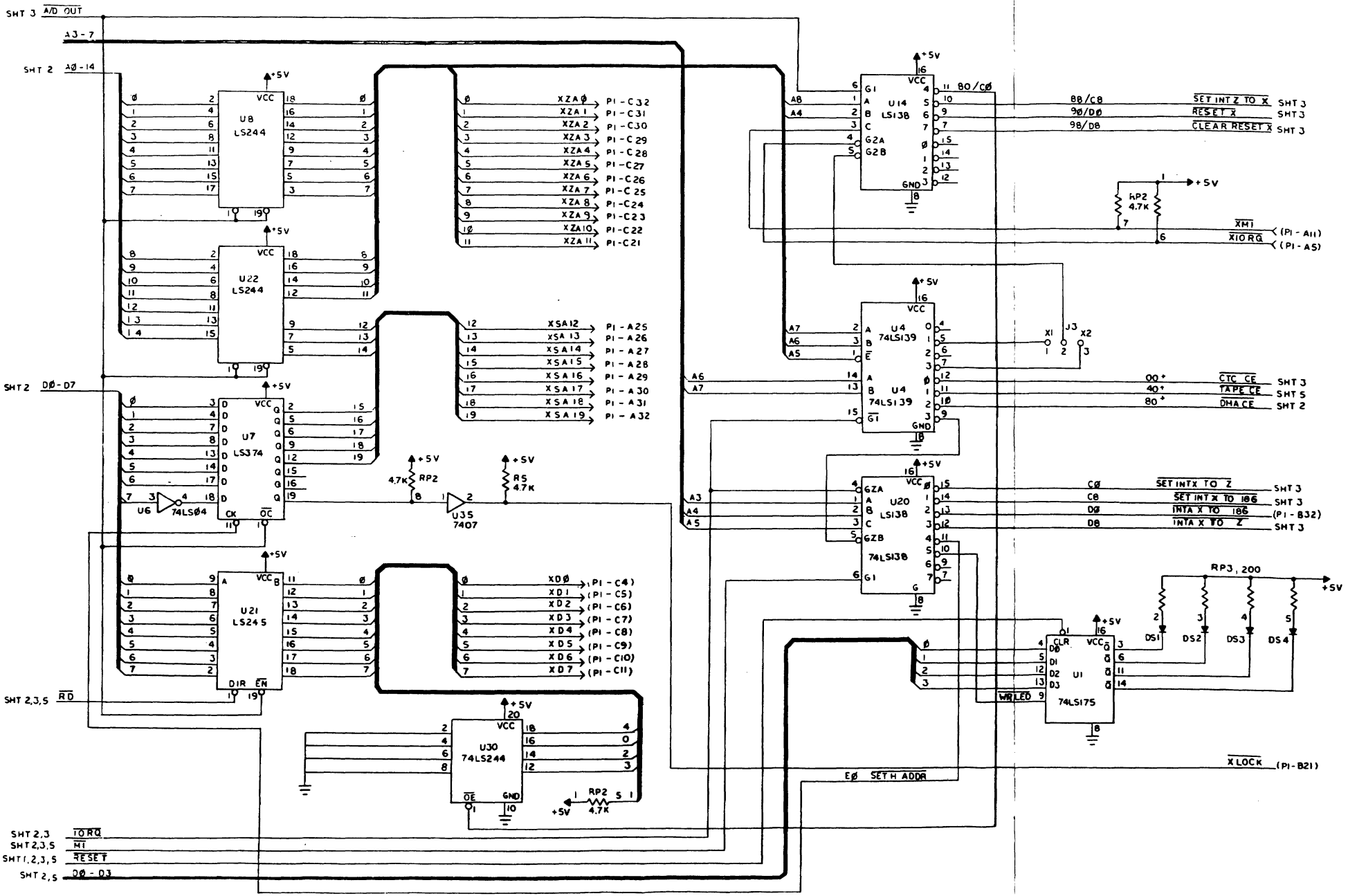
3. NAME OF CONNECTORS
   - P1 1608 MAIN BOARD INTERFACE
   - P2 QIC-02 INTERFACE

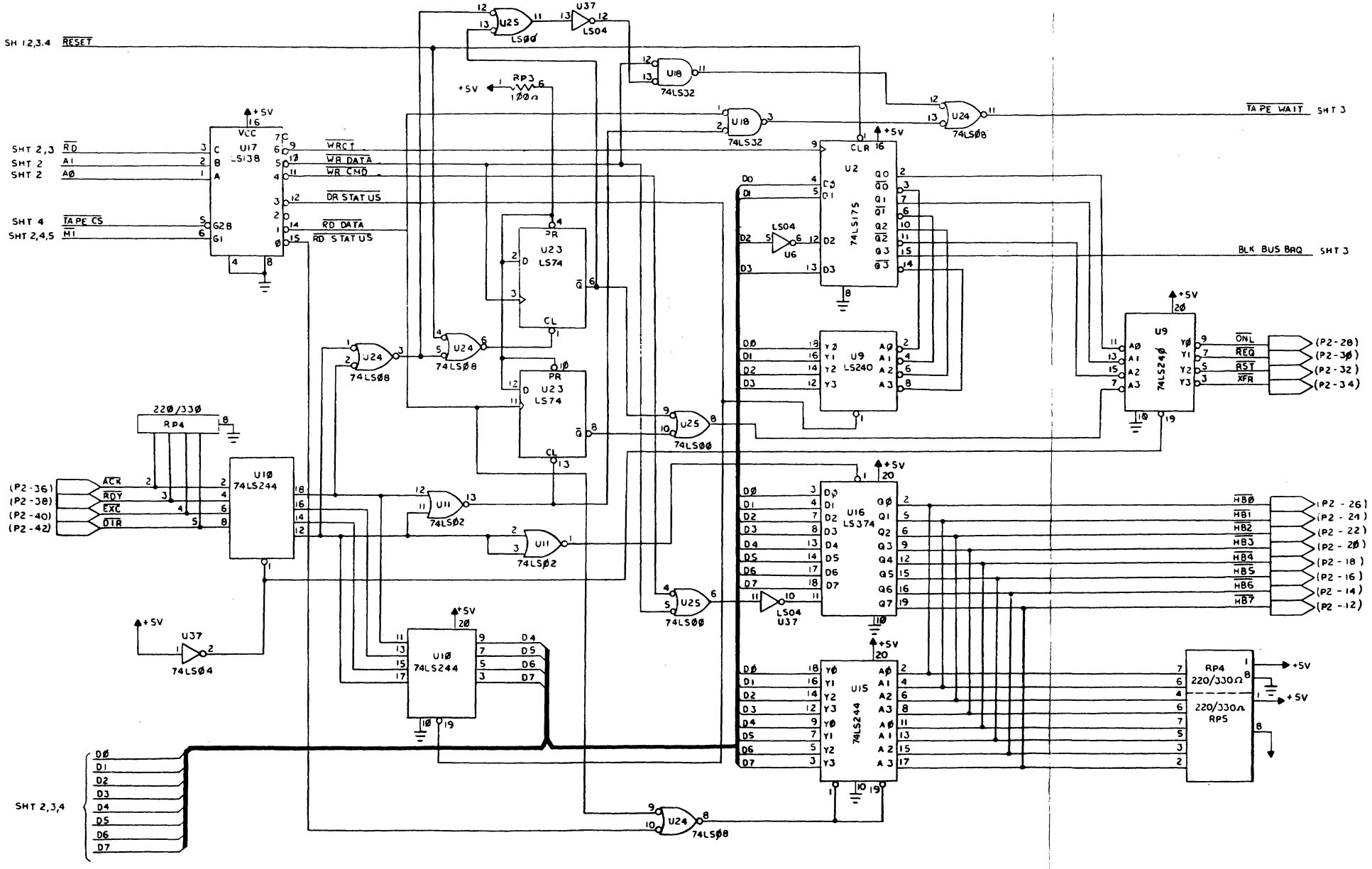
4. ALL RESISTOR ARE VALUED IN OHMS AND ARE 1/4 WATT± 5%




Z80A
U32 Z80A CPU
EPROM
U27 2764 2732
STATIC RAM
U31 6164 6166
STATIC RAM
U28 6164 6116
DMA
U33 Z80 DMA
U29 74LS74
U37 74LS04
U36 74LS08
U5 74LS32
U6 74LS04
U19 256x4 3-STATE
AM27S21 74S287
RP1 4.7K
RP6 150Ω
R1 22
R2 220
R3 1K
C1 47 PF, 50V
Q1 2N2907A
+5V
D0 - D7 SHT 3,4,5
A15 - 13
A10 - 8
A7 - 3
A2
A0 - 1 SHT 4,5
A11 - 12 SHT 3,4
SHT 4
M1 SHT 4,5
IORQ SHT 3,4
RD SHT2,3,4,5
PROM CE SHT 3
MAIN ACC SHT 3
DMA IEO SHT 3
SYSCLK SHT 3
RESET SHT1,3,4,5
SHT 1 PULL UP
(PI-A13) XCLK OUT
SHT 3 CTC INT
(PI-A7) XZRST
SHT 3 LT RESET X
SHT 3 WAIT
SHT 4 DMA CE
J4 8K 2K
J5 4K 16K
RP6 150Ω


SHT 4 SET INT X TO 186
(PI-B30) INTA 186 TO X
SHT 2,4,5,1 RESET
SHT 4 SET INT X TO Z
(PI-B9) INTA Z TO X1
(PI-C16) INTA Z TO X2
SHT 4 SET INZ TO X
SHT 4 INTA X TO Z
SHT 4 RESET X
SHT 4 CLEAN RESET X
U34 LS279
+5V
INT X TO 186 (PI-B13)
INT X1 TO Z (PI-B15)
INT X2 TO Z (PI-B25)
LT RESET X SHT 2
(PI-B10) (PI-B12) (PI-B14) (PI-B16) (PI-B18) (PI-B20) (PI-B22) (PI-B24) (PI-B26) (PI-B28)
(PI-A1) (PI-A2) (PI-B1) (PI-B2) (PI-C1) (PI-C2)
INT Z TO X TIME OUT
SHT 2 PROM CE
SHT 2 SYS CLK
SHT 2,4,5 D0-D7
U26 Z80A CTC
SHT 4 CTC CE
SHT 2,4,5 M1
SHT 2,4 IORQ
SHT 2,5 RD
SHT 2 ZA0 ZA1
(PI-B31) INT 186 TO X
U13 74LS08
U3 LS393
U11 74LS02
U6 74LS04
U18 74LS32
U5 74LS32
U13 74LS08
CTC INT SHT 2
INT BUS RQ SHT 1
A/D OUT SHT 4
WAIT SHT 2
ANYX (PI-B5)
SHT 2 DMA IEO
SHT 5 BLK BUS RQ
(PI-B23) XAACK
SHT 1 EF BUSACK
SHT 5 TAPE WAIT
RP2 4.7K
SHT 2 MAIN ACC
SHT 2,5 RD
SHT 4 WR
U30 74LS244
XMREQ (PI-B6)
XRD (PI-A6)
XWR (PI-A4)
X USE MAP (PI-A8)


SHT 3 A/D OUT
A3-7
SHT 2 A0-14
SHT 2 D0-D7
SHT 2,3,5 RD
SHT 2,3 IORQ
SHT 2,3,5 M1
SHT 1,2,3,5 RESET
SHT 2,5 D0-D3
U8 LS244
U22 LS244
U7 LS374
U21 LS245
U6 74LS04
U35 7407
U30 74LS244
U14 LS138
U4 74LS139
U20 LS138
U1 74LS175
RP2 4.7K
RP3, 200
RS 4.7K
+5V
XZA0 PI-C32
XZA1 PI-C31
XZA2 PI-C30
XZA3 PI-C29
XZA4 PI-C28
XZA5 PI-C27
XZA6 PI-C26
XZA7 PI-C25
XZA8 PI-C24
XZA9 PI-C23
XZA10 PI-C22
XZA11 PI-C21
XSA12 PI-A25
XSA13 PI-A26
XSA14 PI-A27
XSA15 PI-A28
XSA16 PI-A29
XSA17 PI-A30
XSA18 PI-A31
XSA19 PI-A32
XD0 (PI-C4)
XD1 (PI-C5)
XD2 (PI-C6)
XD3 (PI-C7)
XD4 (PI-C8)
XD5 (PI-C9)
XD6 (PI-C10)
XD7 (PI-C11)
B0/C0
B8/C8 SET INTZ TO X SHT 3
90/D0 RESET X SHT 3
98/D8 CLEAR RESET X SHT 3
XM1 (PI-A11)
XIORQ (PI-A5)
00* CTC CE SHT 3
40* TAPE CE SHT 5
80* DMA CE SHT 2
C0 SET INTX TO Z SHT 3
C8 SET INT X TO 186 SHT 3
D0 INTA X TO 186 (PI-B32)
D8 INTA X TO Z SHT 3
E0 SET H ADDR
XLOCK (PI-B21)
WRLED
DS1
DS2
DS3
DS4


SH 1,2,3,4 RESET
SHT 2,3 RD
SHT 2 A1
SHT 2 A0
SHT 4 TAPE CS
SHT 2,4,5 M1
U17 LS138
WRCT
WR DATA
WR CMD
DR STATUS
RD DATA
RD STATUS
U25 LS00
U37 LS04
U18 74LS32
U24 74LS08
RP3 100Ω
+5V
U23 LS74
U2 74LS175
U6 LS04
U9 LS240
U9 74LS240
TAPE WAIT SHT 3
BLK BUS RQ SHT 3
ONL
REQ
RST
XFR
(P2-28)
(P2-30)
(P2-32)
(P2-34)
220/330
RP4
U10 74LS244
(P2-36) ACK
(P2-38) RDY
(P2-40) EXC
(P2-42) DTR
U11 74LS02
U16 LS374
U15 74LS244
HB0
HB1
HB2
HB3
HB4
HB5
HB6
HB7
(P2-26)
(P2-24)
(P2-22)
(P2-20)
(P2-18)
(P2-16)
(P2-14)
(P2-12)
RP4 220/330Ω
RP5 220/330Ω
SHT 2,3,4
D0
D1
D2
D3
D4
D5
D6
D7

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