SeL 810A
School
4 weeks
1972

NGPL

INTER – OFFICE CORRESPONDENCE

DATE January 21, 1971

SUBJECT Computer Course & School

TO Mr. R. L. Jepsen
Mr. R. D. Pilcher
Mr. R. D. Kelly
Mr. G. R. Frimann
Mr. R. E. Praeuner
Mr. T. C. Losh
Mr. L. G. Gillis

FROM Mr. V. K. Patrick
Mr. M. J. Findling

You are scheduled for a four week SEL 810A Computer Maintenance School beginning April 26th, 1971 at Station No. 106, Beatrice, Nebraska. This School assumes that you already have a basic understanding of Computer operation, Computer programming, and logic circuits as covered in the Computer Course lessons which you have received and the attached 8 Lesson book on binary logic. You should complete Computer Course Lessons and the attached binary book prior to the School. With an understanding of these Lessons the Computer School will not be difficult; without this information the School will be extremely difficult. If you have any problems or require assistance understanding these Lessons or parts of these Lessons, please let me know. The Lessons contain a considerable amount of information, much of which is not the easiest to understand, so don't be afraid to ask for help.

The attached Binary Logic Book, Chapter 3, goes into Boolean Algebra in considerable detail. It is not necessary to be able to design circuits via Boolean Algebra but you should understand basic Boolean terminology and operations. The attached write-up on Boolean Algebra will assist you in understanding the subject and in completing the Binary Logic Book Lessons.

Copies of Computer Course Lessons 1 through 4 are also attached to Mr. G. R. Frimann and Mr. L. G. Gillis's copy of this Memo since they were not included in the original distribution of the Computer Course.

MJF/gr
cc: Mr. C. E. Upson

Attach:

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3		INTRODUCTION TO 810A INSTRUCTION SET	INTRODUCTION TO ASSEMBLY LANGUAGE	ANALYZING DIAGNOSTIC PROGRAMS	
4	INTRODUCTION TO TURBINE CONTROL SYSTEM				
5	GENERAL DESCRIPTION OF 810A	INSTRUCTION SET WORK SESSION	CONTROL PANEL LAB	RUNNING DIAGNOSTIC PROGRAMS LAB	REVIEW TEST CRITIQUE
6	BASIC BLOCK DIAGRAM				
7	MEMORY ORGANIZATION		LOADER LAB		
8					

COURSE NGP TURBINE CONTROL SYSTEM PREPARED BY R. H. Daugherty

WEEK 1 DATE 4/21/72

COURSE SCHEDULE

	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY
1					
2	PHYSICAL LAYOUT AND CARD LOCATION OF 810A	INTRODUCTION TO SYSTEMS LOGIC	810A CONTROL UNIT THEORY OF OPERATION	810A ARITHMETIC UNIT THEORY OF OPERATION	SUMMARY OF INSTRUCTION OPERATION
3	BUS BLOCK DIAGRAM	READING LOGIC DRAWINGS AND MAINTENANCE FLOWCHARTS			
4					
5	TROUBLESHOOTING TECHNIQUES FOR THE 810A	TROUBLESHOOTING LAB	TROUBLESHOOTING LAB	TROUBLESHOOTING LAB	REVIEW TEST CRITIQUE
6					
7					
8					

COURSE NGP TURBINE CONTROL SYSTEM PREPARED BY R. H. Daugherty

WEEK 2 DATE 4/21/72

COURSE SCHEDULE

	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY
1					
2	MEMORY THEORY OF OPERATION PART 1	MEMORY THEORY OF OPERATION PART 2	MULTIPLY THEORY OF OPERATION	DIVIDE THEORY OF OPERATION	PRIORITY INTERRUPT THEORY OF OPERATION
3					
4					
5	TROUBLESHOOTING LAB	TROUBLESHOOTING LAB			REVIEW TEST CRITIQUE
6					
7					
8					

COURSE NGP TURBINE CONTROL SYSTEM PREPARED BY R. H. Daugherty

WEEK 3 DATE 4/21/72

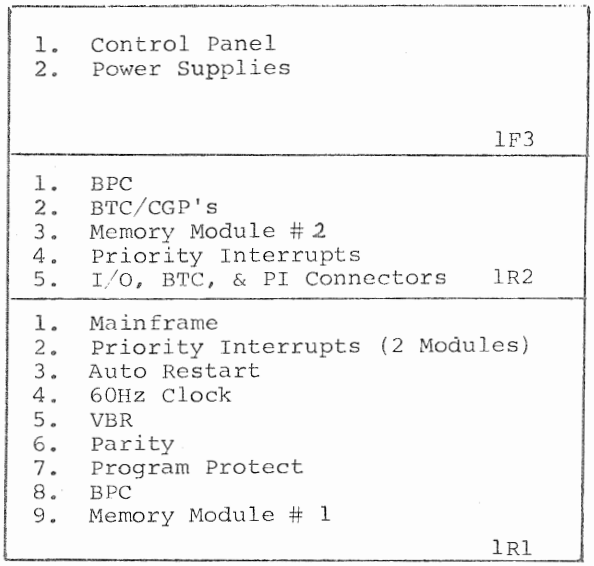
COURSE SCHEDULE

	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY
1					
2	810A I/O UNIT THEORY OF OPERATION	ASR-33 THEORY OF OPERATION	DIGITAL INPUT/OUTPUT UNIT THEORY OF OPERATION	MULTIPLEXER THEORY OF OPERATION	POWER SUPPLIES
3				DATA COMMUNICATIONS THEORY OF OPERATION	POWER FAILSAFE AUTO START THEORY OF OPERATION
4		PAPER TAPE READER THEORY OF OPERATION			
5	TROUBLESHOOTING LAB	TROUBLESHOOTING LAB	TROUBLESHOOTING LAB	TROUBLESHOOTING LAB	REVIEW TEST CRITIQUE
6					
7					
8					

COURSE NGP TURBINE CONTROL SYSTEM PREPARED BY R. H. Daugherty

WEEK 4 DATE 4/21/72

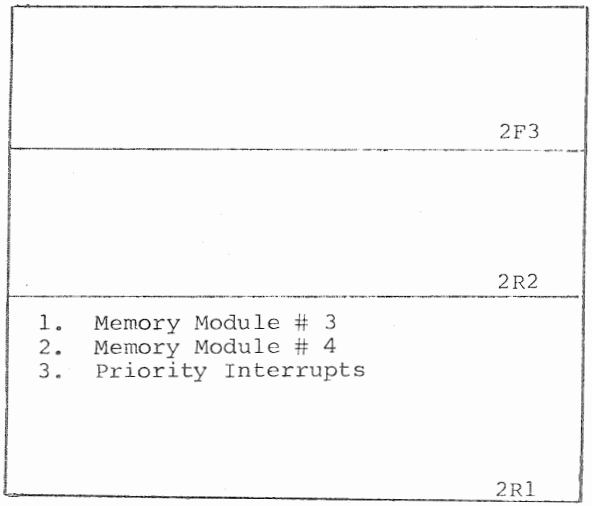
FRONT



1st Cabinet

REAR

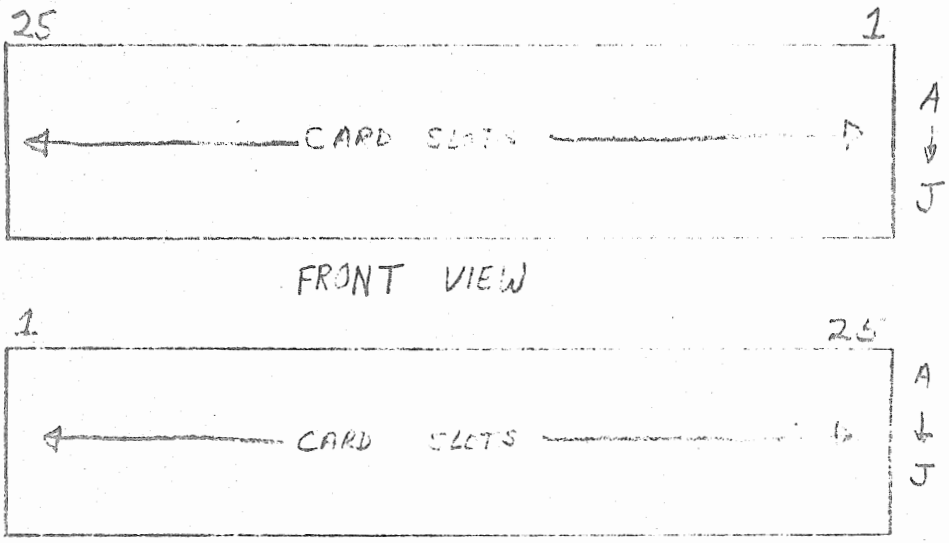
FRONT

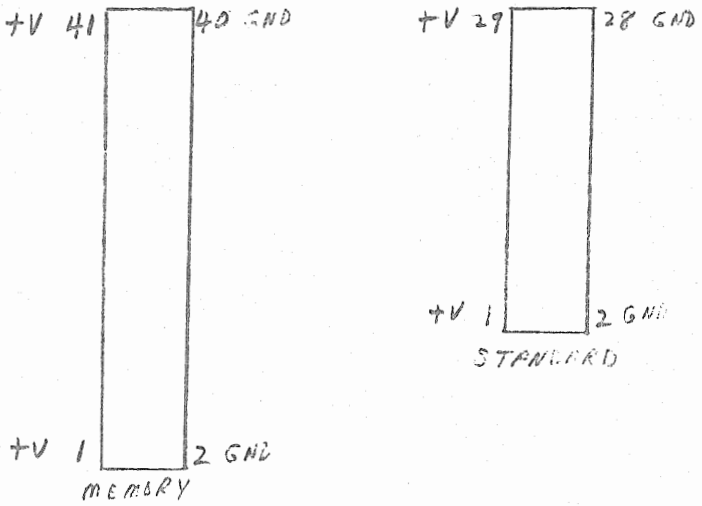


2nd Cabinet

REAR

810A PHYSICAL LAYOUT





810A CARD LOCATION + PIN NUMBERING

810 MEMORY MAP

LOWER CORE	00000 00777	01000 01777	02000 02777	03000 03777	04000 04777	05000 05777	06000 06777	07000 07777	4K
	10000 10777	11000 11777	12000 12777	13000 13777	14000 14777	15000 15777	16000 16777	17000 17777	8K
	20000 20777	21000 21777	22000 22777	23000 23777	24000 24777	25000 25777	26000 26777	27000 27777	12K
	30000 30777	31000 31777	32000 32777	33000 33777	34000 34777	35000 35777	36000 36777	37000 37777	16K
UPPER CORE	40000 40777	41000 41777	42000 42777	43000 43777	44000 44777	45000 45777	46000 46777	47000 47777	20K
	50000 50777	51000 51777	52000 52777	53000 53777	54000 54777	55000 55777	56000 56777	57000 57777	24K
	60000 60777	61000 61777	62000 62777	63000 63777	64000 64777	65000 65777	66000 66777	67000 67777	28K
	70000 70777	71000 71777	72000 72777	73000 73777	74000 74777	75000 75777	76000 76777	77000 77777	32K

810A/B SOFTWARE COURSE

INSTRUCTION SET - NUMERIC SEQUENCE GUIDE

00	(Augmented)	10	DIV
01	LAA	11	BRU
02	LBA	12	SPB
03	STA	13	(Augmented)
04	STB	14	IMS
05	AMA	15	CMA
06	SMA	16	AMB
07	MPY	17	(Augmented)

00-00	HLT	00-17	FLA	00-36	LOB
00-01	RNA	00-20	ASC	00-37	OVS
00-02	NEG	00-21	SAS	00-40	TBP
00-03	CLA	00-22	SAZ	00-41	TPB
00-04	TBA	00-23	SAN	00-42	TBV
00-05	TAB	00-24	SAP	00-43	TVB
00-06	IAB	00-25	SOF	00-44	STX
00-07	CSB	00-26	IBS	00-45	LIX
00-10	RSA	00-27	ABA	00-46	XPX
00-11	LSA	00-30	OBA	00-47	XPB
00-12	FRA	00-31	LCS	00-50	SXB
00-13	FLL	00-32	SNO	00-51	IXS
00-14	FRL	00-33	NOP	00-52	TAX
00-15	RSL	00-34	CNS	00-53	TXA
00-16	LSL	00-35	TOI	00-54	RTX

13-4	SNS	1700	AOP
130600	PIE	1702	AIP
130601	PID	17.0IM.4	MOP
13.0IM.0	CEU	17.0IM.6	MIP
13.0IM.2	TEU		

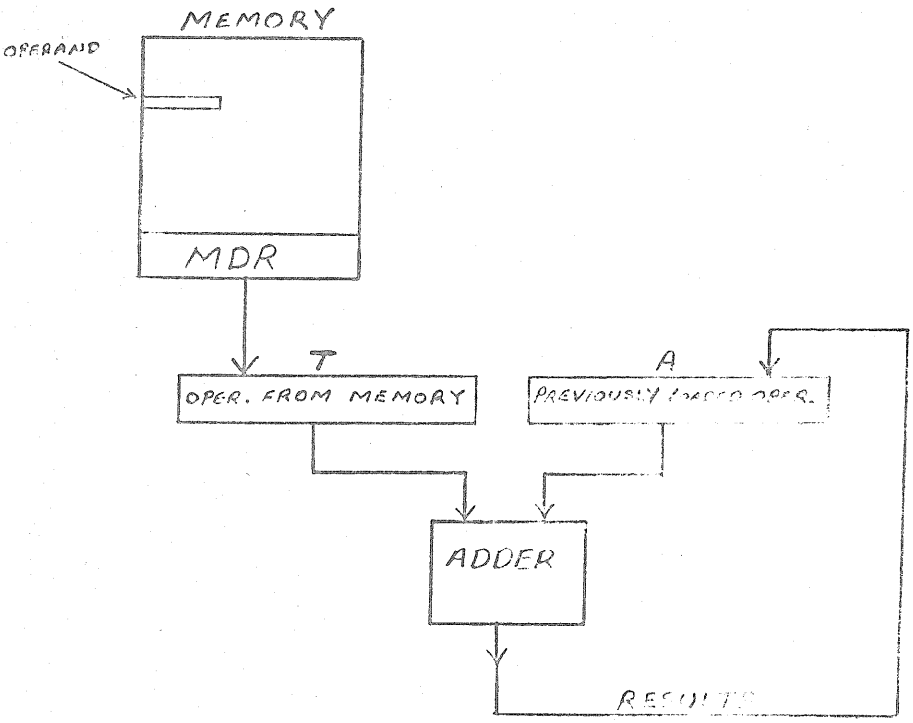
INSTRUCTION SET EXAMPLES

1. AMA

0	1	0	1	X	I	M			m				

05

XIM (100) m1+X = ADDRESS OF OPERAND
XIM (101) [P1—P6, m] +X = ADDR. OF OPER.
XIM (111) ([P1-P6, m]+X) = ADDRESS OF INDIRECT ADDR. WORD (IAW)



2. AME 16 — ADD MEMORY TO [illegible]

SAME AS AMA INSTRUCTION EXCEPT THAT THE B ACCUMULATOR MUST BE LOADED WITH [illegible] PRIOR TO EXECUTION.
THE OPERAND FROM MEMORY IN THE T REG. AND THE OPERAND IN 'B' ARE INPUTS TO THE ADDER.

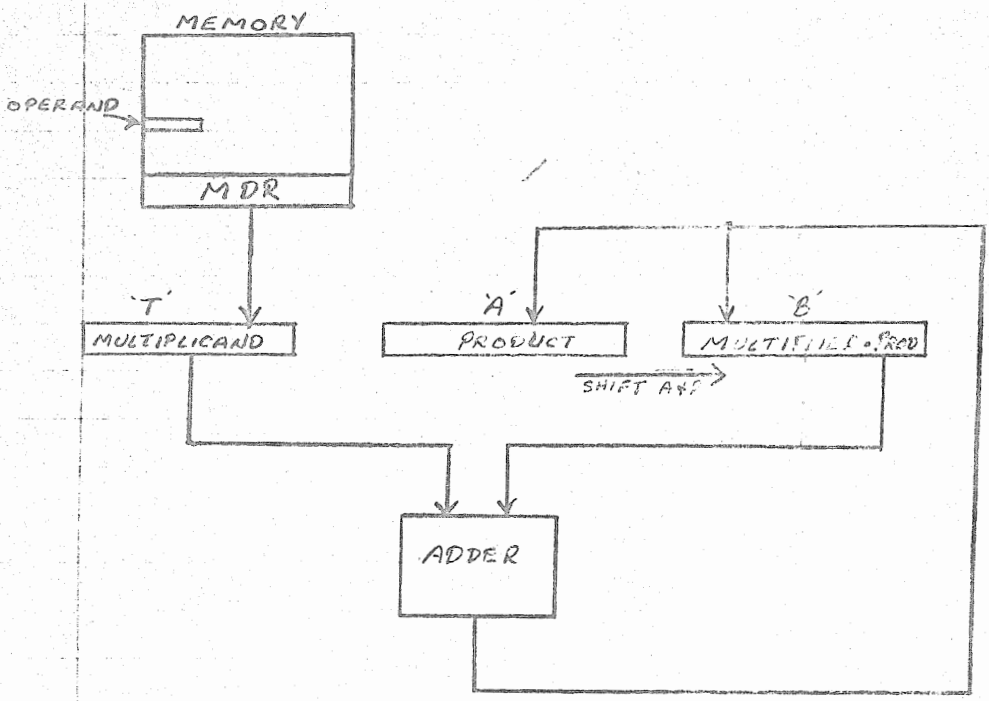
3. SMA 06 — SUBTRACT MEMORY FROM A ACCUMULATOR.

THE 'T' REGISTER'S COMPLEMENT IS SENT TO THE ADDER. THIS COMPLEMENT ADDITION IS PERFORMED ON THE OPERANDS.

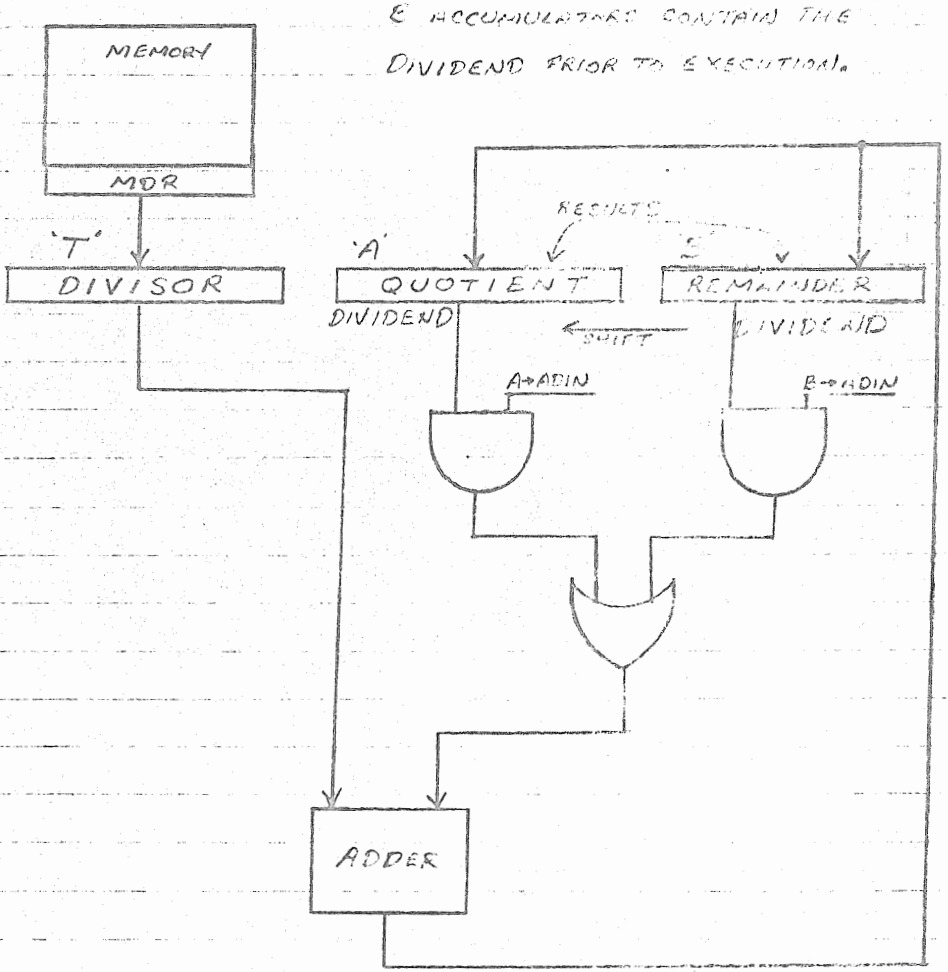
'A' ACCUMULATOR CONTAINS THE MINUEND 'T' REG. CONTAINS THE SUBTRAHEND

4. MPY

07 MULTIPLY

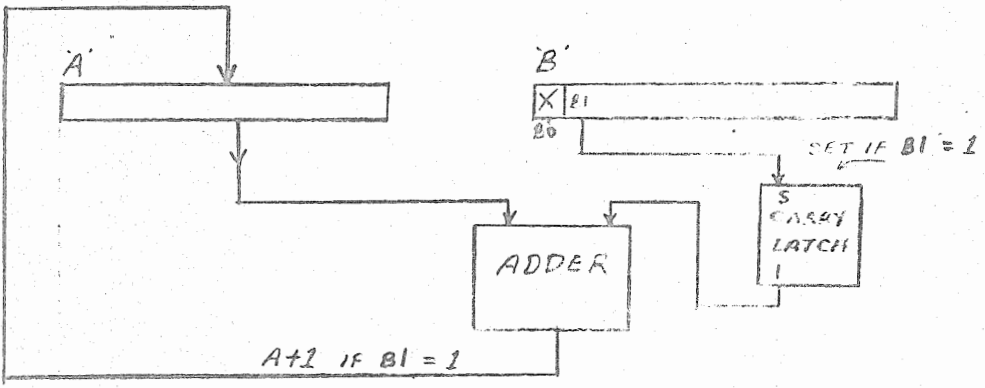


5. DIV DIVIDE - THE DIVIDEND IS ASSUMED
10 DOUBLE PRECISION IN A AND
B ACCUMULATORS CONTAIN THE
DIVIDEND PRIOR TO EXECUTION.



6. RNA
00-01

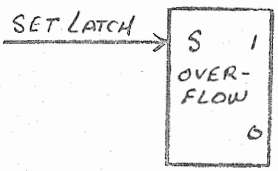
ROUND 'A' ACCUMULATOR



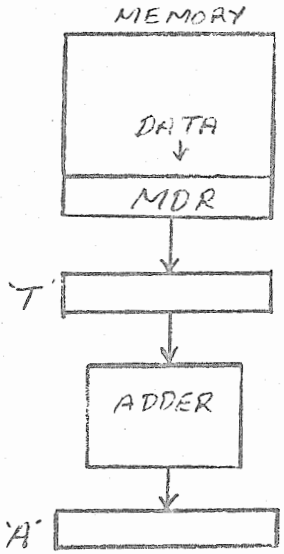
7. OVS
00-37

SET OVERFLOW LATCH

USED WHEN COMING BACK TO THE PROGRAM FROM AN INTERRUPT. IF OVERFLOW EXISTED AT THE TIME OF INTERRUPT, LATCH GETS SET UPON RETURN.

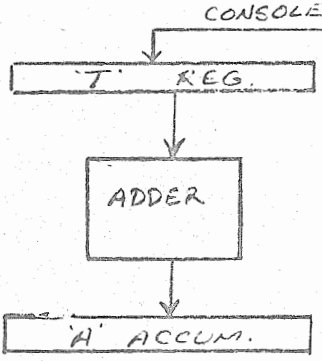


9. LAA
01

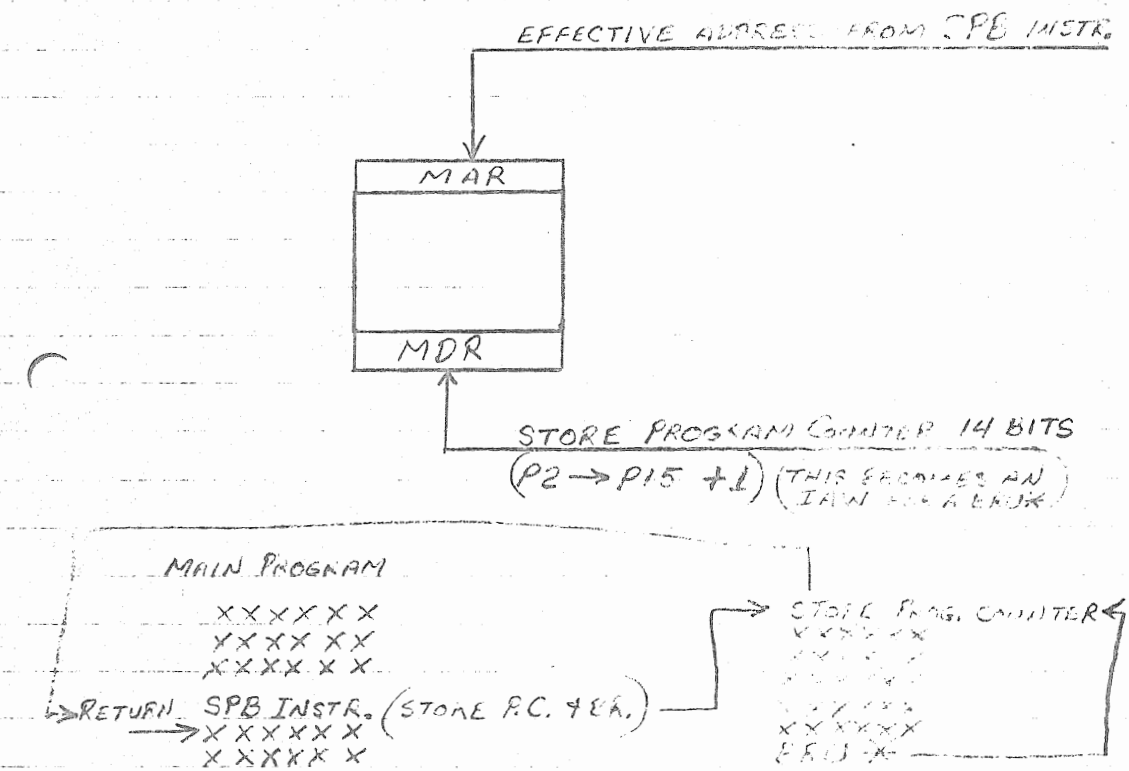


9. LCS
00-31

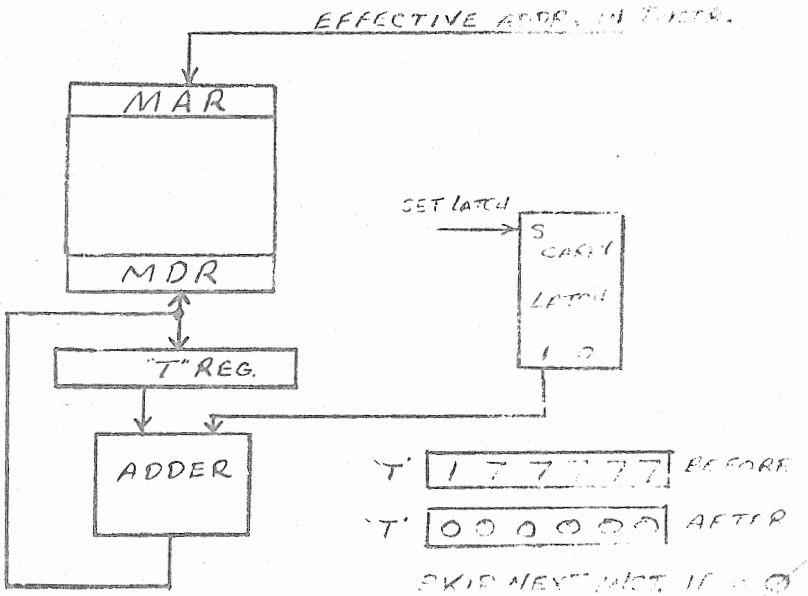
LOAD CONTROL SWITCHES



10. SPB STORE PLACE AND [illegible]



11. IMS 14 — INCREMENT MEMORY & SKIP IF CONTENTS = Ø



12. CMA 15 — COMPARE MEMORY WITH ACCUMULATOR (3 WAY)

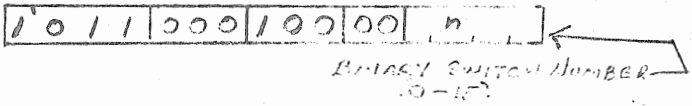
A < M : EXECUTE NEXT INSTR.

A = M : NEXT INST. SKIPPED

A > M : NEXT 2 INST SKIPPED

13. SNS
12-04-N

SKIP IF SPECIFIED SWITCH IS NOT SET.



14. SAS
00-21

SKIP ON 'A' [illegible]

'A' SIGN NEG. – NEXT INST. EXECUTED.
'A' SIGN POS. – NEXT INST. SKIPPED.
'A' SIGN POS. AND [illegible] GREATER THAN ZERO, SKIP NEXT TWO INST.

15. SOF
00-25

SKIP ON OVERFLOW – RESETS OVERFLOW LATCH.
IF OVERFLOW SET – NEXT INST. EXECUTED.
IF OVERFLOW RESET – NEXT INST. SKIPPED.

SAMPLE PROGRAM:

AMM
SOF
BRU — IF OVFLOW → CORRECTIVE ROUTINE
STA

CORRECTIVE ROUTINE
XXX
XXX
XXX

16. SNC

SAMPLE PROGRAM:

```
LOOP  LS  A  (LEFT SHIFT A)
      SNC    (AC = A1 ?)
      BRU  LOOP
      STA    (STORE NORMALIZED
              WORD)
```

1ST A AC A1 ←

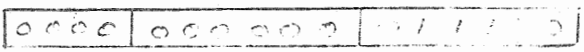
2ND A AC A1 ← SHIFT LEFT

(NORMALIZED

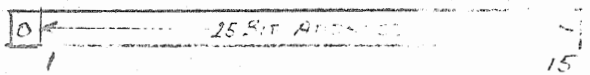
GET RID OF LEADING ZEROS IN POSITIVE NUMBERS.
GET RID OF LEADING ONE'S IN NEGATIVE NUMBERS.

17. LOB

00-36



2ND WORD



ALLOWS FOR ADDRESSING IN 32K

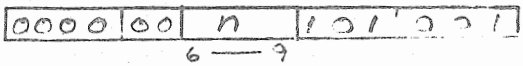
18. SXB
00-50

SKIP IF INDEX POINTER SET TO E ACCUMULATOR.

INDEX POINTER LATCH → E ACCUMULATOR
(MASTER CLEAR POINTS TO 'E' ACCUM.) → OPTIONAL INDEX REG.

19. IXS
00-N-51

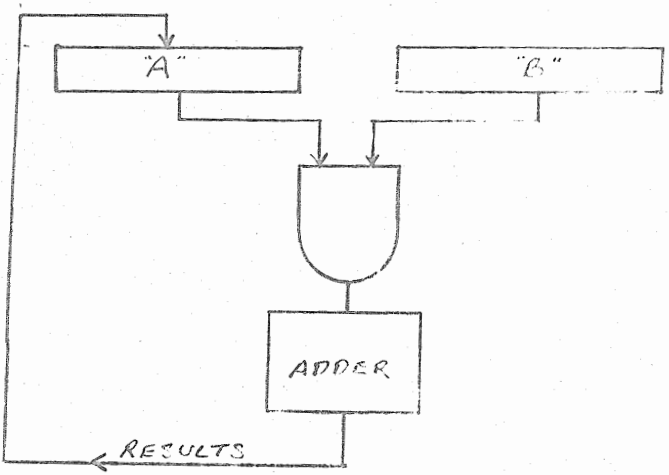
INCREMENT INDEX BY N AND SKIP IF POSITIVE.



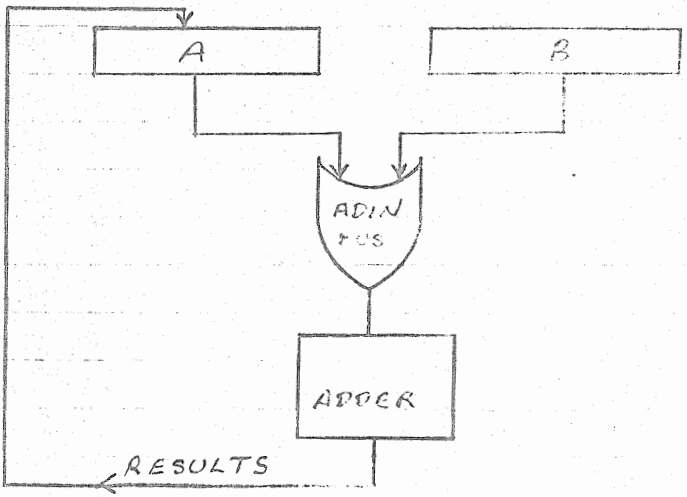
n = VALUE 0-15 IS ADDED TO THE CONTENTS OF THE INDEX REGISTER.

20. ABA
00-27

ADD A AND B ACCUMULATORS



21. OBA "OR" A AND B ACCUMULATORS.
00-30



22. NEG. NEGATE THE A ACCUMULATOR
00-02

"A" BEFORE 000002

"A" AFTER 177776 { 2'S COMPLEMENT 'A' ACCUMULATOR

23. CNS CONVERT NUMBER [illegible]
00-34

EXAMPLE #1

177777 = 2's COMPLEMENT NUMBER

CONVERTED TO:

100001 = SIGN MAGNITUDE NUMBER

SIGN UNCHANGED

EXAMPLE #2

100001 = SIGN MAGNITUDE NUMBER

CONVERTED TO:

177777 = 2's COMPLEMENT NUMBER

EXAMPLE #3

177770 = 2's COMPLEMENT NUMBER

CONVERTED TO:

100010 = SIGN MAGNITUDE NUMBER

EXAMPLE #4

100007 = SIGN MAGNITUDE NUMBER

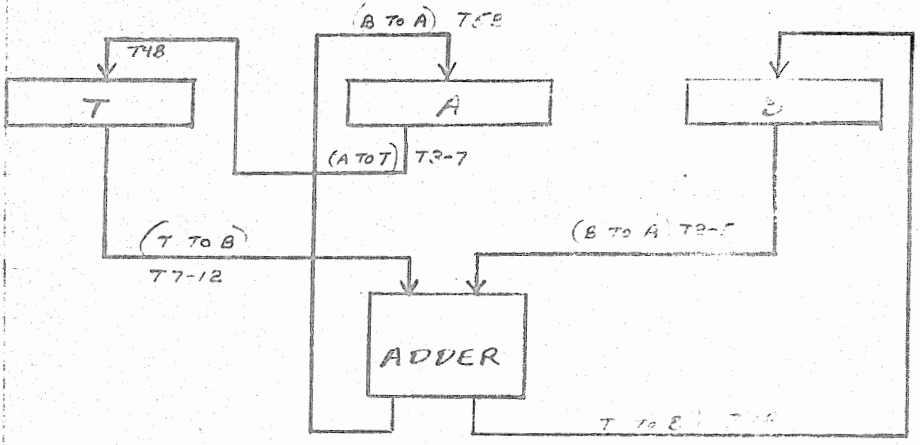
CONVERTED TO:

177771 = 2's COMPLEMENT NUMBER

NOTE: POSITIVE SIGNED NUMBERS ARE NOT AFFECTED.

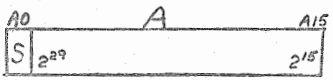
24. IAB
00-06

INTERCHANGE A AND B ACCUMULATORS



25. CSB
00-07

COPY SIGN OF B ACCUMULATOR



SAMPLE PROGRAM (FIXED POINT DOUBLE PRECISION ADDITION)

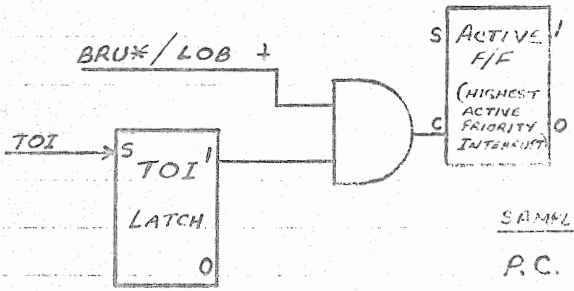
AMB
CSB
AMA
XXX

IF S.D.=1 CARRY LATCH IS SET.
THIS INST. WOULD FOLLOW AMB.
THEN THE CARRY WOULD BE ADDED TO A15

NOTE: CSB INST. WILL NOT ALLOW A-1 INTERLOCK WITH THE NEXT INST. IS EXECUTED.

26. TOI — TURN OFF INTERRUPT. HIGHEST ACTIVE INTERRUPT IS RESET WHEN NEXT LOB OR LOB 18 EXECUTED.

00-35



SAMPLE INTERRUPT PROGRAM:

P.C. (Prog. Counter stored by SPB)

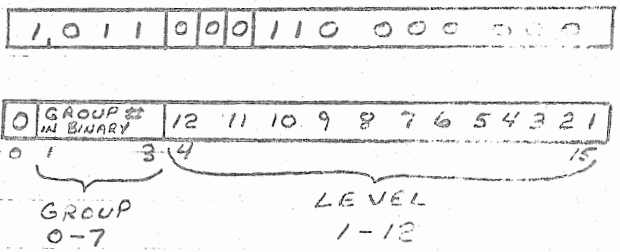
XXX (Interrupt Routine)

TOI (Turned Latched)

BRU*/LOB

27. PIE — PRIORITY INTERRUPT ENABLE (2 WORD INST.)

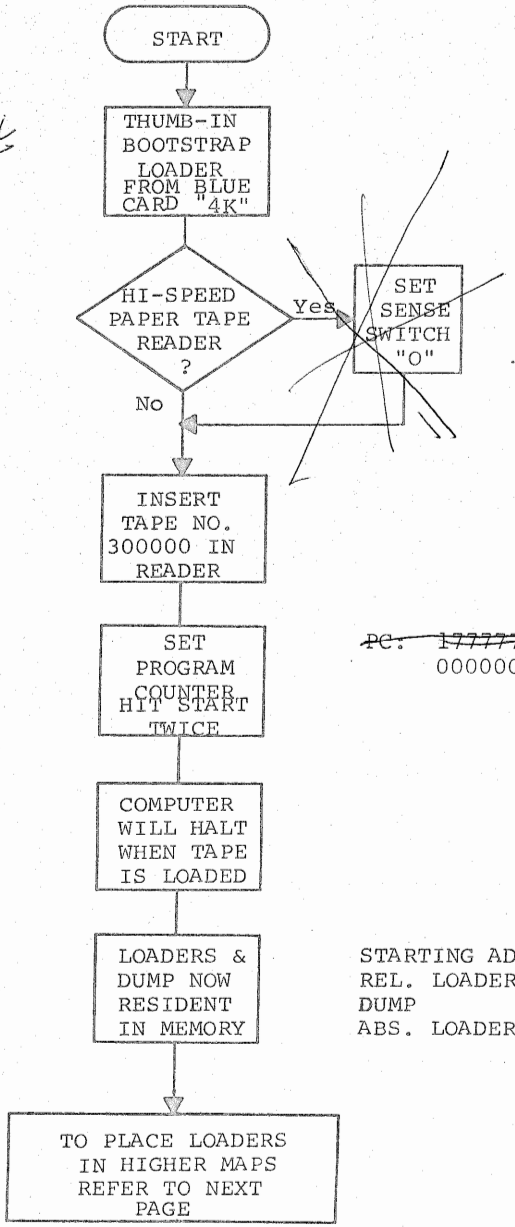
130600



ANY COMBINATION OF INTERRUPT LEVELS CAN BE ENABLED FOR A GROUP.

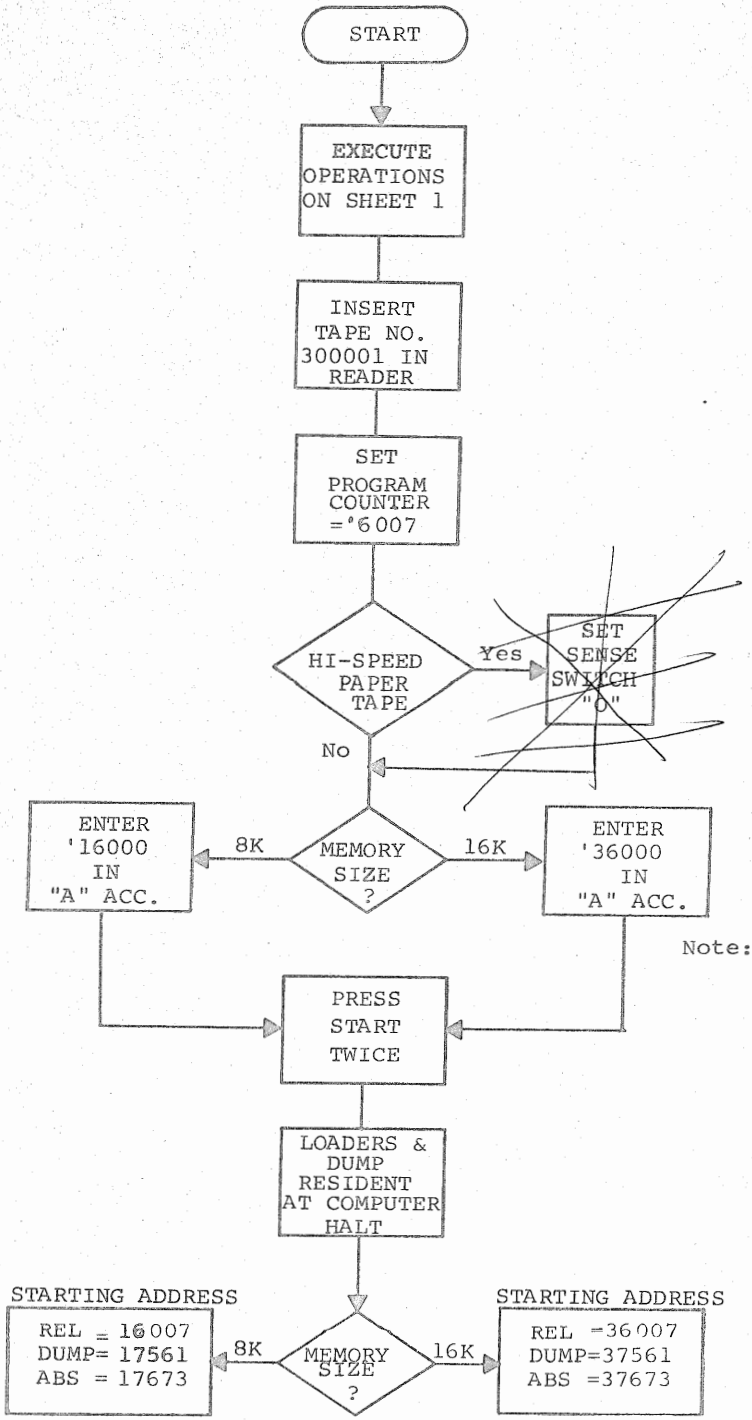
PROCEDURE FOR ENTERING ABSOLUTE VERSION
OF STANDARD BOOTSTRAP PACKAGE - #300000 SHEET 1

300 000 F ABS
300 001 F REL



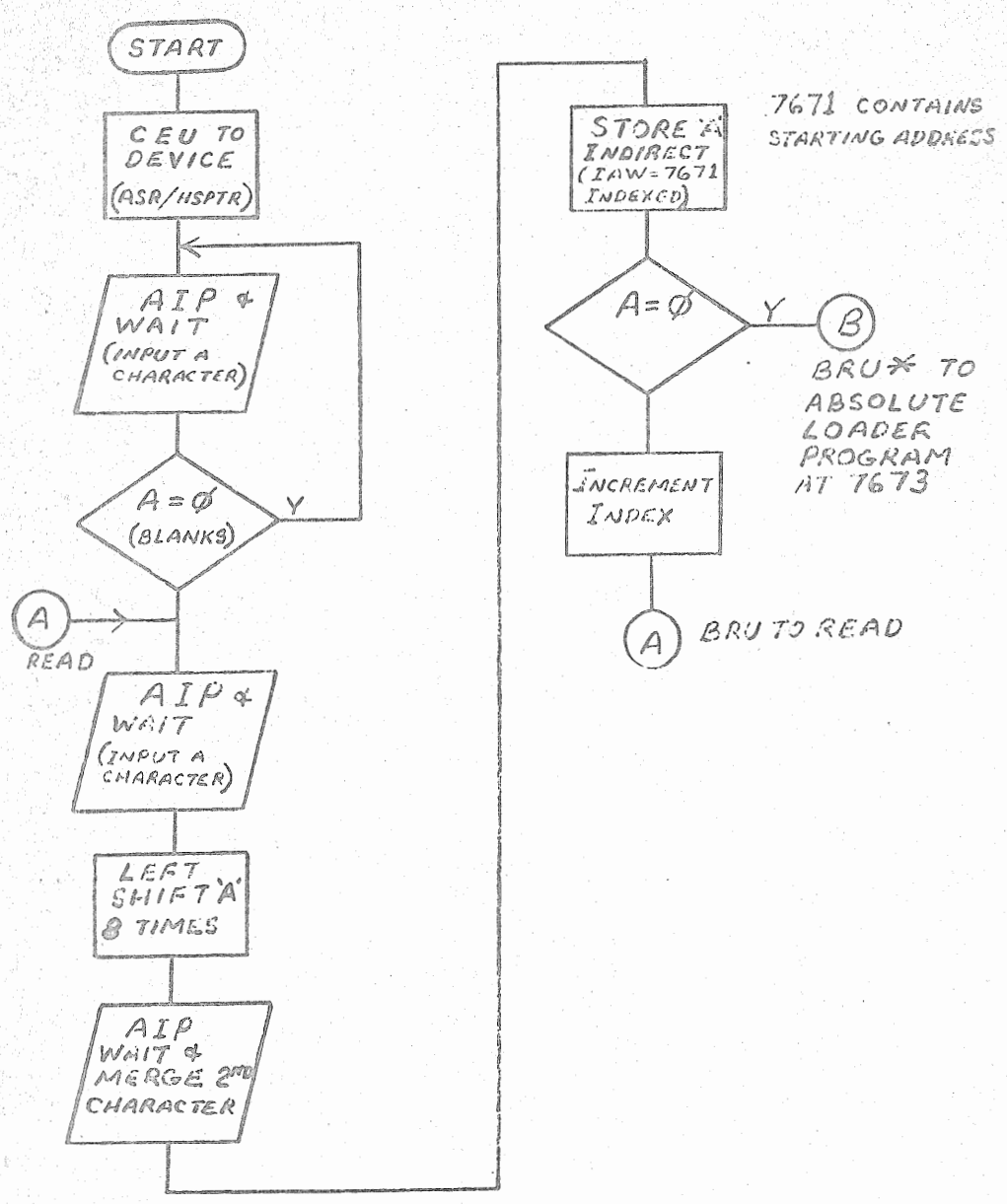
~~PC: 177777 810B~~
000000 810A

STARTING ADDRESSES:
REL. LOADER='6007
DUMP ='7561
ABS. LOADER='7673



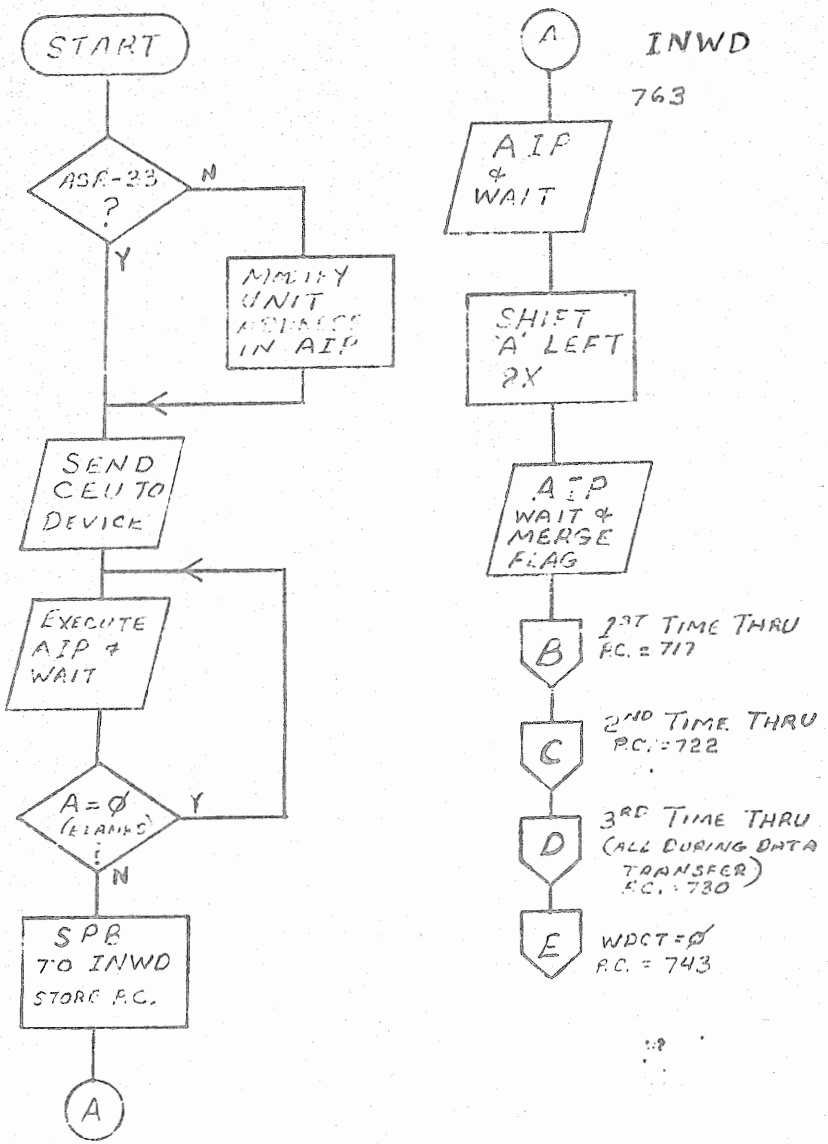
Note: Higher Maps can be used also. Enter relocation factor as desired in "A" Acc.

FLOWCHART OF BINARY BOOTSTRAP LOADER



ABSOLUTE LOADER FLOWCHART

page 26 300 001 F tape



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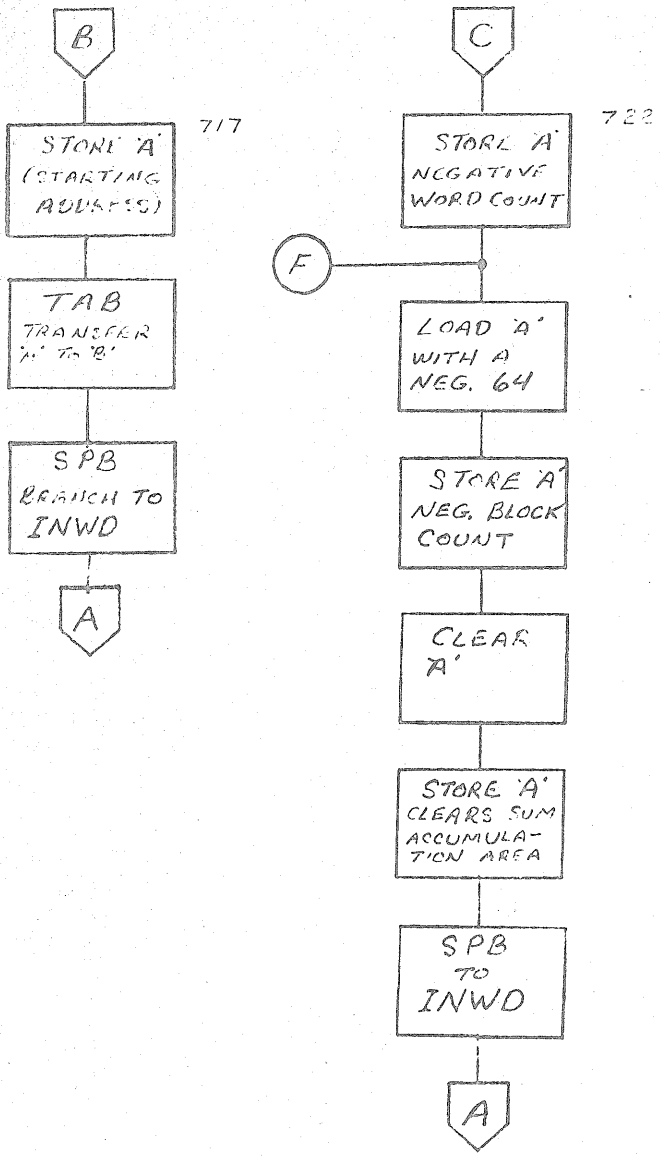
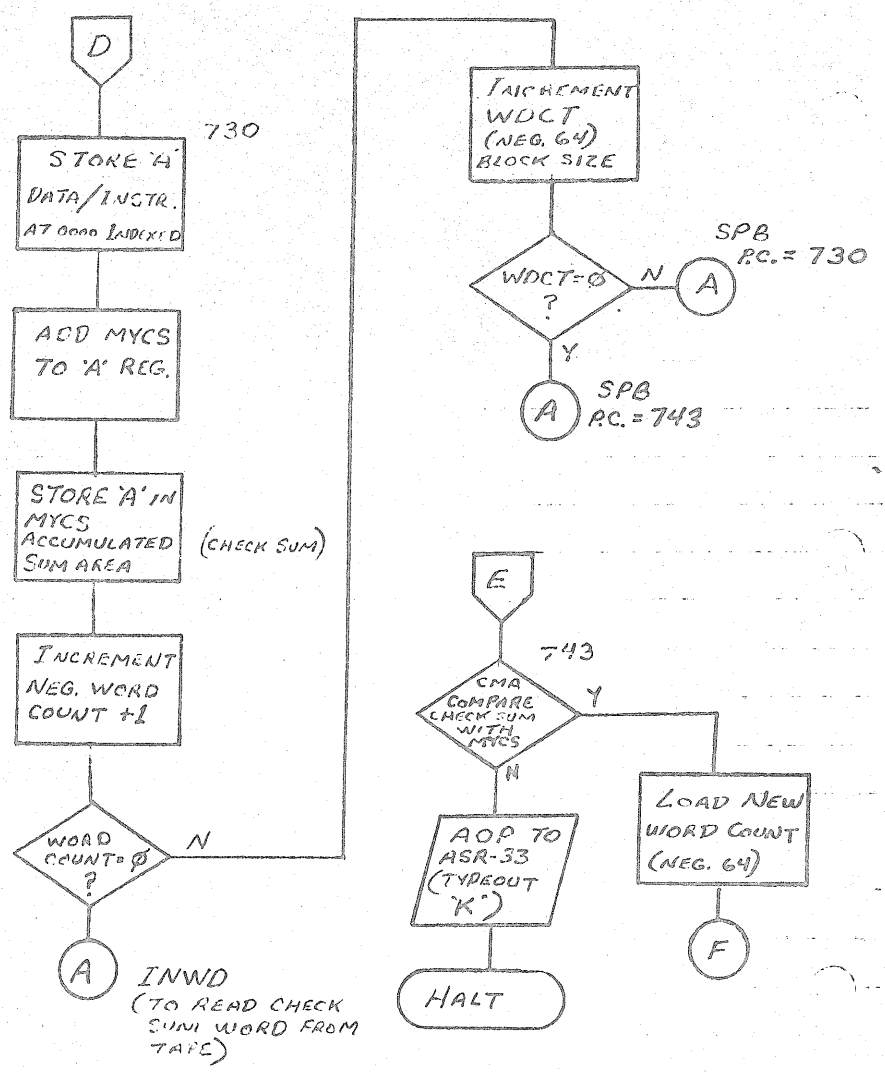

B
STORE 'A' (STARTING ADDRESS)
717
TAB TRANSFER 'A' TO 'Q'
SPB BRANCH TO INWD
A
C
STORE 'A' NEGATIVE WORD COUNT
722
F
LOAD 'A' WITH A NEG. 64
STORE 'A' NEG. BLOCK COUNT
CLEAR 'A'
STORE 'A' CLEARS SUM ACCUMULATION AREA
SPB TO INWD
A


D
730
STORE 'A' DATA/INSTR. AT 0000 INDEXED
ADD MYCS TO 'A' REG.
STORE 'A' IN MYCS ACCUMULATED SUM AREA
(CHECK SUM)
INCREMENT NEG. WORD COUNT +1
WORD COUNT = Ø ?
N
Y
A
INWD
(TO READ CHECK SUM WORD FROM TAPE)
INCREMENT WDCT (NEG. 64) BLOCK SIZE
WDCT = Ø ?
N
Y
A
SPB P.C. = 730
A
SPB P.C. = 743
E
743
CMA COMPARE CHECK SUM WITH MYCS
Y
N
LOAD NEW WORD COUNT (NEG. 64)
F
AOP TO ASR-33 (TYPEOUT 'K')
HALT

SEL PROGRAM LIBRARY

PROGRAM DESCRIPTION

 Catalog No. 303001A

IDENTIFICATION: Mainframe Exerciser (MFE)

AUTHOR: SEL

ACCEPTED: 13 January 1967

PURPOSE: A fast no-loop program designed to use each of the mainframe instructions in such a way that if a Halt occurs, the operator can tell from the program listing which instruction is malfunctioning.

SOURCE PROGRAM LANGUAGE: MNEMBLER - 810A

COMPUTER CONFIGURATION: Standard SEL 810A

STORAGE: 2000_8 to 2303_8 3000_8 to 3021_8 - Not Relocatable

SUBROUTINES REQUIRED: 810A Mainframe Diagnostic Loading Procedure

TIMING Approx. 1 ms/cycle

USE: Start at location 2000_8, the program will run until halted manually. If a halt occurs consult the listing or halt log using the P-Counter location to find the instruction that failed.

HALT LOG FOR MAINFRAME EXERCISER

P-Counter Location	Instruction in Error
2006_8	AMA, SOF
2011_8	AMA
2020_8	AMB SOF
2023_8	AMB
2030_8	LSL
2034_8	RSA, SMA
2041_8	FLL

2044_8	FLL
2051_8	FRA
2053_8	FRA
2061_8	LSA
2065_8	LSA
2071_8	CLA
2102_8	FRL
2106_8, 2107_8	CMA
2112_8, 2114_8	CMA
2117_8, 2120_8	CMA
2125_8, 2127_8	STB
2134_8	ABA
2141_8	OBA
2153_8	NEG, CNS, SMA
2157_8, 2160_8	SAS
2163_8, 2165_8	SAS
2170_8, 2171_8	SAS
2200_8	FLA, SMA
2216_8	RSL, FRA, RNA, TAB, CLA, IAB, ASC
2222_8	SNO
2225_8	SNO
2232_8	LOB
2236_8	SMA
2241_8	IBS
2251_8, 2254_8	MPY
2262_8	MPY, SMA
2267_8	AMA, SMA, TBA
3003_8	BRU Indirect
3013_8	SOF
3016_8	SOF

METHOD: N/A

Catalog No. 303001

```
0001  00000 00000000 *     MAIN FRAME EXERCISOR -- REV  0                    00000100
0002  00000 00000000 *                                                       00000200
0003  00000 00000000       REL                                               
0004  02000 70002000       ORG  *2000                                        00000400
0005  02000 00000000 *                                                       00000500
0006  02000 02102271 STAR   LBA  TES2      LOAD ALL ONES IN B                00000600
0007  02001 01102275       LAA  TES6      LOAD SEVENS IN A                  00000700
0008  02002 05102277       AMA  TE10      ADD 1 TO A                        00000800
0009  02003 00000025       SOF            OVERFLOW                          00000900
0010  02004 11102006       BRU  *+2       YES, GO ON                        00001000
0011  02005 00000000       HLT            NO, HALT                          00001100
0012  02006 00000020       ASC            CHANGE SIGN OF A                  00001200
0013  02007 00000022       SAZ            IS A ZERO                         00001300
0014  02010 00000000       HLT            NO, HALT                          00001400
0015  02011 01102271       LAA  TES2      YES, REPEAT TEST FOR B            00001500
0016  02012 02102275       LBA  TES6                                        00001600
0017  02013 15102277       AMB  TE10                                        00001700
0018  02014 00000004       TBA                                              00001800
0019  02015 00000025       SOF                                              00001900
0020  02016 11102020       BRU  *+2                                         00002000
0021  02017 00000000       HLT                                              00002100
0022  02020 00000020       ASC                                              00002200
0023  02021 00000022       SAZ                                              00002300
0024  02022 00000000       HLT                                              00002400
0025  02023 02102271       LBA  TES2      ALL ONES IN B                     00002500
0026  02024 01102277       LAA  TE10      ONE IN A                          00002600
0027  02025 00001716       LSL  15        SHIFT LEFT 15 PLACE               00002700
0028  02026 00000023       SAN            SHIFT OK                          00002800
0029  02027 00000000       HLT            NO, HALT                          00002900
0030  02030 00001710       RSA  15        YES, NOW SHIFT RIGHT              00003000
0031  02031 06102271       SMA  TES2      SUBTRACT ALL ONES                 00003100
0032  02032 00000022       SAZ            IS A ZERO                         00003200
0033  02033 00000000       HLT            NO, HALT                          00003300
0034  02034 01102277       LAA  TE10      YES, ONE IN A                     00003400
0036  02036 00001713       FLL  15        FULL LEFT LOGICAL SHIFT           00003600
0037  02037 00000023       SAN            SHIFT OK                          00003700
0038  02040 00000000       HLT            NO, HALT                          00003800
```

```
0039  02041 00000006   IAB          YES, CHECK B                    00003900
0040  02042 00000023   SAN                                          00004000
0041  02043 00000000   HLT                                          00004100
0042  02044 00001712   FRA  12      FULL RIGHT SHIFT                00004200
0043  02045 00000007   CSB          COPY SIGN OF B                  00004300
0044  02046 01102270   AMA  TES1    ADD ZERO TO A                   00004400
0045  02047 00000022   SAZ          IS A ZERO                       00004500
0046  02050 00000000   HLT          NO, HALT                        00004600
0047  02051 00000006   IAB          YES                             00004700
0048  02052 00000022   SAZ          IS B ZERO                       00004800
0049  02053 00000000   HLT          NO, HALT                        00004900
0050  02054 01102277   LAA  TE10    YES, ONE IN A                   00005000
0051  02055 02102271   LBA  TES2    ALL ONES IN B                   00005100
0052  02056 00001711   LSA  12      SHIFT LEFT ARITHMETIC           00005200
0053  02057 00000022   SAZ          IS A ZERO                       00005300
0054  02060 00000000   HLT          NO                              00005400
0055  02061 01102275   LAA  TES6    SEVENS IN A                     00005500
0056  02062 00001711   LSA  12                                      00005600
0057  02063 00000022   SAZ                                          00005700
0058  02064 00000000   HLT                                          00005800
0059  02065 01102271   LAA  TES2    ALL ONES IN A                   00005900
0060  02066 00000003   CLA          DOES CLEAR A WORK               00006000
0061  02067 00000022   SAZ                                          00006100
0062  02070 00000000   HLT                                          00006200
0063  02071 00000063   NOP                                          00006300
0064  02072 00000063   NOP                                          00006400
0065  02073 01102271   LAA  TES2    ONES                            00006500
0066  02074 02102273   LBA  TES4    ALT. BITS IN B                  00006600
0067  02075 00001714   FRL  12      ROTATE                          00006700
0068  02076 00000004   TBA                                          00006800
0069  02077 06102271   SMA  TES2                                    00006900
0070  02100 00000022   SAZ                                          00007000
0071  02101 00000000   HLT                                          00007100
0072  02102 01102270   LAA  TES1    ZERO IN A                       00007200
0073  02103 15102277   CMA  TE10    COMPARE ZERO TO ONE             00007300
      02104 ...                                                    ...
0075  02105 00000000   HLT          NO                              00007500
0076  02106 00000000   HLT          NO                              00007600
0077  02107 01102277   LAA  TE10    ONE IN A                        00007700
```

memory address

02102271 = op code X M effective address

```
0001  00000 00000000 *     MAIN FRAME EXERCISØR -- REV  0                          00000100
0002  00000 00000000 *                                                             00000200
0003  00000 00000000       REL                                                     
0004  02000 70002000       ØRG  '2000                                              00000400
0005  02000 00000000 *                                                             00000500
0006  02000 02102271 STAR  LBA  TES2      LØAD ALL ØNES IN B                      00000600
0007  02001 01102275       LAA  TES6      LØAD SEVENS IN A                        00000700
0008  02002 05102277       AMA  TE10      ADD 1 TØ A                              00000800
0009  02003 00000025       SØF            ØVERFLØW                                00000900
0010  02004 11102006       BRU  *+2       YES, GØ ØN                              00001000
0011  02005 00000000       HLT            NØ, HALT                                00001100
0012  02006 00000020       ASC            CHANGE SIGN ØF A                        00001200
0013  02007 00000022       SAZ            IS A ZERØ                               00001300
0014  02010 00000000       HLT            NØ, HALT                                00001400
0015  02011 01102271       LAA  TES2      YES, REPEAT TEST FØR B                  00001500
0016  02012 02102275       LBA  TES6                                              00001600
0017  02013 15102277       AMB  TE10                                              00001700
0018  02014 00000004       TBA                                                    00001800
0019  02015 00000025       SØF                                                    00001900
0020  02016 11102020       BRU  *+2                                               00002000
0021  02017 00000000       HLT                                                    00002100
0022  02020 00000020       ASC                                                    00002200
0023  02021 00000022       SAZ                                                    00002300
0024  02022 00000000       HLT                                                    00002400
0025  02023 02102271       LBA  TES2      ALL ØNES IN B                           00002500
0026  02024 01102277       LAA  TE10      ØNE IN A                                00002600
0027  02025 00001716       LSL  15        SHIFT LEFT 15 PLACE                     00002700
0028  02026 00000023       SAN            SHIFT ØK                                00002800
0029  02027 00000000       HLT            NØ, HALT                                00002900
0030  02030 00001710       RSA  15        YES, NØW SHIFT RIGHT                    00003000
0031  02031 06102271       SMA  TES2      SUBTRACT ALL ØNES                       00003100
0032  02032 00000022       SAZ            IS A ZERØ                               00003200
0033  02033 00000000       HLT            NØ, HALT                                00003300
0034  02034 01102277       LAA  TE10      YES, ØNE IN A                           00003400
0035  02035 02102277       LBA  TE10      ØNE IN B                                00003500
0036  02036 00001713       FLL  15        FULL LEFT LØGICAL SHIFT                 00003600
0037  02037 00000023       SAN            SHIFT ØK                                00003700
0038  02040 00000000       HLT            NØ, HALT                                00003800
```

~~00 000025~~ AUG. Instruction/Data

5-5-5

```
0039  02041 00000006      IAB                 YES, CHECK B                    00003900
0040  02042 00000023      SAN                                                 00004000
0041  02043 00000000      HLT                                                 00004100
0042  02044 00001712      FRA  15             FULL RIGHT SHIFT                00004200
0043  02045 00000007      CSB                 COPY SIGN OF B                  00004300
0044  02046 05102270      AMA  TES1           ADD ZERO TO A                   00004400
0045  02047 00000022      SAZ                 IS A ZERO                       00004500
0046  02050 00000000      HLT                 NO, HALT                        00004600
0047  02051 00000006      IAB                 YES                             00004700
0048  02052 00000022      SAZ                 IS B ZERO                       00004800
0049  02053 00000000      HLT                 NO, HALT                        00004900
0050  02054 01102277      LAA  TE10           YES, ONE IN A                   00005000
0051  02055 02102271      LBA  TES2           ALL ONES IN B                   00005100
0052  02056 00001711      LSA  15             SHIFT LEFT ARITHMETIC           00005200
0053  02057 00000022      SAZ                 IS A ZERO                       00005300
0054  02060 00000000      HLT                 NO                              00005400
0055  02061 01102275      LAA  TES6           SEVENS IN A                     00005500
0056  02062 00001711      LSA  15                                             00005600
0057  02063 00000022      SAZ                                                 00005700
0058  02064 00000000      HLT                                                 00005800
0059  02065 01102271      LAA  TES2           ALL ONES IN A                   00005900
0060  02066 00000003      CLA                 DOES CLEAR A WORK               00006000
0061  02067 00000022      SAZ                                                 00006100
0062  02070 00000000      HLT                                                 00006200
0063  02071 00000033      NOP                                                 00006300
0064  02072 00000033      NOP                                                 00006400
0065  02073 01102271      LAA  TES2           ONES                            00006500
0066  02074 02102273      LBA  TES4           ALT. BITS IN B                  00006600
0067  02075 00001714      FRL  15             ROTATE                          00006700
0068  02076 00000004      TBA                                                 00006800
0069  02077 06102271      SMA  TES2                                           00006900
0070  02100 00000022      SAZ                                                 00007000
0071  02101 00000000      HLT                                                 00007100
0072  02102 01102270      LAA  TES1           ZERO IN A                       00007200
0073  02103 15102277      CMA  TE10           COMPARE ZERO TO ONE             00007300
0074  02104 11102107      BRU  *+3            A LESS THAN M, OK.              00007400
0075  02105 00000000      HLT                 NO                              00007500
0076  02106 00000000      HLT                 NO                              00007600
0077  02107 01102277      LAA  TE10           ONE IN A                        00007700
```

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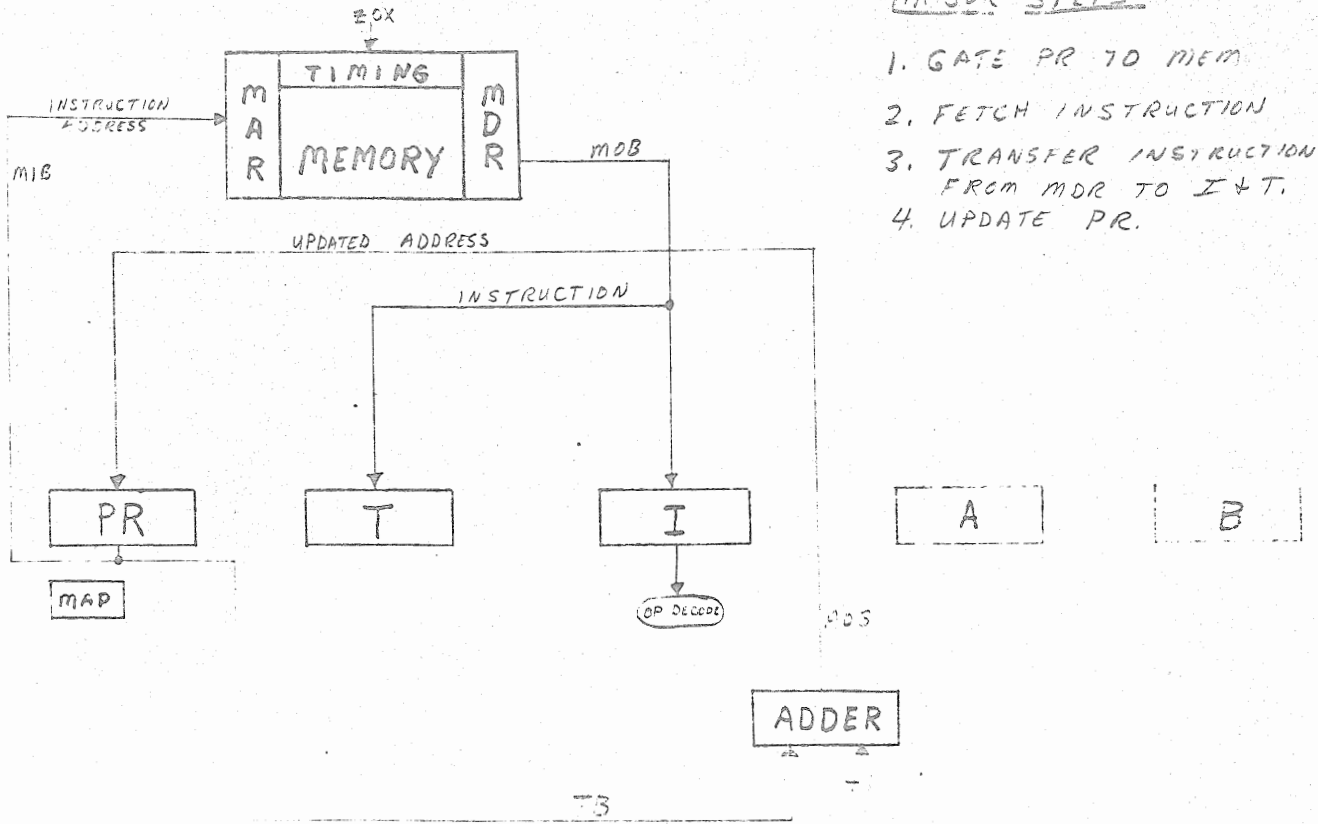
```
0078  02110 15102277      CMA   TE10      CØMPARE ØNE TØ ØNE                00007800
0079  02111 00000000      HLT             NØ                                00007900
0080  02112 11102114      BRU   *+2       A = M, ØK.                        00008000
0081  02113 00000000      HLT             NØ                                00008100
0082  02114 05102277      AMA   TE10      2 IN A                            00008200
0083  02115 15102277      CMA   TE10      CØMPARE 2 TØ 1                    00008300
0084  02116 00000000      HLT                                               00008400
0085  02117 00000000      HLT                                               00008500
0086  02120 02102271      LBA   TES2      A IS MØRE THAN M                  00008600
0087  02121 04102302      STB   LØC1                                        00008700
0088  02122 00000006      IAB                                               00008800
0089  02123 15102302      CMA   LØC1      WAS B STØRED PRØPERLY             00008900
0090  02124 00000000      HLT             NØ                                00009000
0091  02125 11102127      BRU   *+2       YES                               00009100
0092  02126 00000000      HLT             NØ                                00009200
0093  02127 01102272      LAA   TES3      ALT. BITS IN A                    00009300
0094  02130 02102273      LBA   TES4      ALT. BITS IN B                    00009400
0095  02131 00000027      ABA             AND A AND B                       00009500
0096  02132 00000022      SAZ             ANDED CØRRECTLY                   00009600
0097  02133 00000000      HLT             NØ                                00009700
0098  02134 01102272      LAA   TES3      YES                               00009800
0099  02135 00000030      ØBA             ØR A + B                          00009900
0100  02136 05102271      SMA   TES2      SUBTRACT ALL ØNES                 00010000
0101  02137 00000022      SAZ             A ZERØ                            00010100
0102  02140 00000000      HLT             NØ                                00010200
0103  02141 01102270      LAA   TES1      ZERØ IN A                         00010300
0104  02142 03102303      STA   LØC2      STØRE A                           00010400
0105  02143 14102303      IMS   LØC2      MAKE ZERØ A ØNE                   00010500
0106  02144 00000033      NØP                                               00010600
0107  02145 01102303      LAA   LØC2                                        00010700
0108  02146 00000002      NEG             CHANGE TØ A MINUS ØNE             00010800
0109  02147 00000034      CNS             CHANGE TØ SIGN MAGNITUDE          00010900
0110  02150 05102277      SMA   TE10      SUBTRACT ØNE                      00011000
0111  02151 00000023      SAN             NEGATIVE SIGN LEFT                00011100
0112  02152 00000000      HLT             NØ                                00011200
0113  02153 01102271      LAA   TES2      ØNES IN A                         00011300
0114  02154 00000021      SAS             IS A +, 0, ØR -                   00011400
0115  02155 11102160      BRU   *+3       A IS -                            00011500
0116  02156 00000000      HLT             0, HALT                           00011600
```

```
0117  02157 00000000  HLT                 +, HALT                    00011700
0118  02160 06102277  AMA  TE10          ZERØ IN A                  00011800
0119  02161 00000021  SAS                                            00011900
0120  02162 00000000  HLT                                            00012000
0121  02163 11102165  BRU  *+2           A IS ZERØ                  00012100
0122  02164 00000000  HLT                                            00012200
0123  02165 06102275  AMA  TES6          SEVENS IN A                00012300
0124  02166 00000021  SAS                                            00012400
0125  02167 00000000  HLT                                            00012500
0126  02170 00000000  HLT                                            00012600
0127  02171 00000033  NØP               A IS +                     00012700
0128  02172 02102275  LBA  TES6          SEVENS IN B                00012800
0129  02173 00000003  CLA                                            00012900
0130  02174 00001717  FLA  15            MØVE B TØ A                00013000
0131  02175 06102275  SMA  TES6          SUBTRACT SEVENS            00013100
0132  02176 00000022  SAZ                IS A ZERØ                  00013200
0133  02177 00000000  HLT                NØ                         00013300
0134  02200 01102274  LAA  TES5          MINUS ZERØ IN A            00013400
0135  02201 00001715  RSL  15                                       00013500
0136  02202 00000112  FRA  1                                        00013600
0137  02203 00000001  RNA                                           00013700
0138  02204 00000005  TAB                                           00013800
0139  02205 00000003  CLA                                           00013900
0140  02206 00000006  IAB                                           00014000
0141  02207 00000033  NØP                                           00014100
0142  02210 00000020  ASC                                           00014200
0143  02211 00000001  RNA                                           00014300
0144  02212 06102277  SMA  TE10                                     
0145  02213 00000020  ASC                                           00014400
0146  02214 00000022  SAZ                                           00014500
0147  02215 00000000  HLT                                           00014600
0148  02216 01102276  LAA  TES7          146314 IN A                00014700
0149  02217 00000032  SNØ                                           00014800
0150  02220 11102222  BRU  *+2                                      00014900
0151  02221 00000000  HLT                                           00015000
0152  02222 00000116  LSL  1                                        00015100
0153  02223 00000032  SNØ                                           00015200
0154  02224 00000000  HLT                                           00015300
0155  02225 01102271  LAA  TES2          ØNES IN A AND B            00015400
```

```
0156  02226 02102271        LBA  TES2                                    00015500
0157  02227 00000036        LØB                                         00015600
0158  02230 35400000        DAC  CATØ                                   00015700
0159  02231 00000000        HLT                                         00015800
0160  02232 12302304 RTN    SPB* CHAR                                   00015900
0161  02233 06102277        SMA  TE10                                   00016000
0162  02234 00000022        SAZ                                         00016100
0163  02235 00000000        HLT                                         00016200
0164  02236 00000005        TAB                                         00016300
0165  02237 00000026        IBS                                         00016400
0166  02240 00000000        HLT                                         00016500
0167  02241 00000004        TBA                                         00016600
0168  02242 06102301        SMA  TE12                                   00016700
0169  02243 00000022        SAZ                                         00016800
0170  02244 02102300        LBA  TE11      200 IN B                     00016900
0171  02245 07102301        MPY  TE12      MULTIPLY BY 400              00017000
0172  02246 06102277        SMA  TE10      SUBTRACT ØNE                 00017100
0173  02247 00000022        SAZ                                         00017200
0174  02250 00000000        HLT                                         00017300
0175  02251 00000004        TBA                                         00017400
0176  02252 00000022        SAZ                                         00017500
0177  02253 00000000        HLT                                         00017600
0178  02254 02102277        LBA  TE10      ØNE IN B                     00017700
0179  02255 00000117        FLA  1         TWØ IN A                     00017800
0180  02256 07102275        MPY  TES6      MULTIPLY BY SEVENS           00017900
0181  02257 06102277        SMA  TE10      SUBTRACT ØNE                 00018000
0182  02260 00000022        SAZ                                         00018100
0183  02261 00000000        HLT                                         00018200
0184  02262 00000004        TBA                                         00018300
0185  02263 05102277        AMA  TE10                                   00018400
0186  02264 06102275        SMA  TES6                                   00018500
0187  02265 00000022        SAZ                                         00018600
0188  02266 00000000        HLT                                         00018700
0189  02267 11102000        BRU  STAR                                   00018800
0190  02270 00000000 TES1   DATA 0                                      00018900
0191  02271 00177777 TES2   DATA -1                                     00019000
0192  02272 00125252 TES3   DATA '125252                                00019100
0193  02273 00052525 TES4   DATA '52525                                 00019200
0194  02274 00100000 TES5   DATA '100000
```

```
0195  02275 00077777 TES6 DATA '77777                              00019400
0196  02276 00146314 TES7 DATA '146314                             00019500
0197  02277 00000001 TE10 DATA 1                                   00019600
0198  02300 00000200 TE11 DATA '200                                00019700
0199  02301 00000400 TE12 DATA '400                                00019800
0200  02302 00000000 LØC1 ZZZ  **                                  00019900
0201  02303 00000000 LØC2 ZZZ  **                                  00020000
0202  02304 55403003 CHAR DAC  RED                                 00020100
0203  03000 70003000       ØRG  '3000                              00020200
0204  03000 11303001 CATØ  BRU* **+1                               00020300
0205  03001 55402232       DAC  RTN                                00020400
0206  03002 00000000       HLT                                     00020500
0207  03003 00000000 *                                             00020600
0208  03003 00000000 RED   ZZZ  **                                 00020700
0209  03004 00000025       SØF                                     00020800
0210  03005 00000033       NØP                                     00020900
0211  03006 00000003       CLA                                     00021000
0212  03007 00000005       TAB                                     00021100
0213  03010 05103020       AMA  PSEV                               00021200
0214  03011 00000025       SØF                                     00021300
0215  03012 00000000       HLT                                     00021400
0216  03013 16103020       AMB  PSEV                               00021500
0217  03014 00000025       SØF                                     00021600
0218  03015 00000000       HLT                                     00021700
0219  03016 01103021       LAA  ØNE                                00021800
0220  03017 11303003       BRU* RED                                00021900
0221  03020 00077777 PSEV  DATA '77777                             00022000
0222  03021 00000001 ØNE   DATA 1                                  00022100
0223  03022 70400000       END                                     00022200
      STAR    02000
      RTN     02232
      TES1    02270
      TES2    02271
      TES3    02272
      TES4    02273
      TES5    02274
      TES6    02275
      TES7    02276
      TE10    02277
```

TE11	02300
TE12	02301
LØC1	02302
LØC2	02303
CHAR	02304
CATØ	03000
RED	03003
PSEV	03020
ØNE	03021

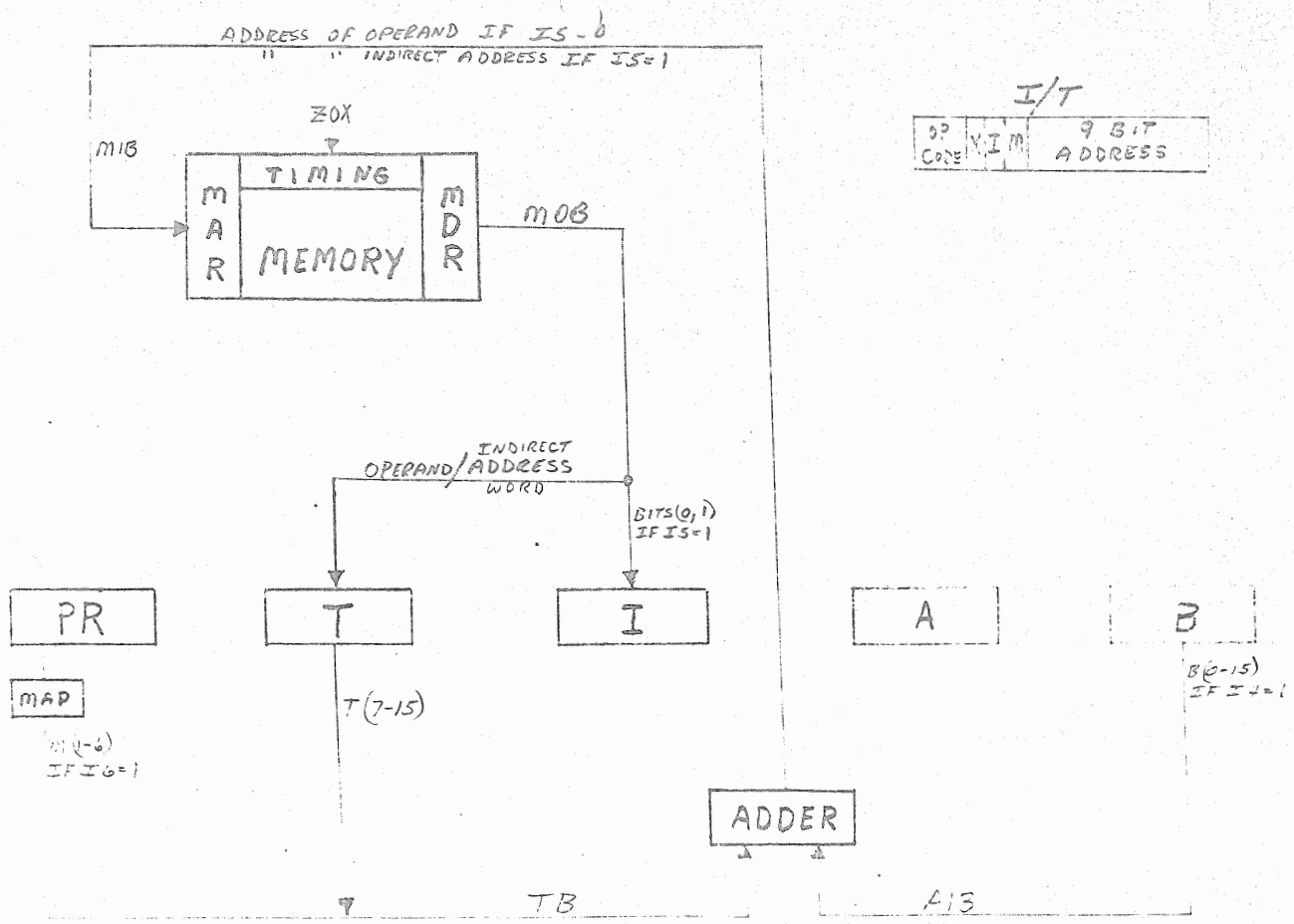


MAJOR STEPS

1. GATE PR TO MEM
2. FETCH INSTRUCTION
3. TRANSFER INSTRUCTION FROM MDR TO I & T.
4. UPDATE PR.

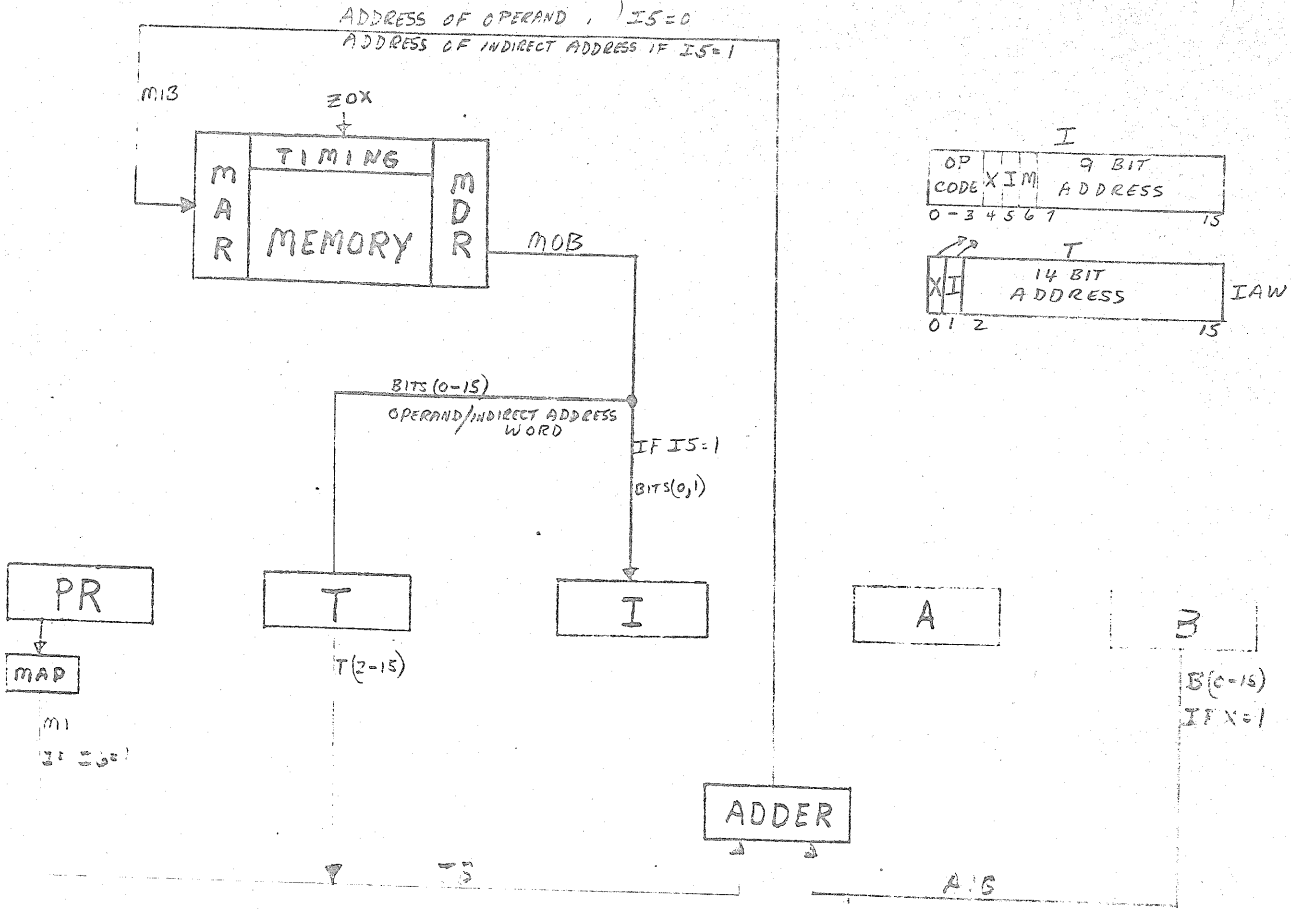
T3

FUNCTIONAL DIAGRAM of INSTRUCTION FETCH



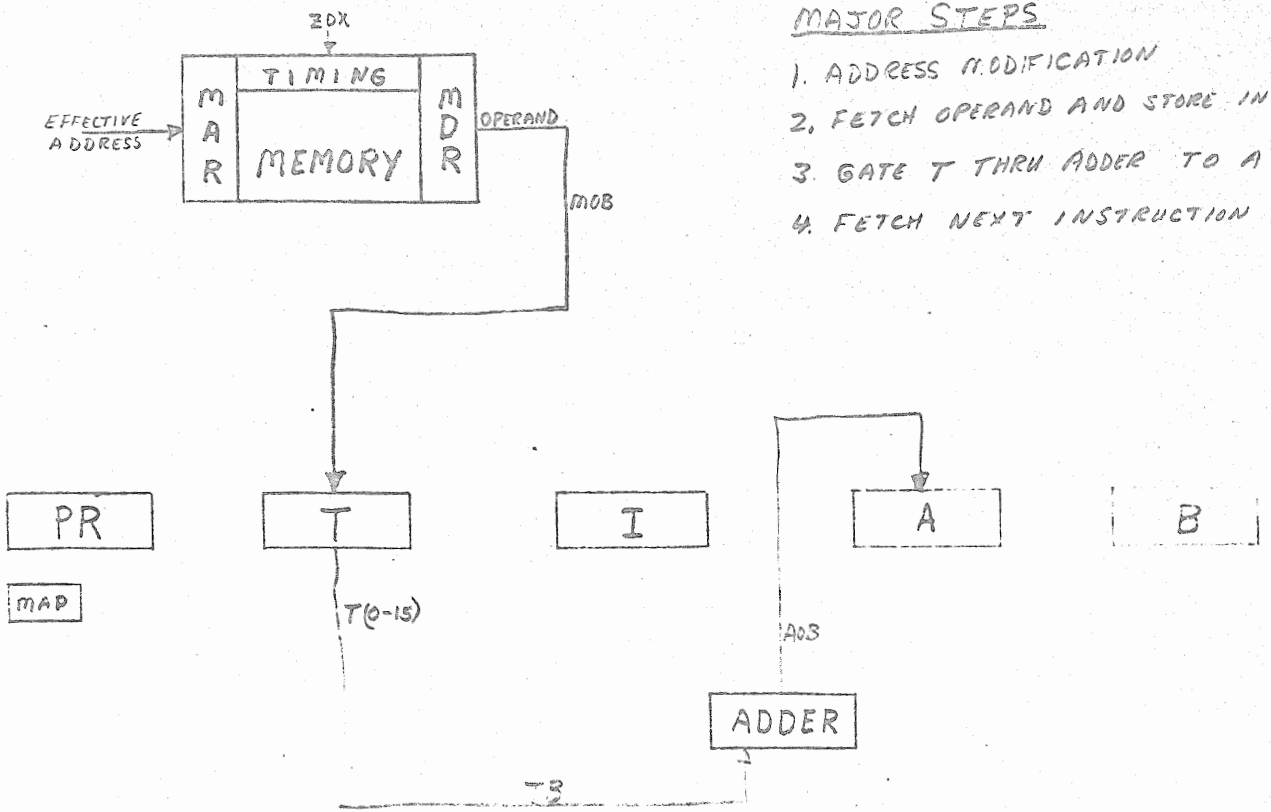
FUNCTIONAL DIAGRAM of MEMORY ADDRESS MODIFICATION (FIRST LEVEL)

2.6



FUNCTIONAL DIAGRAM of MEMORY ADDRESS MODIFICATION

(SECOND AND SUBSEQUENT LEVELS OF INDIRECT ADDRESSING)



MAJOR STEPS

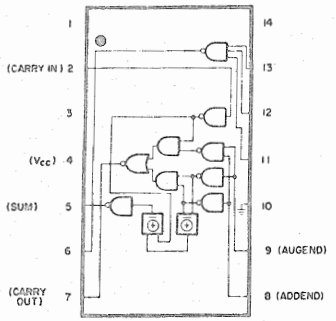
1. ADDRESS MODIFICATION
2. FETCH OPERAND AND STORE IN T
3. GATE T THRU ADDER TO A.
4. FETCH NEXT INSTRUCTION

FUNCTIONAL DIAGRAM of LAA INSTRUCTION EXECUTION

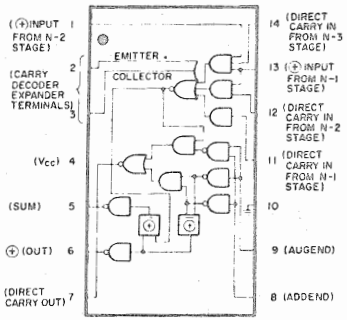
FAST ADDERS
SM10 SERIES SM20 SERIES
SM30 SERIES SM40 SERIES

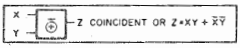
Monolithic Digital Functional Arrays For Military Temp. Range –55°C to +125°C • Industrial 0°C to +75°C

SM-10 SERIES FULL ADDER

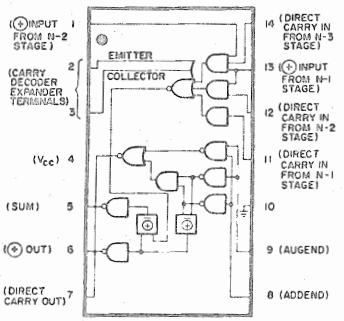


SM-20 SERIES
DEPENDENT CARRY FAST ADDER

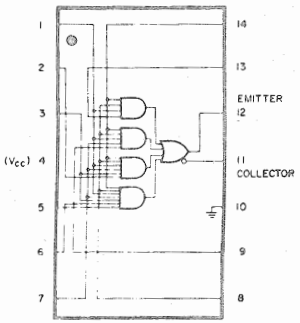




SM-30 SERIES
INDEPENDENT CARRY FAST ADDER



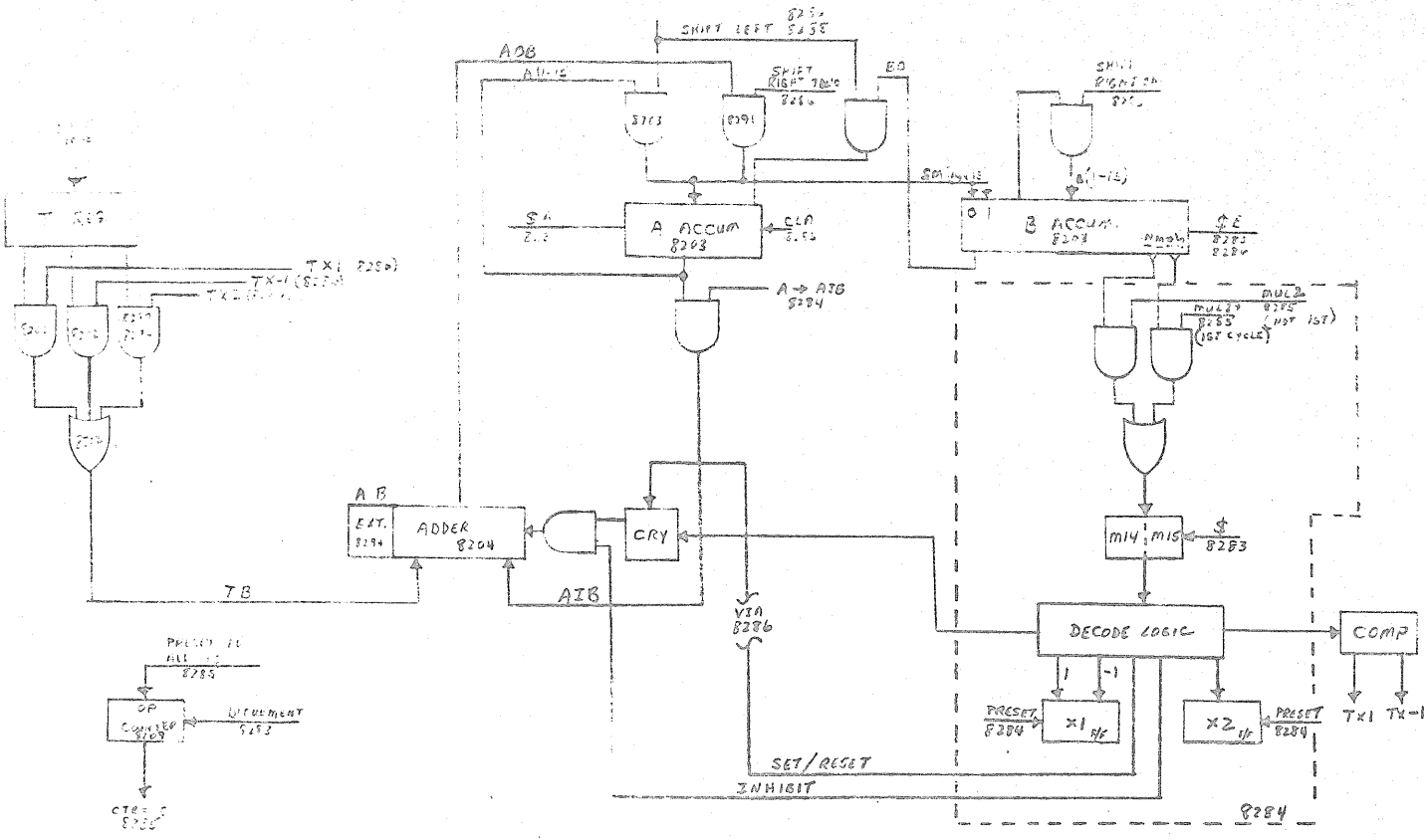
SM-40 SERIES CARRY DECODER



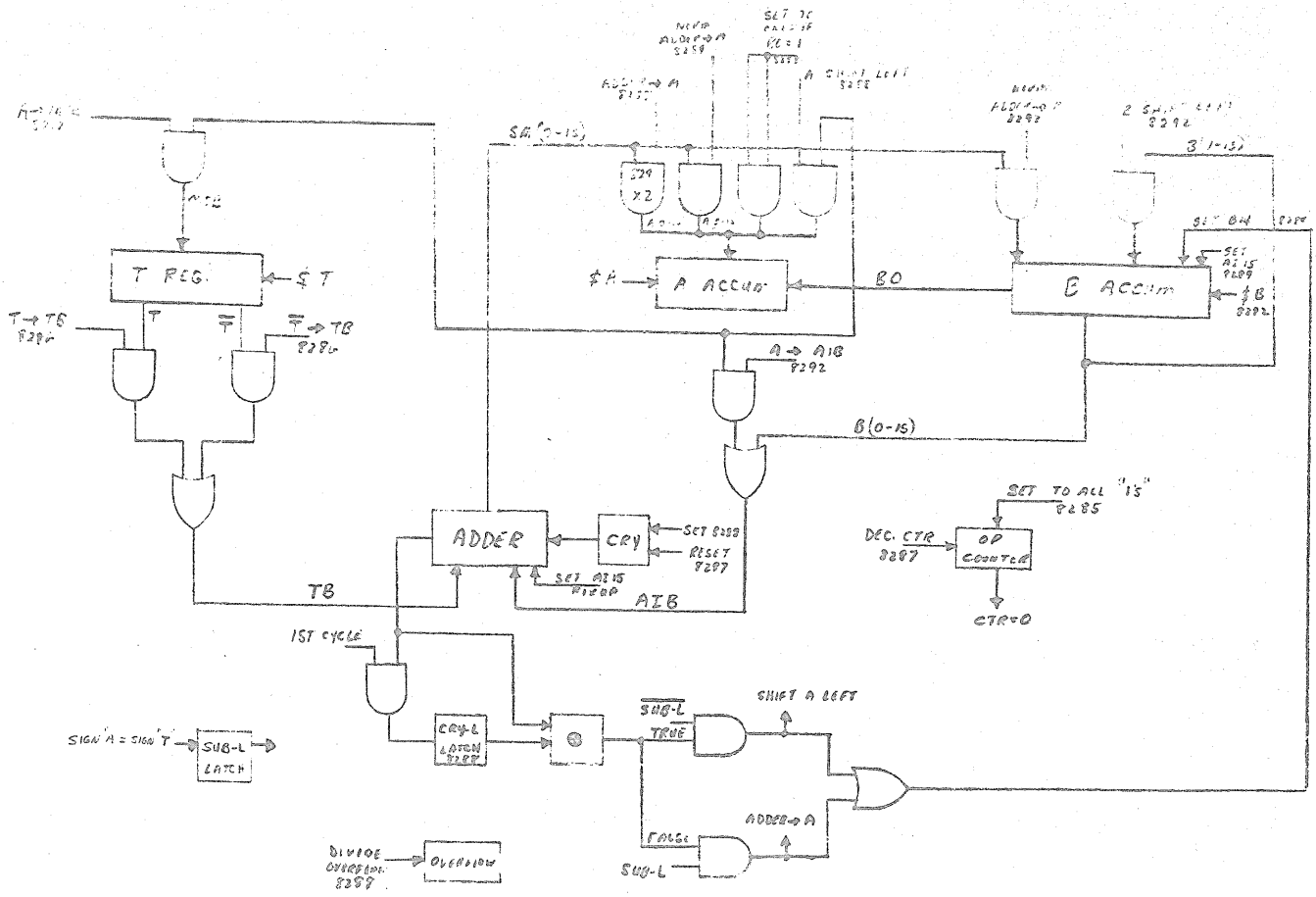
FUNCTIONAL DESCRIPTION

This data sheet specifies Sylvania's Fast Adder Series of Monolithic Digital Functional Arrays designed specifically for implementing high speed binary adder subsystems with "anticipated carry", "ripple carry", or "serial" configurations. All units in the Fast Adder Series are monolithic-silicon, epitaxial, high-level Transistor-Transistor logic integrated circuits having excellent noise immunity, high logic swing, low power consumption, and extremely fast add and carry times. Each circuit in this series operates from a single 5-volt power supply and is available in either the 14-lead ceramic TO-85 flat pack or Sylvania's 14-lead dual in-line ceramic plug-in package. Circuit descriptions and part numbers for military and industrial versions are listed below:

	–55°C to +125°C	0°C to +75°C
Full Adder	SM10, SM11	SM12, SM13
Dependent Carry Fast Adder	SM20, SM21	SM22, SM23
Independent Carry Fast Adder	SM30, SM31	SM32, SM33
Carry Decoder	SM40	SM42



MULTIPLY FUNCTIONAL BLOCK DIAGRAM



DIVIDE FUNCTIONAL BLOCK DIAGRAM

DIVIDE

+7601 = +77 REM = 0

+77

T = 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 = +77

OVFL ('S ADD) = T ≤ A

T_{Φ} = 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 1

LAST CYCLE CORRECTIONS - NONE

	0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 A	0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 B	CO
INIT.	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 1 1 1 1 1 0 0 0 0 0 0 1	
15		0 0 0 1 1 1 1 1 0 0 0 0 0 0 1	0 0 0
14		0 0 1 1 1 1 1 1 0 0 0 0 0 1 0	0 0 0
13		0 1 1 1 1 1 1 0 0 0 0 0 1 0 0	0 0 0
12		1 1 1 1 1 1 0 0 0 0 0 1 0 0 0	0 0 0
11	1	1 1 1 1 1 0 0 0 0 0 1 0 0 0 0	0 0 0
10	1 1	1 1 1 1 0 0 0 0 0 0 1 0 0 0 0	0 0 0
9	1 1 1	1 1 0 0 0 0 0 0 1 0 0 0 0 0	0 0 0
8	1 1 1 1	1 0 0 0 0 0 0 1 0 0 0 0 0 0	0 0 0
7	1 1 1 1 1	0 0 0 0 0 0 1 0 0 0 0 0 0 0	0 0 0
6	1 1 1 1 1 0	0 0 0 0 0 1 0 0 0 0 0 0 0 0	0 0 0
5	1 1 1 1 1 1 0 0	0 0 0 0 1 0 0 0 0 0 0 0 0 0	0 0 0
4	1 1 1 1 1 0 1 0	0 0 0 1 0 0 0 0 0 0 0 0 0 1	0 1 1
3	1 1 1 1 0 1 1 0	0 0 1 0 0 0 0 0 0 0 0 0 1 1	0 1 1
2	1 1 0 1 1 1 0	0 1 0 0 0 0 0 0 0 0 0 1 1 1	0 1 1
1	1 0 1 1 1 1 1 0	1 0 0 0 0 0 0 0 0 0 1 1 1 1	0 1 1
LAST	0 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 1 1 1 1 1	0 1 1
EX	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 1 1 1 1 1 1	
ANS.	0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

RESULT
LAST C

DIVIDE

$-\frac{5}{3} = -1$ & Rem $= +2$

T = 1111111111111101 = −3 in 2's Comp.

OVFL (1ST ADD) = T ≤ A *

* SEE EXCEPTION

LAST CYCLE CORRECTIONS = Q+1 → Q

	A (0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15)	B (C 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15)	15' CA CC Q
INIT.	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 C	0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0	
15	0 ← 0	0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1	0 0 1
14		0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 1	0 1
13		0 0 0 0 0 0 0 0 0 0 0 1 0 1 1 1	0 1
12		0 0 0 0 0 0 0 0 0 0 1 0 1 1 1 1	0 1
11		0 0 0 0 0 0 0 0 0 1 0 1 1 1 1 1	0 1
10		0 0 0 0 0 0 0 0 1 0 1 1 1 1 1 1	0 1
9		0 0 0 0 0 0 0 1 0 1 1 1 1 1 1 1	0 1
8		0 0 0 0 0 0 1 0 1 1 1 1 1 1 1 1	0 1
7		0 0 0 0 0 1 0 1 1 1 1 1 1 1 1 1	0 1
6		0 0 0 0 1 0 1 1 1 1 1 1 1 1 1 1	0 1
5		0 0 0 1 0 1 1 1 1 1 1 1 1 1 1 1	0 1
4		0 0 1 0 1 1 1 1 1 1 1 1 1 1 1 1	0 1
3		0 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1	0 1
2		0 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1	0 1
1	1 0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0 1
LAST	1 0 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0 1 0
EX	0 1 0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	← RESULT OF LAST CYCLE
ANS.	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1	

DIVIDE

103467 ÷ 327
−241

T = 1111111101011111 = −241

$\overline{T_{(2)}}$ = 0000000101000001 = 241

LAST CYCLE CORRECTIONS:
IF LAST ADD = 0 THEN Q#1 → Q

	A (0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15)	B (0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15)	C.O. Q
INIT.	1111111111111110	1111000110010001	
15	1111111111111110	1111000110010001	1 1 0
14	1111111111111101	1110001100100010	1 1 0
13	1111111111111011	1100011000100100	1 1 0
12	1111111111110111	1000110001001000	1 1 0
11	1111111111101111	0001100010010000	1 1 0
10	1111111111011110	0011000100100000	1 1 0
9	1111111110111100	0110001001000000	1 0
8	1111111101111000	1100010010000000	1 1 0
7	1111111011110001	1000100100000000	1 0 1
6	1111110010010101	0001001000000001	1 0 1
5	1111101100010011	0010010000000011	1 1 0
4	1111011000100010	0100100000000110	1 0 1
3	1110110001100101	1001000000001101	1 1 0
2	1101100011001010	0010000000011010	1 0 1
1	1011000110010101	0100000000110101	1 0 1
LAST	1010001100101110	1000000001101011	1 1 0
EX	0000000000000000	0000000001101011	← RESULT OF LAST CYCLE
ANS	0000000011010111	0000000001101011	

Table 3-2. Divide Algorithm

Sign T	Sign A	Div Add	Div Sub	Carry Out First Add	Carry Out	$\overline{\text{Carry Out}}$	Corrections	Overflow First Add
-	+	No	Yes $\overline{T}$→TB 1→CRY	0	/T/≤/A/ Process 1→Q	/T/>/A/ Shift 0→Q	None (DIV, IAB)	/T/≤/A/
-	-	No	Yes $\overline{T}$→TB 1→CRY	1	/T/≥/A/ Shift 0→Q	/T/<A/ Process 1→Q	Last Cycle (DIV, IAB) 1) /T/ = /A/ → 0→R, Q + 1→Q 2) /T/ ≠ /A/ → None	1) /T/<A/ 2) T = A, B = 0, ANS FSN ⇒ OVFL
-	+	Yes T→TB	No	0 "1" (IF T = A B = 0, ANS FSN)	/T/≤/A/ Process 0→Q	/T/>/A/ Shift 1→Q	Last Cycle (DIV, IAB) Q + 1→Q	1) /T/≤/A/ Exception T = A, B = 0, ANS FSN ⇒ INH OVFL, Clear A each cycle
+	-	Yes T→TB	No	1	/T/≥/A/ Shift 1→Q	/T/<A/ Process 0→Q	Last Cycle (DIV, IAB) 1) /T/ = /A/ ⇒ 0→R 2) /T/ ≠ A/ ⇒ Q + 1→Q	/T/<A/

Process = Load sum to A and shift AB
1 → Q = Set LSB of B to ONE
0 → Q = Set LSB of B to ZERO
0 → R = Set remainder to ZERO
Q + 1→ Q= Add carry during IAB

PROJECT MEMORY TIMING

NOTE.

MAIN FRAME TIME

SOURCE DWG. NUMBER	FUNCTIONAL SIGNAL NAME	MNEMONIC
8226	CLEAR MAR	EEB
8227	LOAD MAR	DDU/DDV
8216	CYCLE MEM.	ZØX
8216	CLEAR MDR	ZØY
8271	READ SWITCH	
8271	READ CURR. DR.	
8959	X READ	
8959	Y READ	
8216	UNLOAD	
8226	$MDR *	EEA *
8216	INHIBIT	
8271	WRITE SWITCH	
8271	WRITE CURR. DR.	
8959	X WRITE	
8959	Y WRITE	

10 *

NOTE: EEA ($MDR) Generated during E1 cycle of A STORE INSTRUCTION ONLY.

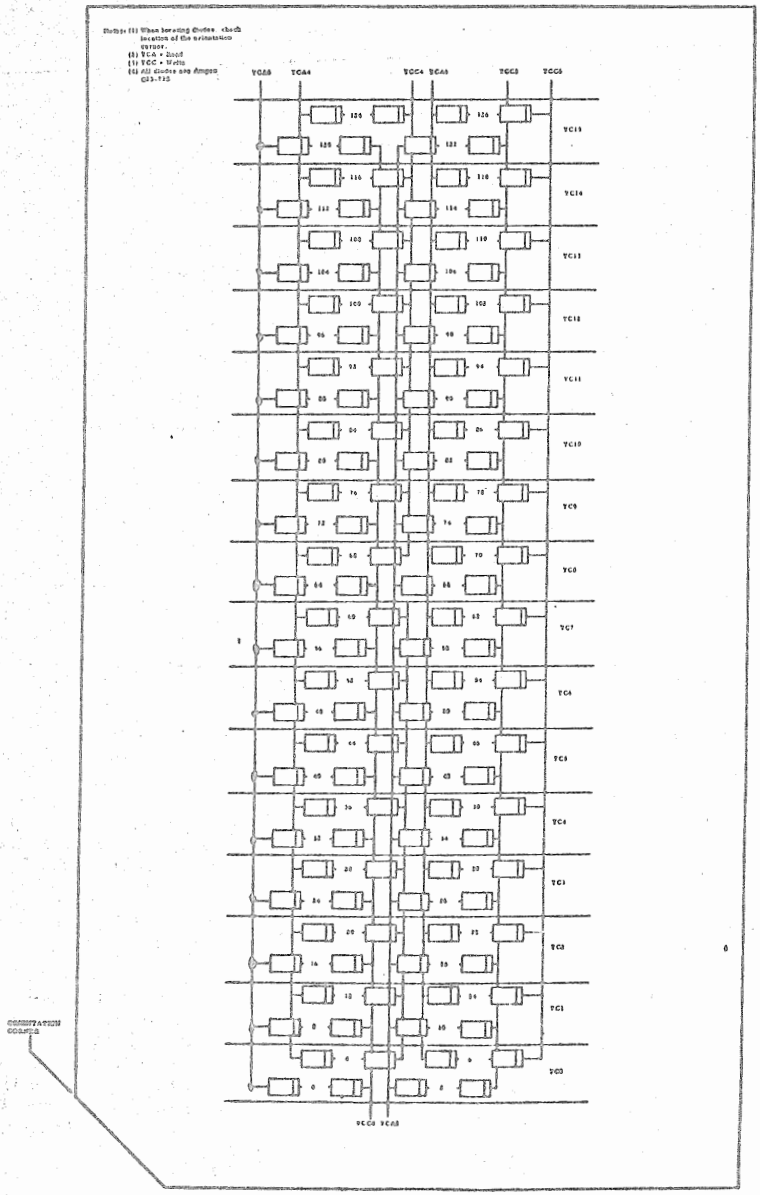


Figure 5-2. Diode Location Chart for Y Even Decode Board Assembly (Top Board)

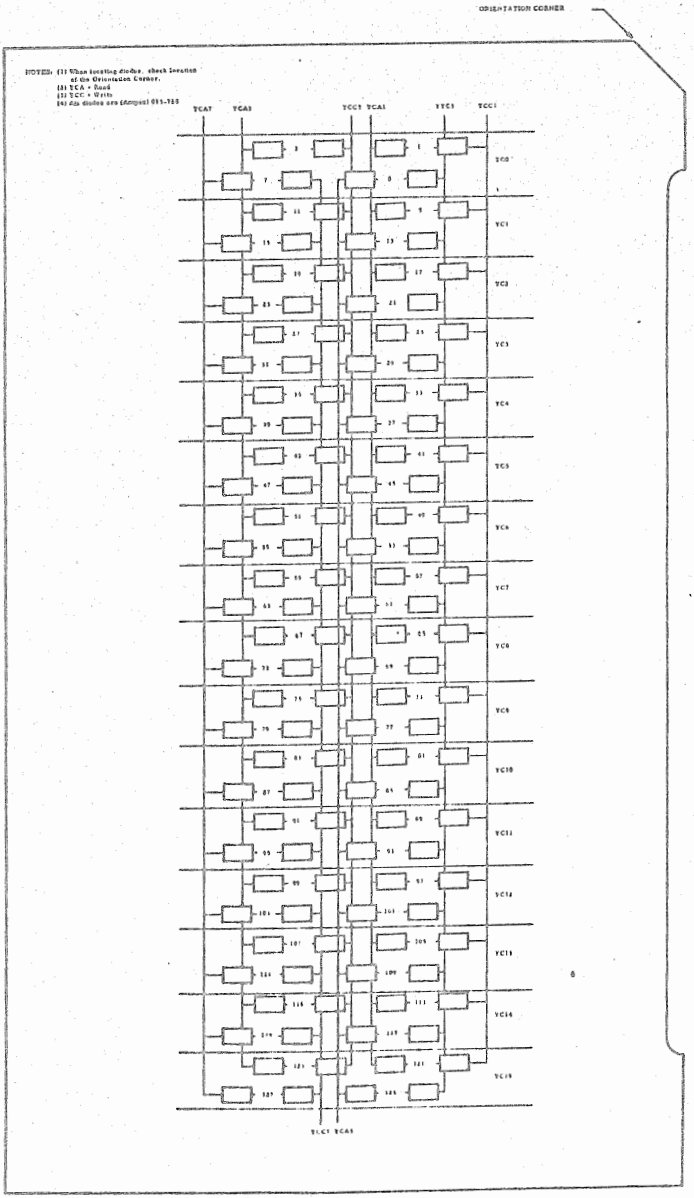


Figure 5-3. Diode Location Chart for Y Odd Decode Board Assembly (Middle Board)

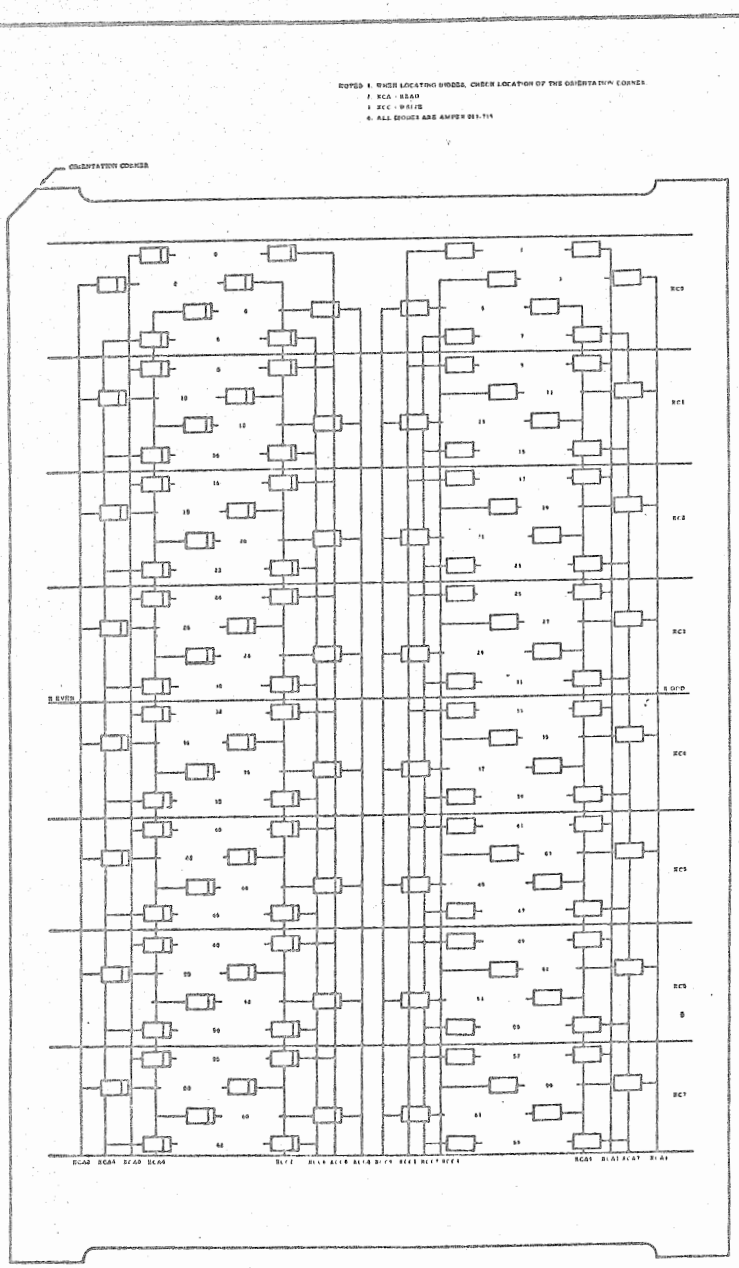
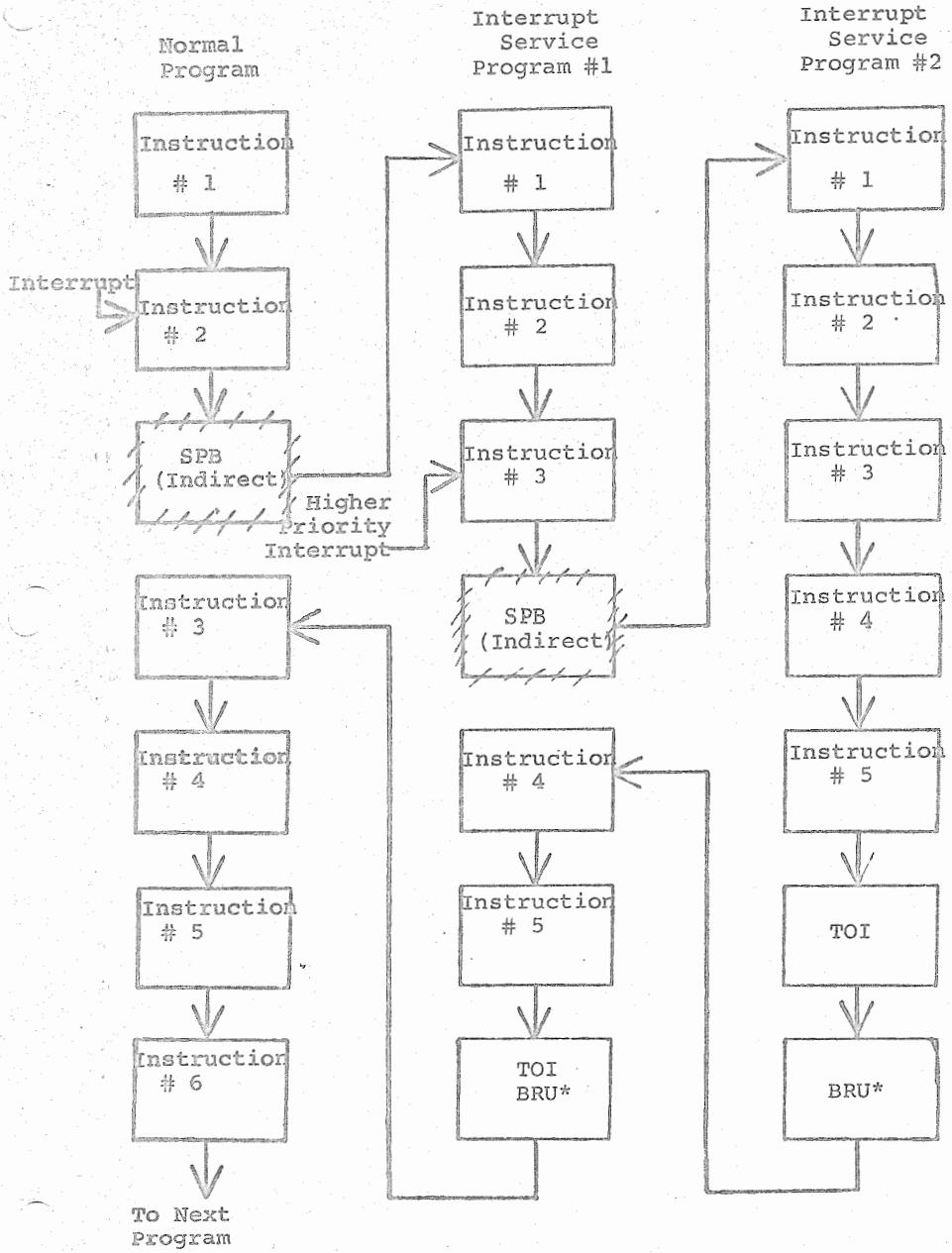
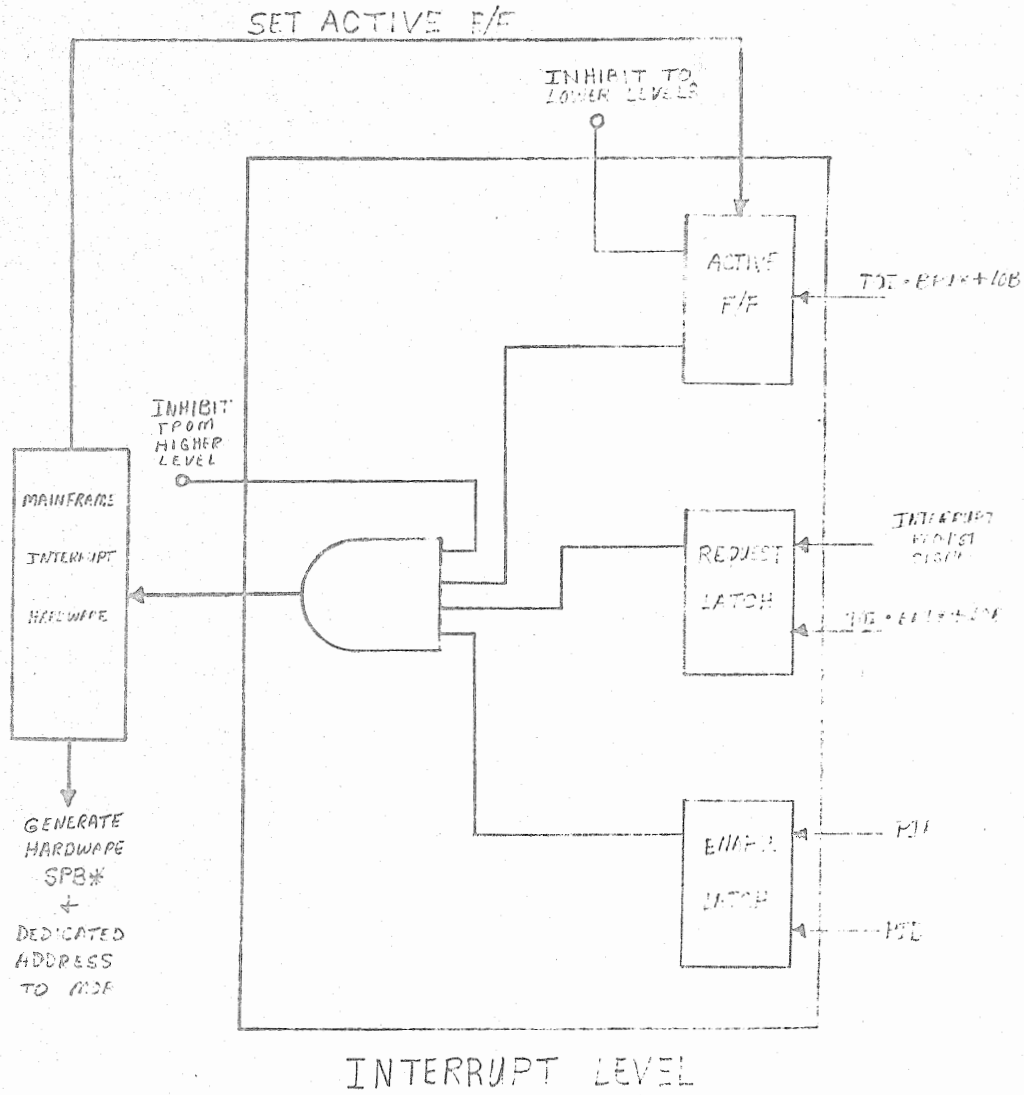


Figure 5-4. Diode Location Chart for X Decode Board Assembly (Bottom Board)

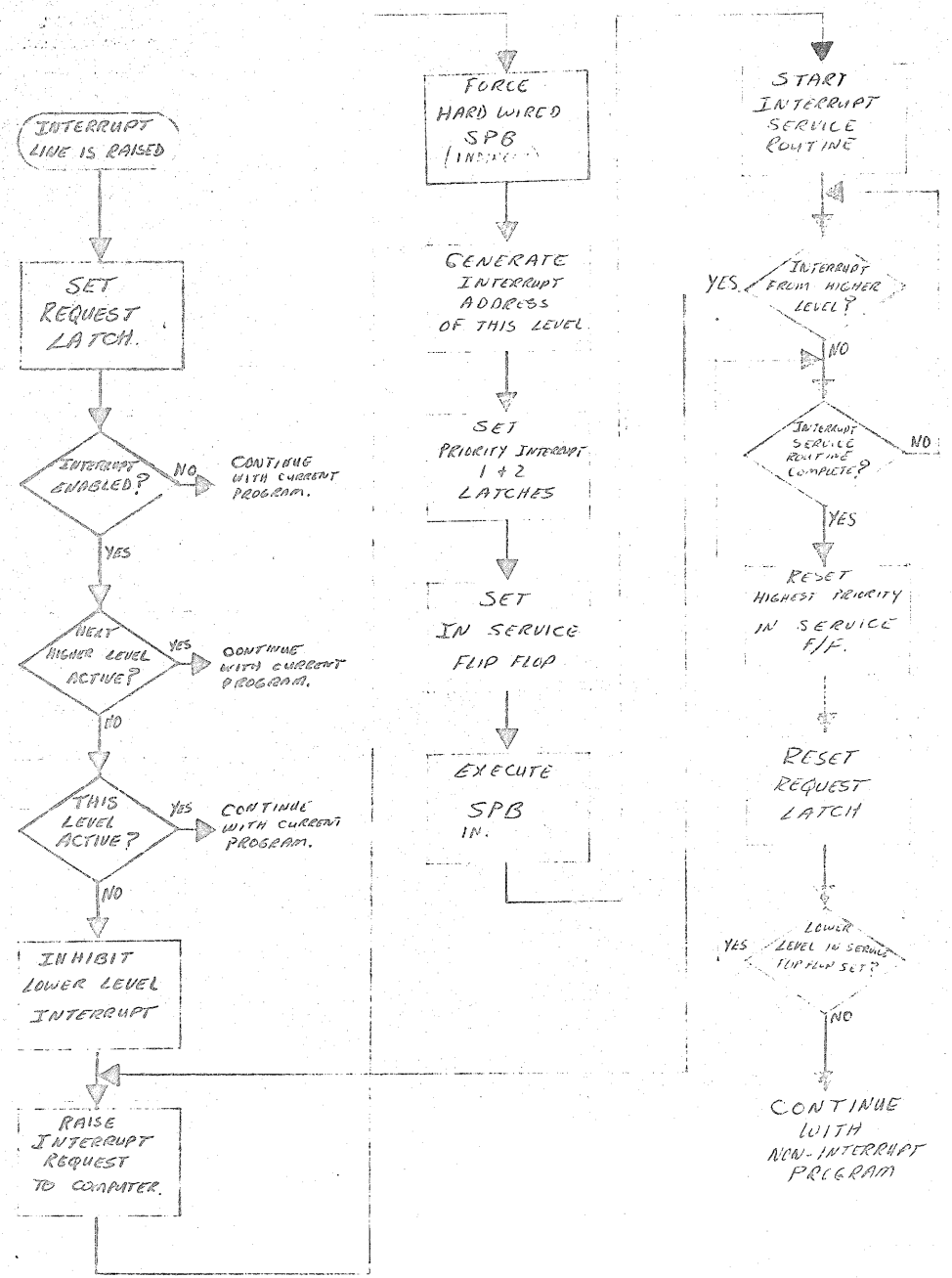
PRIORITY INTERRUPT PROCESSING





PRIORITY INTERRUPT SYSTEM

INTERRUPT PROCESSING SEQUENCE

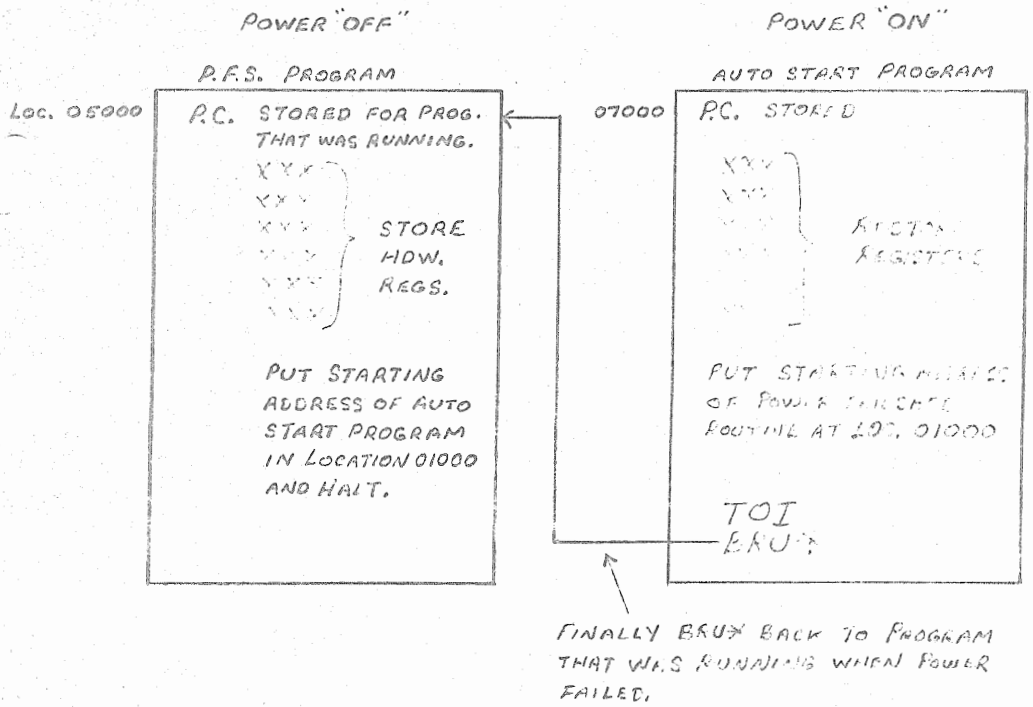


AUTO RESTART & POWER FAILSAFE

PURPOSE: PROVIDES THE CAPABILITY OF THE COMPUTER TO RETURN TO A RUN CONDITION AUTOMATICALLY IN THE EVENT THAT, AFTER BEING LOST, POWER IS RESTORED.

WHEN A POWER FAILURE OCCURS AN INTERRUPT IS GENERATED. PRESENT P.C. IS STORED AND DEDICATED ADDRESS 01000 IS GENERATED.

MEM. LOCATION 01000 | STARTING ADDR. OF POWER FAILSAFE ROUTINE | ← (05000)



NOTE: TWO INTERRUPTS OCCUR, ONE WHEN POWER GOES DOWN AND WHEN POWER COMES ON. THE P.F. SIGNAL CAUSES AN INTERRUPT WHEN GOING DOWN AND THE POWER-UP D.C. RESET CAUSES AUTO-RESTART INTERRUPT GENERATION.

810a Auto Start Option

I. Auto start option enables the computer to resume operation when A. C. power is applied after a power failure if 1) The computer was in the run mode and 2) certain programming techniques are observed prior to, during and after power loss.

This option consists of adding P. C. cards 160-100124 (Loc. 23A 1R1), 160-083240-002 (Loc. 25B 1R1); changing P. C. card in location 9G 1R1 from 8296-001 to 8296-002; and adding wire list W. L. 83240 to 1R1 plane.

II. Drawings 824201, 824501, 829602, 160-083186, 160-083240-002, 160-100124.

III. Adjustments
Note: 29 Pin card extender (8013), Variac, and Weston 0-150 V. A. C. meter are required to perform adjustments.

Verify that P. C. cards 8245 (Loc. 10G 1R1) and 8296 (Loc. 9G 1R1) adjustments are correct as described in 810a tech. manual 303-095000-002 paragraphs 4-70 through 4-73 and paragraphs 4-82 through 4-83. Paragraph 4-84 need not be performed as auto-start option does not use output from 8296 pin 5.

IV. Theory of Operation:

P. C. card 160-083240 contains a relay (K1) which is a bi-stable relay i.e. the armature remains in the position to which it was last operated until sufficient current of opposite polarity is applied. When the computer is in the run mode, the term EEG on pin I6 is ground which causes Q1 and Q4 to conduct. This current flow causes K1 to set which provides continuity between pin 12 and pin 26.

Two types of power failure may occur, A) complete loss of A. C. and B) a power dip which is defined as A. C. voltage being less than 95 Volts and greater than 0 Volts.

A. Sequence of events for complete power loss:

1. When A. C. power drops to 95 Volts, P. C. card 8296 generates + voltage OFF + ON pin 6. This signal at next CL11 time generates interrupt request OFFZ and starts 500 microsecond delay on P. C. 8245. The term OFFZ sets PFS interrupt on 824201. When active F. F. on 8242 P. C. is set, the term AFCO+ on pin 24 goes to + voltage. This term is applied to 160-083240 and prevents K1 from resetting. The computer enters the power down interrupt routine and performs necessary housekeeping functions. After 500 microsecond delay on P. C. 8245 times out, "turn off memory" Term OZOF+ is generated on 8245 pin 23. This signal gates off the data saver P. C. card8639-2 in each memory module (refer to 8K memory module logic diagram 53103). The computer remains in this state while A. C. and D. C. voltages drop to zero.

2. When A. C. is applied to computer, the term ZWW+ is immediately generated on P. C. 83240. This, inturn, generates ICB1 thru ICB4 and ZY4+ terms. These are initial condition pulses that reset all critical latches, flip-flops, registers and force a "HALT" condition. This clearing condition exists for approximately 3.2 seconds. ICB2+ is applied to P. C. 83240 to prevent K1 armature from changing position. At the trailing edge of ZWW+, a 5 microsecond pulse (OROT+) is produced at pin 26 of 83240 P. C. via pin 13 & 12 ~~and~~ of K1. This pulse generates an interrupt request (OFFZ) on P. C. 8245 pin 20 and generates a start pulse (Res+CP) on P. C. 160-083186. The computer enter the "run" mode, an interrupt traps to the power up interrupt routine which restores registers and computer operation is resumed.

B. Sequence of events for A. C. power Dip:

1. When the A. C. voltage drops below 95 volts, the term (OFF) is gated to P. C. 100124 to remove the +16V supplied to P. C. 83240 via Q1 and R4 on 100124. Removing +16V from the junction point of C1, R6 on 83240 allows C1 to discharge through CR4 (CR1 is ommitted on 83240-002).

   The flip-flop (PUD+) is set on P. C. 100124 by the decrease of +16 Volts which is caused by A. C. voltage drop. The term PUD+ is gated to the 83240 card to prevent K1 armature from changing positions due to unreliable voltage levels of AFCO+

2. When the A. C. voltage rises above 105 volts, the term (OFF) at pin 14 of 100124 P. C. card goes positive allowing +16 volts to be applied to the junction of C1, R6 on 83240 card which in turn produces ZWW+. Refer to paragraph IV A.2 for sequence of events. The ICB4+ term resets the PUD+ flip-flop and computer operation resumes.

V. Wire List 83240 A

Remove	10G08	09G05			
Add	FROM	TO	FROM	TO	
	25B04	25B24	25B17	10G08	
	25B08	25B18	25B15	05G25	22ga. Red
	10G26	08F08	04K21	05H25	22ga. Red
	08F08	25B26	23A10	25B06	
	25B16	03D24	25B06	25B20	
	25B10	25B14	23A20	25B21	
	25B08	01B15	23A14	09G10	
	25B04	23D16	02B13	23A08	
	25B13	25B12	23A26	25B15	

. Short program to verify proper operation of auto-start option

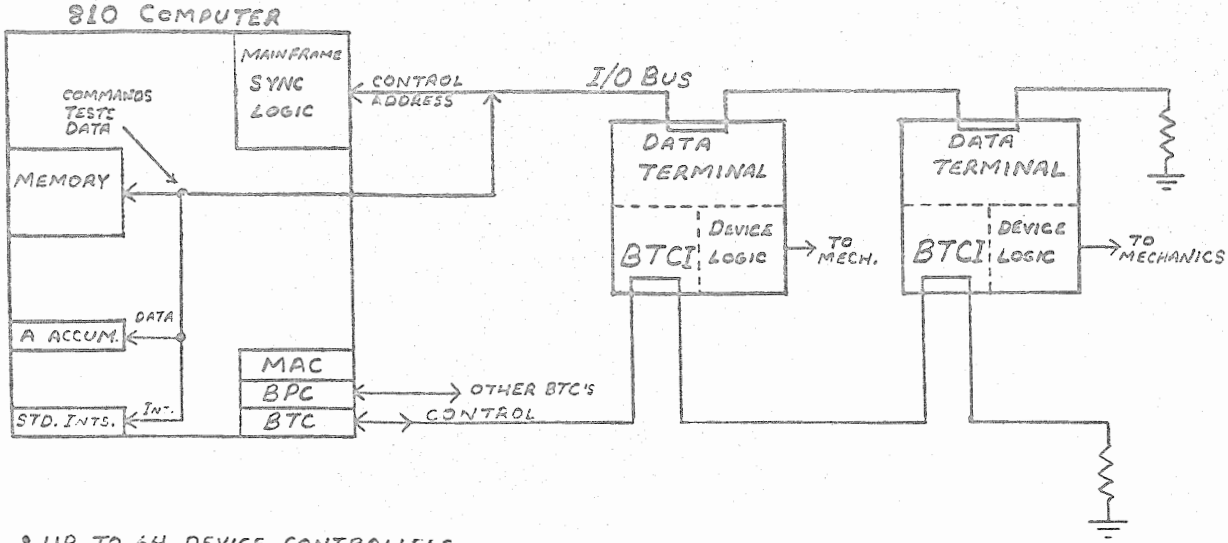
Loc.	Octal Code	Mnemonic
50	010053	LAA'53
51	032054	STA I, '54
52	110052	BRU *
53	000055	'55
54	001000	'1000
55	000000	X--X
56	010055	LAA'55
57	030072	STA'72
60	010063	LAA'63
61	032064	STA I, '64
62	110062	BRU *
63	000065	'65
64	001000	'1000
65	000000	X--X
66	010053	LAA'53
67	032054	STA I, '54
70	000035	TOI
71	112072	BRU I, '72
72	000000	X--X

VII. Program will continuously type message "turn off 810-then on-program will resume" Frequently an extra character will be typed as power is dropping due to unreliable TTY operation, this should be ignored.

Loc.	Octal Code	Mnemonic	Remarks
100	010140	LAA'140	Start of program
101	032141	STA I, '141	
102	010142	LAA'142	
103	030147	STA'147	
104	020143	LBA'143	
105	130101	CEU	
106	002000	DAC	
107	012147	LAA I, '147	
110	170001	AOP	
111	110110	BRU *-1	Unit not ready
112	001016	LSL 8, 0	
113	170001	AOP	
114	110113	BRU *-1	Unit not ready
115	140147	IMS'147	
116	000026	IBS	
117	110107	BRU'107	
120	110100	BRU'100	
121	000000	X--X	Power down routine
122	030144	STA'144	Temp 1
123	040145	STB'145	Temp 2
124	010146	LAA'146	
125	032141	STA I '141	
126	110126	BRU *	
127	000000	X--X	Power up routine
130	010140	LAA'140	
131	032141	STA I '141	

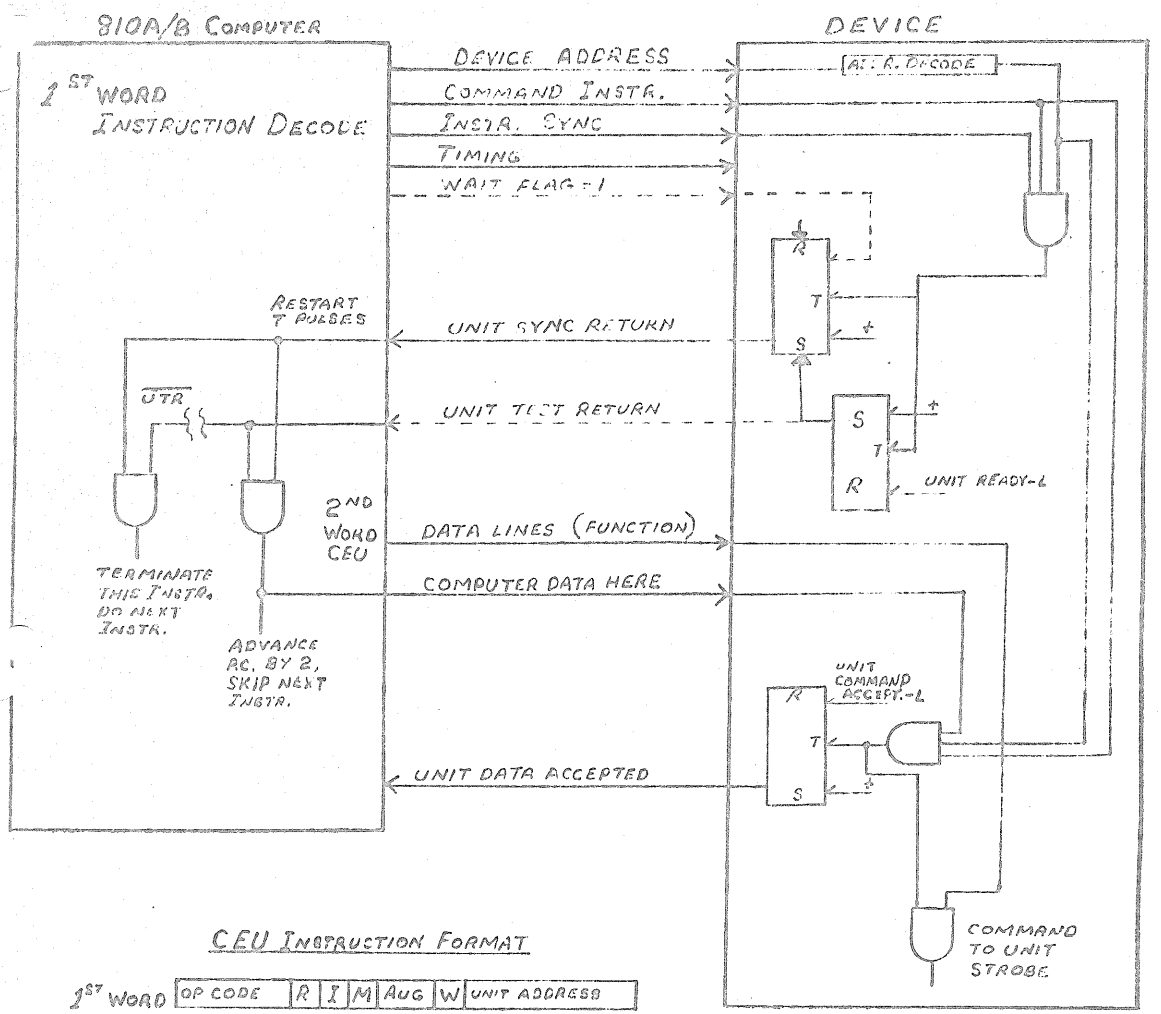
Loc.	Octal Code	Mnemonic	Remarks
132	010144	LAA '144	Temp 1
133	020145	LBA '145	Temp 2
134	130101	CEU W, 1	
135	002000	DAC	
136	000035	TOI	
137	112121	BRU I, '121	Last addr. before P. F. S.
140	000121		1st Loc. of power down
141	001000		P. F. S./Auto-start interr. loc.
142	000150		Loc. of 1st data word
143	177752		No. of data words
144	000000		Temp 1
145	000000		Temp 2
146	000127		1st Loc. of power up
147	000000		Loc. of current data word
150	106612	DATA	C/R L/F
151	152325		T U
152	151316		R N
153	120317		Sp O
154	143306		F F
155	120270		Sp 8
156	130660		1 0
157	120255		Sp -
160	152310		T H
161	142716		E N
162	120317		Sp O
163	147255		N -
164	120320		Sp P
165	151317		R O
166	143722		G R
167	140715		A M
170	120327		Sp W
171	144714		1 L
172	146240		L Sp
173	151305		R E
174	151725		S U
175	146705		M E

I/O STRUCTURE

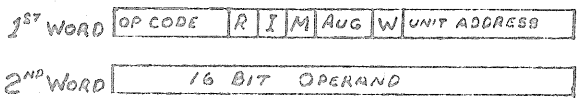


- UP TO 64 DEVICE CONTROLLERS
- 16 DEVICES MAXIMUM ON ONE SET OF CABLE DRIVERS AND TERMINATORS
- COMMAND DEVICE - CEU
- TEST DEVICE - TEU
- INPUT DATA TRANSFERS - AIP / MIP
- OUTPUT DATA TRANSFERS - AOP / MOP

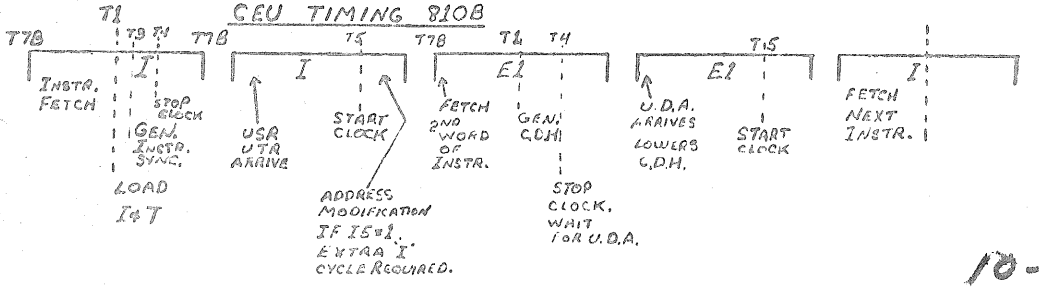
CEU Instruction Execution



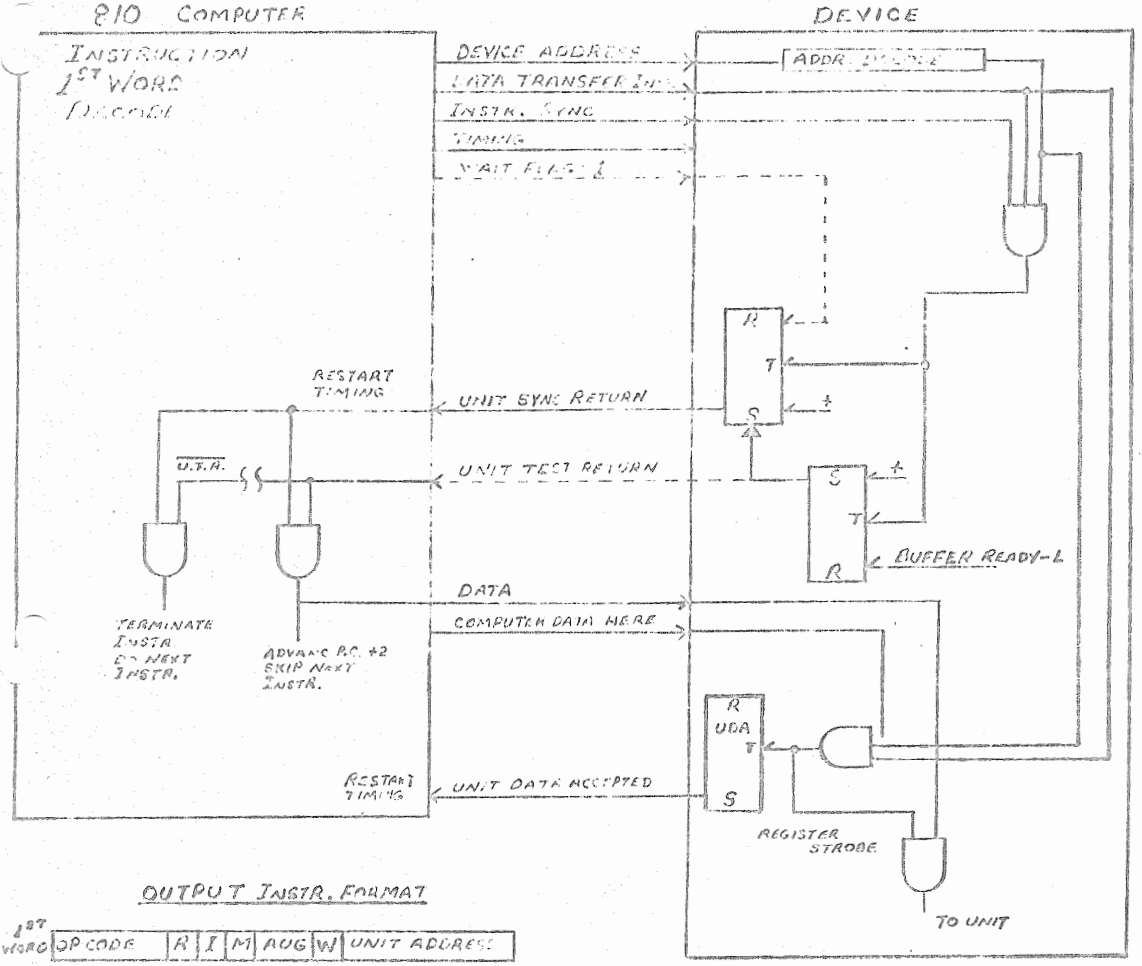
CEU Instruction Format



CEU Timing 810B



OUTPUT INSTRUCTION EXECUTION



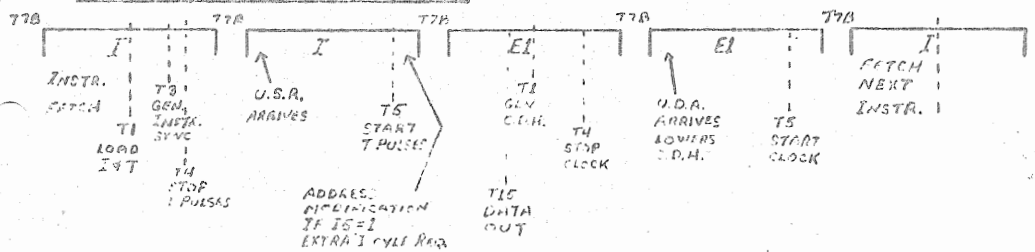
OUTPUT INSTR. FORMAT

1ST WORD	OP CODE	R	I	M	AUG	W	UNIT ADDRESS	
2ND WORD (MOP ONLY)	16 BIT OPERAND							

NOTE: UNIT SYNC RETURN & UNIT DATA ACCEPTED START COMPUTER T PULSES.

1. UNIT SYNC RETURN & UNIT TEST RETURN, DO NEXT INSTR.
2. UNIT SYNC RETURN & UNIT TEST RETURN, SKIP NEXT INSTR.

MOP & AOP INSTR. TIMING 810R



810A/B COURSE

Worksheet 1

1. List the four major units of the 810A Computer.

   a. _____

   b. _____

   c. _____

   d. _____

2. Describe the functions of the memory unit.

   _____

3. Describe the functions of the control unit.

   _____

4. Describe the functions of the arithmetic unit.

   _____

5. Describe the functions of the input/output unit.

   _____

6. How is information transferred between the four major units of the 810A Computer?

   _____

7. How are negative numbers expressed?

   _____

8. Which units form the mainframe?

   _____

9. How many words may be stored in a memory module?

   _____

10. How many bits may be stored in one location of memory?

_____

11. What is the minimum number of memory modules in a memory unit?

_____

12. What is the maximum number of memory modules in a memory unit?

_____

13. List the four elements which comprise each memory module.

a. _____

b. _____

c. _____

d. _____

14. What types of information are stored in memory?

a. _____

b. _____

15. How many memory locations may be addressed by the 13 bit Memory Address Register?

_____

16. How many memory locations may be addressed by the 15 bit Program Counter?

_____

17. What type of information is contained in the memory locations addressed by the Program Counter?

_____

18. What is an instruction?

_____

19. What is an operand?

_____

20. What arithmetic functions may be performed by the 810A Computer?

a. _____

b. _____

c. _____

d. _____

21. What logical functions may be performed by the 810A Computer?

a. _____

b. _____

22. Which bits of any instruction describe the operation code?

_____

23. List the types of instructions.

a. _____

b. _____

c. _____

d. _____

e. _____

f. _____

g. _____

h. _____

24. What do the XIM bits mean in instructions using the memory reference format?

a. _____

b. _____

c. _____

25. What is operand address indexing?

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26. What is preindexing?

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27. What is postindexing?

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28. What is indirect addressing?

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29. What is address mapping?

Map + Index 1st.
Indirect 2nd.

810A/B SOFTWARE COURSE

Instruction Set Worksheet 2

1. Given: Instruction=050505
(00505)=007327
(A)=050450

(A) 057777

What will be contained in the A accumulator after execution of the above instruction?

2. Given: Instruction=160606
(00606)=177337
(B)=000441

(B) = 000000

What will be contained in the B accumulator after execution of the above instruction?

3. Given: Instruction=060606
(00606)=177337
(A)=050450

(A) = 051111

What will be contained in the A accumulator after execution of the above instruction?

4. Given: Instruction=070707
(00707)=000020
(A)=050450
(B)=000331

A) = 000000
B) = 000020

What will be contained in the A & B accumulators after execution of the above instruction?

5. Given: Instruction=103010
Instruction@11111
(11010)=030020
(30020)=000666
(A)=066600
(B)=000000

A = 000111
B = 000010

What will be contained in the A & B accumulators after execution of the above instruction?

6. Given: Instruction=000001
(A)=066600
(B)=066600

(A) = 066601

What will be contained in the A accumulator after execution of the above instruction?

7. Given: Instruction=011011
Instruction@10645
(00011)=124242
(10011)=153535

What will be contained in the A accumulator after execution of the above instruction?

8. Given: Instruction=022022
Instruction@10646
(11111)=022000
(00022)=011111
(10022)=022222
(22022)=033333

What will be contained in the B accumulator after execution of the above instruction?

9. Given: Instruction=033033
Instruction@10647
(B)=003333
(10033)=021111
(00033)=004444

Where will the contents of the A accumulator be stored after execution of the above instruction?

10. Given: Instruction=040404
Instruction@10650

Where will the contents of the B accumulator be stored after execution of the above instruction?

11. Given: Instruction=111111
Instruction@10651

What is the address of the next instruction to be executed?

12. Given: Instruction=121212
Instruction@10652

What is the address of the next instruction to be executed?

13. Given: Instruction=141414
Instruction@10653
(10414)=177776

10413

What is the address of the next instruction to be executed?

14. Given: Instruction=151515
Instruction@10655
(10515)=065217
(A)=047301

10515

What is the address of the next instruction to be executed?

15. Given: Instruction=130413
Instruction@10660
Switches=040404

10662

What is the address of the next instruction to be executed?

16. Given: Instruction=000026
Instruction@10662
(B)=177775

10663

What is the address of the next instruction to be executed?

17. Given: Instruction=000021
Instruction@10664
(A)=177775

10665

What is the address of the next instruction to be executed?

18. Given: Instruction=000036
Instruction@10666
(10667)=030344

030344

What is the address of the next instruction to be executed?

19. Given: Instruction=000027
(A)=050450
(B)=000441

(A) 000440
(B) = 000441

What will be contained in the A & B accumulators after execution of the above instruction?

20. Given: Instruction=000030
(A)=050450
(B)=000441

A = 050451
B = 000441

What will be contained in the A & B accumulators after execution of the above instruction?

21. Given: Instruction=000002
(A)=050450
(B)=000441

A - 127330

What will be contained in the A accumulator after execution of the above instruction?

22. Given: Instruction=000020
(A)=050450

(A) - 150450

What will be contained in the A accumulator after execution of the above instruction?

23. Given: Instruction=000034
(A)=050450

(A) - 050450

What will be contained in the A accumulator after execution of the above instruction?

24. Given: Instruction=000003
(A)=050450

A - 000000

What will be contained in the A accumulator after execution of the above instruction?

25. Given: Instruction=000004
(A)=050450
(B)=000441

(A) - 000441
(B) - 000441

What will the A & B accumulators contain after execution of the above instruction?

26. Given: Instruction=000005
(A)=050450
(B)=000441

(A) - 050450
(B) - 050450

What will the A & B accumulators contain after execution of the above instruction?

27. Given: Instruction=000006
(A)=050450
(B)=000441

(B) 050450
(A) 000441

What will the A & B accumulator contain after execution of the above instruction?

(A) 061211
(B) 000441

28. Given: Instruction=000510
(A)=050450
(B)=000441

What will the A & B accumulators contain after execution of the above instruction?

A = 000504
B = 050004

29. Given: Instruction=000612
(A)=050450
(B)=000441

What will the A & B accumulators contain after execution of the above instruction?

A = 000242
B = 000441

30. Given: Instruction=000715
(A)=050450
(B)=000441

What will the A & B accumulators contain after execution of the above instruction?

A = 022400
B = 000441

31. Given: Instruction=000511
(A)=050450
(B)=000441

What will the A & B accumulators contain after execution of the above instruction?

024002
020400

32. Given: Instruction=001017
(A)=050450
(B)=000441

What will the A & B accumulators contain after execution of the above instruction?

A = 450000
B = 000441

33. Given: Instruction=000716
(A)=050450
(B)=000441

What will the A & B accumulators contain after execution of the next instruction?

A = 045000
B = 044124

34. Given: Instruction=000614
(A)=050450
(B)=000441

What will the A & B accumulators contain after execution of the next instruction?