GENERAL

The CONCEPT 32/27 Computers are SYSTEMS' new low-end 32-bit computers. They are designed to meet the requirements of OEMs who need 32-bit performance, but have only 16-bit budgets and mounting space.

The CONCEPT 32/27 features a single slot CPU, 256K byte Integrated Memory Modules (IMMs) and an I/O Processor (IOP). These three types of functional modules form the basis of the system, and communicate with each other over the SelBUS.

The single slot CPU provides large machine features such as a 16 Megabyte Mapped Memory Management System, instruction lookahead, and floating-point arithmetic instructions. Because it uses the Mapped Programming Executive (MPX-32), the CONCEPT 32/27 is compatible with the larger CONCEPT/32 and 32 SERIES Computers.

The IMMs combine 256K bytes of MOS memory with ECC on a single plug-in module with refresh logic and Memory Controller functions. This self-contained memory subsystem can be easily expanded to provide up to one megabyte of memory in the basic 32/27 chassis, and two megabytes of memory in the basic 32/2750 chassis.

The IOP, also requiring only a single slot, provides several important functions including 16 device controller subchannels, four external priority interrupts, an interval timer, real-time clock, and an operator's console interface.

The CONCEPT 32/27 is packaged in a compact 15 ¾ inch high chassis suitable for mounting in a 19-inch standard EIA rack. With the CPU, IOP, and one IMM installed, the basic chassis still provides seven additional SelBUS slots for IMM's and high performance peripheral processors, and five bus slots for IOP-based peripheral controllers and communications interfaces.

The CONCEPT 32/2750 is a two chassis package; one 18 slot chassis for SelBUS-based logic and memory boards, and one eight slot chassis for IOP-based peripheral controllers.

Through extensive use of LSI chip technology, the CONCEPT 32/27 Computers have been significantly reduced in size and complexity. This has resulted in several user benefits:

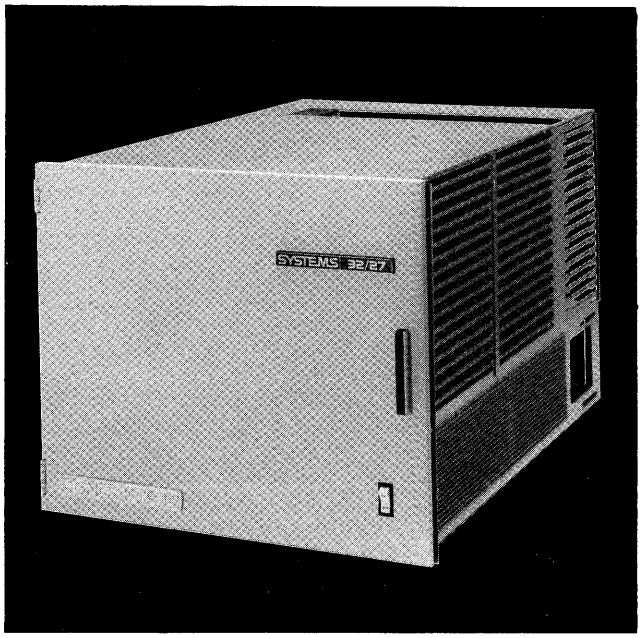
- Increased reliability and improved maintainability due to fewer parts
- Lower power consumption
- High density packaging to provide more capability in a smaller space
- Easier installation

Performance characteristics and features of the CONCEPT 32/27 Computers include:

- Dual Bus Architecture
- Single Slot 32-bit CPU
- 256 KB IMMs with ECC (The 32/27 is expandable to 1M byte within its chassis, the 32/2750 to 2 MB)
- 0, 2, or 4 Way Interleaving
- IOP for Improved System Performance with lower cost I/O controllers and a simple bus interface
- Single Chassis System with integral cooling and power supplies
- Fast Throughput - Up to 26.67 MB per second continuous SelBUS transfer rate
- Modular Expansion Capabilities
- Increased Reliability

PRODUCT BULLETIN

CONCEPT 32/27 COMPUTERS



Models 342X, 344X

- **Single Slot 32-bit CPU**
- **Single Slot I/O Processor**
- **Single Slot Integrated Memory Modules**
- **Optional Battery Backup Units**

Proven COMPUTER Performance

SYSTEMS

A Subsidiary of GOULD INC.

SYSTEM ARCHITECTURE

SelBUS

The SelBUS is a high-speed synchronous bus that can transfer data at the rate of 26.67 million bytes per second (See Figure 1). Each module on the bus is assigned one of 23 SelBUS priority lines by simple jumper settings. Interrupt and SelBUS priority are uniquely defined and are not module position dependent.

MULTIPURPOSE BUS

The Multipurpose (MP) Bus is a medium speed asynchronous bus that can transfer I/O data at a rate of 1.5 million bytes per second. Up to 16 Device Controllers can exist on the MP Bus at a time.

CPU

The CONCEPT 32/27 Computers contain a single slot 32-bit CPU that interfaces with the SelBUS. Large-Scale Integration technology permits a 32-bit CPU to reside in a single SelBUS slot while maintaining performance. The CONCEPT 32/27 CPU uses instruction lookahead for fast execution of instructions. Instruction fetches are made concurrently with instruction decode and execution.

Registers

The CONCEPT 32/27 Computers have a set of eight high-speed, general purpose registers for use by the programmer in arithmetic, logical, and shift operations. Three general purpose registers - R1, R2, and R3 - can also be used for indexing operations. Register R0 can be used as a link register. Register R4 can be used as a mask register.

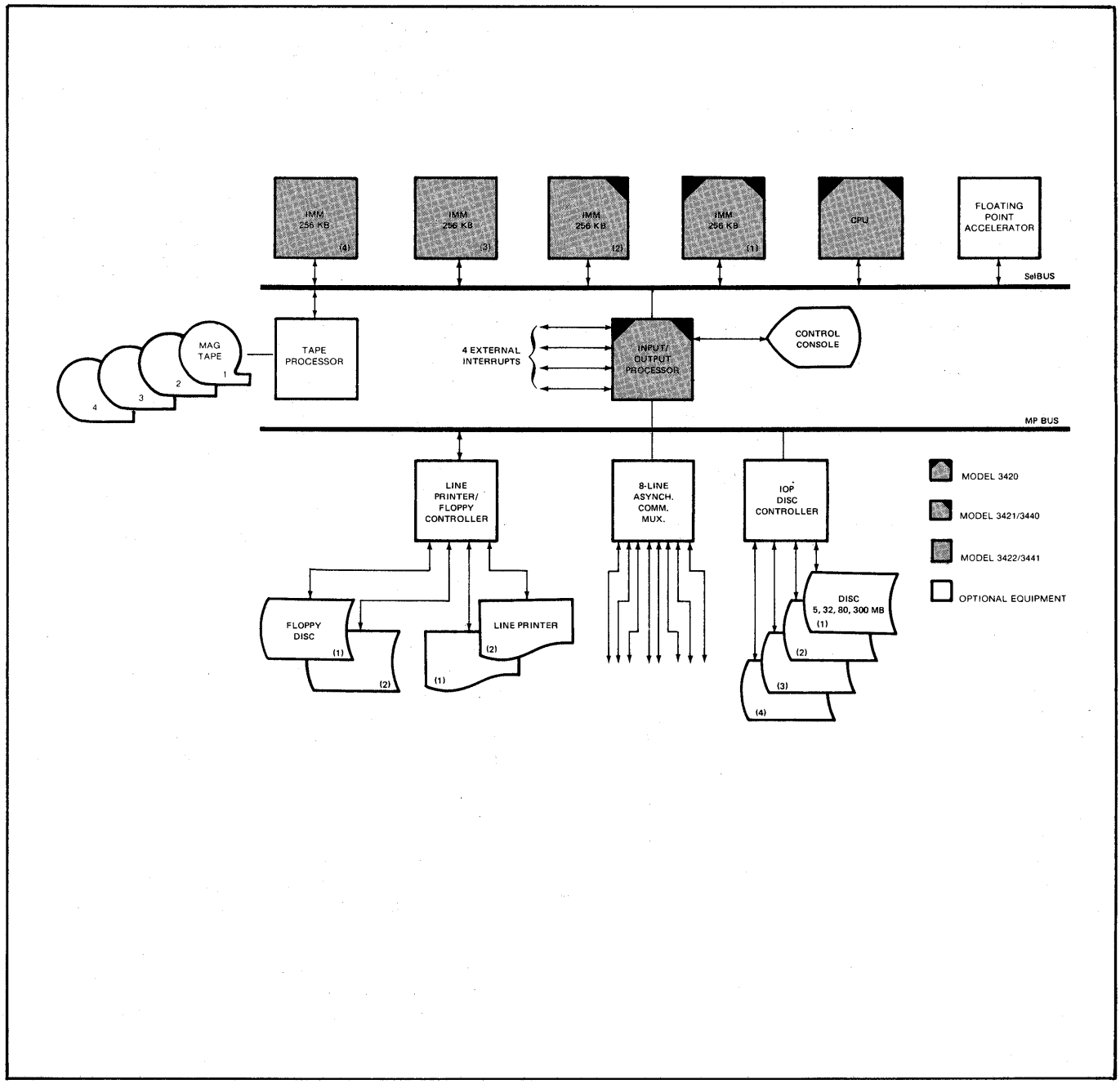


Figure 1. 32/27 System

Instruction Repertoire

The instruction repertoire of the CONCEPT 32/27 CPU contains 176 standard instructions. The functional classification and the number of instructions are as follows:

CLASS	
LOAD	17
STORE	9
ZERO	4
REGISTER TRANSFER	11
MEMORY MANAGEMENT	4
BRANCH	9
COMPARE	11
BOOLEAN	18
SHIFT	13
BIT MANIPULATION	8
FIXED-POINT ARITHMETIC	30
FLOATING-POINT ARITHMETIC	8
CONTROL	14
INTERRUPT	9
INPUT/OUTPUT	11
TOTAL	176

The eight bit-manipulation instructions provide the capability to test and set, test and zero, add to, or simply test any selected bit in any memory location or in any general purpose register.

Instructions are either halfword instructions (16 bits) or word instructions (32) bits. The word instructions primarily reference memory locations, while the halfword instructions deal primarily with register operands.

Because approximately one-third of the instructions are halfword instructions, program memory space is conserved by packing two consective halfword instructions into a single memory location. The two instructions are fetched simultaneously, resulting in fewer memory accesses, making programs execute faster.

Privileged Instructions

One bit in the Program Status Doubleword (PSD) is called the privileged state bit. If the privileged state bit is set, privileged instructions can be executed. If the privileged state bit is not set, any attempt to execute a privileged instruction will cause a Privileged Violation Trap.

The following instructions are privileged:

- All interrupt related instructions such as Enable Interrupt or Request Interrupt
- All instructions that can modify the memory mapping registers
- All Input/Output instructions
- All instructions that can place the machine in a state that requires operator intervention to continue processing, such as Halt

User programs operating in the unprivileged state should use the Supervisor Call (SVC) instruction with the appropriate privileged/unprivileged system.

Certain events can change the CPU from the unprivileged to the privileged state by loading a new Program Status Doubleword. These are:

- An interrupt from an external event or the I/O System
- A hardware trap caused by addressing nonpresent memory, executing an undefined instruction, executing a privileged instruction by nonprivileged program, or writing to protected memory
- A hardware trap caused by a nonrecoverable condition such as an uncorrectable error during a memory read, or an arithmetic exception
- The execution of the Supervisor Call instruction by a user requesting monitor services

In all cases, traps or interrupts are vectored to monitor routines for proper handling. Both the interrupt/trap vectors and the monitor service routines are in protected memory. This insures that an unprivileged user has no way to become privileged or to alter protected memory. The execution of the Load Program Status Doubleword (LPSD) instruction can cause the system to change from the privileged to the unprivileged state.

The operator can SYSTEM RESET to initialize the 32/27 Computer. SYSTEM RESET clears the eight general purpose registers, resets all memory protection, and sets the privileged state bit.

MEMORY

Memory in the CONCEPT 32/27 Computers interfaces directly to the SelBUS. The Integrated Memory Module is a high density memory subsystem, implemented on a single board, including 256 KB of dynamic MOS RAM, memory controller, error correction logic, and refresh circuitry. The IMM can overlap two read cycles, allowing reads to be initiated every 300 nanoseconds. A write can be initiated every 300 nanoseconds to a single IMM, but when more than one IMM is used, writes can be initiated every 150 nanoseconds to the IMMs as a group.

The MOS Memory is organized in 39-bit words: 32 bits of data and 7 Error Correction Code Bits (ECC). During write operations, the ECC bits are generated and stored in memory. When a read memory operation takes place, the ECC bits are checked. If a 32-bit error is detected, the error is corrected. If two bits are in error, an error is generated.

Up to one megabyte (four IMMs) of memory can exist in the basic chassis of a CONCEPT 32/27 Computer. Four additional IMMs can be integrated with the addition of a Model 8920 Logic/Memory Support Package.

The CONCEPT 32/2750 can support up to two megabytes of memory in it's basic chassis, and can also support memory expansion with the addition of a Model 8925 Logic/Memory Support Package, which can support another two megabytes of IMMs.

The CONCEPT 32/27 Computers can be optionally equipped with Battery Backup Units in both the basic and Logic/Memory Support Package. The Model 8990 Battery Backup Unit replaces the standard power tray in each chassis and maintains power to preserve the integrity of 1 MB of IMM data for up to five minutes.

The CONCEPT 32/2750 Computer can be equipped with a Model 2374 Battery Backup Unit, which can maintain memory power to 1 MB of IMMs for 2.5 hours, or more memory for a slightly reduced time.

HARDWARE MEMORY MANAGEMENT

The CONCEPT 32/27 Computers operate under either the MPX-32 disc-based or the MPX-32/M memory-only operating system. Both are mapped executives and have two ways to address memory; Mapped, Nonextended; and Mapped, Extended.

Mapped, Nonextended

Mapped, Nonextended addressing allows the CPU to address any instruction or operand (bit, byte, halfword, word, or doubleword) within a task's logical address space. This space consists of
512 KB of logical memory dispersed anywhere within the
16 MB physical memory.

MPX-32 allows multiple logical address spaces. A user can access instructions and operands within the logical address space in which his task resides. Physical blocks of memory can be common to many logical address spaces; thus, tasks in different logical address spaces can share common blocks of physical memory.

Mapped, Extended

Mapped, Extended addressing provides all the capabilities of Mapped, Nonextended addressing plus access to a extended logical address space. This space consists of 1.5 megabytes of memory beyond the primary logical address space. It allows the user additional memory space to store data (operands). Each extended logical address space can be 1.5 megabytes long, dispersed anywhere within 16 megabytes of physical memory. The combination of primary and extended logical address space supports programs up to two megabytes long. The executable code must lie within the primary logical address space but operands can be in either the primary logical or extended logical address space.

Nonmapped Addressing

The CONCEPT 32/27 hardware supports two other addressing methods. These are provided for compatibility with earlier machines and are not supported by MPX-32 or MPX-32/M. They are; Nonmapped, Nonextended-Indexed; and Nonmapped, Extended-Indexed.

INPUT/OUTPUT SUBSYSTEM

The Input/Output Processor (IOP) multiplexes Device Controllers on its MP Bus with a transfer rate of 1.5 MB/sec. The CONCEPT 32/27 Computers also support standard high-performance I/O. Regional Processing Units, intelligent "Class D" Input/Output Microprogrammable processors, Real-Time Option Modules, and High-Speed Data Interfaces connect directly to the SelBUS.

Input/Output Processor

The IOP is a powerful multiplexing channel for I/O operations. The IOP operates independently of and in parallel with the CPU and takes over some of the functions previously performed by the CPU. The result is increased CPU availability and improved system performance. Up to 16 Device Controllers supporting a total of up to 124 devices can be handled by a single IOP. Larger systems can use multiple IOPs, if required.

Four user-defined external interrupts for Real-Time sense and control, a 32-bit programmable timer, and a Real-Time Clock are included in the IOP.

A Control Console Port on the IOP provides system control functions, eliminating the need for an operator control panel.

Control Console

The traditional control panel functions have been combined with the operator's console functions on the operator's console CRT.

The port can support modems, making remote control of the system possible over a telephone or private line.

The Control Console has two modes; Operator's Console mode and Control Panel mode. The operator can switch between the two modes at any time.

Operator's Console mode is the normal mode for the Control Console when the system is running. Job status, user status, and operator information are displayed. The operator can monitor and control the operation of the system. In the Operator's Console mode, the CRT can also function as a user terminal with all MPX-32 functions available.

The Control Panel mode displays status and allows the operator to modify Machine State, General Purpose Register contents, and memory locations.

Interrupts/Traps

The CONCEPT 32/27 Computers can accommodate up to 96 hardware priority interrupt levels used for I/O Controllers and external signals. The interrupts associated with the I/O are provided by the I/O Controllers.

The IOP provides four external interrupt levels, a real-time clock, and a 32-bit programmable interval timer. The real-time clock and interval timer each use one interrupt level.

Each interrupt level has an assigned dedicated memory location. All interrupt levels can be selectively enabled, disabled, activated, deactivated, or requested under software control. All Interrupt Control Instructions are privileged. Attempts at execution by unprivileged programs will yield a Privilege Violation Trap.

Users requiring more external interrupt lines can add one or more Model 2345 Real-Time Option Modules (RTOM). Each RTOM provides 16 external interrupt levels.

SOFTWARE

SYSTEMS provides a number of system software layers. These are:

- Operating System (MPX-32)
- Languages
- Libraries
- Tools

Each layer provides capabilities to help reduce the cost of developing specific application programs by helping the programmer create high quality software that can be readily maintained.

MPX-32

MPX-32 Model 1401, is a multitasking operating system that fully supports real time, multibatch, and interactive processing.

MPX-32 allows a task to activate, communicate, and share memory with other tasks. The interactive environment allows the user at a terminal to communicate with the system through single line interaction, command files, and macro command files. System management is simplified with the use of project accounting. The system manager may track use of the system on a person, project names, or task name basis.

LANGUAGES

MPX-32 has been designed to accommodate the full spectrum of programming languages. Support for Assembly Language programming is provided by a powerful and versaile Macro Assembler.

SYSTEMS FORTRAN 77+, Model 1413, compiles with ANSI X3.8 (1978), MIL STD 1753, and ISA S61.1 and S61.2 It also includes extensions to the industry standards to more than satisfy the needs of high performance real-time applications.

The Model 1420 SYSTEMS COBOL satisfies the levels defined in X3.23 (1974). It also contains features including runtime diagnostics, compiler diagnostics, a performance optimization enhancement package, and additional statement capabilities.

SYSTEMS Pascal, Model 1414, targets the Jensen and Wirth definition of Pascal. Pascal programs can interface with any FORTRAN 77+ or Macro Assembly subroutine. Both Pascal and FORTRAN may call Scientific Runtime Library routines.

LIBRARIES

Libraries are groups of standard subroutines that can be called from application programs, saving the customer the time needed to write these standard pieces of code.

Libraries available from SYSTEMS include:

- The USMA Graphics Compatibility System for interactive 2-D and 3-D graphics.
- The PLOT 10™ Terminal Control System for producing hardcopy graphics.
- The TOTAL® Data Base Management System
- The Statistical Subroutine Library, containing over 100 math and statistical routines.
- The Scientific Run Time Library, containing subroutines and special extensions for FORTRAN 77+, FORTRAN 66+, and assembly language programs.

TOOLS

The application program development phase for a new system has always been a critical phase for users. Therefore, SYSTEMS has placed special emphasis on providing software development tools to make this programming task as easy as possible.

Program development tools include an interactive Text Editor, A Task Debugger, A File Manager, a Cataloger capable of linking code written in several languages into a single task, library editors, and media conversion programs. All utilities are capable of running in either the batch or interactive environment. In fact, the system is designed so that any task, user or SYSTEMS provided, can run either in the batchstream or interactively without modification.

Also included with these general utility programs is an Interactive System Generation Program (SYSGEN). Because of its interactive nature, SYSGEN can be activated and used with any terminal in the system. This capability makes it possible for an operating system to be generated on one machine and used on an entirely different machine.

Optional Software Tools are available to the programmer including a FORTRAN formatter, a Symbolic Debugger, the Instrumenters™, the Documenter A™, the Auditor™, and the Interface Documenter™. All are offered as interactive programs which operate under the MPX-32 operating system.

PACKAGING

The CONCEPT 32/27 Computers are packaged for the OEM customer. Standard 19-inch rack-mount chassis with industry standard (EIA) hole spacing contain the basic systems. The CONCEPT 32/27 chassis contains a 15 slot backplane split into two sections - the SelBUS and the MP Bus (See Figure 2).

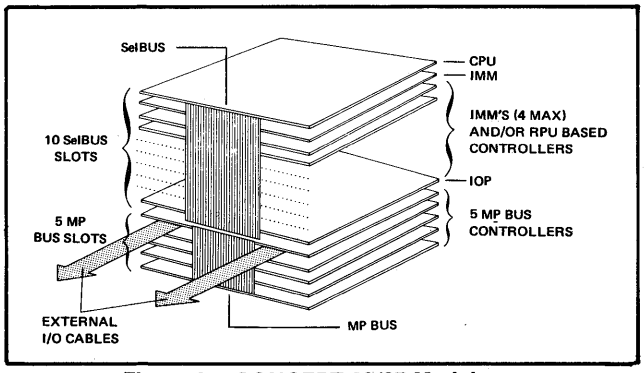


Figure 2. CONCEPT 32/27 Modules

The SelBUS is the system bus. It consists of ten slots and contains the single-slot CPU, the single-slot IOP, up to four single-slot IMMs, and up to four RPU, IOM or High-Speed Device Interfaces. SelBUS slots that are not used for the full complement of IMM's are available for RPU's, IOM's, etc. The SelBUS can be expanded with the addition of a Logic/Memory Support Package.

The MP Bus is a 16-bit I/O bus for IOP-based Device Controllers. Up to five single-slot Device Controllers can be placed in the MP Bus area of the system chassis. Additional Device Controllers can be placed in an I/O Expansion Chassis.

The I/O Expansion Chassis (See Figure 3) adds eight MP Bus slots to the basic system, or permits the addition of a second IOP to the system. The I/O Expansion Chassis is split into two separate MP Bus sections. This permits one IOP to control all eight Device Controllers in the chassis, or allows two IOPs to each control four Device Controllers.

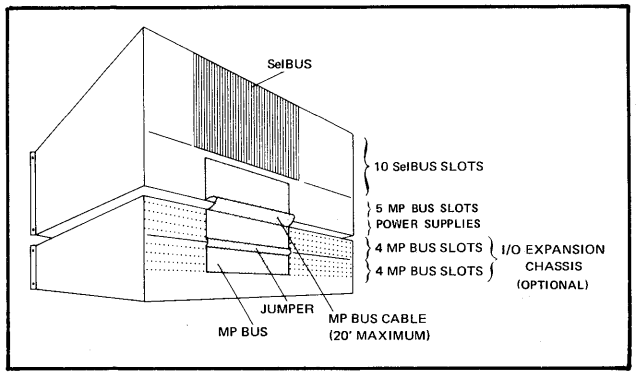


Figure 3. CONCEPT 32/27 Chassis

The CONCEPT 32/2750 is packaged in two chassis, shown in figure 4. One chassis is an 18-slot SelBUS chassis, and the other is an eight slot I/O Expansion chassis.

The CONCEPT 32/27 CPU is functionally similar to other SYSTEMS MPX-32 supported CPUs. It has been reduced in size to a single slot unit, increasing reliability while decreasing power conceumption and cost.

Integrated Memory Modules are complete memory subsystems on a single board. They include 256K Byte memory, onboard refresh logic, error correction code logic and memory controller functions.

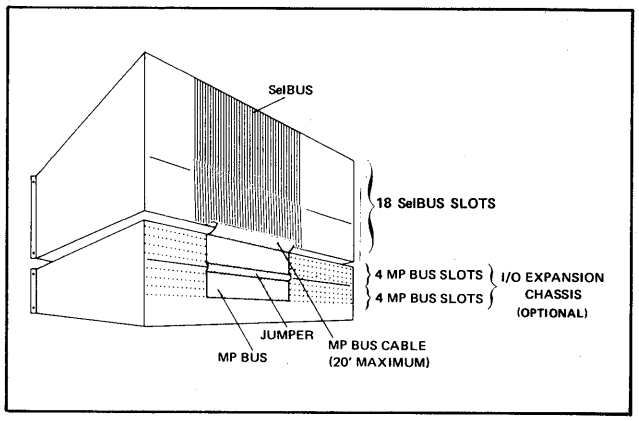


Figure 4. CONCEPT 32/2750 Chassis

The Input/Output Processor is a 16-bit processing unit. It reduces system overhead by performing I/O functions that the processor would normally do. Microprocesor-based Device Controllers are multiplexed by the IOP on the MP Bus, resulting in a low cost, efficient I/O system.

Power supplies and cooling fans are internal to the CONCEPT 32/27 system chassis. A minimum number of connections between the chassis and the outside world are required, resulting in a simple interfacing and configuration task.

Both the CONCEPT 32/27 and the CONCEPT 32/2750 can be expanded with the addition of Logic/Memory Support Packages.

The CONCEPT 32/27 Logic/Memory Support Package is physically and electrically identical to the Nucleus Chassis, but with a 15 slot SelBUS backplane capable of supporting an 1 MB of IMMs. Similarly, the CONCEPT 32/2750 Logic/Memory Support Package is identical to the CONCEPT 32/2750 Nucleus Chassis, with a 18 slot SelBUS backplane capable of supporting an additional 2 MB of IMMs.

The CONCEPT 32/27 chassis requires 30 Amps of single phase power when installed alone. However, cabinets for both the CONCEPT 32/27 and 32/2750 require three phase power for AC distribution to multiple chassis.

PERFORMANCE SPECIFICATIONS

PROCESSOR

Word Length	32 bits
Data Sizes	1, 8, 16, 32, 64 bits
General Purpose Registers	8 (3 of which can be used for indexing)
Additive Timing for Instruction Execution:	
Indexing	None
Mapping	None
Instruction Repertoire	176 Instructions
Floating-Point Arithmetic	Integral to processor
Integrity Features	Memory Protect, Power Fail Safe, Memory ECC, Arithmetic Exception, Privilege Violation, Nonpresent Memory

MODEL NUMBERS

Model Number	Nomenclature/Description
3420	CONCEPT 32/27 NUCLEUS The CONCEPT 32/27 Nucleus is the basis for configuring systems to meet specific customer requirements. The MPX-32 Operating System, I/O Controllers, and peripherals are available separately. Each CONCEPT 32/27 Nucleus includes: • Single SelBUS slot CPU • Single SelBUS slot IOP • Single SelBUS slot 256K Byte IMM • System Chassis with: Seven available SelBUS slots for Memory or RPU-based I/O Controller Expansion Five available MP Bus for IOP-based controllers All required power supplies and cooling fans
3421	CONCEPT 32/27 NUCLEUS, 512 KB Same as 3420, except 512 KB (two IMMs) of memory. Six available SelBUS slots.
3422	CONCEPT 32/27 NUCLEUS, 1 MB Same as 3420, except 1 MB (four IMMs) of memory. Four available SelBUS slots.
8920	CONCEPT 32/27 LOGIC/MEMORY SUPPORT PACKAGE Provides 15 additional SelBUS slots for expansion of a CONCEPT 32/27 Nucleus. Supports up to 1 MB of IMMs.
3440	CONCEPT 32/2750 NUCLEUS, 512 KB The CONCEPT 32/2750 is an integrated processor consisting of: • Single SelBUS slot CPU • Single SelBUS slot IOP • Two single SelBUS slot IMMs (512 KB) • 18 slot Logic/Memory chassis with 1500 watt power supplies • 8 slot I/O chassis (Multipurpose Bus) • System Panel • 14 available SelBUS slots for Logic/Memory expansion
3441	CONCEPT 32/2750 NUCLEUS, 1 MB Same as 3440, except 1 MB (four IMMs) of memory. 12 available SelBUS slots.
8925	CONCEPT 32/2750 LOGIC/MEMORY SUPPORT PACKAGE Provides 18 additional SelBUS slots for expansion of a CONCEPT 32/2750 Nucleus. Supports up to 2 MB of IMMs.
8910	I/O EXPANSION CHASSIS Provides two groups of four MP BUS slots for expansion of IOP-based I/O.

All model numbers are available in 50 Hz versions. Their model numbers have a "-1" suffix.

PREREQUISITES

The 32/27 requires the following:

- An RS-232C compatible or current loop terminal for Control Console functions.
- The MPX-32 Operating System, Revision 1.4 or higher.

The 32/2750 additionaly requires a Model 3902-X Cabinet with an AC Distribution Panel.

PRODUCT INTERRELATIONSHIPS

In addition to the products discussed so far, the CONCEPT 32/27 and 32/2750 can support the following products:

- MPX-32
- MPX-32/M
- All software products supported by MPX-32 (or MPX-32/M)
- Floating Point Accelerator
- Multiprocessor Timing Products
- Power Fail
- Real-Time Option Module
- Battery Backup
- MBC/MBA - based memory
- Disc Processor products
- Tape Processor products
- General Purpose Multiplexor Controller products
- HSD and HSD II

PHYSICAL/ENVIRONMENTAL

	32/27 Chassis and 32/27 Logic/Memory Support Package		32/2750 Chassis and 32/2750 Logic/Memory Support Package	
Weight	130 lbs (59 Kg)		149 lbs (67.7 Kg)	
Dimensions:				
Height	15.75 in. (40.0 cm)		12.25 in. (31.11 cm)	
Width	19 in (48.26 cm)		19 in. (48.26 cm)	
Depth	29.3 in. (74.42 cm)		20.25 in. (51.43 cm)	
Electrical:				
Voltage	115 Vac	220 Vac	115 Vac	220 Vac
Current	24.0 Amps	12.0 Amps	24.5 Amps	33 Amps
Breaker Rating	30 Amps	15 Amps	30 Amps	50 Amps
Frequency	60 Hz	50 Hz	60 Hz	50 Hz
Power Connector Type (NEMA #)	L5-30P	L6-30P	Hardwired	
Power Cable Length	12 Feet	12 Feet	Wired to A.C. Distribution Panel	
Environmental:				
Operating Temperature (°C)	10° to 40°		10° to 40°	
Relative Humidity	5% to 95%		5% to 95%	
Storage Temperature(°C)	-40° to 60°		-40° to 60°	
Relative Humidity	2% to 95% Non-condensing		2% to 95% Non-condensing	
Heat Dissipation	9425 BTU/hr.		9425BTU/hr.	

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