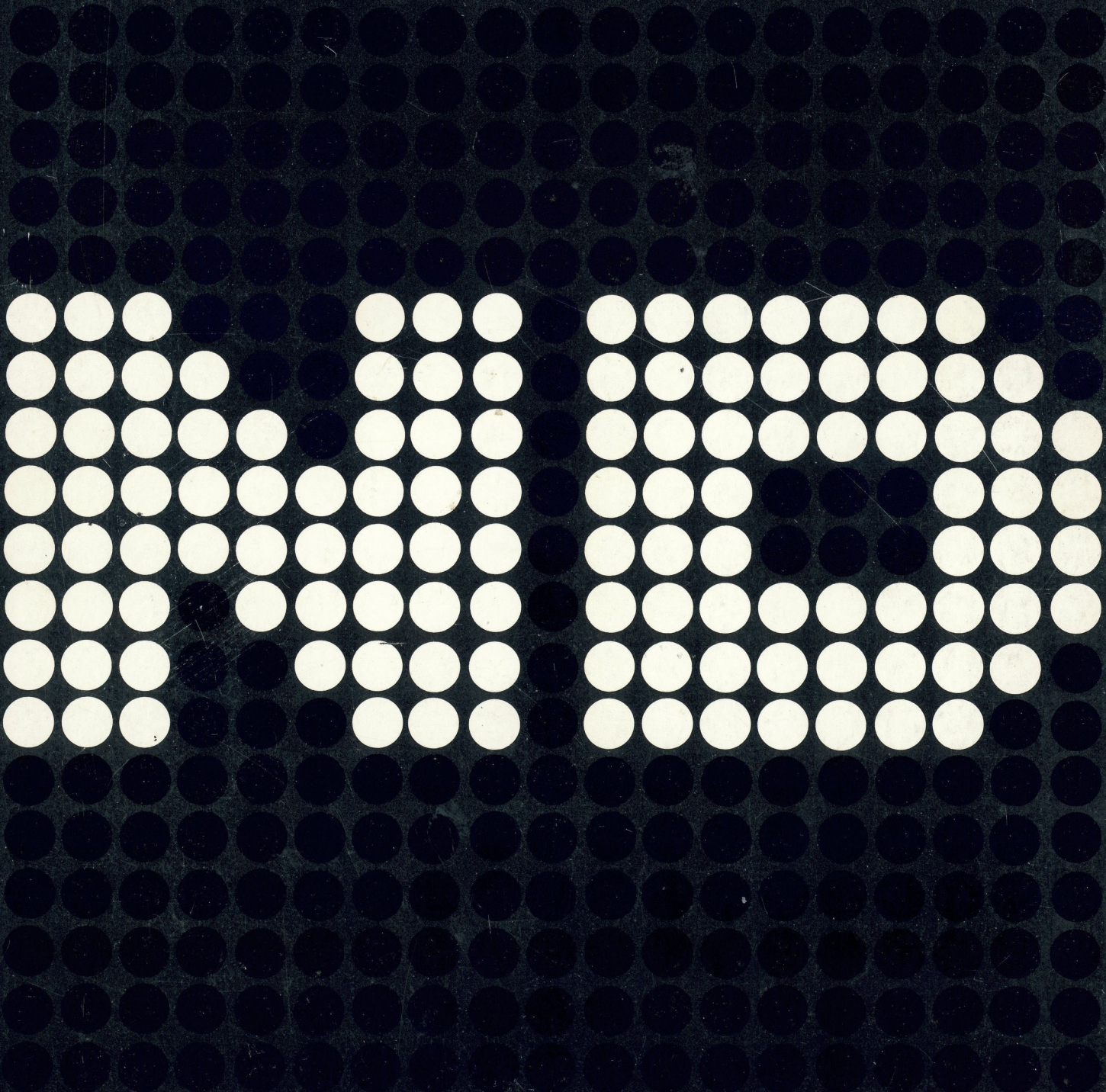


FLOPPY DISK

SYSTEM

**NORSK DATA A.S**







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**SECTION I**

**SYSTEM/GENERAL**



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## I.1 INTRODUCTION

The Floppy Disk Drive was developed by IBM, in 1967, under direction of Alan Shugart. In 1970, IBM took advantage of their research results, and put the Floppy Disk into a computer system where it was used as a read-only device for diagnostic programs.

In 1973, the usage was extended and the Floppy Disk system was used in a data entry system. From now on, the Floppy Disk was added on the list of peripheral products. Peripheral product's manufacturers became interested in the new product, and (of course), followed the IBM standard.

However, the first drives had a reputation of being unreliable, having high error rates and head and media wear.

Intensive efforts have been made to reduce the problems, so we today have a low cost, reliable and easy-to-handle device with many applications.



I.2 GENERAL

Floppy Disk introduces a new data storage facility into a computer system. Refer to Figure I.2.1.

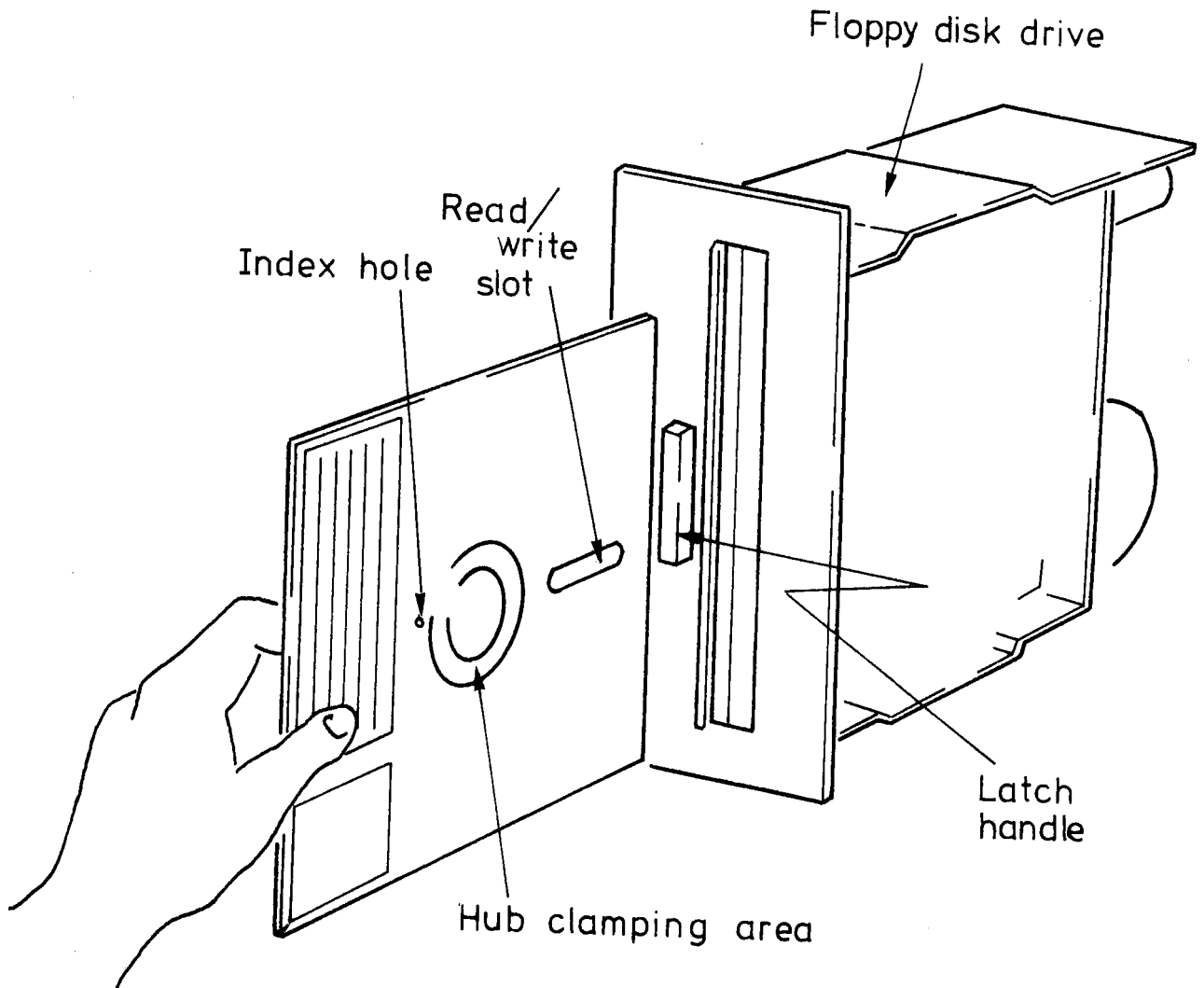


Figure I.2.1.

The storage medium itself is a flexible disk (also referred to as a diskette). The diskette is free to rotate inside a semi-rigid envelope. The inside of this envelope is lined with a wiping material to clean the disk of foreign particles, as it rotates.

### I.2.1 *DISKETTE LOADING*

To load the diskette, depress the latch and insert the diskette with its label facing out, i.e., the index hole is *above* the center of the diskette. Move the latch handle to the left. The diskette will then be attached to the rotating spindle for a Hub Clamp.

For ease of operation, the diskette can be loaded (or unloaded) with the drive in operating condition, i.e., the spindle rotating.

It is theoretically possible to utilize both sides of the diskette. However, at the present time, only one side is used by the drive since only one read/write head exists. One should also notice that the side used is the one *opposite* the label.

If the diskette is turned, the read/write head will still have access to the surface, however, the index transducer will not see the hole and the drive will attain the ready condition.

### I.2.2 *DISKETTE HANDLING*

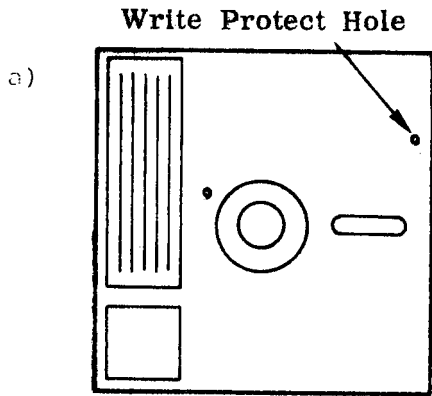
When removed from the drive, the diskette is stored in an envelope. To protect the diskette, the same care and handling procedures, specified for computer magnetic tape, apply. These precautionary procedures are as follows:

1. Return the diskette to its storage envelope whenever it is removed from the drive.
2. Keep diskettes away from magnetic fields and from ferromagnetic materials. Strong magnetic fields can damage the data recorded on the diskette.
3. Replace storage envelopes when they become worn, cracked or disorted. Envelopes are designed to protect the diskette.
4. Do not write on the plastic jacket with a lead pencil or ball-point pen. Use a felt pen.
5. Heat and contamination from a carelessly dropped ash can damage the diskette.

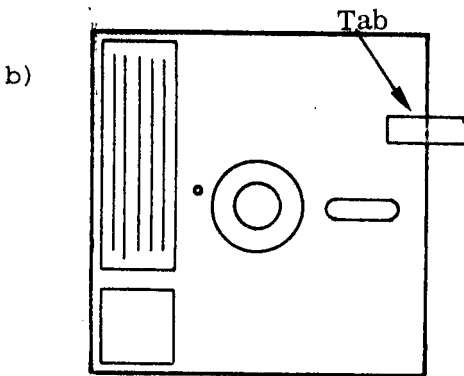
6. Do not expose diskette to heat or sunlight.
7. Do not touch or attempt to clean the disk surface. Abrasions may cause loss of stored data.



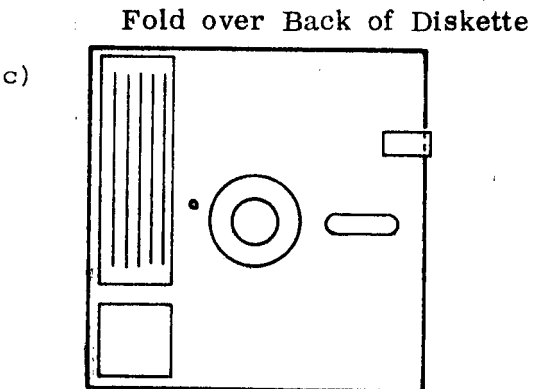
**1.2.3 WRITE PROTECTION FEATURE**



A diskette with a hole punched as indicated in Figure 1.2.2a is write protected.



By covering the hole with a tab as indicated in Figure 1.2.2b,c, the protection is removed.



If a diskette is purchased without the write protection feature, a hole can be punched according to the specification depicted in Figure 1.2.2d.

**Figure 1.2.2, continued**

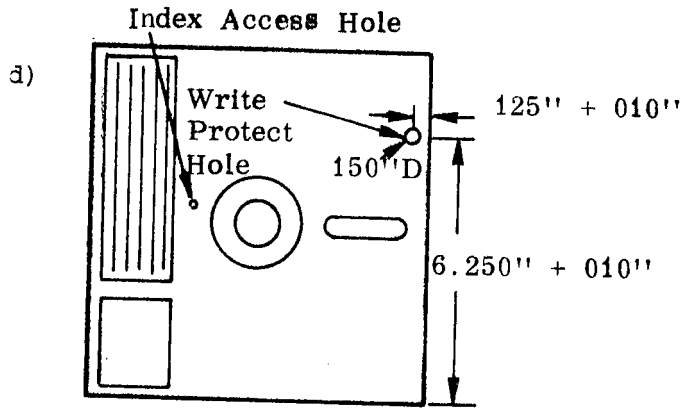


Figure I.2.2, concluded.



### I.3 SYSTEM CONFIGURATION

The Floppy Disk System is a low cost, highly reliable mass storage system with a relatively low access time and transfer rate.

Normally, a Mass Storage Device requires a Direct Memory Access (DMA). However, due to total system cost, a specially designed Programmed Input/Output (PIO) interface has been preferred.

Figure I.3.1 will illustrate the data transfer paths during a read operation. A write operation would be illustrated by reversing the arrows.

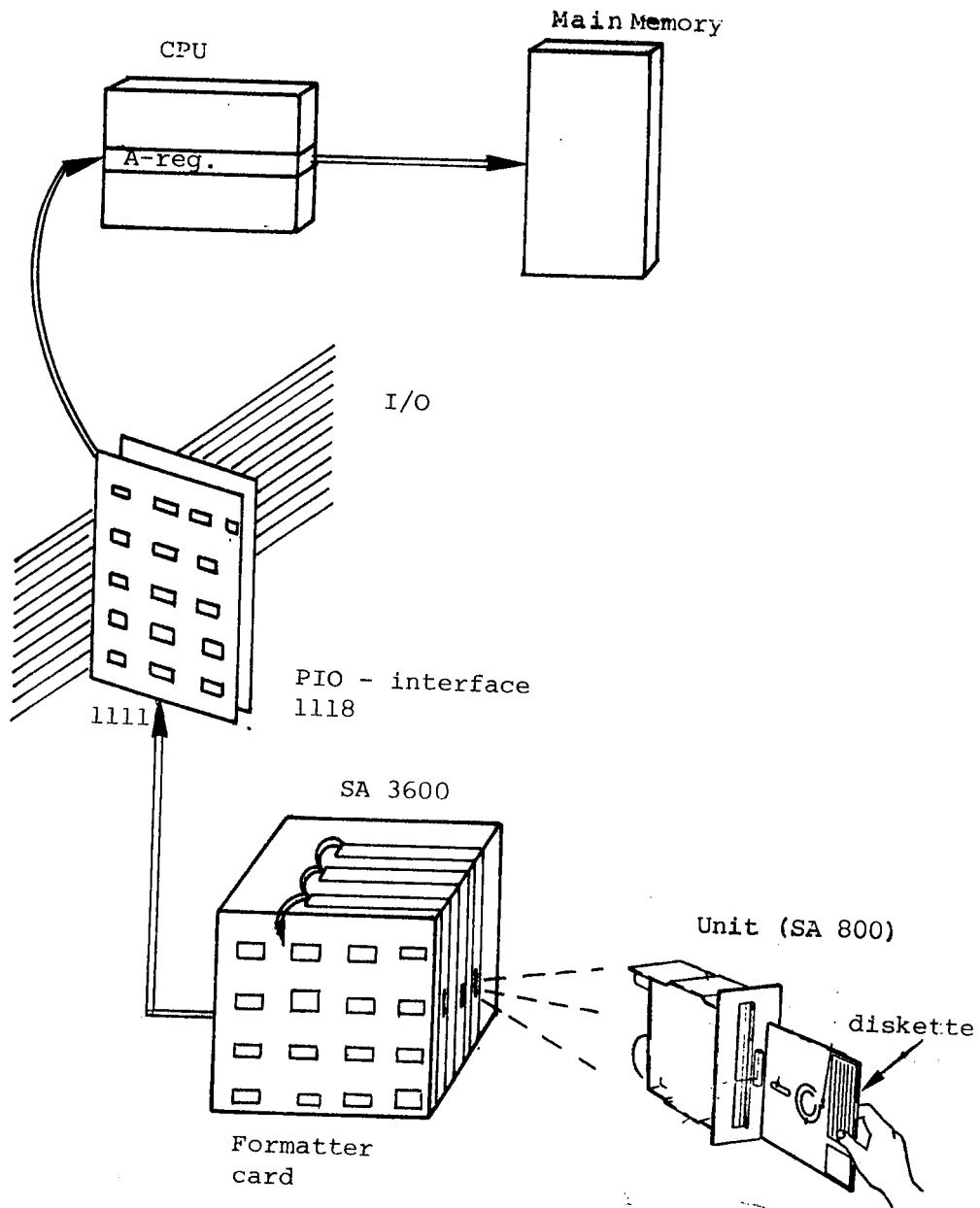


Figure I.3.1.

A floppy disk system (SA 3600) can have up to 3 drive units (SA 800).

As depicted in Figure I.3.1, up to 3 drives are daisy-chained to one formatter card. The Formatter is cabled to the Interface located in the I/O System. Two interfaces will be discussed in this manual.

- *The interface between the Interface and the Formatter*  
and
- *the interface between the Formatter and the drive units.*

The first one will be discussed in Section II.1, the second one in Section III.1.



I.4 FLOPPY DISK PROGRAMMING SPECIFICATIONS

I.4.1 DEVICE REGISTER ADDRESS

Read Data Buffer

IOX 1560 (IOX RDAT)

Write Data Buffer

IOX 1561 (IOX WDAT)

Read Status Register No. 1

IOX 1562 (IOX RSR1)

Write Control Word

IOX 1563 (IOX WCWD)

Read Status Register No. 2

IOX 1564 (IOX RSR2)

Write Drive Address/Write Differences

IOX 1565 (IOX WDAD)

Read Test

IOX 1566 (IOX RTST)

Write Section/Write Test Byte

IOX 1567 (IOX WSCT)

**For** Disk System II add 10g to the codes specified above. Each disk system can handle up to 3 drives.

Ident code for Disk System I is 21g. Ident code for Disk System II is 22g.

Interrupt level is 11<sub>10</sub>.

## I.4.2 *INSTRUCTION FORMATS AND DESCRIPTION*

### I.4.2.1 *Read Data Buffer IOX RDAT*

Reads one 16 bit word from the Interface Buffer. The buffer address is automatically incremented after execution of the instruction.

### I.4.2.2 *Write Data Buffer IOX WDAT*

Write one 16 bit word to the Interface Buffer. The buffer address is automatically incremented after execution of the instruction.

### I.4.2.3 *Read Status Register No. 1 (IOX RSR1)*

Bit 0: Not used

Bit 1: Interrupt enabled

Bit 2: Devicy busy

Bit 3: Device ready for transfer

Bit 4: Inclusive or of bits set in Status Register No. 2 (sense)

Note: When bit 4 is set, an error has occurred and Status Register No. 2 *must* be read before proceeding.

Bit 5: Deleted record  
This bit is set after the read data command if the sector contained "Deleted Data Address Mark".

Bit 6: Read/Write Complete  
A read or write operation is completed.

Bit 7: Seek Complete  
The status bit is set after seek or recalibration command when the disk has finished moving the R/W head.

Bit 8: Time Out  
Approximately 1,5 seconds

Bits 9-11: Are only used when formatting:

Bit 9 is active when buffer address bits 1 and 6 are active.  
Bit 10 is active when buffer address bits 1 and 7 are active.  
Bit 11 is active when buffer address bits 1 and 8 are active.

Note: Bits 4-7 are only significant after interrupt or when device busy is reset.

Bits 12-15: Not used

#### 1.4.2.4 *Write Control Word IOX WCWD*

Bit 0: Not used

Bit 1: Enable interrupt

Bit 2: Not used

Bit 3: Test Mode (for description see IOX RTST and -IOX WSCT)

Bit 4: Device clear (NB: *Select drive is deselected*)

Bit 5: Clear interface buffer address

Bit 6: Not used

The following bits are commands to the Floppy Disk Drive and these are the only control bits that generate device busy and interrupts (NB: *with the exception of bit 15, control reset*).

Bit 8: Format track

Bit 9: Write Data

Bit 10: Write Selected Data

Bit 11: Read ID

Bit 12: Read Data

Bit 13: Seek

Bit 14: Recalibrate

Bit 15: Control Reset

A detailed description of these commands are given in the appendix.

#### I.4.2.5 *Read Status Register No. 2*

- Bits 0-7: Not used
- Bit 8: Drive not ready  
This bit is set if the addresses drive has no power, its door is open, or the diskette is not properly installed. The drive address is invalid.
- Bit 9: Write Protect  
This bit is set if a write operation is attempted on a write protected diskette.
- Bit 10: Not used
- Bit 11: Sector Missing and No AM  
This bit is set if the desired sector for Read Data/Write Data or Write Detected Data cannot be located on the diskette.  
  
In addition, this bit may indicate a non-locatable data field address mark or a non-locatable address mark.
- Bit 12: CRC Error
- Bit 13: Not used
- Bit 14: Data overrun  
A data byte was lost in the communication between N-10 Interface and the Floppy Disk System.
- Bit 15: Not used.

#### I.4.2.6 *Write Drive Address/Write Differences IOX WDAD*

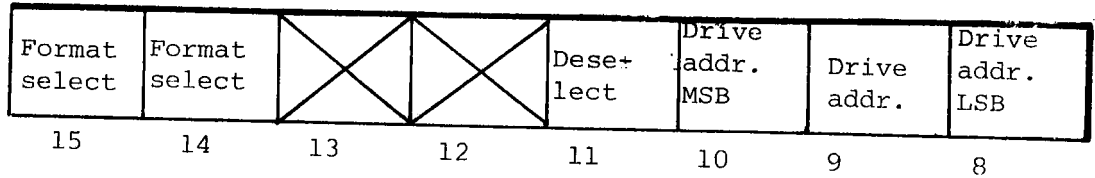
This can be two instructions, depending on bit 0 in the A register.

A)

- Bits 0-1: Load Drive Address  
This instruction selects Drive and Format
- Bits 1-7: Not used
- Bits 8-10: Drive address (unit number) 0, 1 or 2
- Bit 11: Deselect drive

Bit 15	Bit 14	Format (all numbers decimal)
0	x	IBM 3740 128 bytes/sector 26 sectors/track
1	0	IBM 3600 256 bytes/sector 15 sectors/track
1	1	IBM System 32-II 512 bytes/8 sectors/track

sector



B)

Bit 0-0: Write Differences

This is the differences between current track and desired track.. It is used as an argument for the seek command.

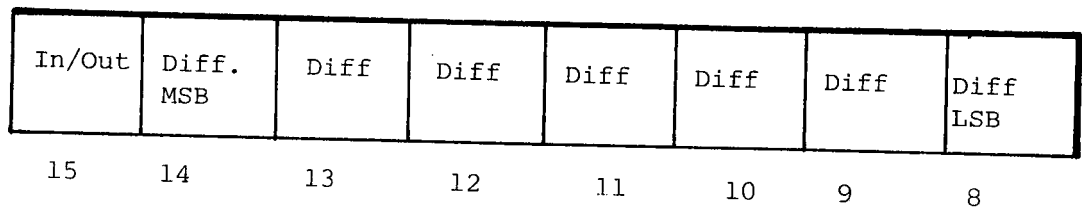
Bits 1-7: Not used

Bits 8-14: Differences between current and desired track

Bit 15: Direction select

Bits 15-0: Access "Out" to a lower track address

Bits 15-1: Access "In" to a higher track address





#### I.4.2.7 *Read Test Data IOX RTST*

This instruction is used for simulation of a data transfer between the Floppy Disk System and N-10 interface. It does not transfer data from the N-10 interface to the A register, but puts one 8 bit byte into the interface buffer, each time the instruction is executed. The bytes are packed to 16 bit words in the buffer and may later be read by IOX RDAT instruction. The byte may be chosen by using the IOX WSCT instruction (see description of IOX WSCT). IOX RTST is used for test purposes only and does not generate interrupt and busy signals.

The instruction is only activated when the interface is set in test mode by the following instruction:

*SAA 10  
IOX WCWD*

#### I.4.2.8 *Write Sector/Write Test Byte IOX WSCT*

When the interface is in test mode, this instruction loads the test byte which is transferred by the IOX RTST command. If not in test mode, this instruction loads the sector number to be used in a subsequent Read/Write command.

A)

Not in Test Mode:

Bits 0-7: Not used

Bits 8-14: Sector to be used in a subsequent Read/Write command

Sector range (octal) for different formats:

1-32	for IBM 3740
1-17	for IBM 3600
1-10	for IBM System 32-II

*NB: Sector 0 must not be used.*

Bit 15: Sector autoincrement  
If this bit is true the sector register is automatically incremented after each Read/Write command.

*Note: This autoincrement is not valid past the last sector of a track.*

Auto incr.	Sect. MSB	Sect.	Sect.	Sect.	Sect.	Sect.	Sect. LSB
15	14	13	12	11	10	9	8

B)

In Test Mode:

Bits 0-7: Not used

Bits 8-15: Test byte



**SECTION II**

**INTERFACE**





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## II.1 THE INTERFACE SIGNALS

### II.1.1 GENERAL

Described here, are the interface signals between the Interface and the Formatter. Listed separately, are signal/pin/plug assignments.

As illustrated, the interface consists of a general bi-directional, 8 bits X-fer bus and 12 special purpose lines. The X-fer bus is used by the Interface to transfer:

- *Write data bytes*

*and*

- *Control bytes*

The X-fer bus is used by the Formatter to transfer:

- *Read data bytes*

- *Status bytes (Status word I)*

*and*

- *Sense bytes (Status word II)*

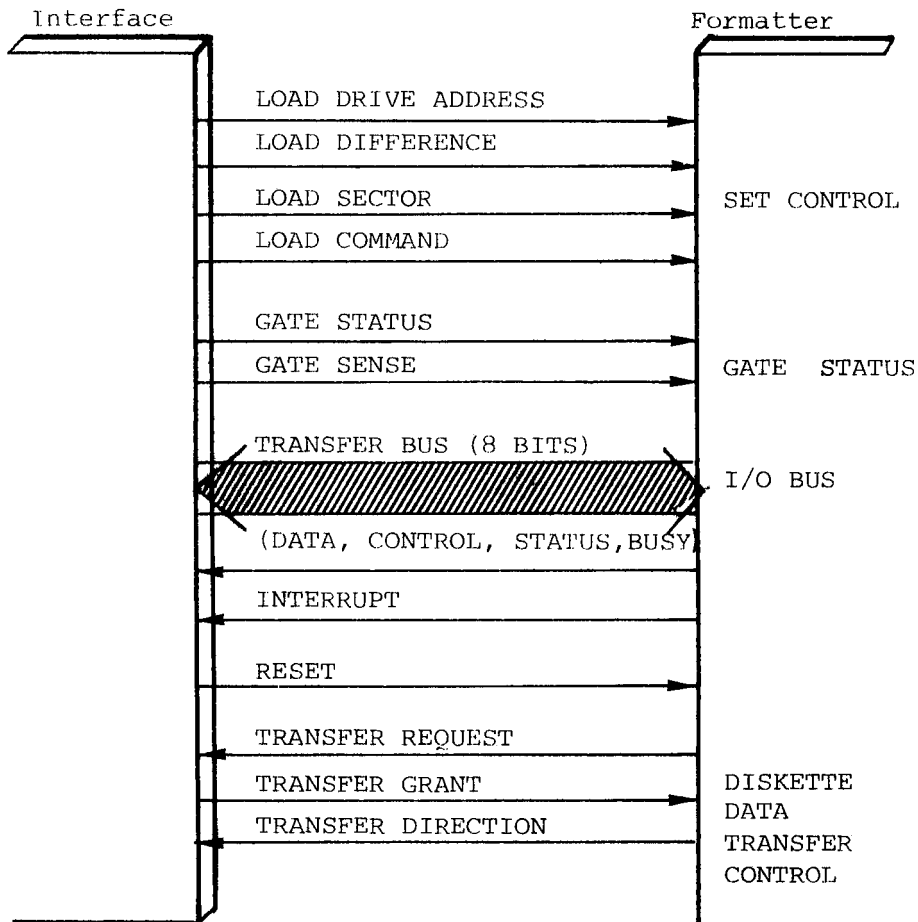


Figure II.1.1: *Interface Signals*

There are three basic modes of interface line operation.

The *first* mode involves the use of the X-fer bus by the Interface to load control information into the Formatter's control registers. In this mode, the Interface places an 8-bit control argument on the X-fer bus, then pulses one of the "set control lines"

- LOAD DRIVE ADDRESS<sub>0</sub>
- LOAD SECTOR<sub>0</sub>
- LOAD DIFFERENCE<sub>0</sub>
- or
- LOAD COMMAND<sub>0</sub>

causing the Formatter to store the X-fer bus argument in the appropriate control register.

The *second* mode of operation involves the use of the X-fer bus by the Interface to retrieve system status information from the Formatter. In this mode, the Interface activates one of the status gate lines

- *GATE STATUS<sub>0</sub>*
- *GATE SENSE<sub>0</sub>*

and the Formatter places the appropriate status byte on the X-fer bus for storage in the interface.

The *third* mode of operation involves the use of the X-fer bus under control of the Formatter, for transferring diskette system data (read or write). The Formatter automatically activates

- *TRANSFER REQUEST<sub>0</sub>*

whenever a new byte of data is either to be read or written, simultaneously forcing the

- *TRANSFER DIRECTION<sub>0</sub>*

signal to indicate the direction of transfer. The Interface acknowledges the requested transfer by activating the

- *TRANSFER GRANT<sub>0</sub>*

line.

The *BUSY<sub>0</sub>* line indicates, to the Interface, that a command is being executed, so that the Interface does not activate any control line. The *INTERRUPT<sub>0</sub>* line is driven by the Formatter to indicate to the Interface completion of a non-immediate command or an error condition.

II.1.2 CONTROL LINES

II.1.2.1 Load Drive Address<sub>0</sub>

This signal clocks the data on the X-fer bus into the Formatter's Drive Address Register. The Interface places the desired drive address in the format shown below on the X-fer bus and pulses

— LOAD DRIVE ADDRESS<sub>0</sub>

with a negative pulse.

7	6	5	4	3	2	1	0
Optional Format	512/»1» 256/»0»	NA	NA	Deselect	Drive Address 4	Drive Address 2	Drive Address 1

Bits 0-2 are the binary drive address. Bit 3 deselects all drives if it is active. Bit 7 specifies an optional format and bit 6 specifies 512 byte records (0 = 256 byte records). Pulsing of the Load Drive Address<sub>0</sub> line forces a deselection/selection sequence at the drive interface of the Formatter. That is, the previously selected drive is deselected, and if the DESELECT bit (3) is inactive, another drive is selected according to the newly loaded drive address. In addition, the format used on the newly selected drive is set at this time. Note that any drive may operate on 128, 256 or 512 byte records.

II.1.2.2 Load Difference

This signal clocks the data on the X-fer bus into the Formatter's Track Difference Register. The Interface places the desired difference argument (shown below) on the X-fer bus, then pulses

— LOAD DIFFERENCE<sub>0</sub>

with negative pulse.

7	6	5	4	3	2	1	0
P-direct »1»=FWD »0»=REV	Diff 64	Diff 32	Diff 16	Diff 8	Diff 4	Diff 2	Diff 1



Bits 0-6 are the binary value of the difference between the current physical track location and the desired track. This value is the number of steps to be taken in a subsequent seek command. Bit 7 designates the direction of stepping.

If this bit is true, the R/W head will be accessed "in" to a higher track address; if this bit is false the R/W head will be accessed "out" to a lower track address.

Note that there is no detection of invalid difference arguments.

**II.1.2.3**     *Load Sector*

This signal clocks the data on the X-fer bus into the Formatter's Sector Address Register. The Interface places the desired sector address (record number) in the format (shown below) on the X-fer bus, then pulses

— *LOAD SECTOR<sub>0</sub>*

with a negative pulse.

7	6	5	4	3	2	1	0
NA	Sector Address 64	Sector Address 32	Sector Address 16	Sector Address 8	Sector Address 4	Sector Address 2	Sector Address 1

There is no detection of invalid sector arguments when the sector byte is loaded. The error will be detected when a Read/Write command is started.

Bits 0-6 are the Binary Record Address which will be used as the next search argument for a

- *READ DATA*
- *WRITE DATA*
- or*
- *WRITE DELETED DATA*

operation.

Note that an all zero byte is not valid and will result in a read/write of an indeterminate record.

#### II.1.2.4 *Load Command<sub>0</sub>*

This signal clocks the data on the X-fer bus into the Formatter's Command Register. The Interface places the command byte, in the format shown below, on the X-fer bus, then pulses

— *LOAD COMMAND<sub>0</sub>*

with a negative pulse.

7	6	5	4	3	2	1	0
Control Reset	Recall- brate	Seek	Read Data	Read ID	Write Deleted Data	Write Data	Format Track

A valid command argument has only one bit active, since each bit denotes a unique operation to be performed by the Formatter. If two or more command bits are specified, the Formatter sequence is indeterminate and will result in a Unit Check (Status I Bit 4).

#### Command Descriptions

##### II.1.2.4.1 IMMEDIATE COMMAND

###### II.1.2.4.1.1 Control Reset

This command is used by the **Interface** to halt a command in process or to ensure that all interrupts and status are cleared. The Command Register, Read/Write Control Circuitry, Interrupt Circuitry, and Status and Sense Registers are reset with this command.

The command is immediately executed and does not generate BUSY or INTERRUPT. However, no new command should be loaded for 8 $\mu$ s to allow the system to fully reset.

CONTROL RESET does not deselect the currently selected drive.

##### II.1.2.4.2 SEEK COMMANDS

###### II.1.2.4.2.1 Recalibrate

The RECALIBRATE function provides a means of automatically accessing the selected drive's R/W head to track 00. This command is used to correctly orient the access circuitry after system powerup, or when the system detects a seek error.

The RECALIBRATE command causes the Formatter access circuitry to STEP the selected drive's R/W head to the outermost track. The Formatter then generates an INTERRUPT and presents a status of SEEK COMPLETE (Status I Bit 7). The execution time of this command is 0.8 seconds, maximum.

#### II.1.2.4.2.2 Seek

The seek function provides R/W head accessing for the selected drive, positioning the R/W head to any one of the 77 tracks on the selected drive's diskette. A prerequisite track difference argument must be sent by the Interface with a LOAD DIFFERENCE<sub>0</sub> signal. At the reception of the subsequent SEEK command, the Formatter steps the R/W head at nominal rate of 10ms/track (plus 10ms for the last track due to R/W head settling). When the Formatter has stepped the R/W head the number of times designated by the difference register, it generates an interrupt with a corresponding status of SEEK COMPLETE. (Status I Bit 7)

There is no error detection circuitry for the SEEK function.

*The Formatter merely issues the required number of step pulses to the selected drive.*

Mechanical stops prevent the R/W head from exceeding travel limits; however, an invalid difference argument may result in head positioning at an unformatted track. RECALIBRATE can be used for error recovery.

The Interface should command READ ID after every SEEK command in order to verify head position. That is, the Interface should compare the first byte of any *ID field* with the assumed track address and interpret a mis-comparison as a SEEK error.

#### II.1.2.4.3 READ COMMANDS

##### II.1.2.4.3.1 Read ID

The READ ID command causes the Formatter to transfer the first *ID field* encountered by the Read/Write head on the selected drive. The four bytes of data contained in the *ID field* are transferred to the Interface via the X-fer bus. The contents of the bytes are illustrated in Figure III.3.2.

#### II.1.2.4.3.2 Read Data

The READ DATA command provides for the transfer of the data fields of a requested record from the diskette to the Interface. The READ DATA command forces the Formatter to read each *ID field* encountered (not transferring bytes to the Interface) until a comparison is obtained between the third byte of an *ID field* (sector byte) and the desired sector. The Formatter then reads the next data field encountered, transferring each data byte (excluding the *data field address mark* to the Interface.

#### II.1.2.4.4 WRITE COMMANDS

##### II.1.2.4.4.1 Write Data

The WRITE DATA command provides the **system** function of storing a record on the selected drive's diskette.

This command forces the Formatter to read each *ID field* encountered until a comparison is obtained between the third byte of an *ID field* (sector byte) and the desired sector. The Formatter then sequences up the Write Circuitry in the gap following this *ID field* and starts writing zero bytes. At the end of the gap (17 bytes) the Formatter writes the *data address mark* and requests the Interface to provide the first data byte. The Formatter then writes the *data field* controlling the transfer of each data byte from the Interface.

After writing the *data field*, the Formatter writes two *CRC bytes* which have been generated over the *data field* (including the *address mark*).

##### II.1.2.4.4.2 Write Deleted Data

The WRITE DELETED DATA command is operationally identical to the WRITE DATA command, but results in the Formatter writing a *Deleted Data Address Mark* byte in front of the *data field*.

##### II.1.2.4.4.3 Format Track

The Format Track command provides the function of writing an entire track of information. (Refer to Figure III.3.2.)

When executing this command, the Formatter provides all *gaps*, *address marks*, and *CRC bytes* while the Interface provides the 4 *ID bytes* and all *data bytes* for each record (under Formatter transfer control).

## II.1.3 STATUS LINES

### II.1.3.1 Gate Status (Status I)

This signal is driven by the Interface and forces the Formatter to place the status byte, shown below, on the X-fer bus for acceptance by the Interface. Gating occurs whenever this line is driven to a logical zero level.

7	6	5	4	3	2	1	0
Seek Complete	R/W Complete	Deleted Record	Unit Check	NA	NA	NA	NA

Reset of all bits occurs at the end of the GATE STATUS<sub>0</sub> signal, that is, after the status acceptance by the Interface. The system must pulse GATE STATUS<sub>0</sub> after every interrupt to obtain further interrupts.

#### II.1.3.1.1 STATUS BIT DESCRIPTIONS

##### II.1.3.1.1.1 Seek Complete (Status I Bit 7)

This status bit is set at the completion of any SEEK or RECALIBRATE command (even if the command results in no head movement). It generates an interrupt to the Interface.

##### II.1.3.1.1.2 R/W Complete (Status I Bit 6)

This status bit is set at the normal completion of any READ or WRITE command. It generates an interrupt to the Interface.

##### II.1.3.1.1.3 Deleted Record (Status I Bit 5)

This status bit is set during a READ DATA command if the *data field* is preceded by a *Deleted Data Address Mark*.

##### II.1.3.1.1.4 Unit Check (Status I Bit 4)

This bit is set whenever any error condition is detected by the Formatter, specifically, when the SENSE BYTE transition from no error bits to any error bit active. Detection of a UNIT CHECK condition generates an interrupt to the Interface.

II.1.3.2 *Gate Sense (Status II)*

This signal is driven by the Interface and forces the Formatter to place the SENSE BYTE (error conditions shown below) onto the X-fer bus for acceptance by the Interface.

Reset of all of the bits occurs at the trailing edge of the GATE SENSE<sub>0</sub>, that is, after sense acceptance.

*Note that the presence of any sense bit generates a UNIT CHECK interrupt.*

The Interface *must* pulse GATE SENSE<sub>0</sub> whenever the UNIT CHECK status bit is set in order to obtain further error detection and command processing.

Status II as presented on the X-fer bus:

7	6	5	4	3	2	1	0
NA	Data Overrun	NA	CRC Error	Sector Missing NO AM	NA	Write Protect	Drive Not Ready

II.1.3.2.1 SENSE BIT DESCRIPTIONS

II.1.3.2.1.1 Data Overrun (Status II Bit 14)

This bit is set if the Interface fails to respond to a TRANSFER REQUEST by the Formatter within a time interval which insures data integrity. In the case of a write operation, the Interface must supply a new byte on the X-fer bus and supply the TRANSFER GRANT signal within 26 microseconds of the TRANSFER REQUEST signal.

II.1.3.2.1.2 CRC Error (Status II Bit 12)

This bit is set during a READ command or during orientation for a WRITE command if a read error is detected for any *ID field* or *data field* read from the selected diskette. A read error is determined by use of a Cyclic Redundancy Code (CRC). Two *CRC bytes* are appended to every field written on the diskette and during a read operation, the CRC is regenerated for the read data and compared with the CRC recorded on the diskette (checked for syndrome = 0). A mismatch denotes a read error.

#### II.1.3.2.1.3 Sector Missing and No AM (Status II Bit 11)

This bit is set if the desired diskette sector for a READ DATA, WRITE DATA, or WRITE DELETED DATA command cannot be located by the Formatter. It compares the third byte of each *ID field* encountered with the sector byte which has been transferred by the Interface. If there is no comparison within a full revolution of the diskette, the desired sector (record number) is not locatable. In addition, this bit may indicate a non-locatable *data field address mark*.

This error bit can also indicate that the appropriate *ID field address mark* is not locatable for the above commands or the READ ID command.

#### II.1.3.2.1.4 Write Protect (Status II Bit 9)

This bit is set if a write operation is attempted on a *Write protected* diskette (see Drive Reference Manual for details on the Write Protected Diskette).

#### II.1.3.2.1.5 Drive Not Ready (Status II Bit 8)

This bit is set if:

- *the addressed drive has no power,*
- *its door is open,*
- *the diskette is not properly installed,*  
*or*
- *the drive address is invalid.*

## II.1.4 DATA TRANSFER CONTROL LINES

### II.1.4.1 *Transfer Direction*

This signal is driven by the Formatter to the Interface to indicate the direction of data transfer on the X-fer bus. A logical zero (true) on this line indicates that data is to be transferred from the Interface to the Formatter and a logical one indicates the reverse direction of transfer. This signal is valid only when TRANSFER REQUEST is active.

#### II.1.4.1.1 TRANSFER REQUEST

This signal is driven by the Formatter to the Interface to initiate the transfer of a data byte during the execution of any READ or WRITE command. During a read operation, this signal is forced active (logical zero) when the last bit of a new byte has been read from the diskette and that byte is active on the X-fer bus. During a write operation, this signal is activated and requests the Interface to place the next byte to be written on the X-fer bus. This signal goes to the inactive state when the Interface responds with X-fer bus.

#### II.1.4.1.2 TRANSFER GRANT

This signal is driven by the Interface to the Formatter in response to the TRANSFER REQUEST signal. During a READ operation, this signal is activated (logical zero) when the data byte on the X-fer bus has been stored by the Interface. During a WRITE operation, this signal is activated after the requested data byte has been placed on the X-fer bus by the Interface. This signal transition deactivates when the TRANSFER REQUEST signal goes inactive.



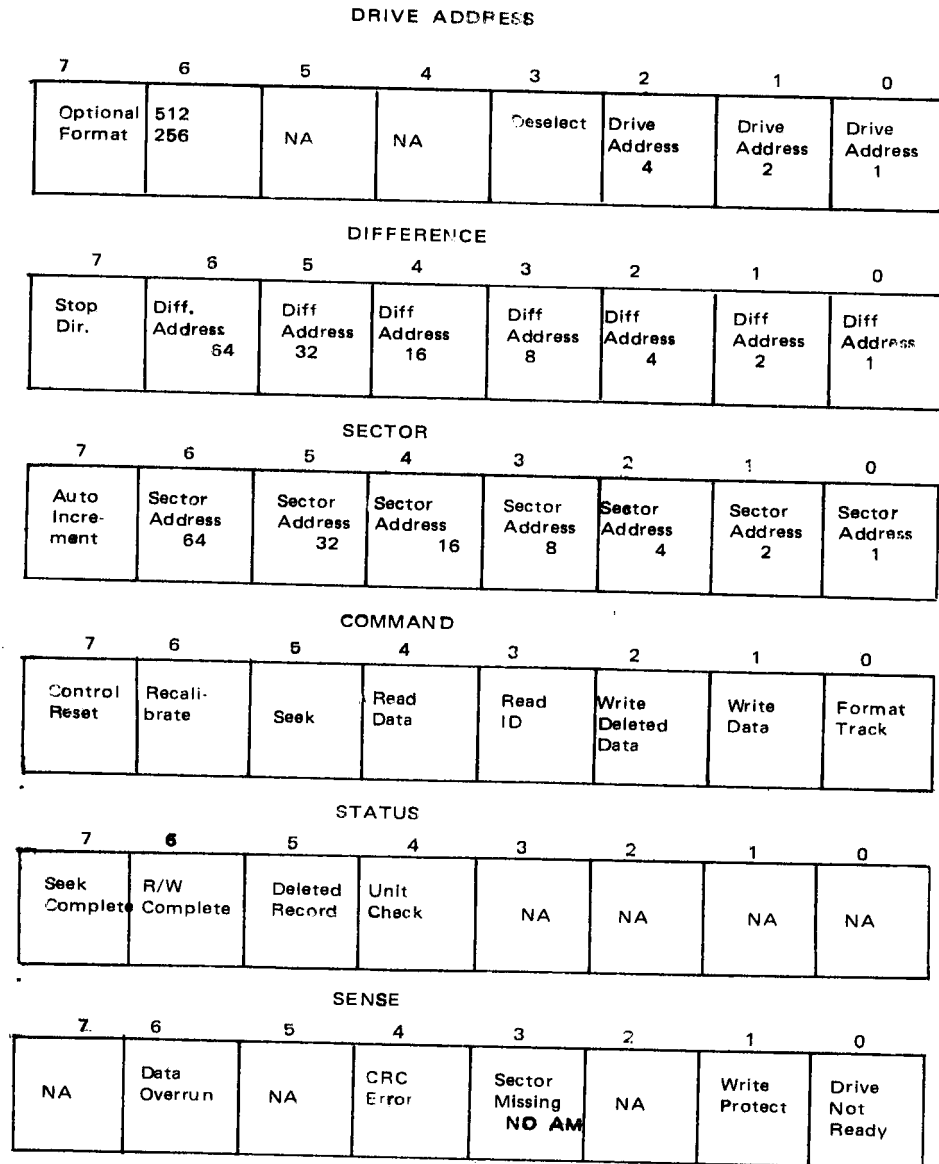


Figure II.1.2: X-fer Bus Usage and Bit Assignment (excluding data)

**II.1.5**      *SPECIAL PURPOSE LINES***II.1.5.1**    *Busy*

This signal is sent to the Interface whenever a command is being executed. The Interface must insure that this signal is inactive before forcing any of the SET CONTROL or GATE STATUS. lines.

**II.1.5.2**    *Interrupt*

This signal is sent to the Interface to flag the completion of command execution (exception CONTROL RESET) or the detection of an error. If an error is detected, the command under execution is automatically reset. (It is reset by the trailing edge of the GATE STATUS line.)

**II.1.5.3**    *Reset*

This signal performs a general reset to the Formatter, equivalent to turning on system power. This is an asynchronous signal and is generally used only in error recovery.

*Note the following difference between the Reset line and the Control reset command:*

*The Reset line deselects all drives, while the control reset does not.*

**II.2 GENERAL COMMAND SEQUENCE – INTERFACE/FORMATTER**

**II.2.1 GENERAL**

In order to study a command sequence, a proper knowledge of the Interface Formatter is required. Refer to Chapter II.1.

**II.2.2**      *OPERATION*

A general command sequence is initiated from the CPU by executing an IOX <WCWD> (write control word). Control gates will place the upper byte of the Control Word on the X-fer bus as a command argument and pulse the LOAD COMMAND<sub>0</sub> line. In the Formatter, the argument will be placed into the Command Latch and a BUSY<sub>0</sub> signal will be sent back to the Interface and set the Busy FF, which has a busy status (RSR1 Bit no. 2) available for the CPU. (A new command must not be issued from the CPU while the Interface is in a Busy state.)

II.2.3 *COMMAND CLASSIFICATIONS*

The Formatter will start processing the specified command, exchange the required data and control information with the selected unit.

The commands presented on the X-fer bus may be classified into three groups:

- *Commands that perform any READ or WRITE operation*
- *Commands that perform any SEEK operations*
- *Immediate command (Control reset)(No Busy or Interrupt generated)*

WCWD Bit No.:	X-fer Bit No.:	Command:	Group:
8	0	Format track	Any
9	1	Write data	Read
10	2	Write Deleted Data	or
11	3	Read ID	Write
12	4	Read Data	
13	5	Seek	Any
14	6	Recalibrate	Seek
15	7	Control reset	Immediate command

#### II.2.4 READ DATA COMMAND (example)

Let us assume a Read Data operation is specified.

Since this command belongs to any READ or WRITE group, the "R/W Idle" becomes inactive as the Formatter starts processing the command.

Then, when the READ operation is accomplished, i.e., one sector of data is transferred from the unit to the Formatter to the Data Buffer in the Interface, the "R/W Idle" goes to its active state which in turn clears the Command Register. Sensing the Command Register in its cleared state, the  $BUSY_0$  signal will drop. However, the  $BUSY_0$  signal is buffered in the Interface and remains set for some additional time. (Refer to Figure II.2.1.) Provided no R/W Error condition has occurred, the INTERRUPT line will be activated. The INTERRUPT signal received from the Formatter has two main tasks to handle in the Interface.

- *Pass on the Interrupt to the CPU*
- *Generate a Gate Status ( $GSTAT_0$ ) signal back to the Formatter requesting the status byte to be placed on the X-fer bus.*

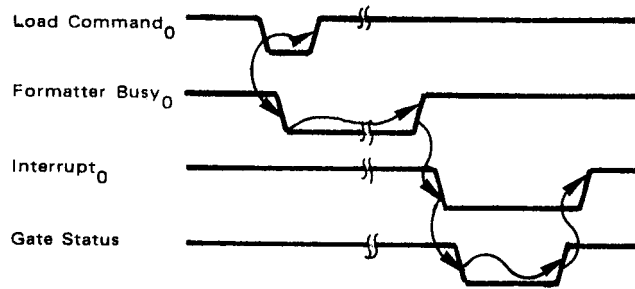
When the GATE STATUS (GSTAT) signal drops (pulse width 0,7 – 1,3 $\mu$ s) the X-fer bus holding the status information will be latched into a 4 bits status latch located on the "Floppy Disk Data card". As the GSTAT is dropped (timed out) a RST STATUS<sub>0</sub> (Reset Status) signal is activated in the Formatter. This signal has two functions:

- *Read Status indicators in the Formatter*  
*thus,*
- *dropping the Interrupt line*

The interrupt line will, in turn, drop the Busy FF in the Formatter.

Since the CPU received an Interrupt, it reads the fresh status information (which initially caused the interrupts) from the Interface.

It should be observed that the CPU will be presented with a 16 bit status word where bits 4 through 7 are derived from the Formatter.

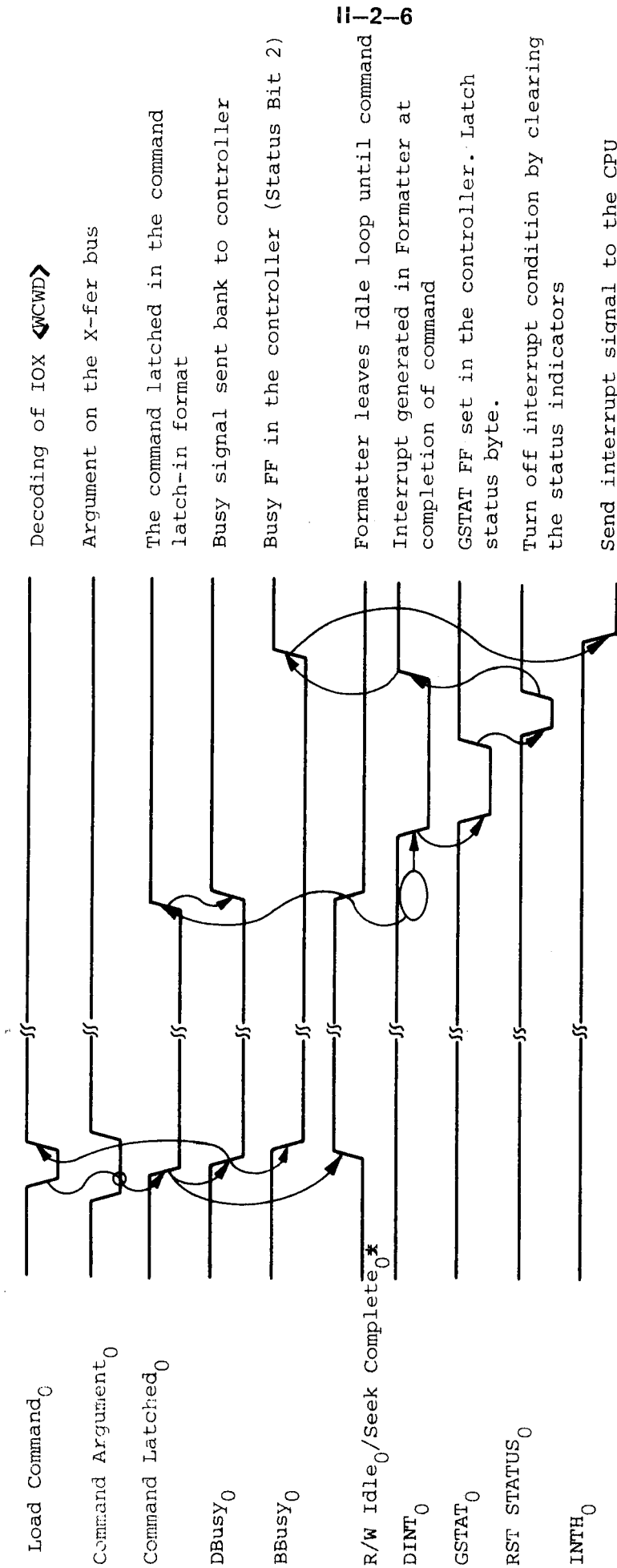


**Figure II.2.1:** *General Command Sequence – Principal Timing*

The sequence of events will be the same for commands belonging to the any SEEK group with the following exception.

- *The Formatter R/W Idle signal will, in this case, be replaced by SEEK COMPLETE giving the same sequence as described above.*

If a Control Reset, classified as an immediate command, is issued, no BUSY or INTERRUPT signals are sent back to the Interface.



Decoding of IOX  $\leftarrow$  WCWD  $\rightarrow$

Argument on the X-fer bus

The command latched in the command latch-in format

Busy signal sent bank to controller

Busy FF in the controller (Status Bit 2)

Formatter leaves Idle loop until command

Interrupt generated in Formatter at completion of command

GSTAT FF set in the controller. Latch status byte.

Turn off interrupt condition by clearing the status indicators

Send interrupt signal to the CPU

\* 'R/W Idle' applies to 'Any Read of Write' command while 'Seek Complete' applies for 'Any Seek' operation.

$\Delta t$  = No significant time for 'Any Seek' operation. 10 $\mu$ s for 'Any read or write' operation.

Figure 11.2.2: General Command Sequence



II.3 INTERRUPT GENERATION AND HANDLING

II.3.1 GENERATION

The Floppy disk Interface is wired up to interrupt level  $11_{10}$ . The various interrupt sources are discussed and illustrated at a general level.

The interrupt system is enabled in the Interface by specifying bit no. 1 in the control word.

Refer to Figure III.3.1.

:  
SAA 2  
IOX WCWD (1563)

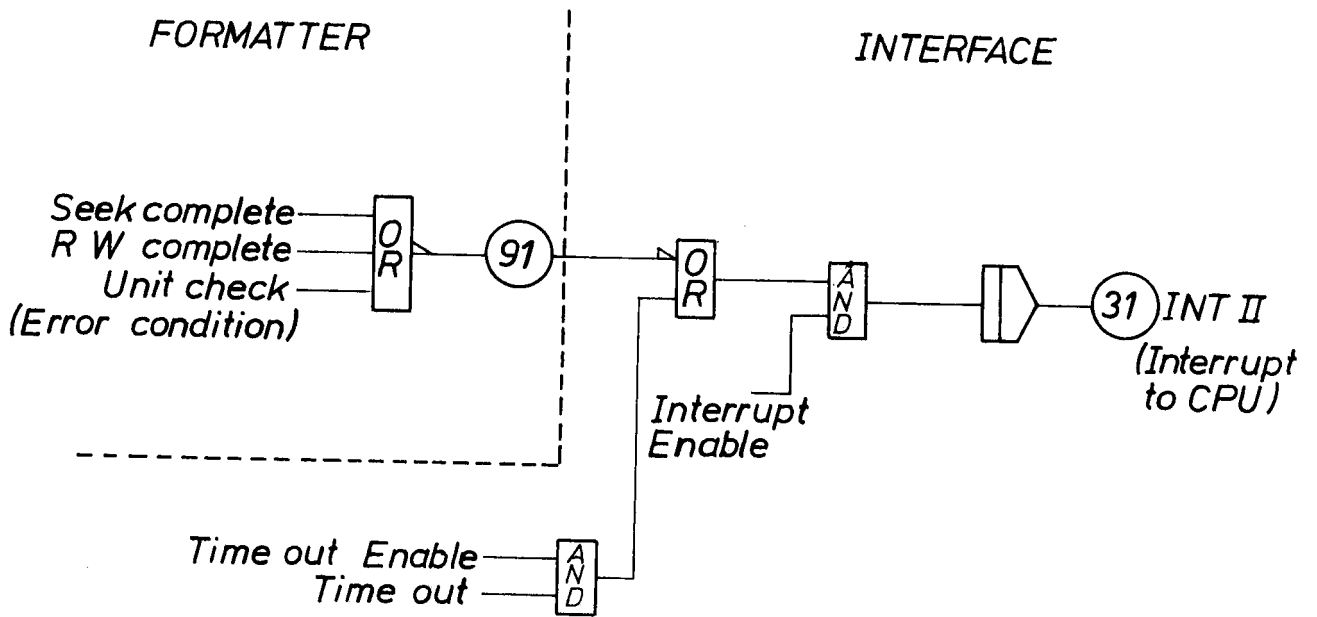


Figure III.3.1: Interrupt System – Principal Ooperation

One interrupt condition – TIMEOUT – originating in the Floppy Disk Control card, enabled by WCWD bit no. 6, while the remaining interrupt conditions originate in the Formatter and enter the Floppy Disk Control card on terminal 91, labelled DINT<sub>0</sub>. On completion of any command issued from the Interface, an INTERRUPT is generated in the Formatter. (Refer to the previous chapter, General Command Sequence.) An INTERRUPT is also generated in the Formatter if an error condition occurs (unit check) while executing a command. (The executing command is aborted.)

II.3.2 **READING STATUS**

Upon receiving an INTERRUPT and identifying the device, the CPU will read the device status to find out what happened and where (Interface, Formatter or unit).

Since the IOX <RSR1> (Read Status Register no. 1) communicates with the Interface only it is the Interface which is responsible for maintaining fresh status information for the CPU.

This is accomplished via an automatic feature in the Interface Formatter communication. Upon reception of an INTERRUPT from the Formatter, the Interface will gate the status information from the Formatter to the Interface. The CPU will, thus, receive status information that corresponds to the INTERRUPT (refer to Figure II.3.2).

To obtain more information about an INTERRUPT sequence — a general command sequence should be studied (refer to Chapter II.2).

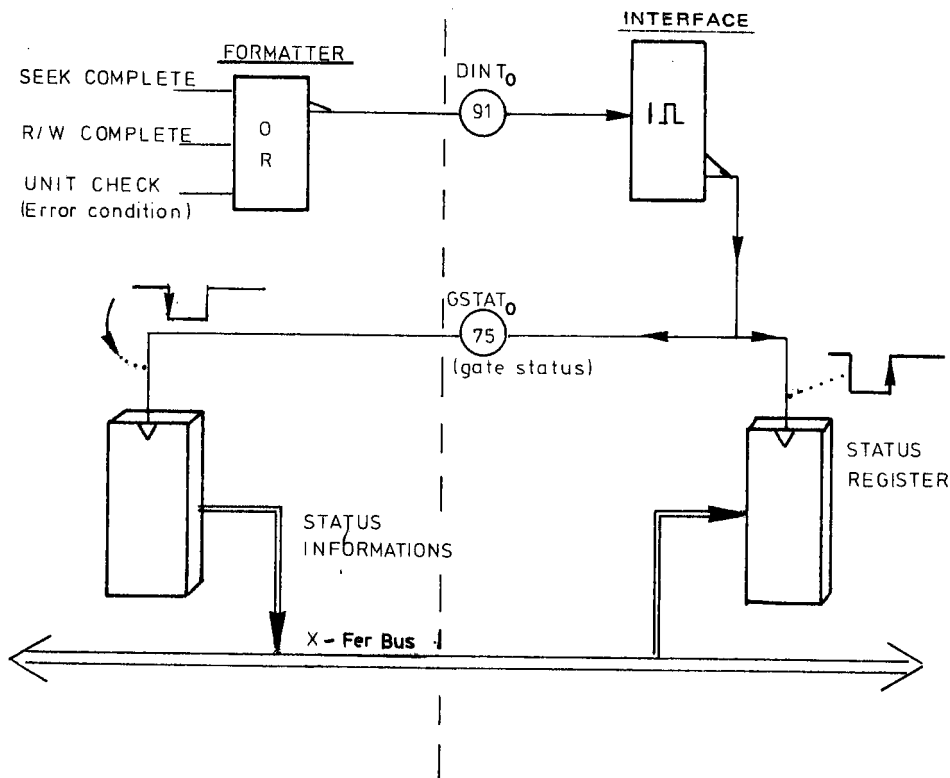


Figure II.3.2: *Gating Status*



## II.4 INTERFACE DATA ROUTES

### II.4.1 GENERAL DESCRIPTION

The following discussion refers to Figure II.4.1.

The Floppy Disk Data card communicates with the CPU on a 16 bit I/O bus labelled BD 0-15. The card also communicates with the Formatter over an 8 bits bi-directional bus labelled TBUS 0-7. All data exchanged between the Formatter (Floppy disk) and the CPU will be routed through a 1k 16 bits sequentially accessed Data Buffer.

This buffer can be used as a byte oriented memory (8 bits) or a word oriented memory (16 bits), i.e., two bytes may be accessed independently within the same buffer address by activating "CE1" or "CE2". (A 16 bits word will be accessed by activating both.)

As mentioned above, the Data Buffer will be accessed from two sources:

- *The CPU can access this buffer through execution of an IOX <RDAT> (Read) or IOX <WDAT> (Write) instruction.*

The 16 bits word length access will always be performed from the CPU.

- *The Formatter will also access this buffer over the 8 bits X-fer bus. A READ or WRITE operation is by a DIRECTION signal issued from the Formatter.*

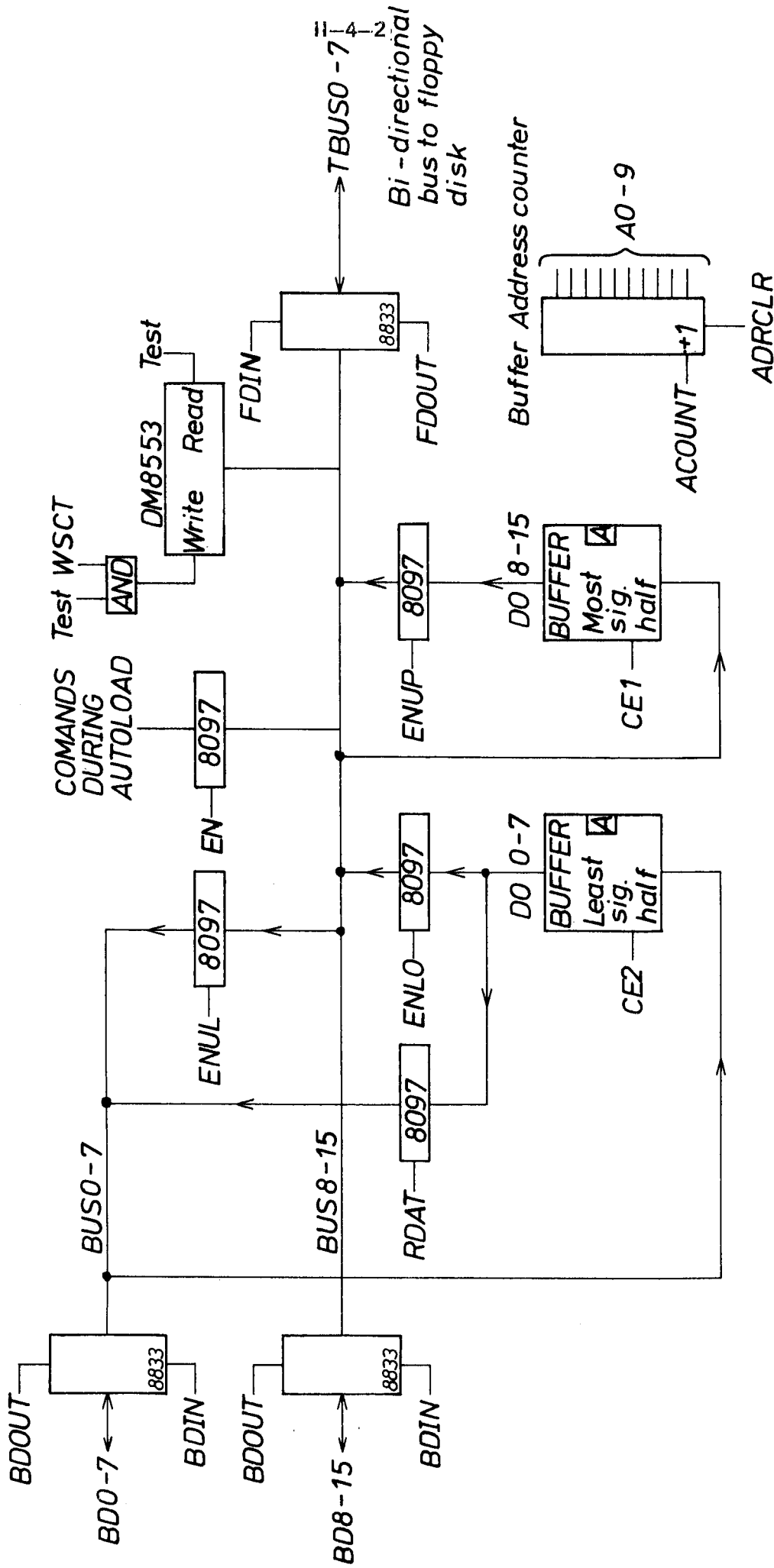
Eight bits data bytes will be assembled or disassembled in the Data Buffer when accessed from the Formatter.

The data exchanged between the Data Buffer and the Formatter over the X-fer bus, may be regarded as a DMA type of data transfer. The data transfer is initiated from the CPU – while an INTERRUPT from the Formatter indicates a transfer complete.

The upper part of the internal (BUS 8-15) is "connected" to the X-fer bus directly through an X-mitter/receiver circuit where "FDOUT" enables X-mission and "FDIN" enables reception.

The most significant half of the Data Buffer communicates with BUS 8-15.

BLOCK DIAGRAM 1118 (FLOPPY DISK DATA)



ND-11.012.01

Figure 11.4.1.

Data from the Formatter to the least significant half of the buffer must be enabled onto the lower internal bus (BUS 0-7) by the control signal "ENUL" before being written into the buffer.

Data to the Formatter, from the least significant part of the buffer, must be enabled onto the upper internal bus (BUS 8-15) before being enabled out to the Formatter. This is accomplished by the control signal "ENLO".

## II.4.2 ADDRESS COUNTER

A sequential address counter will contain the address of the next reference to be made in the Data Buffer.

Except for an *address register clear* operation, no address manipulation can be performed. As an automatic feature, the address is incremented by one for:

- *each access made from the CPU (IOX <RDAT> or IOX <WDAT>)*
- *every second access made from the Formatter (CE1 and CE2 will toggle to enable lower and upper bytes)*

Since the address register cannot be preset to any value (except zero by an *address counter clear* operation), all read or write should be started from address zero. It is, therefore, of importance to notice that:

- *before a READ or WRITE operation from the CPU or Formatter an "address counter clear" operation must be performed*

This is accomplished in one of four ways:

- *IOX <WCWD> with bit no. 5 specified (clear Interface buffer address)*
- *IOX <WCWD> with bit no. 4 specified (device clear)*
- *depressing the master clear button on CPU panel*
- *after buffer has been loaded with one sector of data (512 bytes) during a master clear load sequence (the start address is then prepared for the microprogram read operation)*

Refer to Figure II.4.2.



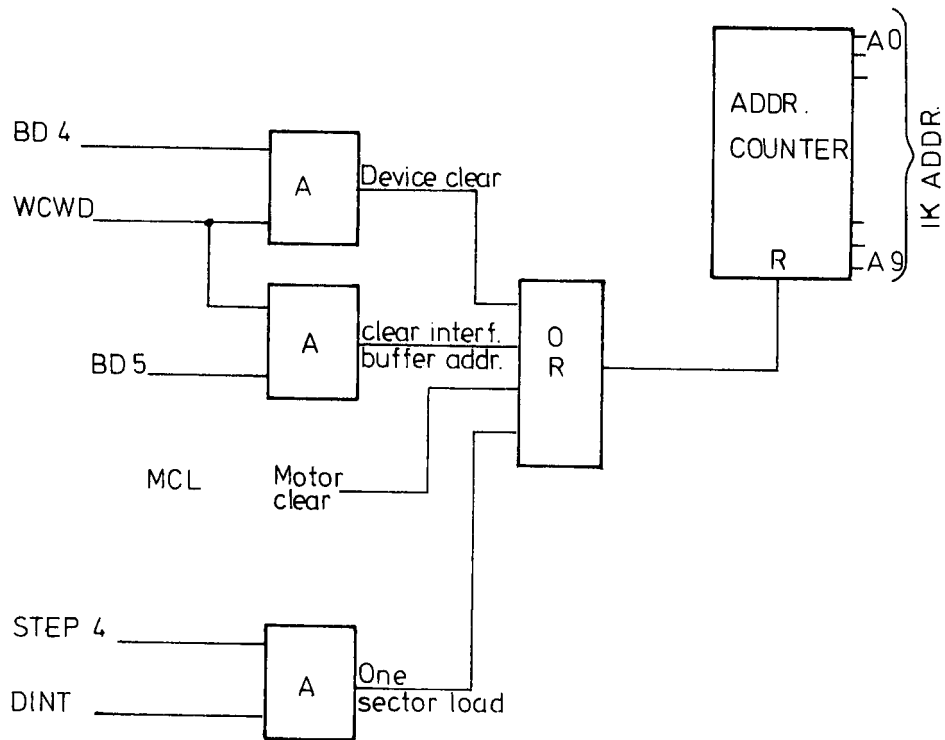


Figure II.4.2: Address Counter Clear Illustration

II.4.2.1 Address Counting

As previously mentioned, the counter is incremented by one for each access made from the CPU and every other access made from the Formatter. For more details, refer to Sections II.4.3 to II.4.6.

### II.4.3 READ DISK OPERATION

The program sequence in which a data read operation can be performed will be discussed separately.

In this section, we will handle the control signals involved during a data transfer from the Formatter to the Interface.

The following discussion refers to Figure II.4.1 and Figure II.4.3.

From the selected unit, the data and clocks will alternate on one line labelled READ DATA.

In the Formatter, data and clocks will be separated (described in Section III.4). Data will be assembled into 8 bit bytes in the Formatter; transferred to a Buffer Register driving the X-fer bus. A request (TREQ<sub>0</sub>) will be sent to the Interface. Looking at the DIRECTION line (TDIR), the Interface will know if a READ or a WRITE operation is in progress. (An inactive state indicates a read operation.)

Upon receiving the request signal, the following sequence will be initiated in the Interface. (Assuming an odd byte number X-ferred.)

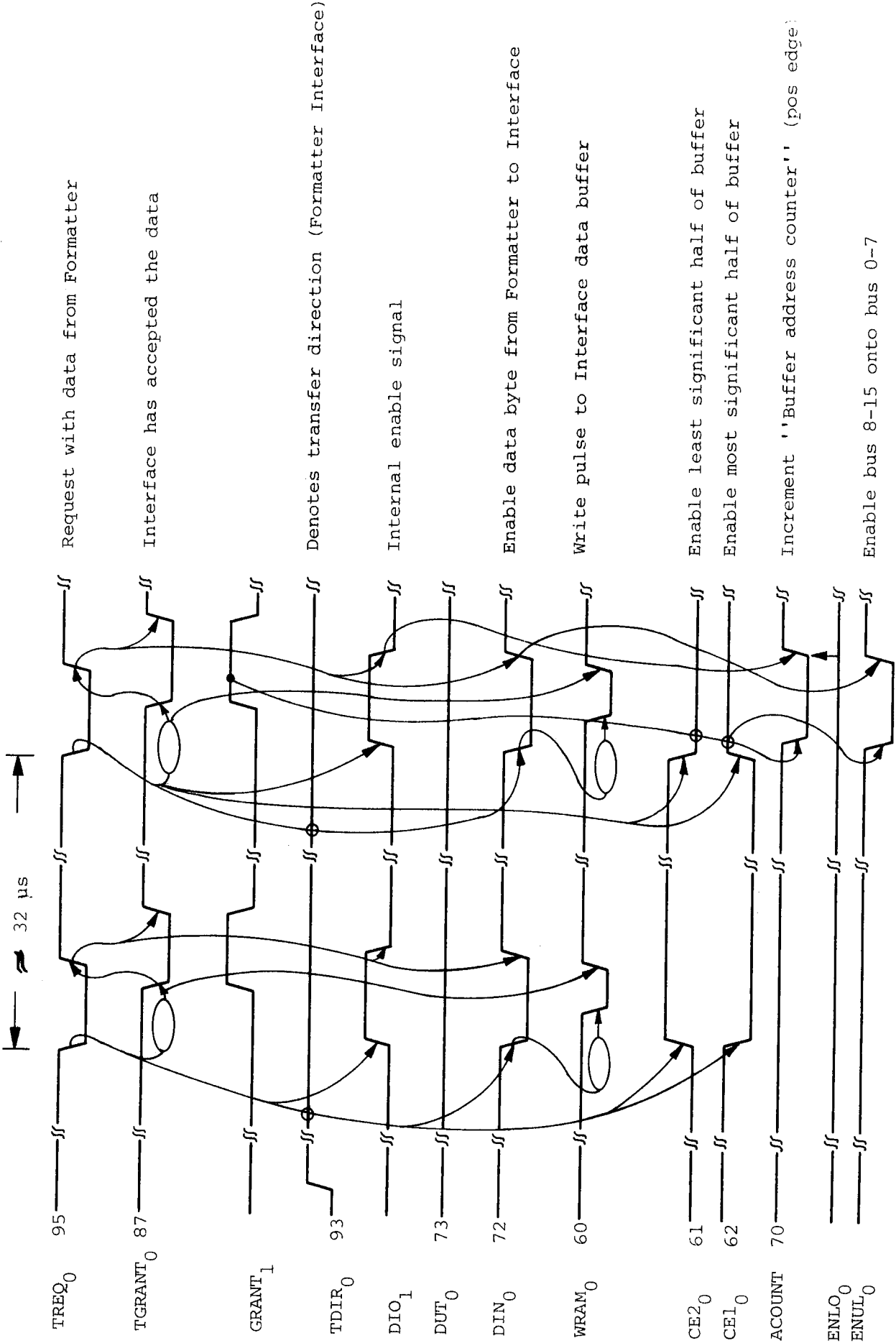
- *Enable X-mitter/receiver to receive data from the X-fer bus (DIN<sub>0</sub>)*
- *Chip enable 1 (CE1) will be turned on to enable the data bytes to the most significant half of the Data Buffer.*
- *after a short delay a write pulse will be sent to the Data Buffer (WRAM)*
- *as the write pulse drops, i.e., the Data Buffer has accepted the data, a GRANT (TGRANT) signal is sent back to the Formatter turning off the REQUEST (TREQ)*

Seeing the REQUEST line being dropped

- *the Interface will respond by turning off the GRANT (IGRANT) line.*

The sequence for an odd data byte has now been terminated.

(Interface/Formatter Control Timing)



**Figure 11.4.3: Read Disk Operation**  
(2 bytes transfer illustration)

After approximately  $32\mu\text{s}$ , the second or odd data byte is ready for transfer and the following sequence will be followed:

- *Enable X-mitter/receivers to receive data from the X-fer bus (DIN)*
- *Enabled Bus 8-15 (ENUL) onto Bus 0-7*
- *Chip selection will be toggled to turn on CE2 to enable the data into the least significant half of the Data Buffer*
- *after a short delay, a write pulse (WRAM) will be sent to the Data Buffer*
- *as the write pulse drops, i.e., Data Buffer has accepted the data, a GRANT (TGRANT) signal is sent back to the Formatter turning off the request (TREQ)*

Seeing the request line being dropped, the Interface will:

- *increment the Buffer Address Counter (ACOUNT)*
- *drop the GRANT (TGRANT) line*

The above described sequences will be repeated until one sector (512 bytes) of data is transferred.

In the Data Buffer, the 512 data bytes are packed into 256 CPU words. When the READ operation is completed, an INTERRUPT is given to the CPU. By analyzing the status word the CPU should know the Buffer Address Counter and commence reading the Data Buffer by means of IOX <RDAT> instructions.

#### II.4.4 WRITE DISK OPERATION

In this section, we will take a closer look at the control signals involved during a data transfer from the Interface to the Formatter. Refer to the Figure II.4.4 and Figure II.4.1 for the following discussion.

Data written on the diskette must, prior to a write operation, be placed in the Data Buffer.

However, this operation should start with a *Buffer Address Counter Clear* operation (WCWD bit no. 4 or WCWD bit no 5).

Data from the CPU will, by executing IOX <WDAT> (refer to Section II.4.5) be put into the Data Buffer in sequential order starting with address zero.

The operation should be appended with a *Buffer Address Counter Clear* operation.

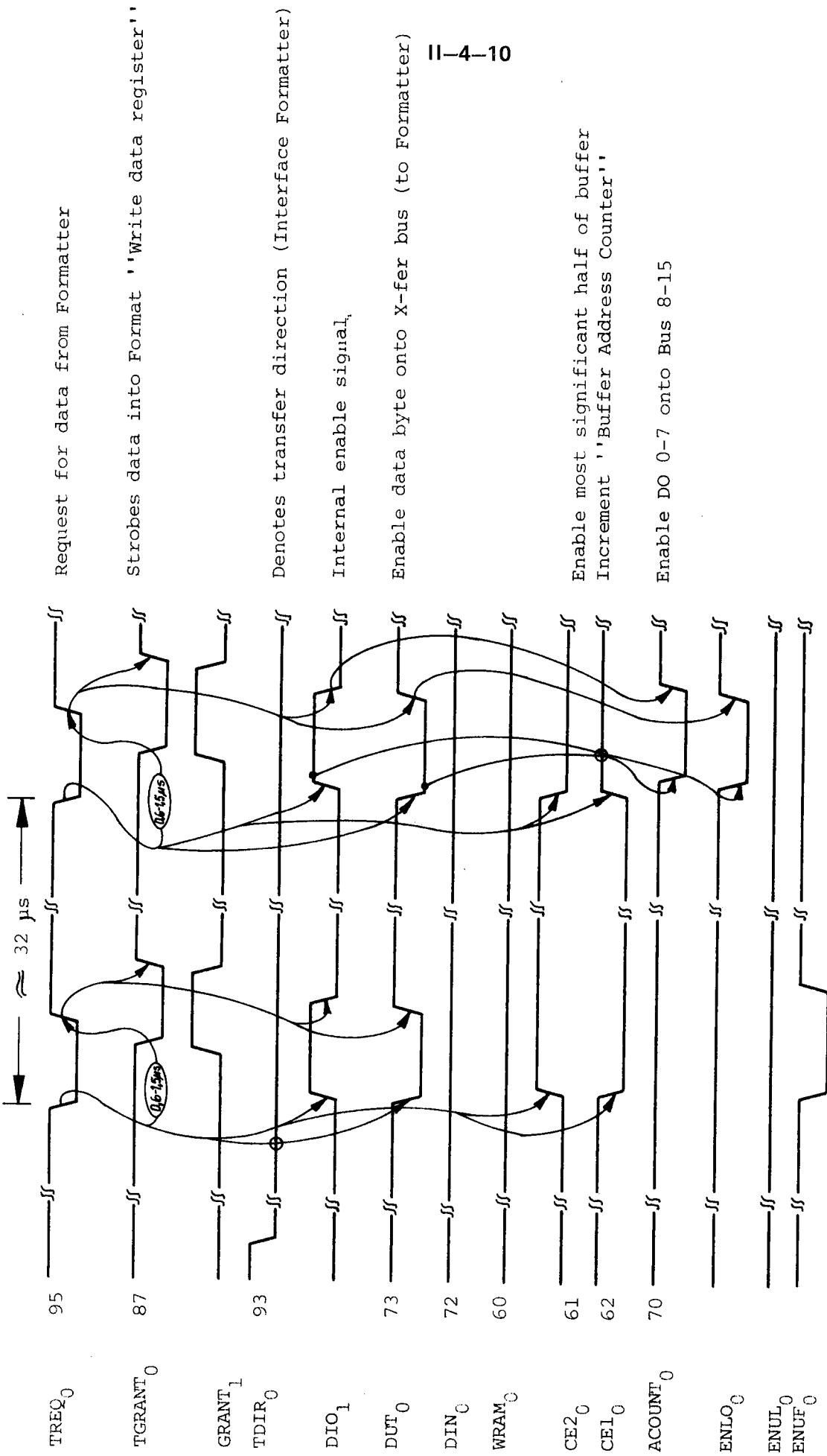
The actual unit will be prepared for a write operation.

Before the R/W head approaches the actual *data field*, the first data byte to be written on the diskette must be ready in a disassembly register in the Formatter. Prior to this, a request (TREQ) for the first data byte must have been issued from the Formatter. Since a WRITE operation is in progress, the DIRECTION line (TDIR) will be activated by the Formatter.

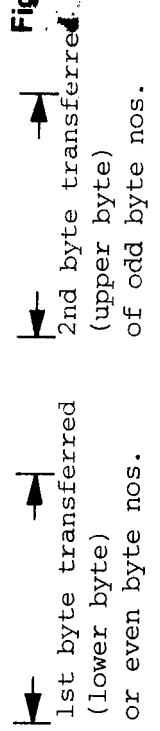
Receiving the REQUEST, the Interface will start the following sequence:

- *enable X-mitter/receivers to transmit data onto the X-fer bus (DUT)*
- *chip enable 1 will be turned on to enable data from the most significant half of the Data Buffer*
- *the write line (WRAM) is inactive, performing a read operation from the Data Buffer*
- *as a certain amount of time has elapsed, a GRANT (TGRANT) signal is sent back to the Formatter, indicating that a data byte is placed on the X-fer bus*
- *sensing the GRANT signal, the Formatter will pick up the first data byte and put it into the Data Write Register*
- *the Data Write Register will be copied into a Disassembling Register*

(Interface/Formatter Control Timing)



**Figure 11.4.4: Write Disk Operation**  
(2 bytes transfer illustration)



As the R/W heads move into the pre-requested data field (predefined part of the addresses sector) the data bits will start shifting out.

The data bits will be encoded with clock pulses and sent to the unit as WRITE DATA.

At this point in time, a new request will be made for the second byte.

The following will describe the sequence of events.

- *enable the X-mitter/receiver to transmit data onto the X-fer bus (DUT)*
- *enable Bus 0-7 onto Bus 8-15 (ENLO)*
- *chip selection will be toggled to turn on CE2 to enable the data from the least significant half of the Data Buffer*
- *the write line (WRAM) is inactive, performing a READ operation from the Data Buffer*
- *as a certain amount of time has elapsed, a GRANT (TGRANT) signal is sent back to the Formatter indicating that a data byte has been placed on the X-fer bus*
- *sensing the grant signal, the Formatter will pick up the data byte and put it into a Data Write Register and turn off the REQUEST line.*

Seeing the REQUEST line being dropped, the Interface will

- *increment the Buffer Address Counter (ACOUNT)*
- *drop the GRANT (TGRANT) line*

As the first data byte is shifted out to the unit, the disassembly register will be loaded in parallel from the Data Write Register and a new REQUEST will be issued. (The Data Write Register will, thus, function as a one byte buffer in the Formatter).

The above described sequence will be repeated until one sector is written on the diskette (512 bytes) and no more requests will be made.

As the write operation is finished an INTERRUPT is sent to the CPU to indicate termination of the requested operation (refer to Figure II.3.1).

#### II.4.5 WRITE DATA BUFFER

Prior to a write disk operation (data flow from the Data Buffer located in the Interface to the Formatter) the Data Buffer must be loaded with data. This is accomplished using IOX <WDAT> instructions. The data flow is illustrated in Figure II.4.5.

The sequence of control is described below. Refer to Timing Chart II.4.6.

- *IOXE timing signal received from CPU*
- *the transmitter/receivers are enabled to read data from the I/O bus (BDOUT)*
- *after a short delay, a delayed CONNECT is sent back to the CPU indicating an active transfer (DLCON)*
- *both the least and most significant parts of Data Buffer are constantly enabled (CE1 and CE2)*
- *when the data on the bus is assumed to be stable, a data write pulse is generated to the Data Buffer. A 16 bits data word is placed in the buffer*

When the IOXE signal from the CPU drops the:

- *delayed connect (DLCON) signal drops*
- and*
- *the write pulse drops*

A small delay is introduced before

- *disabling the receiver function*

to guarantee stable data during the entire write pulse period.

- *the Buffer Address Counter will be incremented (ACOUNT)*

when a WRITE Data Buffer sequence is terminated.



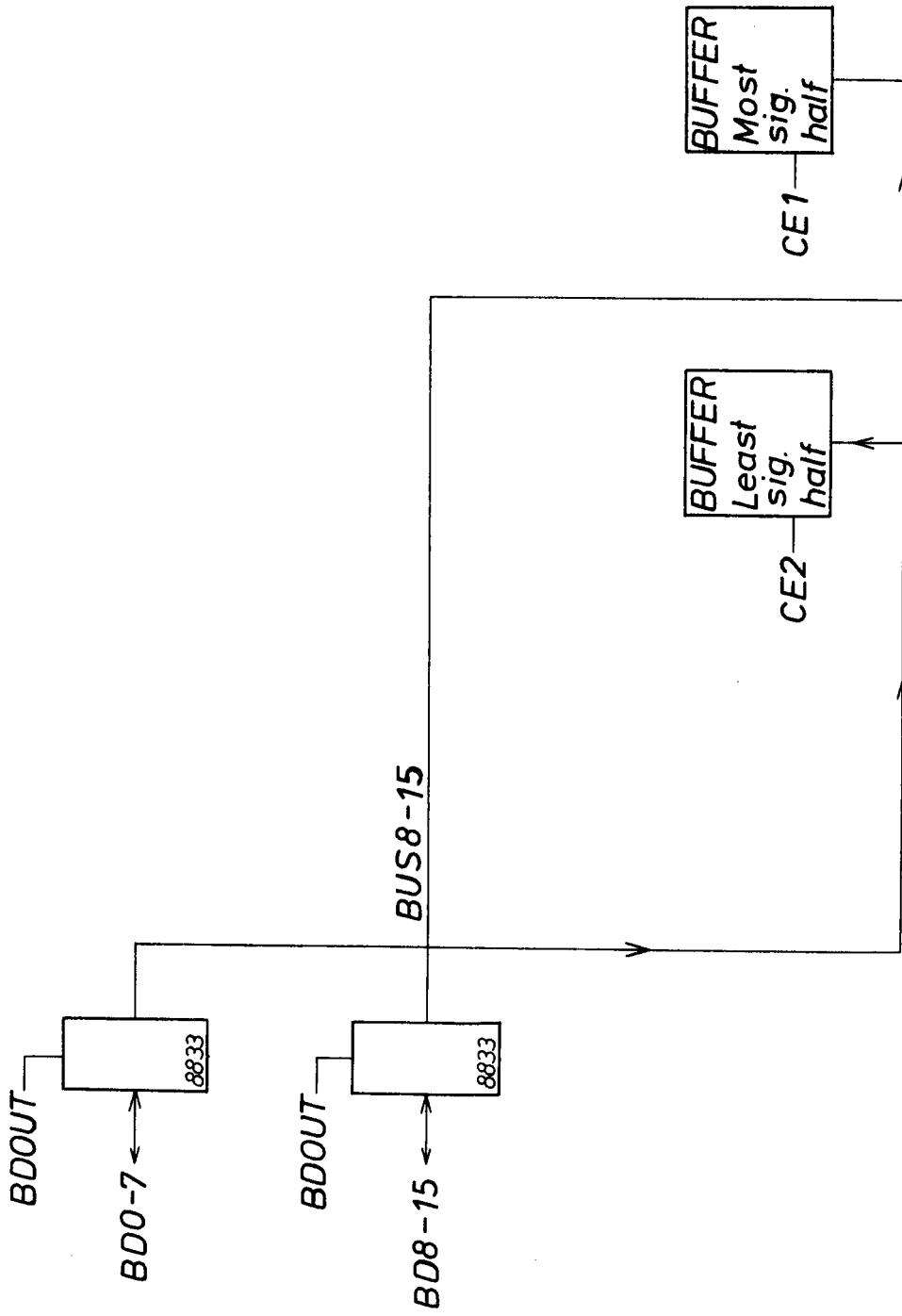


Figure 11.4.5: Write Data Buffer

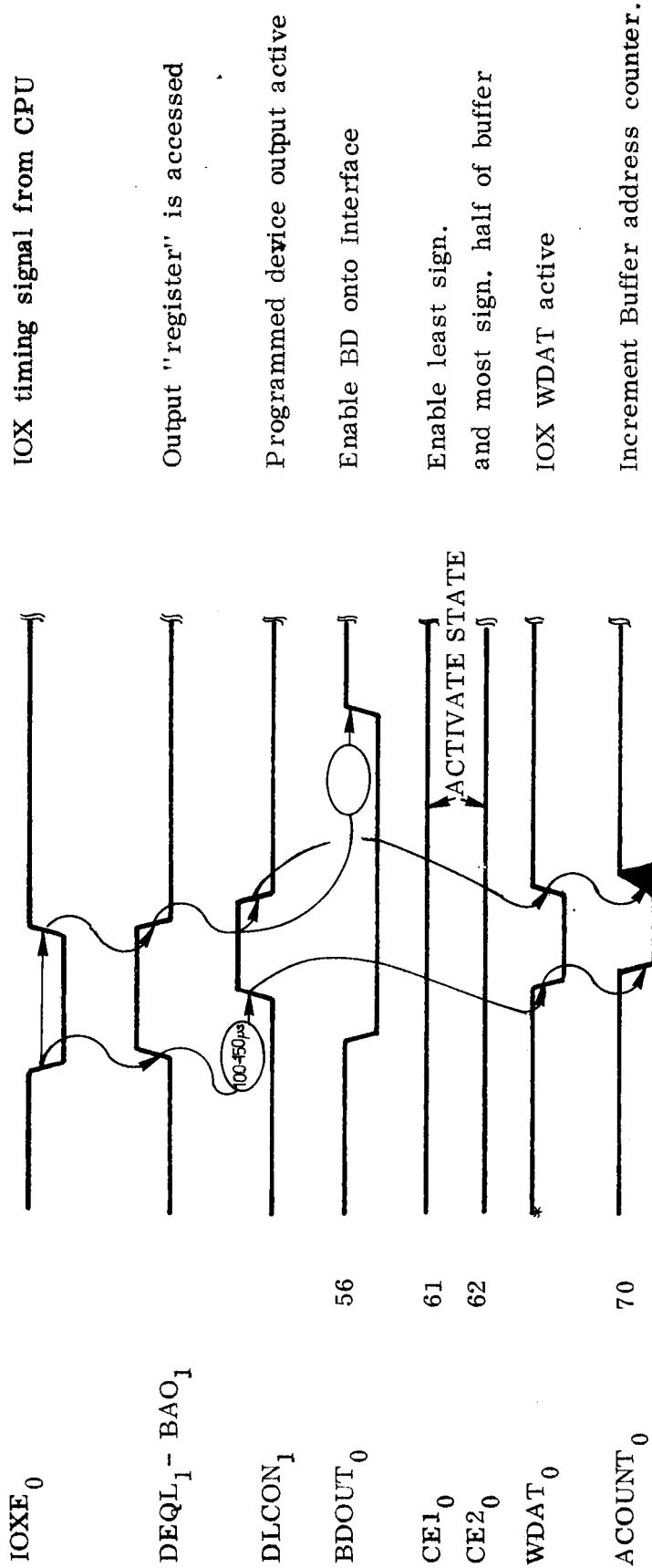


Figure II.4.6: Write Data Buffer - Timing Diagram

#### II.4.6 READ DATA BUFFER

After a read disk operation (data flow from the Formatter to the Data Buffer located in the Interface), the Data Buffer holds one sector of data equivalent to 512 bytes packed into 256 CPU words.

This Data Buffer will be transferred to the CPU by means of IOX <RDAT> instructions.

The data flow is illustrated in Figure II.4.7.

The sequence of control is described below. Refer to Timing Chart II.4.8 throughout the following discussion.

- *IOXE timing signal received from the CPU*
- *connect signal (CON) sent to the CPU to indicate an active transfer*
- *input signal (INP) generated to prepare for an input data transfer*
- *both least significant and most significant parts of Data Buffer are constantly enabled (CE1 and CE2)*
- *the output of the least significant half of the Data Buffer DO 0-7 is enabled onto the internal bus, BUS 0-7 (RDAT)*
- *the output of the most significant half of the Data Buffer DO 8-15 is enabled onto the internal bus, BUS 8-15 (ENUP)*
- *after a short delay, the internal data bus, BUS 0-15, is enabled onto the I/O bus (BDIN)*

When the IOXE signal drops from the CPU

- *the connect signal drops (CON)*
- *the input signal drops (INP)*
- *disable least (RDAT) and most (ENUP) significant bytes from Buffer onto internal bus*

After a short delay

- *disable the internal bus from the I/O bus (BDIN)*
- *the buffer address counter will be incremented (ACOUNT)*

The above sequence will be repeated until the Data Buffer is transferred.

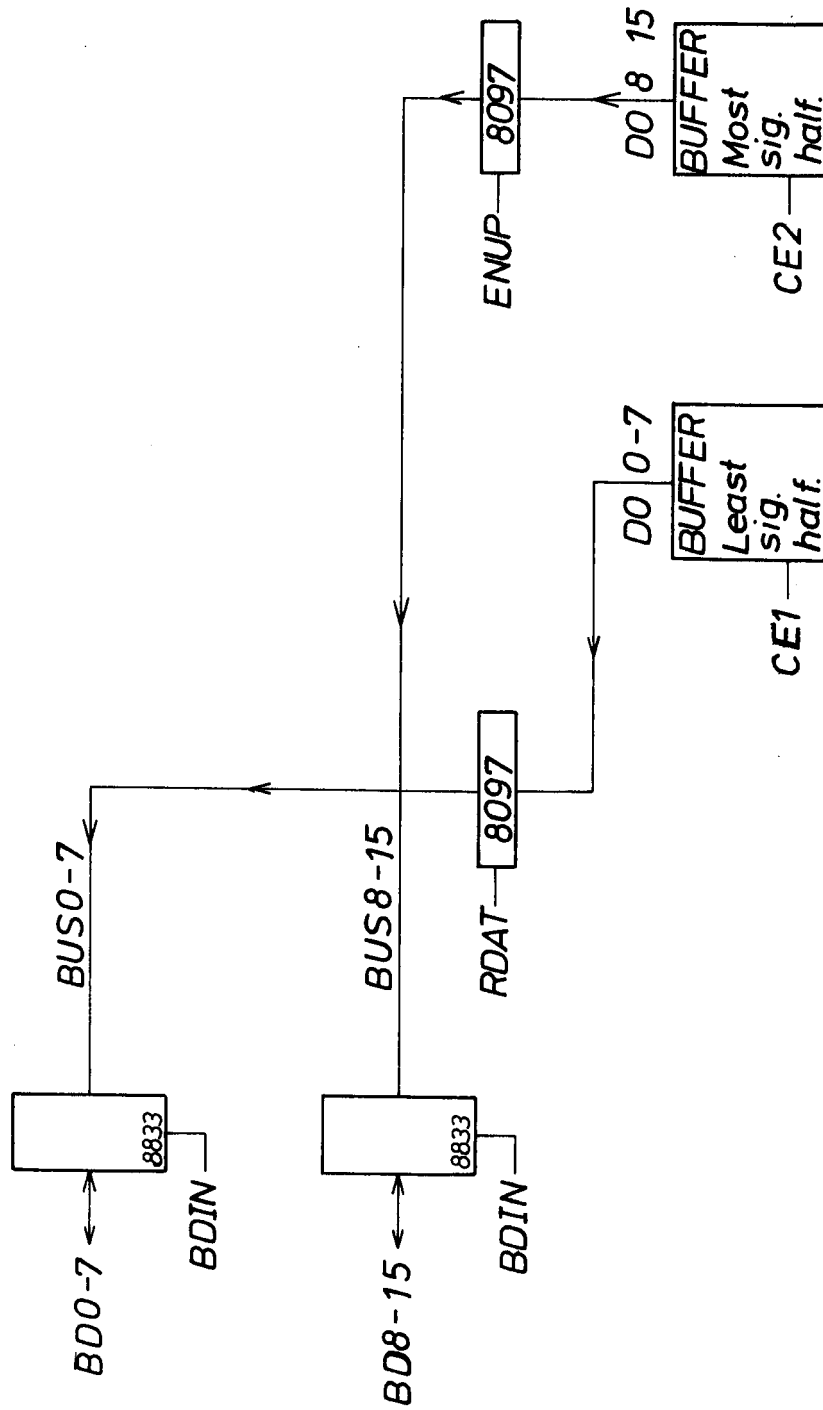


Figure II.4.7.

READ DATA BUFFER (IOX < RDAT >) TIMING DIAGRAM

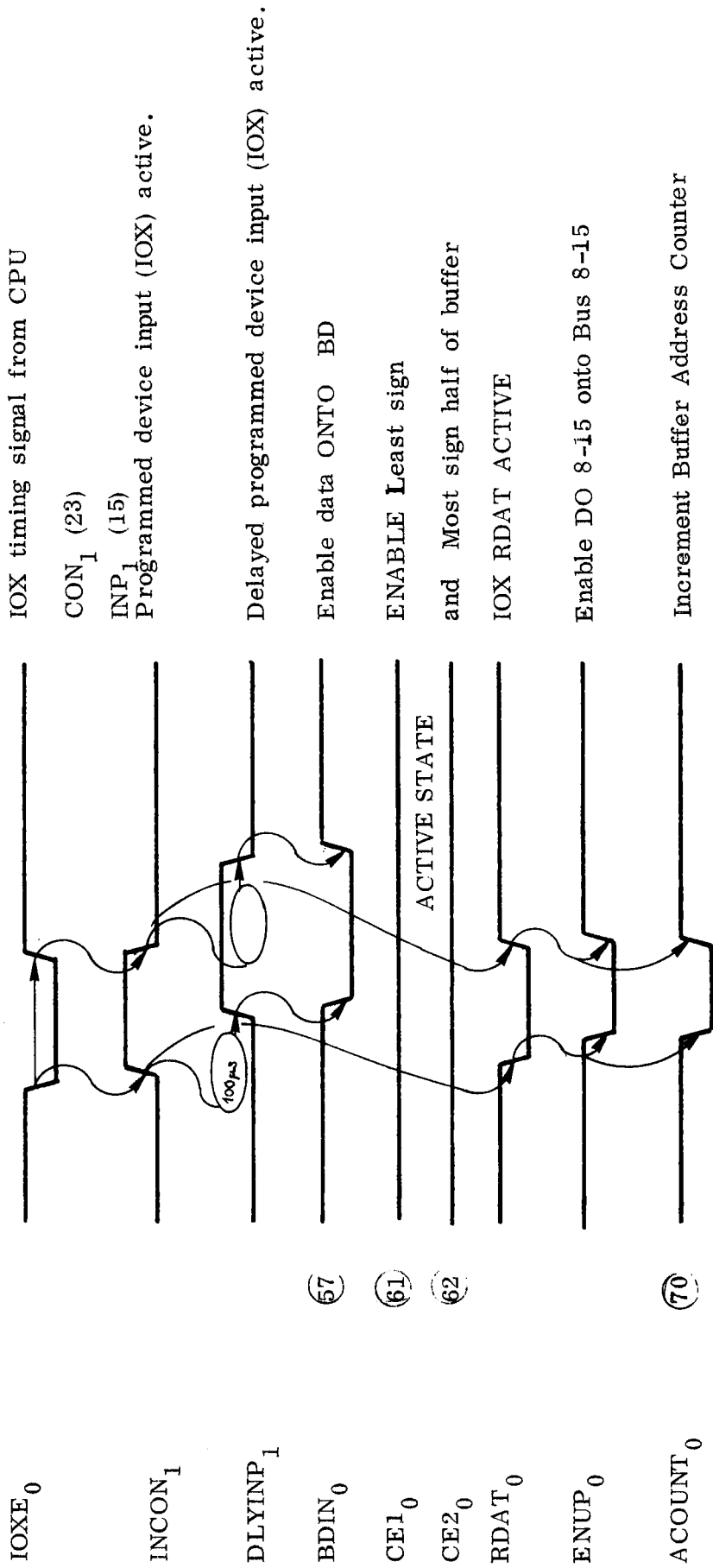


Figure 11.4.8: Read Data Buffer - Timing Diagram



## II.5 PROGRAMMED NONDATA OUTPUT/INPUT

### II.5.1 GENERAL

By non-data input/output we mean the flow of nondata information to/from CPU, i.e., information flow necessary to operate the system.

### II.5.2 NONDATA OUTPUT

In this section, we will discuss programmed output, excluding

- *IOX <WDAT> Write Data*
- *and*
- *IOX <WSCT> Write Test Byte*

which are discussed in Section II.4.5 and II.6.1 respectively.

What then remains for this discussion is

- *IOX <WCWD> Write Control Word*
- IOX <WDAD> Write Drive Address or Write Difference*
- and*
- *IOX <WSCT> Write Sector*

The general data flow is illustrated in Figure II.5.1.

Except for the Control Word, the data must be held in the upper byte which is transmitted directly to the Formatter. (Refer also to Section I.4.)

The timing chart in Figure II.5.2 shows the active control signals in the correct time perspective.

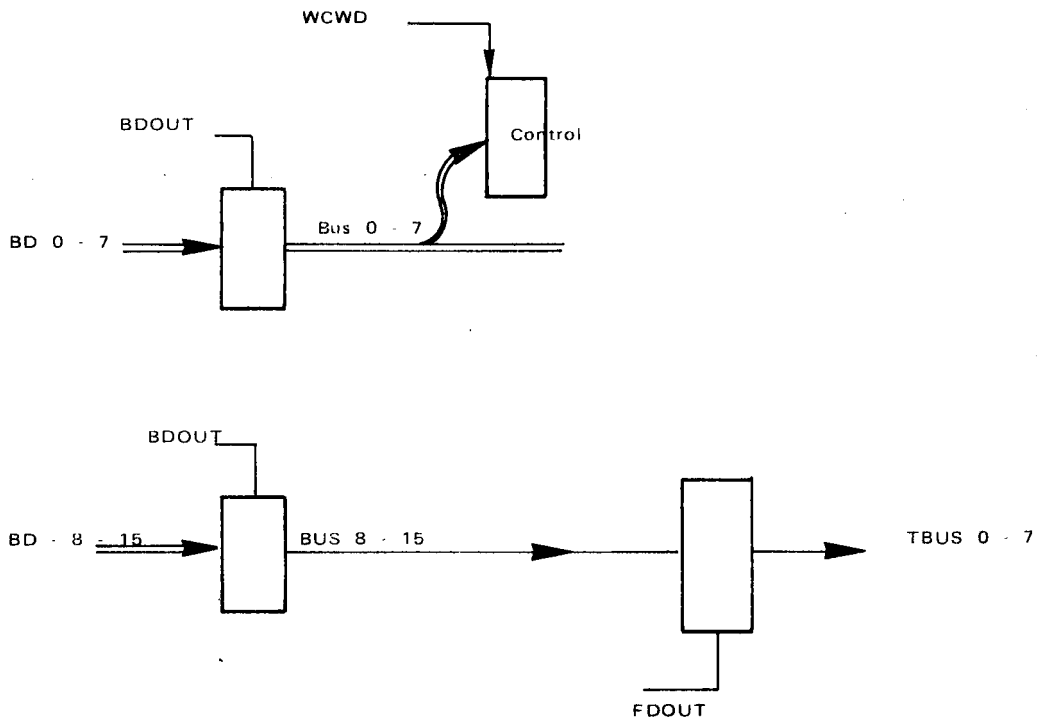


Figure II.5.1: Nondata Output – Data Flow

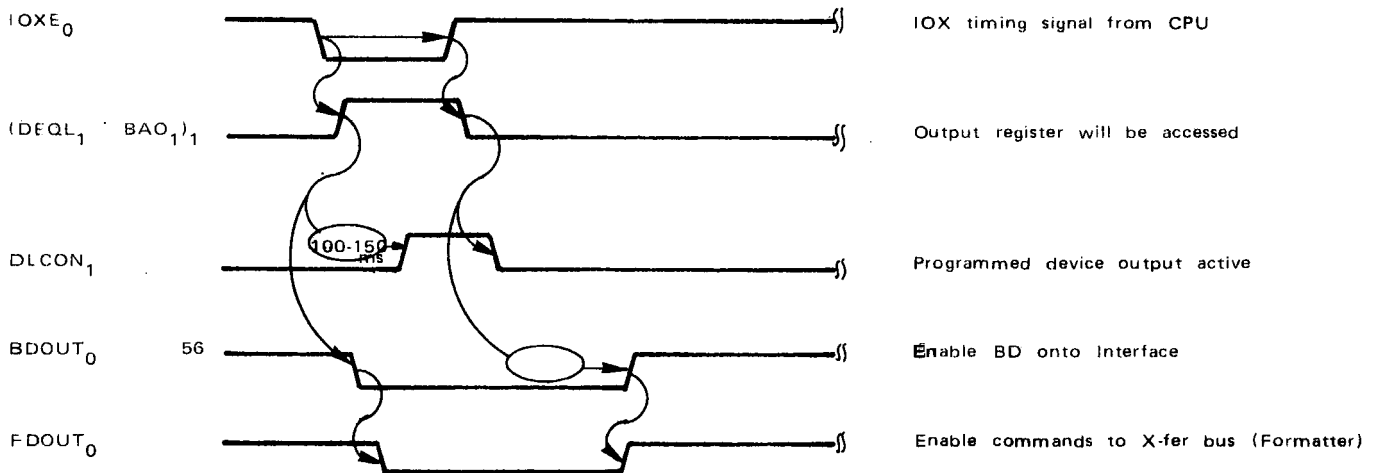


Figure II.5.2: Programmed Output (IOX) Timing



II.5.2.1 IOX <WCWD> Write Control Word

The IOX <WCWD> will generate an LCOM pulse that will strobe the TBUS into the Command Register located in the formatter. For bit assignment, refer to Section 1.4 - Programming Specifications and/or Section II.1 - The Interface Signals.

As described in Figure II.5.3, the lower bits transmitted from the A register will be used locally in the Interface to set up different control functions.

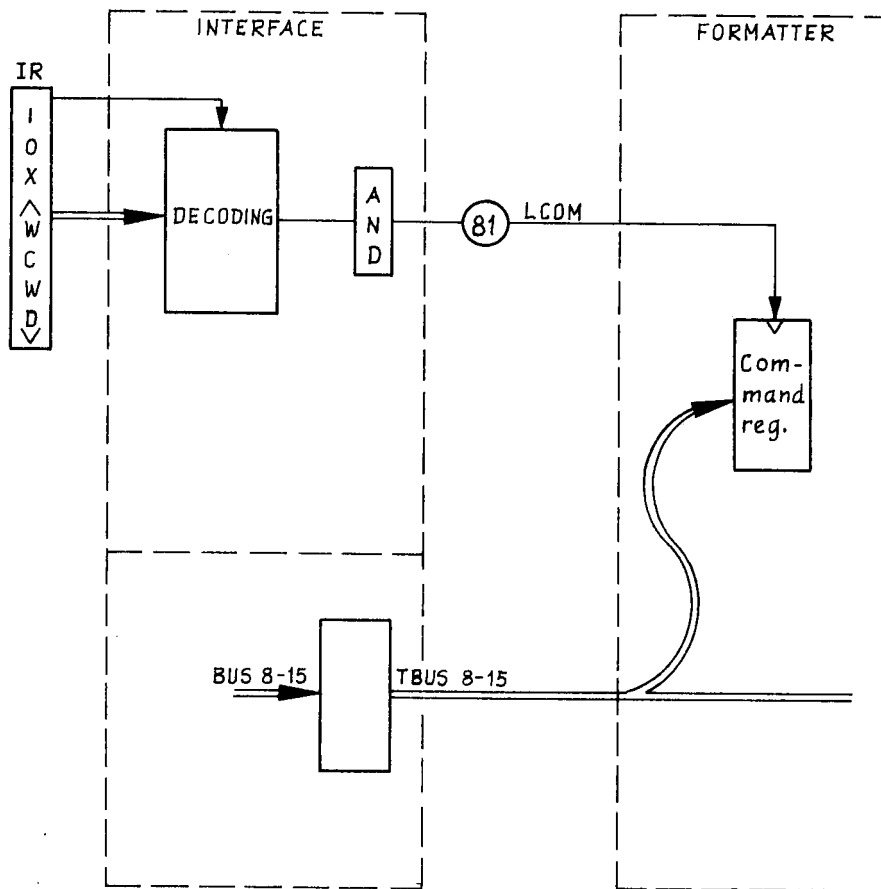


Figure II.5.4: IOX <WCWD> – Data Flow

II.5.2.2 IOX <WDAD> Write Drive Address

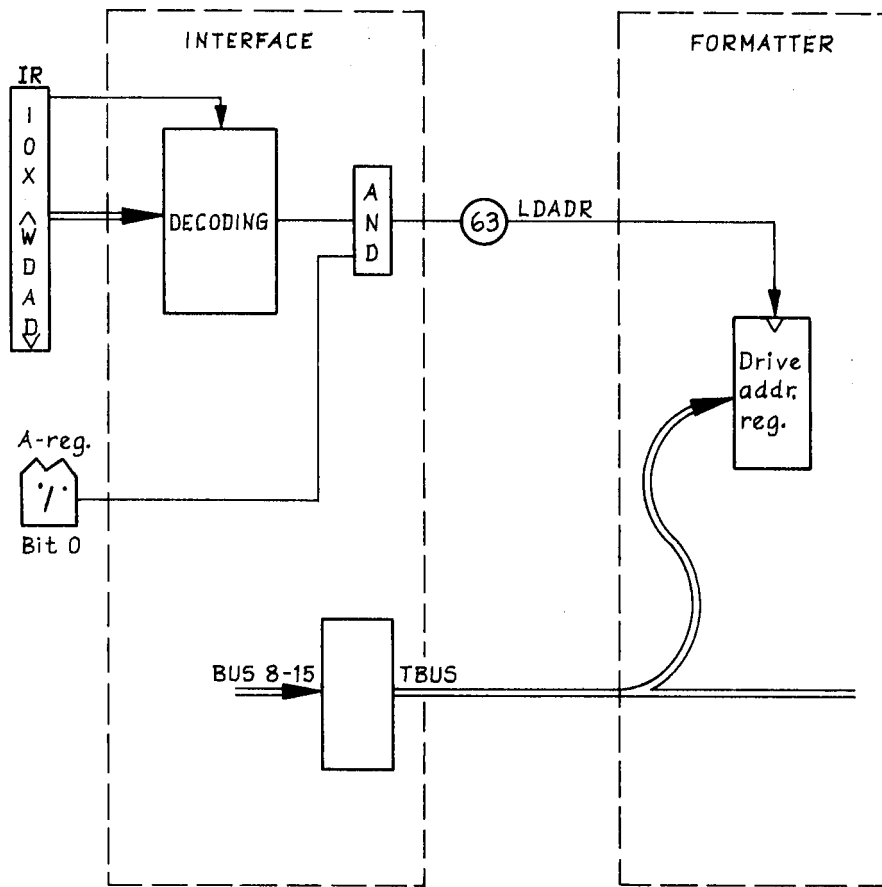


Figure II.5.4: IOX <WDAD> - Data Flow

As illustrated above, Load Drive Address (unit and format selection) will be performed by executing IOX <WDAD> with A register bit 0 = 1.

II.5.2.3 IOX <WDAD> Write Difference

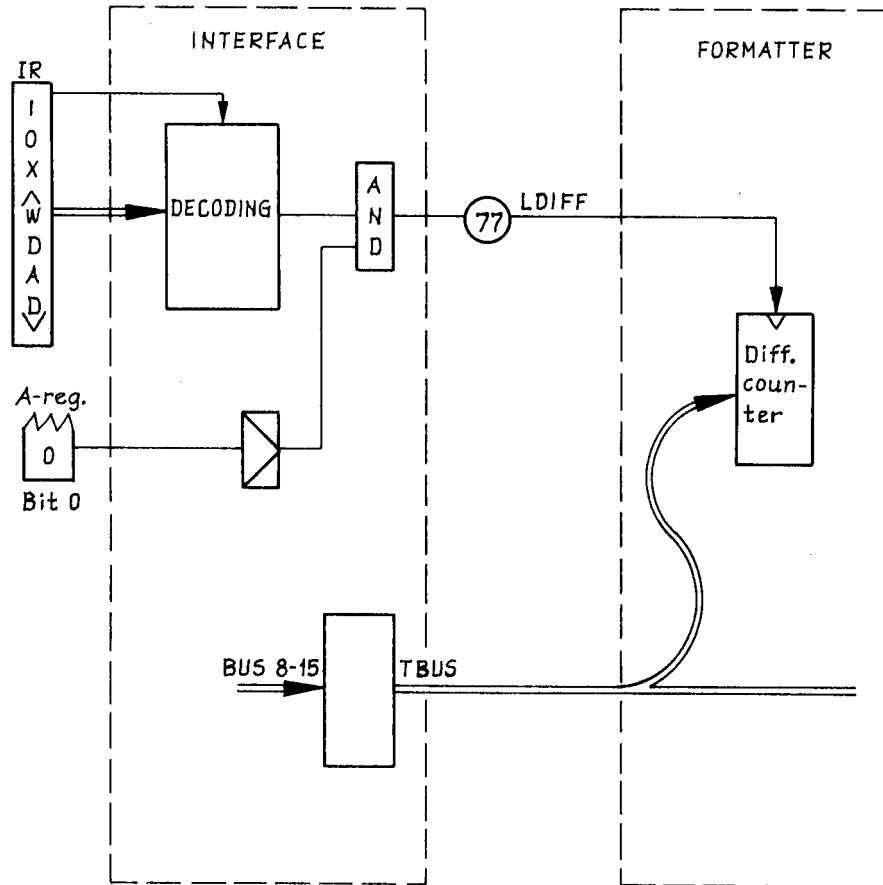


Figure II.5.5: IOX <WDAD> – Data Flow

As illustrated above, "tracks to go" will be put into the Difference Counter by executing an IOX <WDAD> instruction with bit 0 of the A register = 0 and the upper byte of the A register holding the difference.

II.5.2.4 IOX <WSCT> Write Sector

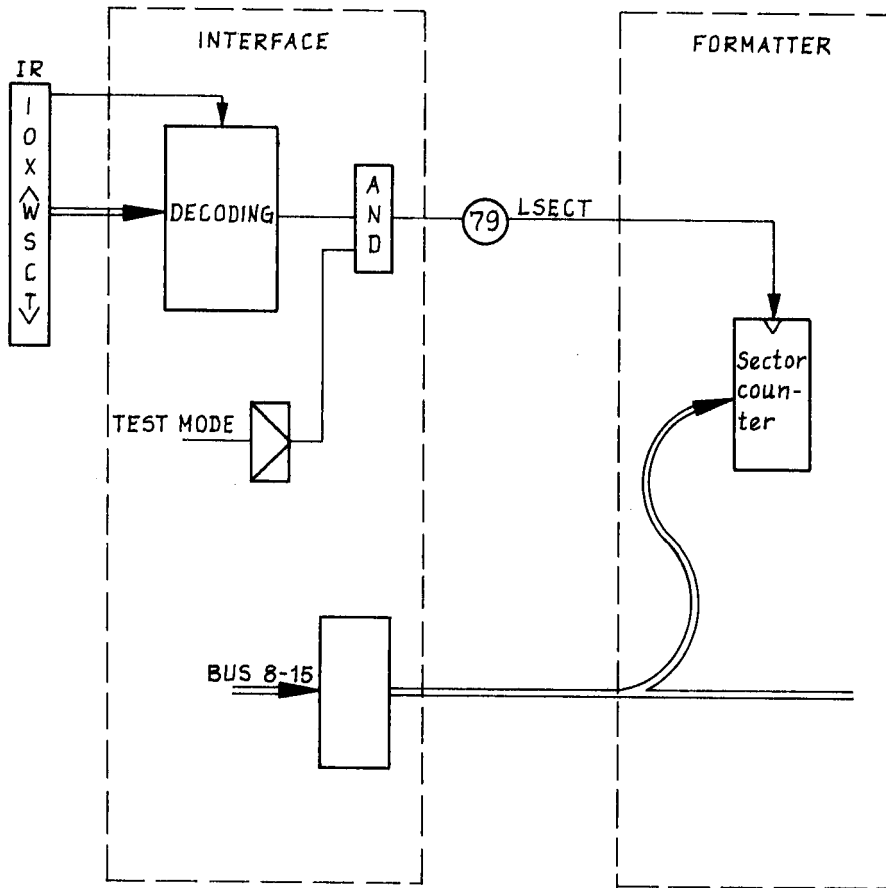


Figure II.5.6: IOX <WSCT> -Data Flow

When an IOX <WSCT> is executed and the Interface is *not* in test mode, the Sector Counter in the Formatter will be loaded with the upper byte of the A register.

11.5.3 NONDATA INPUT

In this section, we will discuss programmed input excluding

- IOX <RDAT> Read Data
- and
- IOX <RTST> Read Test

which are discussed in Section 11.4.6 and 11.6 respectively.

To be discussed here are:

- IOX <RSR1> Read Status Register No. 1
- IOX <RSR2> Read Status Register No. 2

Figure 11.5.7 will illustrate the major control signals in a time perspective.

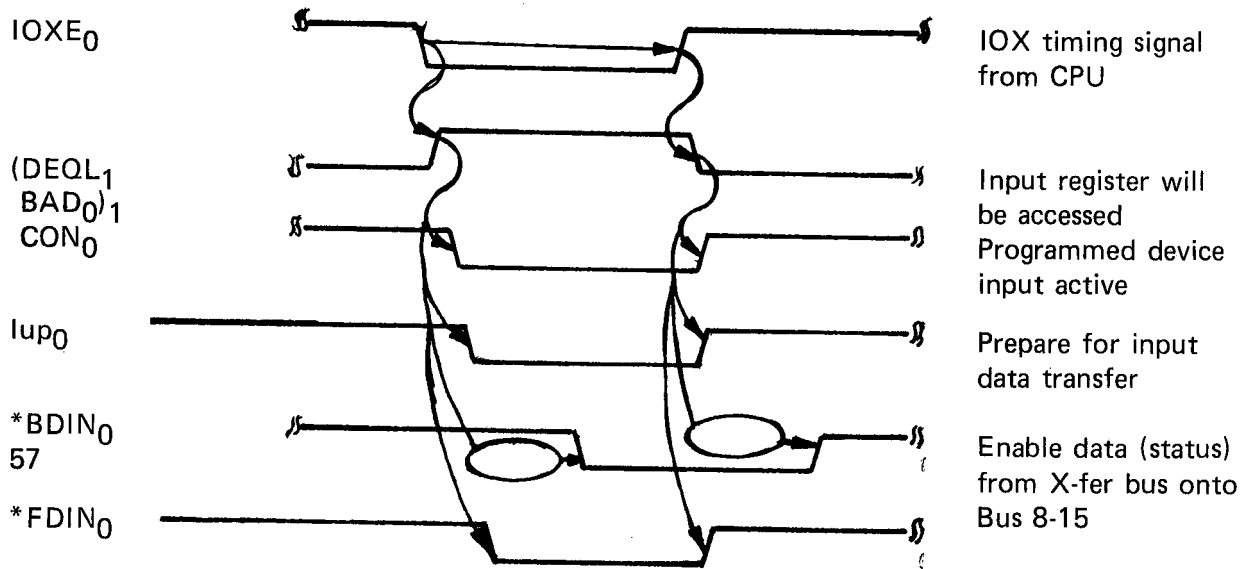


Figure 11.5.7: Programmed Input (IOX) Timing

II.5.3.1 IOX <RSR1> Read Status Register No. 1

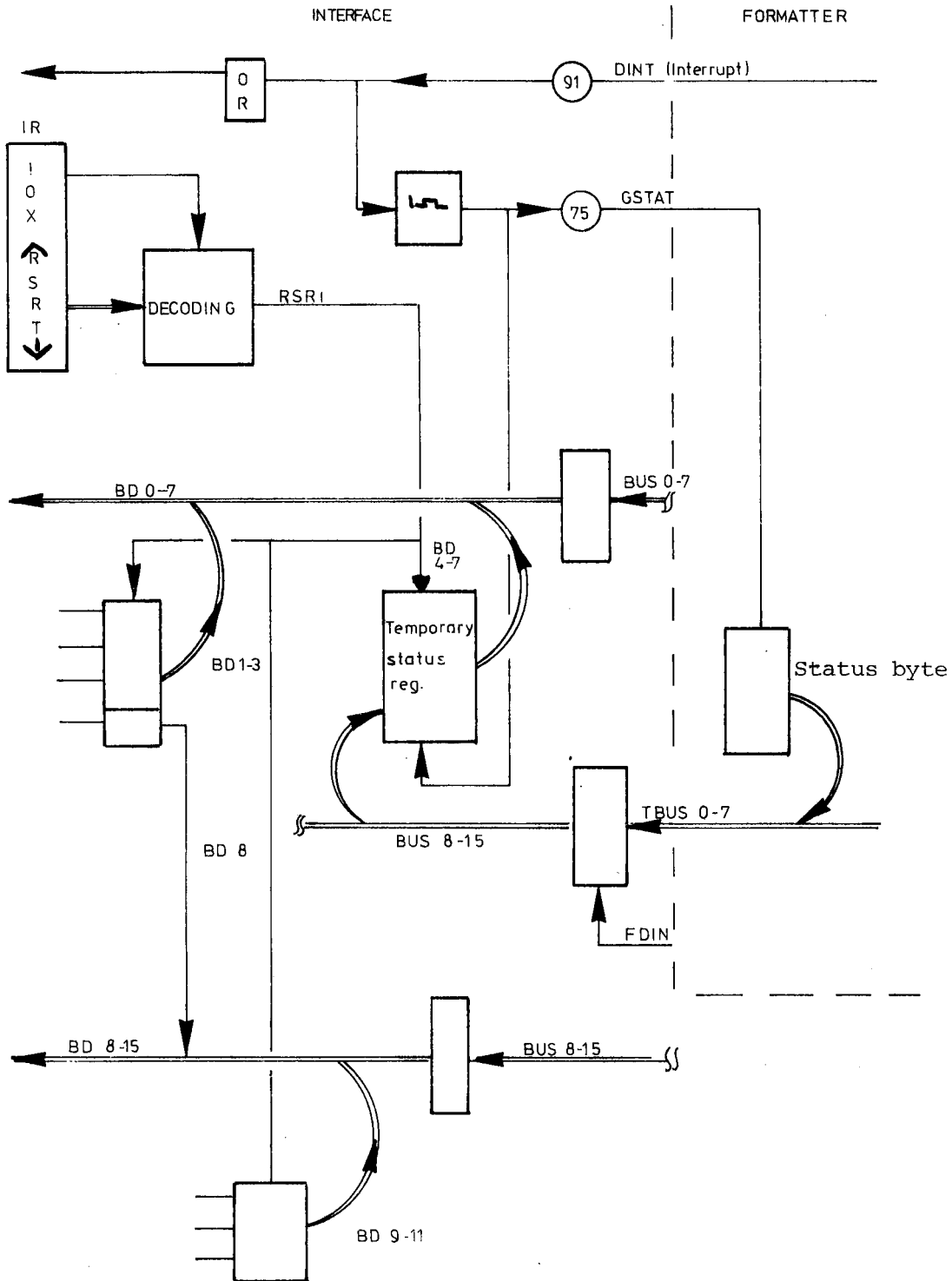


Figure II.5.8: IOX <RSR1> - Data Flow

Upon reception of INTERRUPT, the CPU will issue an IOX <RSR1> to gain information about the "interrupt source".

As a hardware feature, the Interface will, upon reception of an INTERRUPT from the Formatter, as the Formatter to present the Status Byte (GSTAT). The status byte (4 bits of significance) will be loaded into a Temporary Status Register. (Refer also to Section II.2 - General Command Sequence.) Decoding of IOX <RSR1> will enable the Temporary Status Register together with some other status indicators onto BD (I/O bus) directly.

II.5.3.2 IOX <RSR2> Status Register No. 2

Finding bit 4 (inclusive OR of bits in Status Register No. 2, i.e., sense register) set in Status Register No. 1, the CPU will execute an IOX <RSR2> to gain information about the error condition. Figure II.5.9 will explain.

The sense byte will be presented for the CPU in the upper byte. Refer to Section I.4 and Section II.1 for bit assignment.

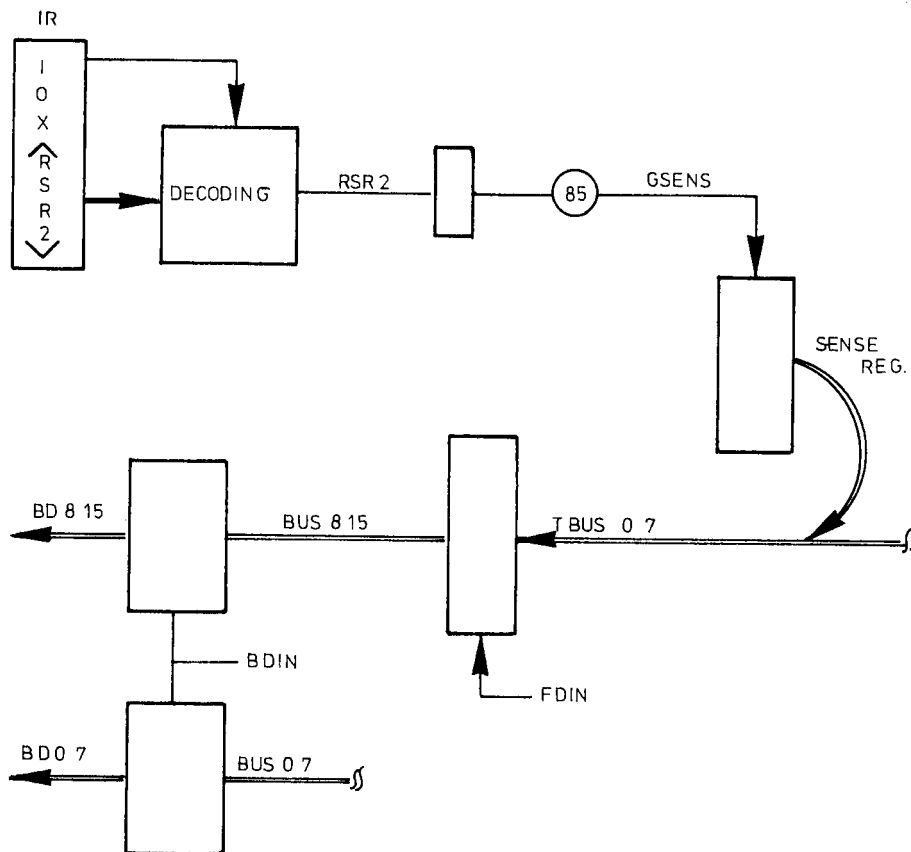


Figure II.5.9: IOX <RSR2> - Data Flow





## II.6 TEST MODE

Involved in the test modes are:

- *IOX <WCWD> Write Control Word*
- *IOX <WSCT> Write Test Byte*
- *IOX <RTST> Read Test Data*

Refer to Section I.4 for the above operations.

The purpose of the test mode is to simulate a data transfer between the Formatter and the Interface. From studying a Read Disk Operation, we know that all data from the Formatter will be routed through the Data Buffer. The same data routes will also be used in test mode.

The Interface will be put into test mode by executing:

```
SAA 10
IOX <WCWD>
```

By executing *IOX <RTST>* (Read Test) a predefined byte (refer to Section II.6.1) will be put onto the internal bus and written into the Data Buffer, i.e., no data will be moved into the A register during this operation.

By executing a number of *IOX <RTST>* instructions, the test bytes will be packed into the Data Buffer, i.e., the test byte will alternatively be written into the most and then the least significant position of the Data Buffer.

Being in test mode, the Interface will:

- *force the DIRECTION signal inactive, i.e., simulate a disk read operation*
- *disable Transmitters for I/O bus (disable FDIN)*
- *disable receivers from the X-fer bus (disable DIN)*
- *set the Busy FF to enable for toggling of CE1 and CE2*
- *disable the GRANT signal*
- *enable for reading or writing the "test byte" on/off BUS 8-15.*

The data flow is illustrated below:

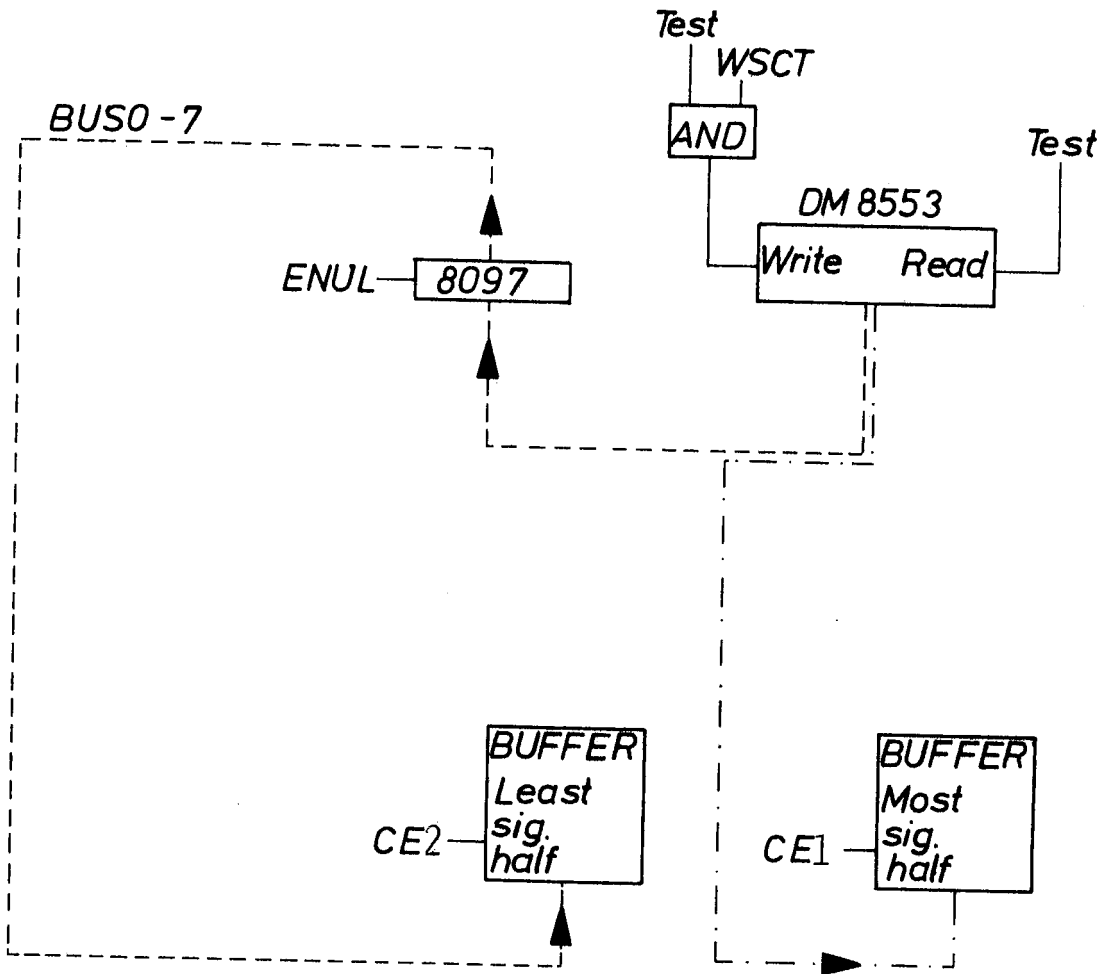


Figure II.6.1: Read Test Data – Data Flow

As depicted in Figure II.6.3, execution of IOX <RTST> instructions are a combination of Read Disk Operation and IOX <RDAT> operations with the above described inhibitations.

*Note: No data will be sent to the CPU.*

**II.6.1 SELECTING THE TEST BYTE**

The test byte written into the Data Buffer, by executing the IOX <RTST> can be selected, as desired, by setting up the test byte in the upper byte of the A register and executing an IOX <WSCT>.

Data flow is indicated in Figure II.6.2.

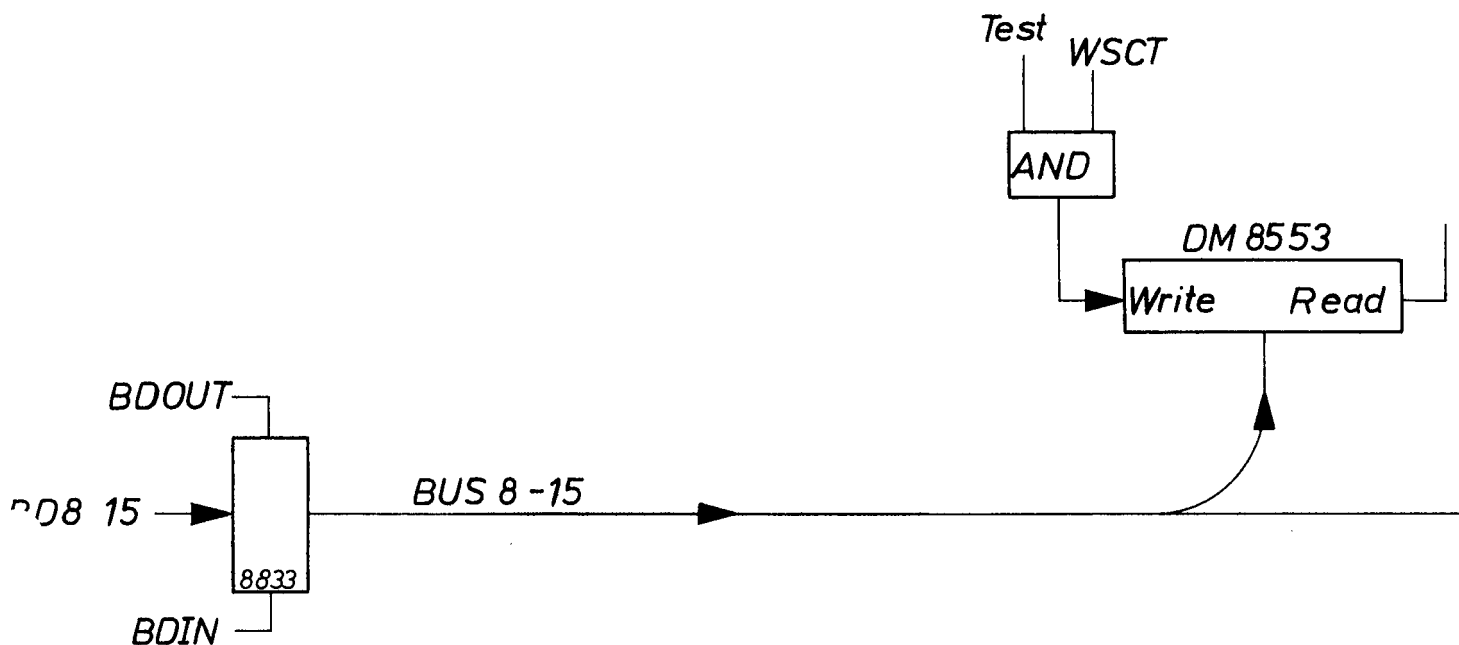


Figure II.6.2: Write Test Byte – Data Flow

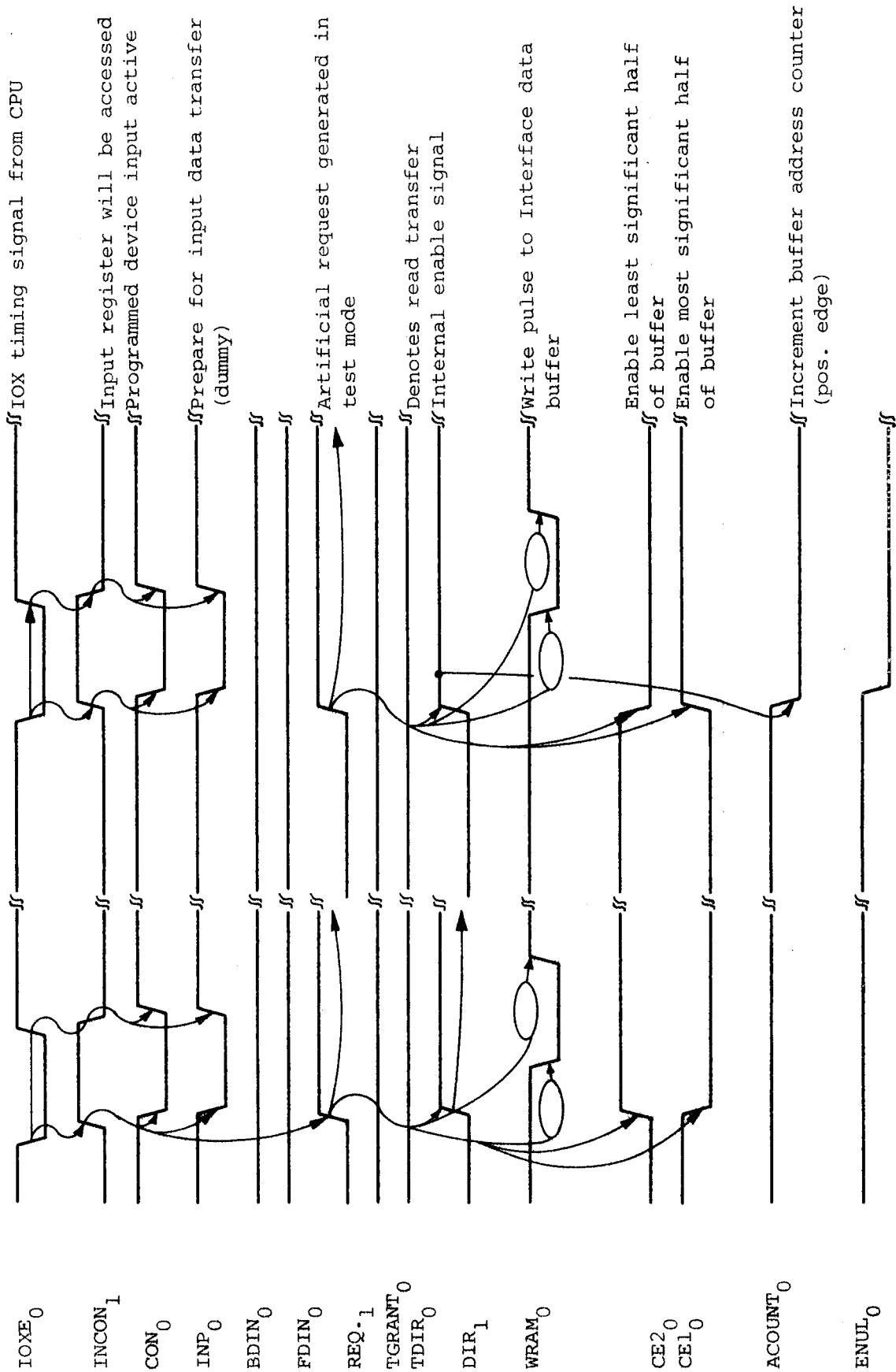


Figure 11.6.3: IOX <RTST> Timing Diagram (Test Mode active)  
 (Execution of two IOX <RTST> instructions illustrated)

## II.7 MASTER CLEAR – AUTOLOAD

### II.7.1 GENERAL

The Floppy Disk is to be considered as a Master Storage Device. Normally, such a device would be handled by a DMA interface, however, due to cost, access time and type of usage considerations, a PIO interface has been chosen. A load must, thus, conform to the program specifications for a teletype or paper tape reader.

However, in order to do a load operation from a Floppy Disk, a sequence of commands must be issued. Since the microprogram performing the load operation does not handle such a sequence, the microprogram will start operating on the data after they have been put into the Data Buffer. An automatic command sequence generator triggered off by WCWD<sub>0</sub> and B#2 handles the task. A load operation is then divided into two parts.

When the load m-program is started it issues a standard activate device command (bit 2 in control word). This is used to initiate autoload sequence. Bit 2 in the control word MUST NOT be used by standard software.

#### *Load*

*will initiate the load sequence which will move the data from the Data Buffer into main memory.  
(Illustrated in Figure II.7.1.)*

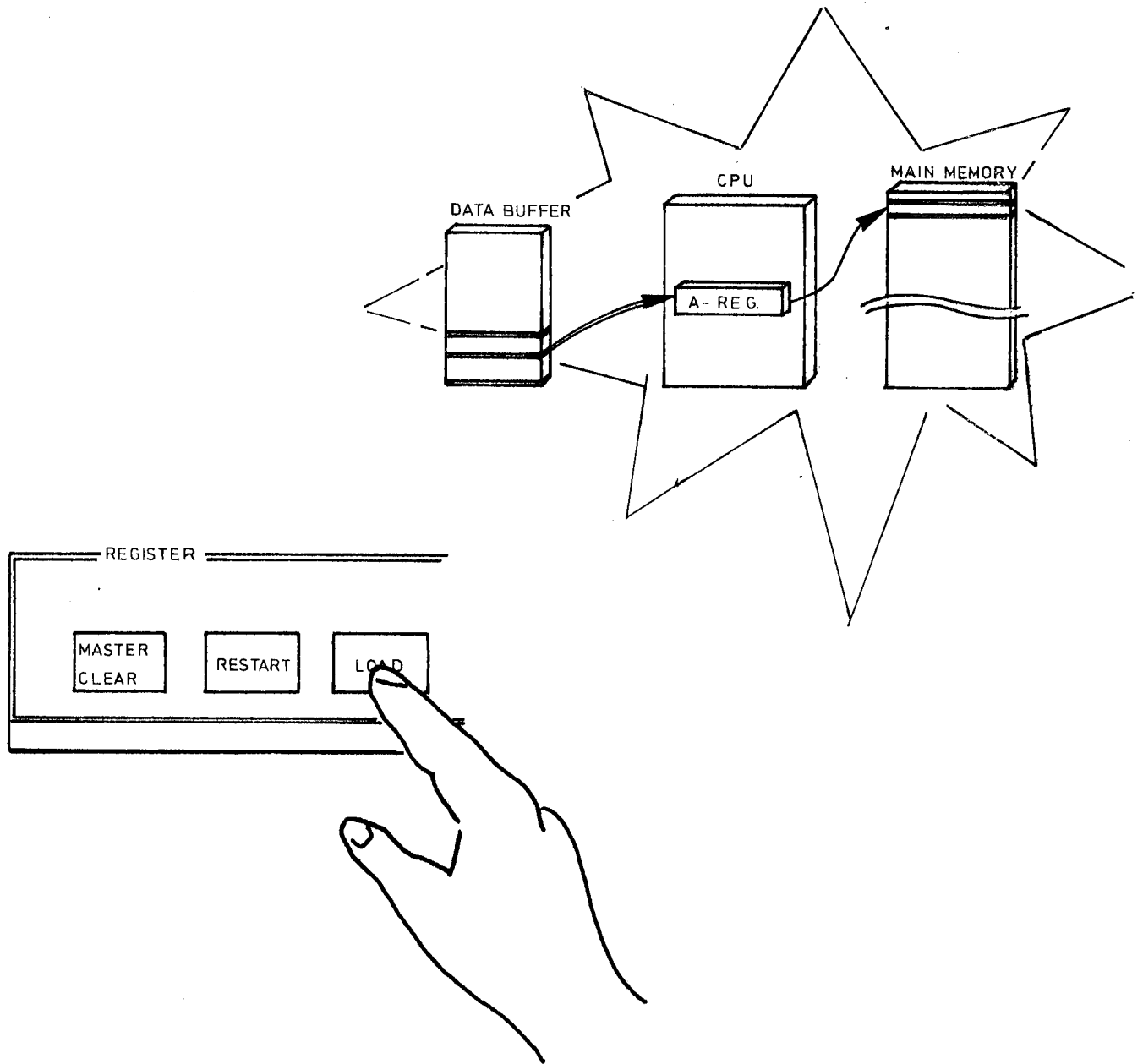


Figure II.7.1: Load-Data Flow

The microprogram initiated by the "load" will not start moving data until it senses the Ready Bit (Status Bit I No. 3). This bit will not be true until one sector of data has been read off the diskette and put into the Data Buffer.

We will, in the following, describe the hardware sequence initiated by WCWD, Bit No. 2.

II.7.2 AUTOLOAD SEQUENCE

II.7.2.1 General

BD2 of WCWD<sub>0</sub> will initiate a hardware sequence that reads sector no. 1 on track 0 and transfers the data to the Data Buffer.

The following commands must be presented for the Formatter in the sequence indicated:

- select Drive No. 0 and Sector Format
- recalibrate (reposition the heads to track no. 0)
- specify sector no. 1
- send read command

At the terminal point of the read operation, an INTERRUPT will be sent to the Interface. A Buffer Address Counter Clear will be performed and the ready flag set (Status I bit no. 3).

The microprogram initiated by the LOAD may now start moving the data.

II.7.2.2 Detailed Description

As indicated above, several commands must be issued from the Interface during the "autoload sequence".

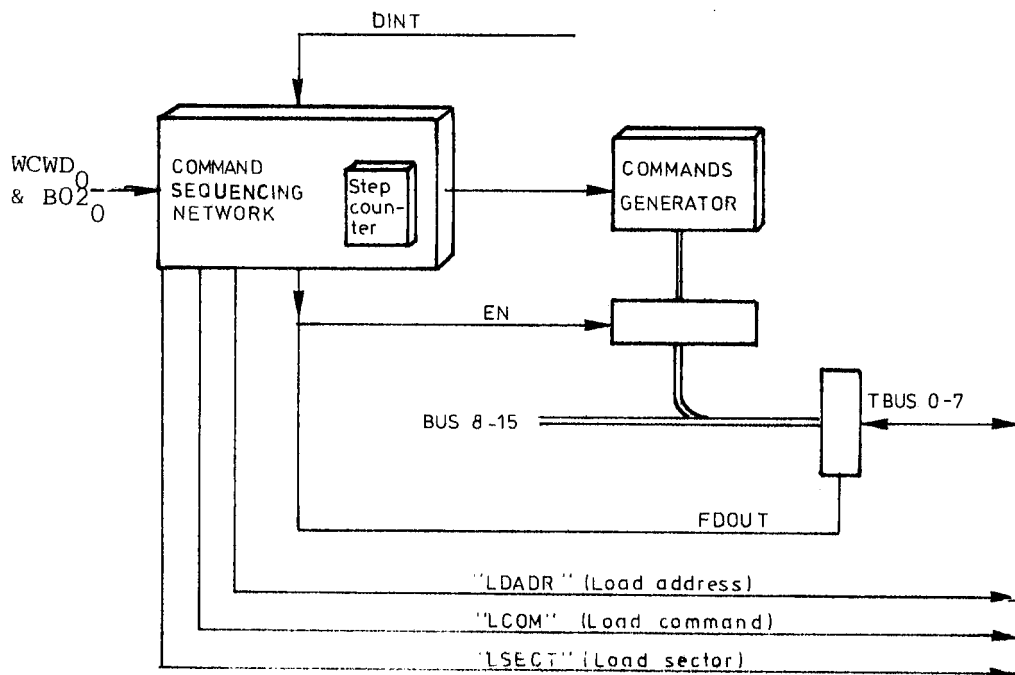


Figure II.7.2: Autoload Illustration



As depicted in Figure II.7.2, a command sequencing network is realized on the control card (1111). This network is responsible for issuing the different commands in the proper order with the correct time perspective. The Command Generator will enable the different command arguments onto the bus.

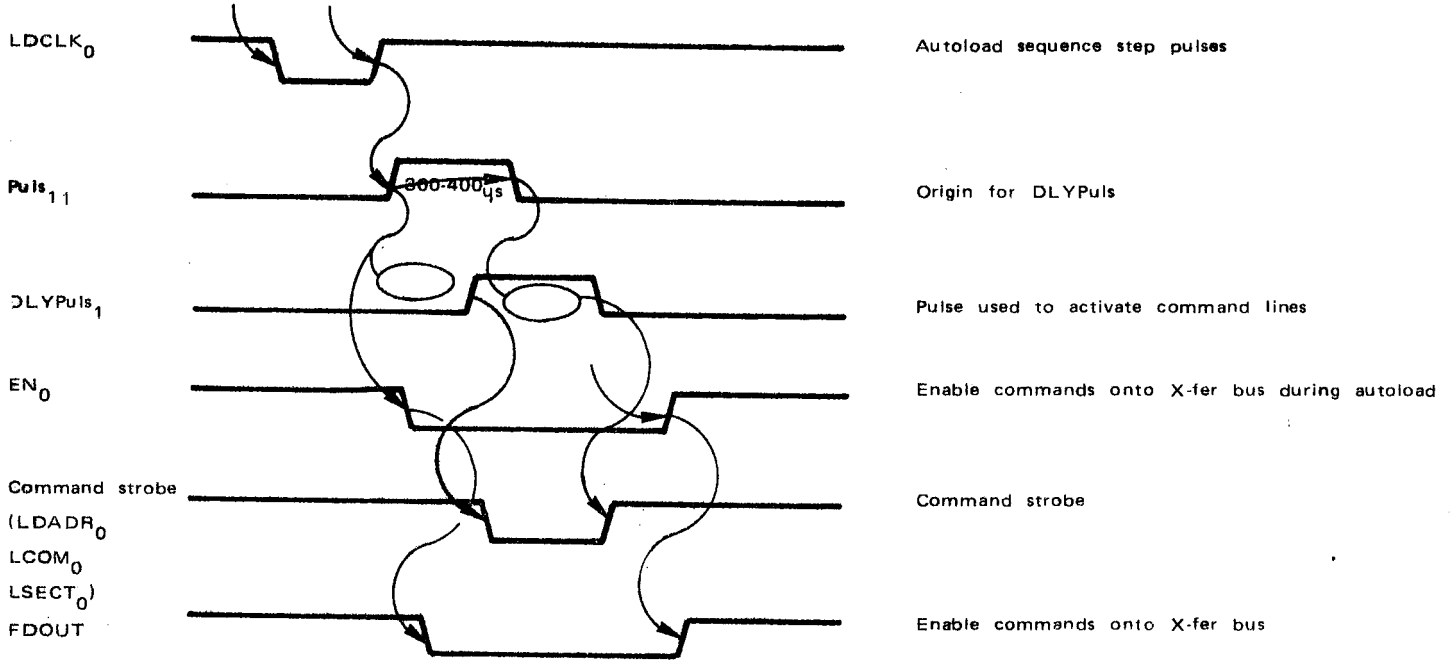
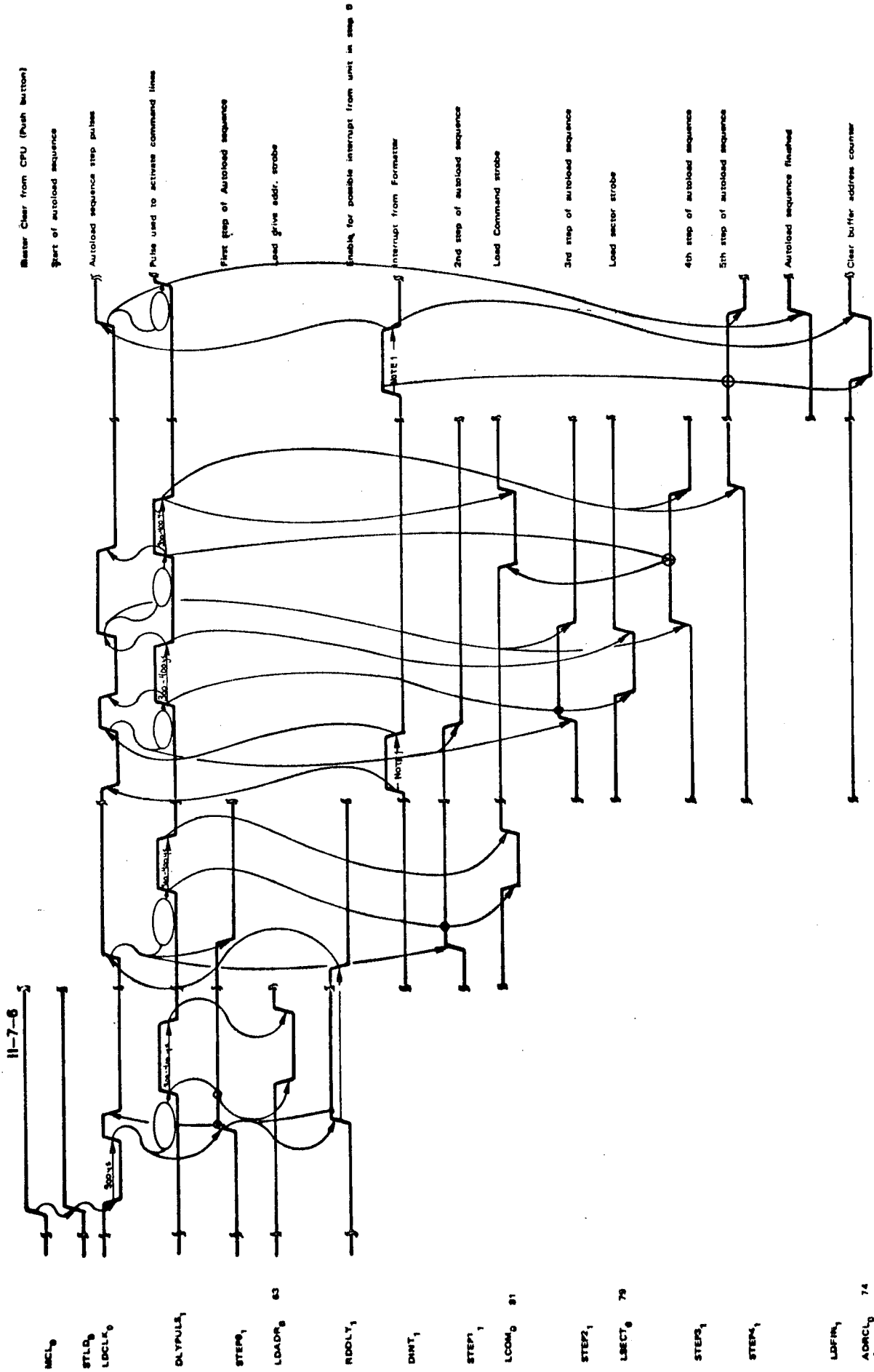


Figure II.7.3: General Autoload Command Timing

The sequence depicted in Figure II.7.3 will be run through for each command sent to the Formatter. When "LDCLK" goes off a "DLYPULS" will activate the command lines (one for each run-through) and the "EN" will enable the command argument onto the bus. (Refer to Figure II.5.1.) The "FDOUT" generated from "EN" will drive the internal bus onto the X-fer bus.

A step counter located in the Command Sequence Network will allow repetition of the above generally described sequence until the last step is reached (LDFIN). For study of the complete sequence, refer to the timing chart labelled "Autoload Sequence - When Disk is Ready", Figure II.7.4.



NOTE 1: Ref. interrupt timing sequence for time generation and termination conditions.

Figure 11.7.4: Load Sequence - When Disk is Ready

Sending IOX <WCWD> with B02 set starts off the sequence, i.e., generates the first "LDCLK". "STEP<sub>0</sub>", the first step in the autoloading sequence, will be entered.

During this step, a "LDADR" (load address strobe) will be generated.

Step no.	Command strobe	X-fer bus								
		7	6	5	4	3	2	1	0	
0	LDADR	1	1	0	0	0	0	0	0	Select drive no 0 and format
1	LCOM	0	1	0	0	0	0	0	0	Perform a recalibration
2	LSECT	0	0	0	0	0	0	0	1	Sector no 1 specified
3	LOM	0	0	0	1	0	0	0	0	Perform a read data command
4	---	---	---	---	---	---	---	---	---	Wait read completion
LDFIN	---	---	---	---	---	---	---	---	---	Set ready and clear »Buffer address counter«.

Figure 11.7.5: X-fer Argument for Autoload Sequence

Figure 11.7.5 shows the argument enabled onto the bus for different commands. The argument will select driver number 0 and the desired sector format. A one shot "RDDLY" is set up to handle INTERRUPT from the disk if it is not ready (described in Section 11.7.3.). If no INTERRUPT occurs, we assume the drive is ready and the sequence may continue.

Step 1 will be entered and will generate a "LCOM" (load command) strobe. The argument with bit no. 6 will specify a recalibration. The time of this operation depends upon where the R/W head is currently located. An INTERRUPT from the disk will give the information that the R/W head is settled on track number 0. The step counter will advance and enable for step 2. During this step, the argument enabled to the bus will indicate the sector number to be operated on, which in our case, is sector number 1.

*NB: Sector counting starts from 1 NOT 0.*

After an internal delay, step number 3 will be entered. This step will order a read command by activating bit number 4 on the X-fer argument and pulsing the "LCOM" control line.

Step 4 will be entered. The data field of sector 0 in track 0 will be assembled and transferred to the Data Buffer in the Interface. At the completion of the read operation (512 bytes read), an INTERRUPT will be presented for the Interface. The last step (LDFIN) is entered to indicate termination of the "Autoload Sequence". A Buffer Address Counter Clear pulse will be generated to prepare for the microprogram load operation. Status bit no. 3 (ready) will also be activated. The microprogram load will test on this bit before doing a read operation.

### II.7.3 MASTER CLEAR – AUTOLOAD – WHEN DISK IS NOT READY

Above is described a load sequence, where it has been assumed that the disk unit was in the ready state.

Any of the following conditions will make the disk NOT ready:

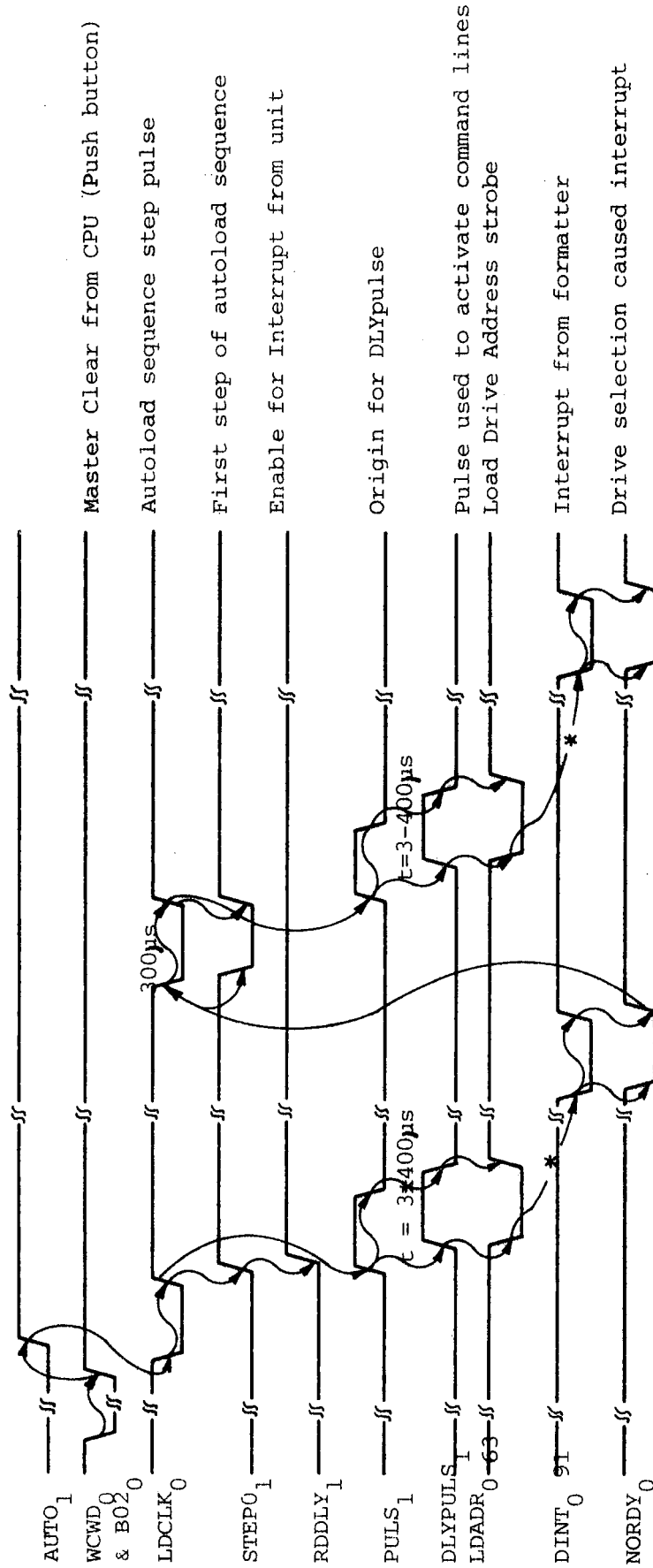
- *unit is not powered up*
- *the diskette access door is open*
- *the diskette is not perfectly installed*
- *an illegal drive address is issued*

If one or more of the above indicated conditions are not satisfied when doing a "LADR" (load address), step 0 of the autoload sequence, the Formatter will respond with an INTERRUPT (DINT) within 2 $\mu$ s.

From the timing diagram (Figure II.7.6), we see that step 0 will be re-entered after receiving an INTERRUPT during the one-shot interval "RDDLY".

The signal "STLD" will clear the step counter such that step 0 will be re-entered. The sequence described by the timing diagram will be active until the disk becomes ready. The normal load sequence (as described above) will then be executed.

WE NOTICE that no status information will be given to the CPU if the unit is not ready during the Autoload sequence.



\* When drive is not ready within 2µs, an interrupt is generated

Figure 11.7.6: Load Sequence if Disk is Not Ready

#### II.7.4 *THE LOAD OPERATION*

The Autoload sequence is terminated when one sector of data has been transferred to the Data Buffer and the ready flag (Status I bit no. 3) has been set.

Seeing Status I bit no. 3 set, the microprogram will perform the load operation. For further details regarding load format, etc., refer to the NORD-10 Reference Manual – Chapter 8.





**SECTION III**

**FORMATTER**



## DETAILED CONTENTS

+ + +

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### III.1 FORMATTER/UNIT(S) INTERFACE SIGNALS

#### III.1.1 GENERAL

As mentioned in Chapter 1.3, up to 3 drives (units) can be "daisy chained" onto the Formatter. The assignment of the lines to/from the Formatter will be described in this section. Refer also to Figure III.1.1.

The figure also depicts plug and pin numbers on the Formatter as well as on the unit side. The Interface may be divided into two groups:

- *Signal Interface*
- *Power Interface*

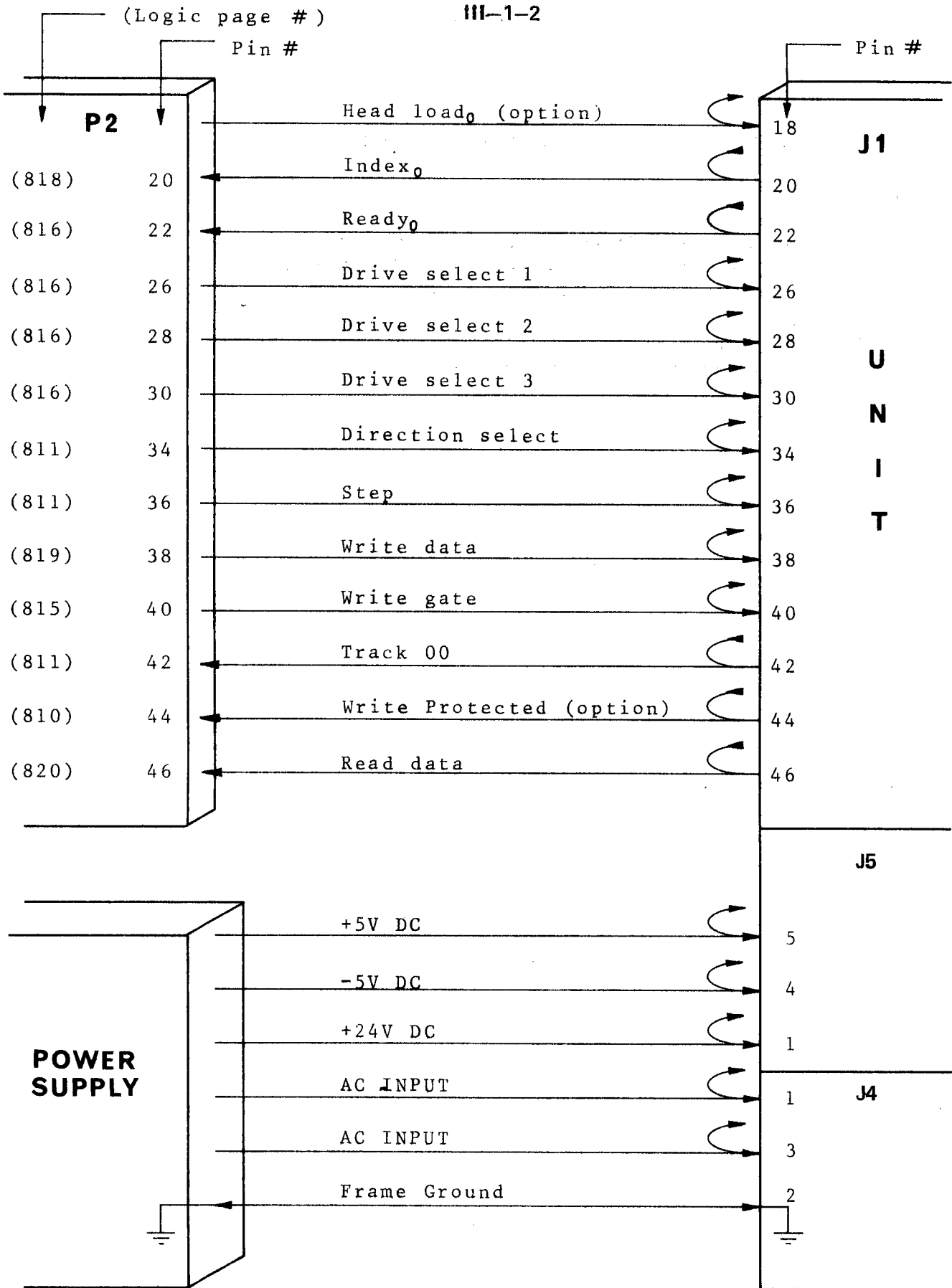


Figure III-I-1

FORMATTER/UNIT(S) INTERFACE LINES

### III.1.2 SIGNAL INTERFACE

#### III.1.2.1 *Head Load<sub>0</sub>*

Normally, this line is not used but is a customer installation option line. With this option installed (refer to Maintenance Manual, Section 7), the R/W head will load when this line is activated and the door is closed without the unit being selected.

#### III.1.2.2 *Index<sub>0</sub>*

This line is activated by the selected drive once for each revolution of the diskette (166.67ms) to indicate the beginning of a track (pulse width 1.7 $\mu$ s).

#### III.1.2.3 *Ready<sub>0</sub>*

Normally, this interface line, when active, will indicate the following:

- *two index holes have been sensed after properly inserting a diskette and closing the door*
- or*
- *two index holes have been sensed after applying + 5VDC power to the drive*

For additional use, refer to the Maintenance Manual, Section 7.5.

#### III.1.2.4 *Drive Select 1-3*

By activating one of these lines the corresponding unit will load the R/W head and respond to the Input lines and gate the Output lines.

Traces DS1, DS2 and DS3 have been provided to define the unit number.

**Note:** *As shipped from the factory, a shorting plug is installed on DS1. To define another unit number, the shorting plug should be moved to the appropriate DS-pin.*

### III.1.2.5 *Direction Select*

This interface line is a control signal which defines the direction of motion for the R/W head when the STEP line is pulsed.

A "high" (or open circuit) defines the direction OUT, i.e., the R/W head will move to a lower track number. Conversely, if the line is "low" the R/W head will move toward the center of the diskette.

### III.1.2.6 *Step*

This interface line is a control signal which causes the R/W head to move the direction defined by the DIRECTION line.

The access motion is initiated on each trailing edge of the pulse (repetition rate 10ms — pulse width 10 $\mu$ s).

### III.1.2.7 *Write Data*

This line provides encoded clocks and data to be written on the diskette. The leading edge will clock a Write Toggle FF which, in turn, will reverse the write current, thus, writing one bit on the spinning diskette.

*Note: The WRITE GATE must be active in order to perform a write operation.*

### III.1.2.8 *Write Gate*

This line, while in the active state, enables data to be written on the diskette and disables stepping of the R/W head. The Read Circuitry and the Step Motor Control Logic are enabled when the WRITE GATE is turned off.

### III.1.2.9 *Track 00*

The active state of this line indicates that the R/W head is located over track 0.



**III.1.2.10** *Write Protected*

This interface signal is provided by the drive to give the Formatter (system) an indication that a Write Protected Diskette is installed.

Under normal operation, the drive will inhibit writing on a protected diskette in addition to notifying the Formatter. For optional use, refer to Section 7.9 in the Maintenance Manual.

**III.1.2.11** *Read Data*

This interface line provides "raw data", i.e., alternate clocks and data as detected by the units Read Circuitry.

### III.1.3 POWER INTERFACE

The unit requires both AC and DC power for operation. The AC power is used for the Spindle Drive Motor while the DC is used for the Electronics and Stepper Motor.

#### III.1.3.1 AC Power

For our environments, 220V AC 50Hz is carried on pin 1 and 3 of J4/P4 located below the AC Motor Capacitor.

*Note: For different power environments refer to the Maintenance Manual, Section 4.2.*

#### III.1.3.2 DC Power

DC power to the unit is applied via the J5/75 connector located on the non-component side of the PCB near the P4 connector.

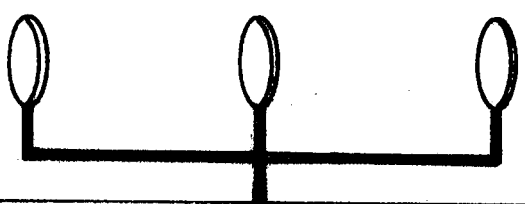
For more specific information, refer to the Maintenance Manual, Section 4.2.2.

### III.2 FORMATTER – FUNCTIONAL OPERATION

For the following study refer to Figure III.2.1, the description of the Formatter/Interface lines (Section II.1) and description of the Formatter/Unit interface lines (Section III.1).

The different "building blocks" will be discussed in detail as the different operations are discussed. Formatter physical locations are depicted in Figure I.3.1, while logic diagrams, etc. are labelled Appendix D/I-II-III.

When the two above mentioned interfaces have been studied, it should be possible to understand the major control and data flow by looking closely at Figure III.2.1.



SA 810 FORMATTER

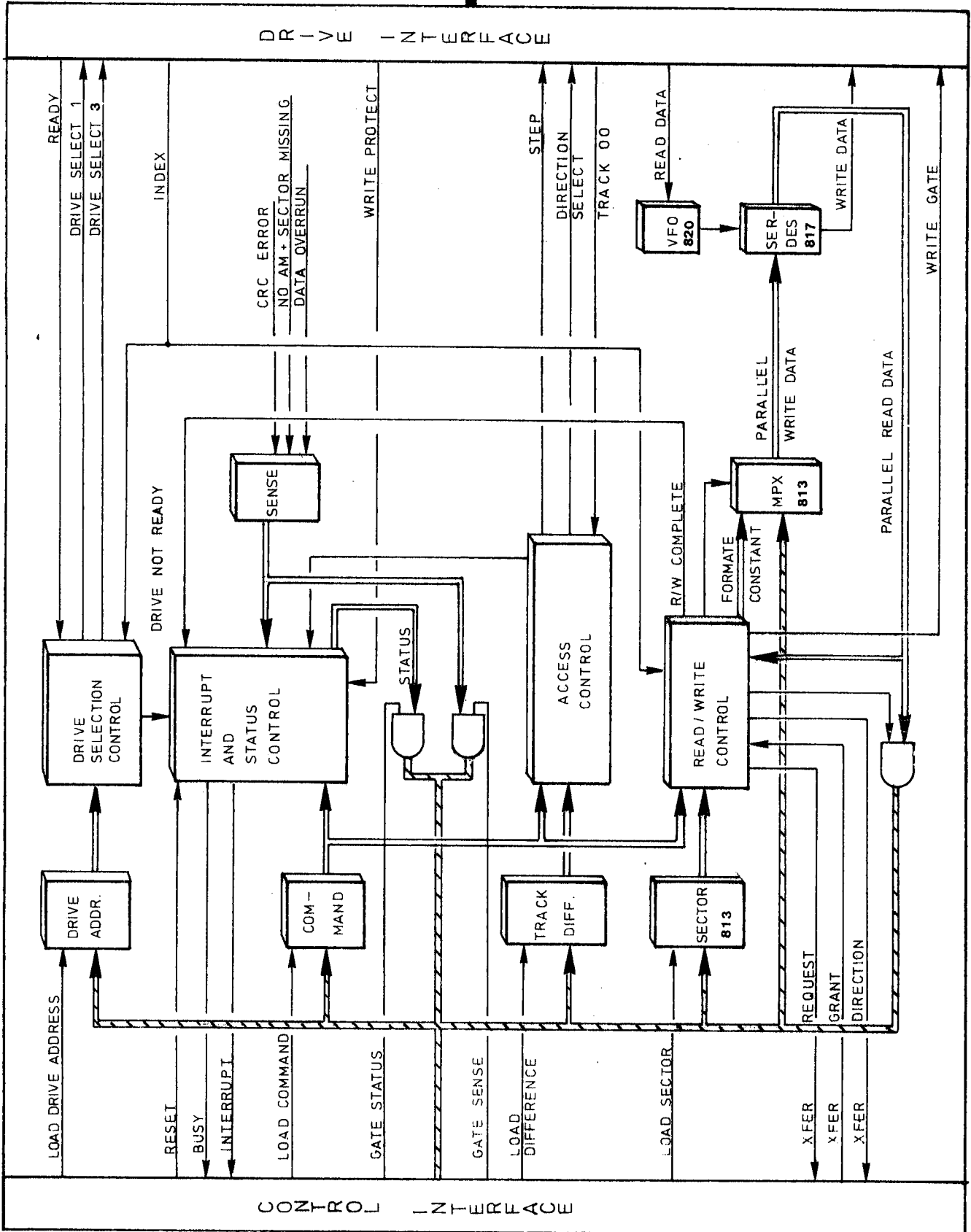


Figure III.2.1: Formatter - functional diagrams

### III.3 TRACK FORMAT

#### III.3.1 GENERAL

Tracks may be formatted in a number of ways as indicated in Table III.3.1.

Format selection is under software control, and is selected in parallel with drive selection, by the use of IOX <WDAD> (refer to Section I.4, Programming Specifications.)

FORMAT	RECORDS/ TRACK	BYTES/ RECORD	SUBSYSTEM STORAGE (In mega-bytes)	
			1 drive	3 drives
A (3740).	26	128	.25	.75
B (Sys 32-I).	15	256	.28	.85
C (Sys 32-II).	8	512	.30	.90
AA (Double A).	32	256	.63	1.9

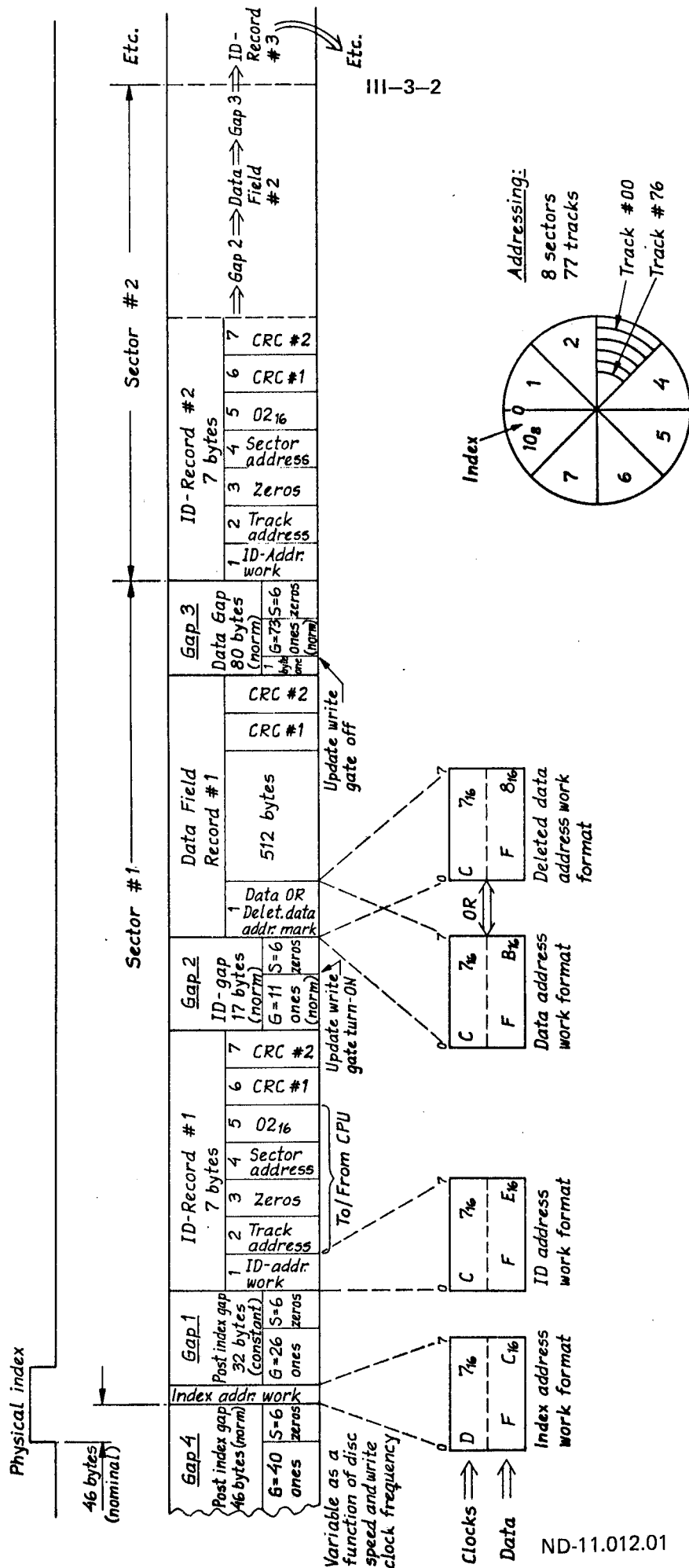
**Table III.3.1: Format Selection**

**NOTES:**

1. Subsystem storage may contain from one to three drives.
2. All diskettes have 77 tracks (0 through 76).
3. Data recording technique is FM for formats A, B, C and M<sup>2</sup>FM for format AA.

Due to the usage of "Soft Sectoring Format (only a physical index pulse is detected on the diskette), a track may be divided into the desired number of sectors.

Only SYS 32-II format is discussed and illustrated in the following sections.



6 = Gap bits consist of ones. (Number will vary for Gap 2, 3 and 4)  
 S = Read Sync-up bits consist of zeros (constant)

Figure III.3.2: FLOPPY DISC - SYS/32-II TRACK FORMAT

### III.3.2 GAPS

Each field on a track is separated from adjacent fields by a number of bytes containing no *data bits*. These areas are referred to as gaps, and are provided to allow the updating of one field without affecting adjacent fields. As can be seen from Figure III.3.2, there are four different types of gaps.

#### III.3.2.1 Gap 1, Post-Index Gap

This gap is defined as the 32 bytes between Index Address Mark and the ID Address Mark for Sector one (excluding the *address mark bytes*). This gap is always 32 bytes in length and is not affected by any updating process.

#### III.3.2.2 Gap 2, ID Gap

The seventeen bytes between the *ID field* and the *data field* is defined as Gap 2 (ID Gap). This gap may vary in size slightly after the *data field* has been updated.

#### III.3.2.3 Gap 3, Data Gap

The eighty bytes between the *data field* and the next *ID field* are defined as Gap 3 (*data gap*). As with the *ID gap*, the *data gap* may vary slightly in length after the adjacent *data field* has been updated.

#### III.3.2.4 Gap 4, Pre-Index Gap

The forty-six bytes between the last *data field* on a track and the *Index Address Mark* are defined as Gap 4 (*pre-index gap*). Initially, this gap is nominally 46 bytes in length; however, due to write frequency tolerances and disk speed tolerances, this gap may vary slightly in length. Also, after the *data field* of record 26 has been updated, this gap may again change slightly in length.

### III.3.3 ADDRESS MARKS

*Address marks* are unique bit patterns, one byte in length and, used in this typical recording format to identify the beginning of *ID* and *data fields* and to synchronize the Deserializing Circuitry with the first byte of each field. *Address Mark* bytes are unique from all other data bytes in that certain bit cells do not contain a clock bit (all other data bytes have clock bits in every bit cell). There are four different types of *address marks* used. Each of these are used to identify different types of fields.

#### III.3.3.1 *Index Address Mark*

The *index address mark* is located at the beginning of each track and is a fixed number of bytes in front of the first record. The bit configuration for the *index address mark* is as shown in Figure III.3.2.

#### III.3.3.2 *ID Address Mark*

The *ID address mark* byte is located at the beginning of each *ID field* on the diskette. The bit configuration for this *address mark* is shown in Figure III.3.2

#### III.3.3.3 *Data Address Mark*

The *data address mark* byte is located at the beginning of each *non-deleted data field* on the diskette. Refer to Figure III.3.2.

#### III.3.3.4 *Deleted Data Address Mark*

The *deleted data address mark* byte is located at the beginning of each *deleted data field* on the diskette. Refer to Figure III.3.2.



**III.3.4** *CYCLIC REDUNDANCY CHECK (CRC)*

Each field written on the diskette is appended with two *Cyclic Redundancy Check (CRC)* bytes. These two CRC bytes are generated from a cyclic permutation of the data bits starting with bit zero of the *address mark* and ending with bit seven of the last byte within a field (excluding the CRC bytes).

When a field is read back from a diskette, the data bits (from bit zero of the *address mark* to bit seven of the second CRC byte) are divided by the same generator polynomial. A non-zero remainder indicates an error within the data read back from the drive, while a remainder of zero indicates the data has been read back correctly from the disk.



### III.4 DATA RECOVERY

From the unit, data and clocks appear as READ DATA. The main tasks for the Data Recovery Circuits are to:

- *separate data from clocks*
- *indicate start of assembly or disassembly of data (Enable BR)*

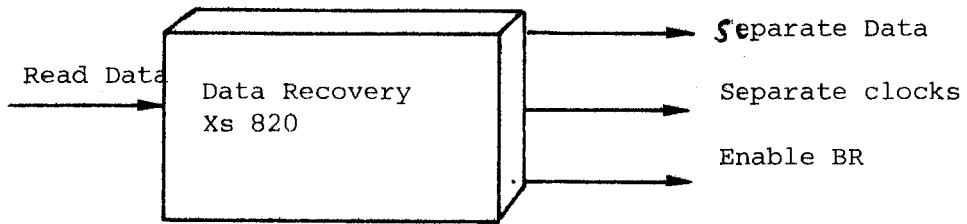
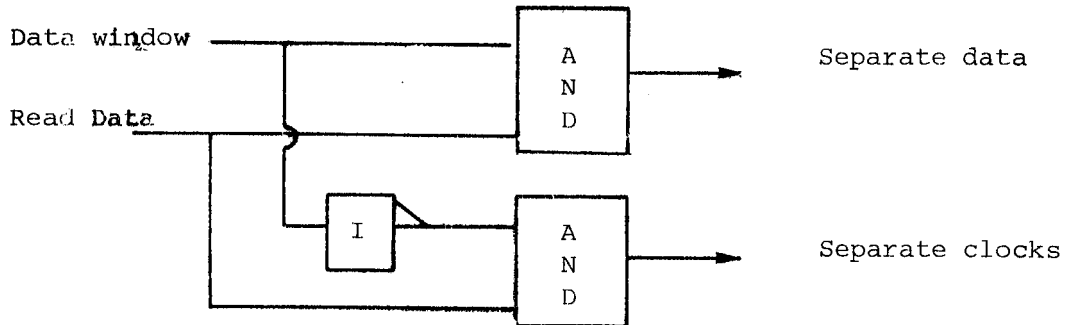


Figure III.4.1: *Data Recovery*

### III.4.1 DATA SEPARATION – GENERAL

A pulse train named *Data Window* is internally generated in the Data Recovery Circuit. Basically, this pulse train is ANDed in its true and inverted form with READ DATA and generates SEPARATE DATA and SEPARATE CLOCKS, respectively. Figure III.4.2 will help illustrate.



**Figure III.4.2:** *Data Separation – General*

SEPARATE CLOCKS will function as main clocks during a read operation while SEPARATE DATA will be assembled and sent to the CPU.

Since the *Data Window* is internally generated in the Formatter, and read clock pulses arrive from the spinning diskette, the initial phase relationship is random.

When a read operation starts, the *Data Window* must be set up such that:

- *READ CLOCKS appear in the middle of the "Data Window", i.e., data will appear in the middle of the "Data Window".*

*A specially designed Sync Up Circuitry handles this task (discussed in Section III.4.2.3).*

Another consideration that should be made is:

- *Should the "Data Window" be symmetrical or not, i.e., should we look for data for the same amount of time as we look for clocks.*

The answer is no – we look for data for 40% and clocks 60% of the cycle time of the *Data Window*. *Peak Shift* (described in Section III.4.2.2.1) is the effect that has been considered.

Variation in spindle speed – Write Oscillator drift, and drift in *Data Window* frequency, is accomplished by adjusting the *Data Window* frequency of the READ CLOCKS from the diskette. A Phase Lock Loop accomplishes this task.

### III.4.2 DATA RECOVERY – FUNCTIONAL OPERATION

Refer to Figure III.4.3 for the following discussion.


#### III.4.2.1 Phase and Frequency Tracking

Phase and frequency tracking is accomplished by a Phase Locked Loop. The VFO (Variable Frequency Oscillator) ① outputs a *ramp voltage* at a frequency of 500KHz. The Comparator Network ② will compare the voltage of the *ramp* at the time when a clock is applied. If the clock pulse (*standardized data*) occurs in the middle of the *ramp*, i.e., when the *ramp* erases ground level, no *error violation* is produced. If the *ramp* has an offset at the clock time – an *error voltage*, corresponding to the offset magnitude and polarity, will be produced.

Due to the *peak shift effect*, etc., clocks will shift back and forth on a short term basis.

A Long Time Constant Integrator Network ③ will produce an average offset (TP 28 *error voltage*) and set up variable impedance change path to the relaxation oscillator and, thus, change the frequency of the clocks read off the diskette.

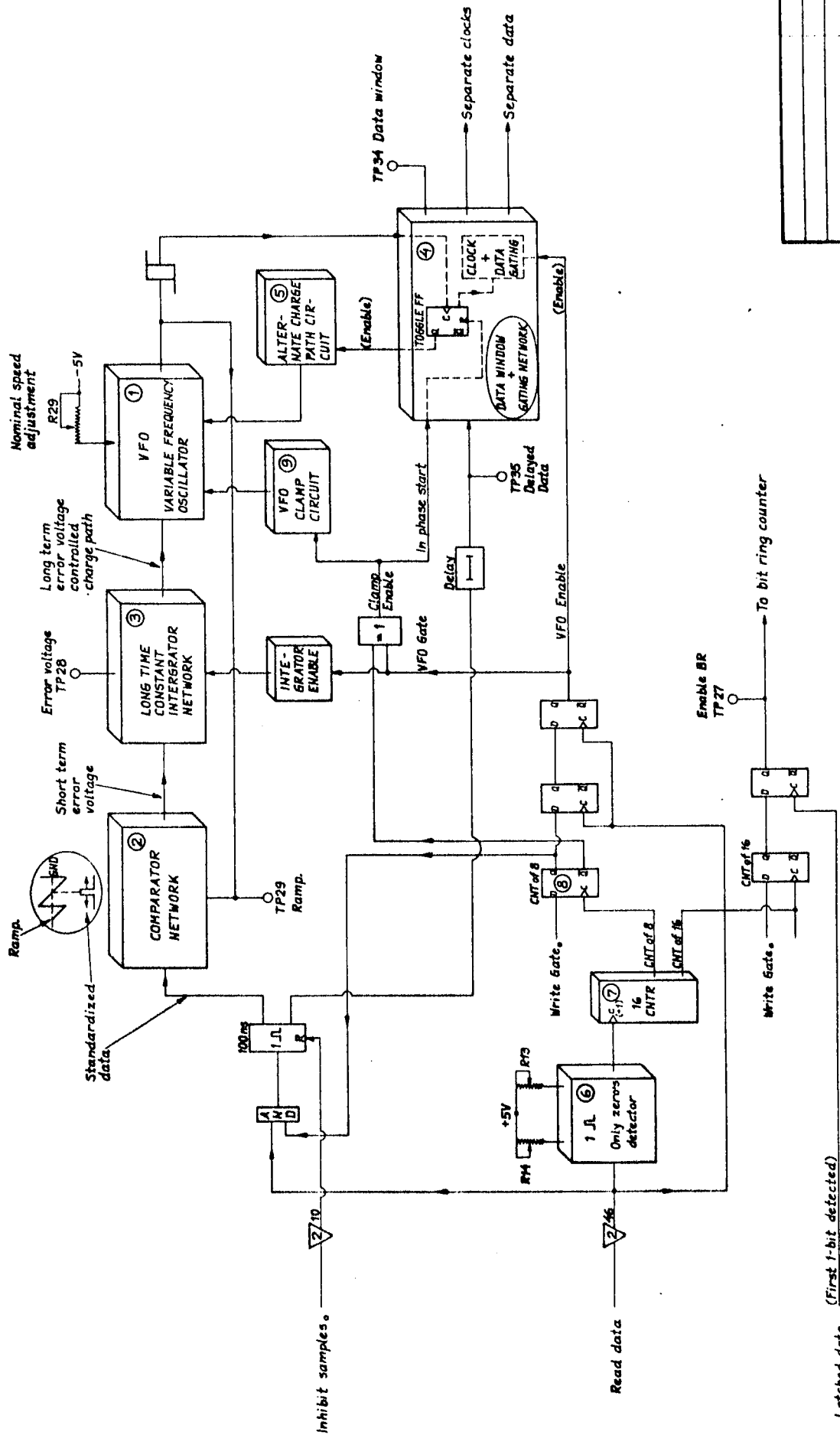
The normal change path for the *relaxation oscillator* ① is through potentiometer R29, i.e., the nominal speed of the oscillator will be set up by this potentiometer. This can be done in one of two ways:

- GND on TP27 (no correction)
- or
- GND on  10 (inhibit samples)

where the latter should be preferred.

#### III.4.2.2 Non-Symmetrical Data Window Generation

The *ramp* formed by the VFO ① is the origin for the Data Window Generation Network ④. The *ramp* will clock a Toggle FF, giving a *Data Window* frequency of 250KHz (TP34). Due to the *Peak Shift* effect (which is NOT precompensated during write) a non-symmetrical *Data Window* is formed to obtain highest possible readability. This is accomplished by the Toggle FF controlling an Alternate Charge Patch Circuit. This circuit will be activated for every second *ramp*, thus, giving a non-symmetrical *Data Window*.



Latched data (First 1-bit detected)

Figure III.4.3.

Project	Date	Sheet	3.8.76
DATA RECOVERY		Topo	3.8.76
Functional Diagram		Kontor	E/B
A/S NORSE DATA-ELEKTRONIKK		Appt.	
		OS 800	

III.4.2.2.1 THE PEAK SHIFT EFFECT

Using modern high frequency techniques, adjacent clocks and data pulses are close enough to interact with each other. The *bit crowding* effect is the interaction of the adjacent pulses.

Because two pulses tend to have a portion of their individual signals superimposed, the actual read-back voltage is the algebraic sum of the two pulses. The *bit crowding* will only take place when the read-back voltage frequency changes. Figure III.4.4 illustrates this.

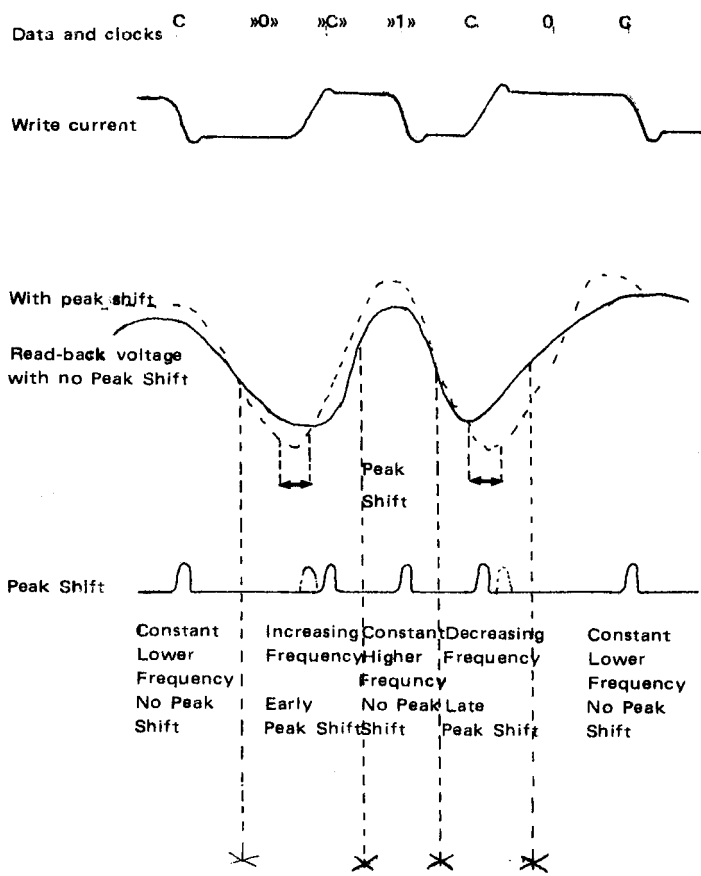


Figure III.4.4: Peak Shift - Illustration



In FM recording technique, each data cell starts with a clock pulse. A "1" data bit will, therefore, be placed between two clock pulses. However, a clock pulse is written between:

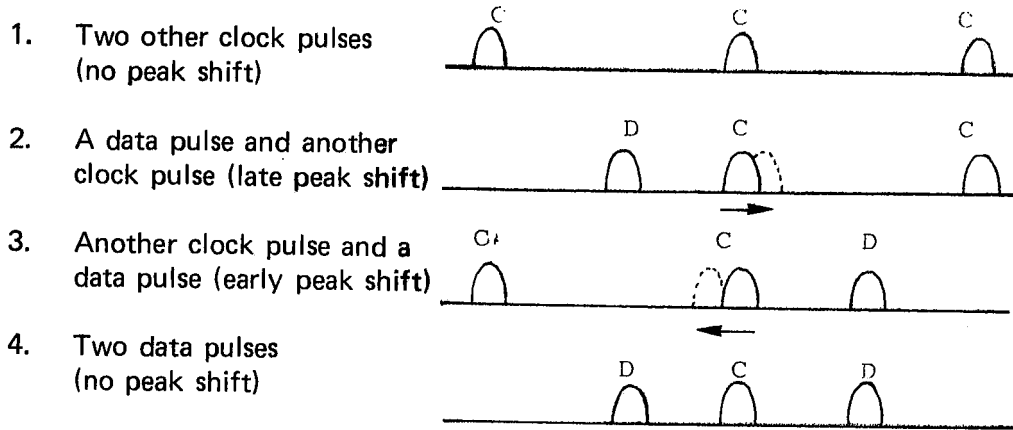


Figure III.4.5: Peak Shift Illustration

In conclusion, a peak shift will not occur to a data bit, but will occur in both directions to a clock pulse. A longer window is, therefore, required for clock pulses than for data pulses.

The ramp (TP29) and, thus, the Data Window (TP34) will, by the Alternate Charge Path Circuit, be formed as depicted in Figure III.4.6.

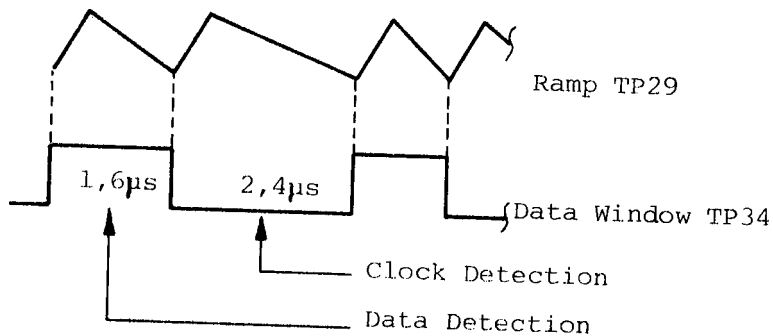


Figure III.4.6: Data Window Generation

### III.4.2.3 *Sync Up Circuitry*

#### III.4.2.3.1 GENERAL

For the following discussion, refer to Figure III.3.2 (SYS/32-II track format). Gaps have been introduced between the *ID record* and *data field* and between *data field* and *ID record*. The nominal gap lengths are indicated in Figure III.3.2. However, the gap lengths will vary slightly while the *data field* is being updated. A gap may be considered as two portions, the first part consists of all ones, while the last part always consists of 6 bytes of zeros, i.e., only clocks written. This part of the gap is rewritten as the *data field* is updated and will, therefore, always consist of 6 bytes. The purpose of those bytes are to sync up the Phase Locked Loop in the Data Separator and set the *Data Window* 180° out of phase of the clocks.

#### III.4.2.3.2 OPERATION

Reading the first part of a gap, the READ DATA line will carry alternating clocks and data pulses. The only Zeros Detector (6) will give no output and the 16 Bits Counter (7) will stay cleared.

As the *Sync-Up Pattern* (6 bytes of zeros) are entered the Only Zeros Detectors (6) will produce a pulse for each zero detected (only clock pulses). The counter (7) will start counting up zeros and as a *Cnt Of 8* is reached, a *Cnt Of FF* (8) sets the clock pulses and will be applied to the Comparator Network (2). A VFO Clamp Circuit (9) will clamp the *ramp* from the oscillator to AV. The Toggle FF located in Data Window and Gating Network (4) will be kept in the cleared state by the clamp. *After two clock pulses the clamp will be disabled and the ramp will go.*

- *The described operation has now set the "Data Window" 180° out of phase with the clock pulses, i.e., in phase then later appearing data pulses.*

At this time, the Long Time Constant Integrator Network (3) is enabled and a closed loop for phase and frequency tracking is established. Separate clocks are now gated to the Formatter as main clocks.

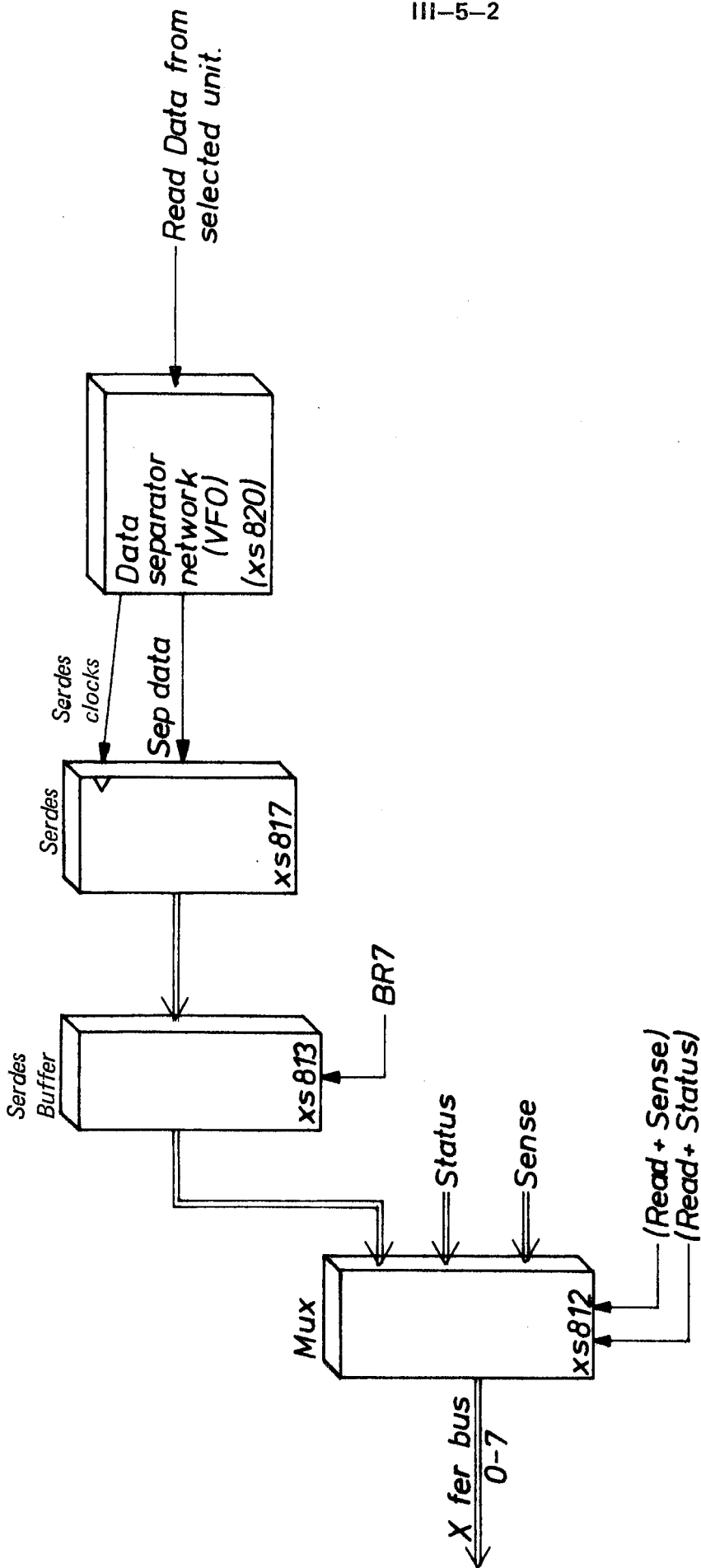
As a count of 16 is reached, we enable "looking for data". When the first data bit is found (first one in the *address mark*), the BR Enable, TP27, becomes active. The process of data assembly is now in process.

**III.5 FORMATTER – DATA FLOW****III.5.1 READ OPERATION**

Refer to Figure III.5.1.

During a read operation data and clocks are received as READ DATA from the selected unit. The Data Separator Network (VFO) (described in Section III.4) will separate clocks and data.

In the Serdes (abbreviation for serializer/deserializer) the data will be assembled into 8 bit bytes. As a new byte is assembled, it will be strobed into a Serdes Buffer. The Multiplexer will select the data byte and send it onto the X-fer bus to the Interface.



III-5-2

ND-11.012.01

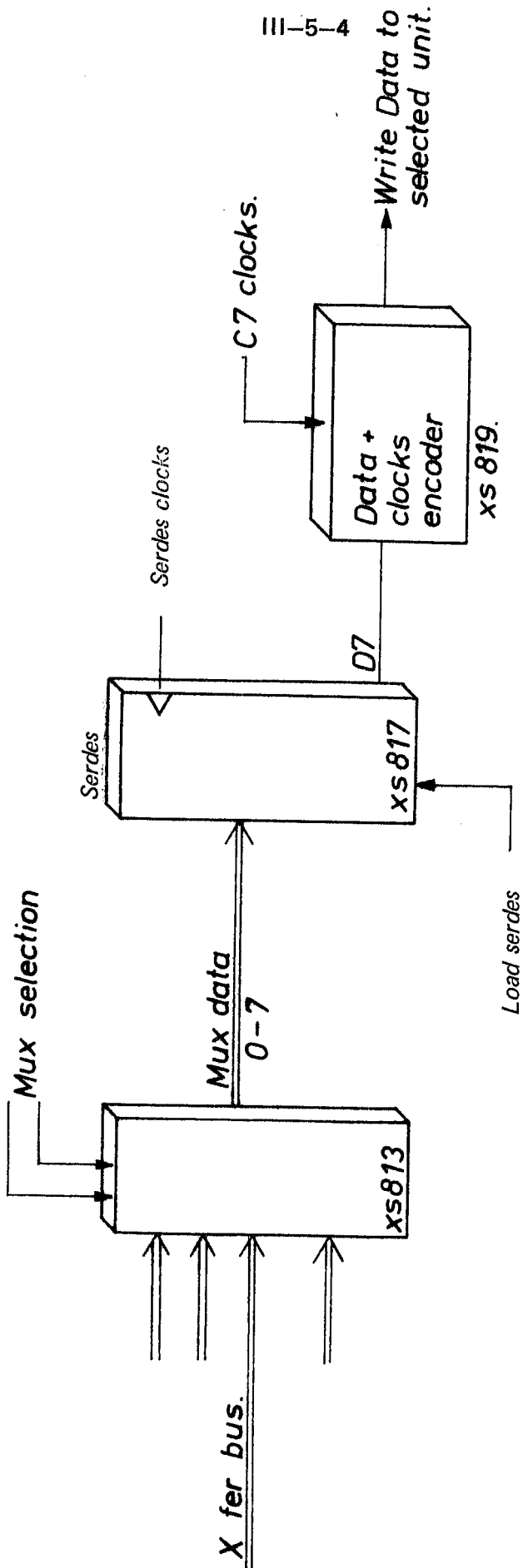
Fig. III-5-1  
READ - DATA FLOW

Tegn. 29.7.76. EIB

**III.5.2**     *WRITE OPERATION*

Refer to Figure III.5.2.

During a write operation, the requested data byte will be selected by the Multiplexer and loaded into the Serdes. The data byte will be disassembled and encoded with clock pulses (clocks and data 180° out of phase) and sent to the selected unit.



III-5-4

Fig: III - 5-2  
WRITE - DATA FLOW.

## III.6 READ/WRITE CONTROL

### III.6.1 GENERAL

This section describes commands previously referred to as "any READ or WRITE" commands (Section II.2).

The commands are:

- *Format Track*
- *Write Data*
- *Write Deleted Data*
- *Read ID*
- *Read Data*

The above mentioned commands will be executed by a Special Purpose Microprocessor. The commands will generate a start address (entry point) — and the microprocessor will increment or branch through a predetermined sequence of states. The microprocessor will increment or branch to the next state depending upon certain conditions decoded in the different parts of the logic. When the microprocessor is not busy with "any READ or WRITE", it remains in its idle state (State A) indicated by R/W Idle being active. Upon completion of any of the above mentioned commands, the microprocessor will return to this state (State A).

The microprocessor is composed of the following building blocks:

- *An Increment Condition Selector*
- *A Branch Condition Selector*
- *A Five Bit Program Counter*
- *A 32 bits by 32 locations read only memory (ROM)*
- *Command Latches*

The ROM addresses will be referred to as State A through N. (Refer to Figure III.6.6.)

III.6.2 *READ ID*

The READ ID command causes the Formatter to transfer the first *ID field* encountered by the Read/Write head from the selected drive. The four bytes of data contained in the *ID field* are transferred to the Interface via the X-fer bus. The contents of the bytes are shown below, in the order of transfer.

<u>Byte No.:</u>	<u>Contents:</u>
1	Track address represented in binary (0-76)
2	Binary zero
3	Sector address represented in binary (1-10g)
4	Hex 02

See also Figure III.2.1 representing the Sys 32-II Track Format.

As each of the four bytes are read off the diskette, they are assembled and placed on the X-fer bus on the way to the Interface. Refer to Figure III.5.1 illustrating the data flow.

After transferring the four *ID bytes*, the Formatter reads the next two **CRC bytes**, checking for CRC error on the field just transferred. If the *CRC bytes* read "compare" (CRC syndrom = 0), with the CRC generated for the data just read, a non-error INTERRUPT is generated with corresponding status of R/W COMPLETE.

- *If there is a "mismatch", a UNIT CHECK INTERRUPT is generated and the CRC ERROR sense bit is set along with status of R/W COMPLETE.*
- *If the Formatter detects no "ID address mark" within a full revolution of the diskette (2 index pulses), a UNIT CHECK INTERRUPT is generated and the NO AM sense bit is set (without R/W COMPLETE).*
- *The DATA OVERRUN sense bit is set during the READ ID command if the Interface does not respond to a TRANSFER REQUEST in sufficient time to insure correct storage of each data byte. That is, if a new data byte is ready on the X-fer bus before TRANSFER GRANT has been received for the previous byte, the overrun condition is detected. In this case, the read operation is allowed to continue to its normal ending, but the Formatter presents a status of UNIT CHECK as well as R/W COMPLETE.*



### Read ID - State Diagram

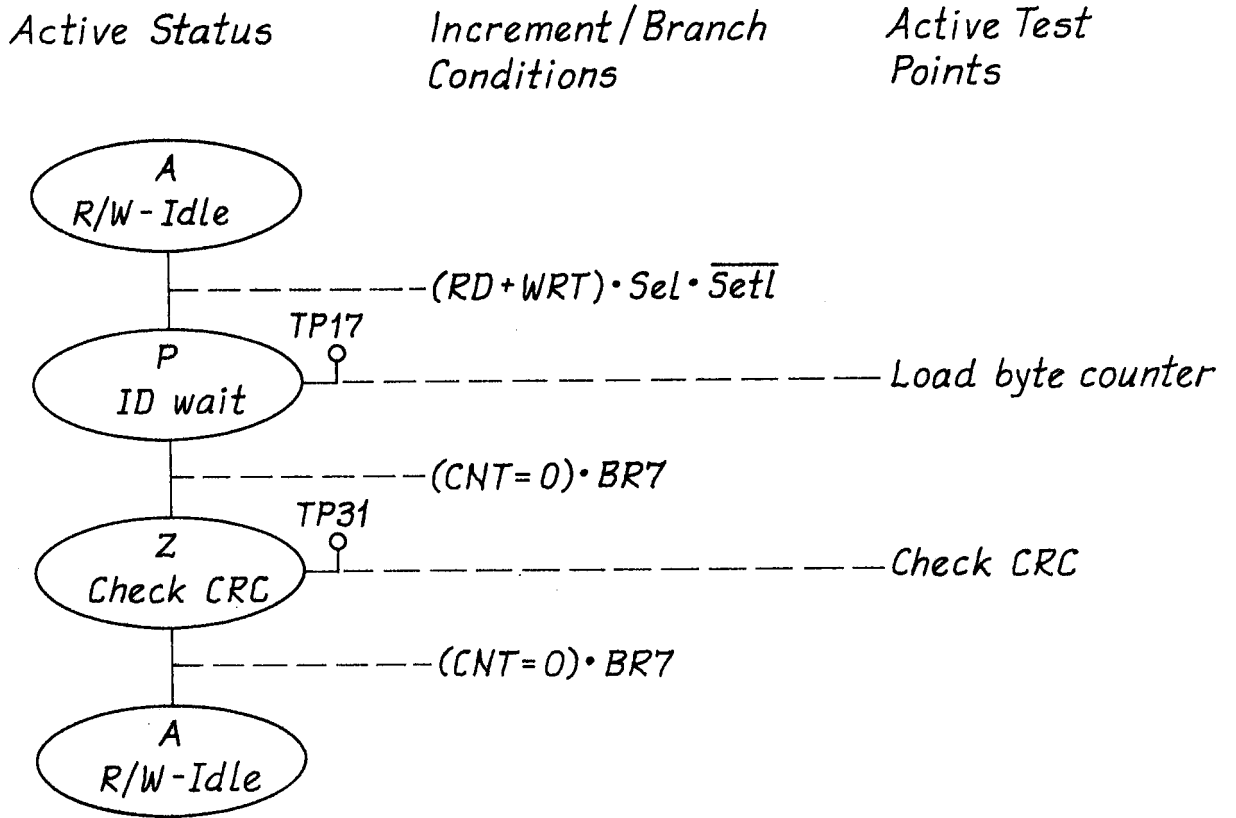


Figure III-6-1

Note: For more detailed study, ref. fig. III-6-6 and appendix D

### III.6.3 READ DATA

The READ DATA command provides for the transfer of the *data field* of the requested record from the diskette to the Interface. The Interface must supply the Formatter with a prerequisite argument (sector) by placing the sector address byte on the X-fer bus and pulsing LOAD SECTOR line. The subsequent READ DATA command forces the Formatter to read each *ID field* encountered (not transferring bytes to the Interface) until a comparison is obtained between the third byte of an *ID field* (sector byte) and the desired sector. The Formatter then reads the next *data field* encountered, transferring each *data byte* (excluding the *data field address mark*) to the Interface Buffer in the manner defined for READ ID. After transferring the *data field*, the Formatter checks for a CRC read-error and:

- *generates a R/W COMPLETE with UNIT CHECK INTERRUPT for a read error.*
- *If the desired "data field" is preceded by a "deleted data address mark", rather than the "normal data address mark", the DELETED RECORD status bit is set and is also presented to the Interface in the servicing of the command completion INTERRUPT.*
- *DATA OVERRUN and NO AM errors are defined for the READ ID command.*
- *In addition, if while searching the track for the requested record, a CRC read error is encountered at any "ID field", command execution is immediately halted and a UNIT CHECK INTERRUPT is generated.*
- *An error condition also results if the desired record cannot be located. That is, the MISSING SECTOR sense bit is set (with its associated UNIT CHECK INTERRUPT when a sector byte comparison is not obtained within one full revolution of the diskette (2 index pulses).*

*Correct usage of the READ DATA command presumes that the R/W head has been previously positioned to the track of the record desired.*

# III-6-5 Read Data - State Diagram

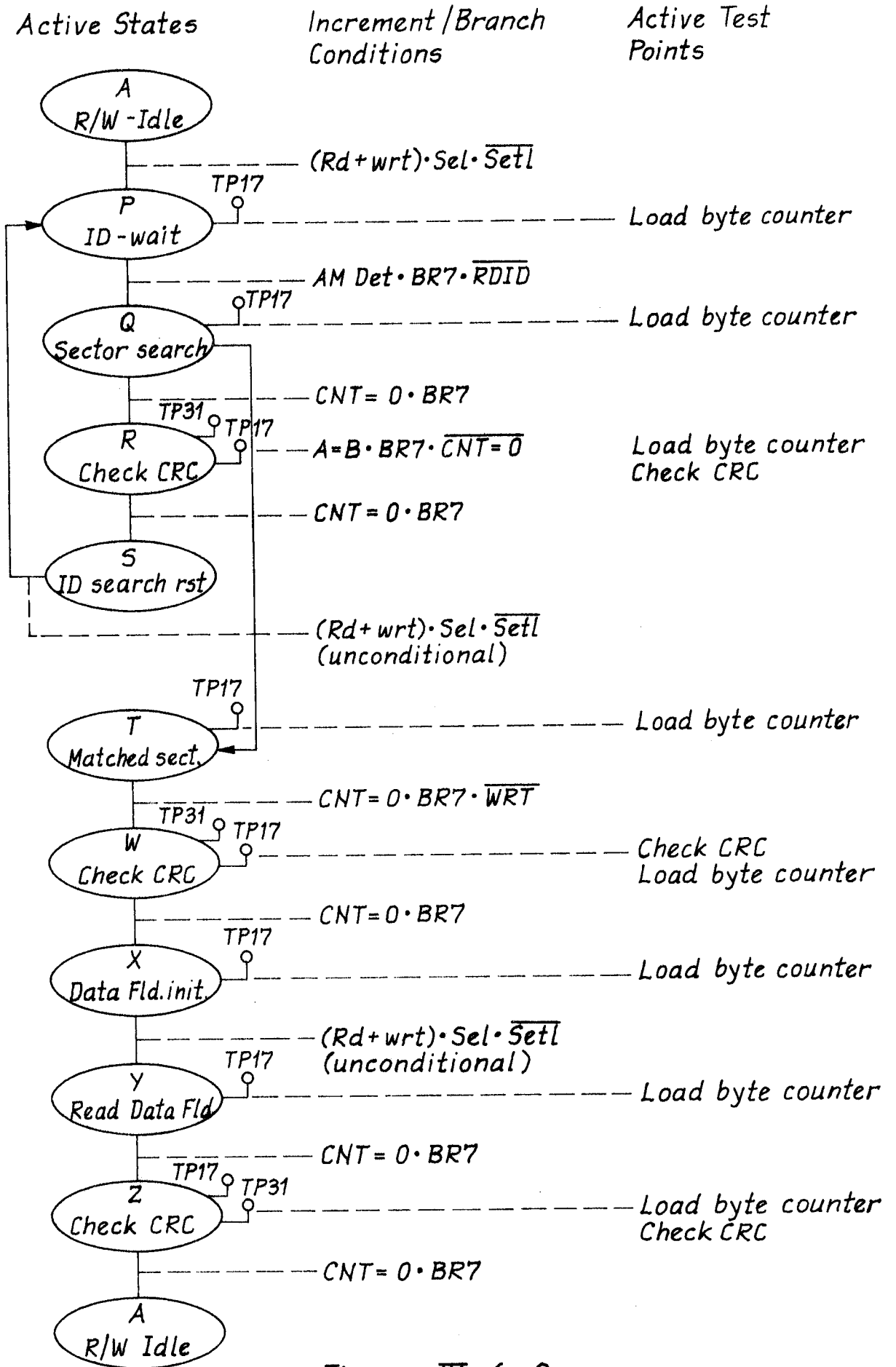


Figure III-6-2

Note: For more detailed study, ref. fig. III-6-6 and appendix D  
ND-11.012.01

#### III.6.4 WRITE DATA

The WRITE DATA command provides the system function of storing a record on the selected drive's diskette. The Interface must supply the Formatter with a prerequisite argument (sector) by placing the *sector address byte* on the X-fer bus and pulsing LOAD SECTOR line.

The subsequent WRITE DATA command forces the Formatter to read each *ID field* encountered until a comparison is obtained between the third byte of an *ID field* (sector byte) and the desired sector. The Formatter then sequences up the write circuitry in the gap following this *ID field* and starts writing zero bytes. At the end of the gap (17 bytes) the Formatter writes the *data address mark* and requests the Interface to provide the first *data byte*. The Formatter then writes the *data field*, controlling the transfer of each *data byte* from the Interface. As each byte is needed by the diskette, the Formatter activates TRANSFER REQUEST. When the Interface has supplied the requested data on the X-fer bus, it responds with TRANSFER GRANT. When the Formatter accepts the data byte, it deactivates TRANSFER REQUEST, resetting TRANSFER GRANT. TRANSFER DIRECTION is held at a constant logical zero level to indicate a WRITE transfer operation.

After writing the *data field data bytes*, the Formatter writes two **CRC bytes** which have been generated over the field (including the *address mark*). At this point, the Formatter has completed the WRITE DATA command and it generates an INTERRUPT with R/W COMPLETE STATUS.

- *The Control Unit terminates WRITE DATA command execution if any of the following conditions are detected.*  
  
*NO AM + MISSING SECTOR*  
*or*  
*CRC ERRORS.*
- *The NO AM + MISSING SECTOR error is defined as for the READ DATA command. CRC ERROR may be generated while searching the desired "ID field", before performing a WRITE operation. These error conditions generate a UNIT CHECK INTERRUPT with the corresponding sense bit set.*
- *The R/W COMPLETE bit is never set with the above error conditions.*

- *The DATA OVERRUN sense bit is set during the WRITE DATA command if the Interface does not respond to a TRANSFER REQUEST in sufficient time to insure correct writing of each "data byte". That is, if the Formatter needs a new "data byte" on the X-fer bus before TRANSFER GRANT has been received (to indicate that a byte is ready from the Interface) the overrun condition is detected. The WRITE operation continues to its normal ending (still writing X-fer bus data without sending TRANSFER REQUEST), but at completion of the command a status of UNIT CHECK as well as R/W COMPLETE is presented to the Interface.*

## Write Data - State Diagram

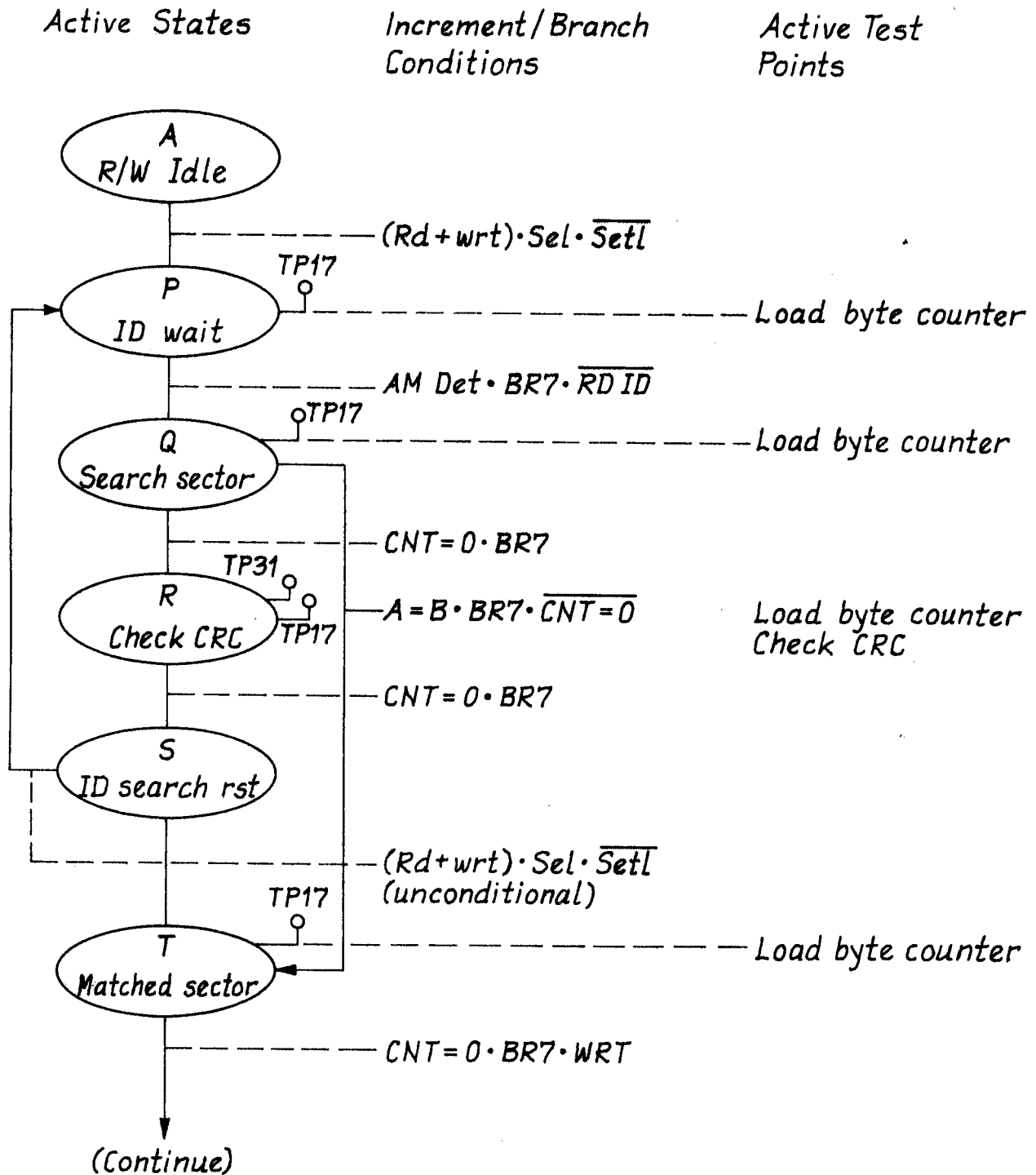


Figure III.6.3, continued on following page

III-6-9  
Write Data - continued

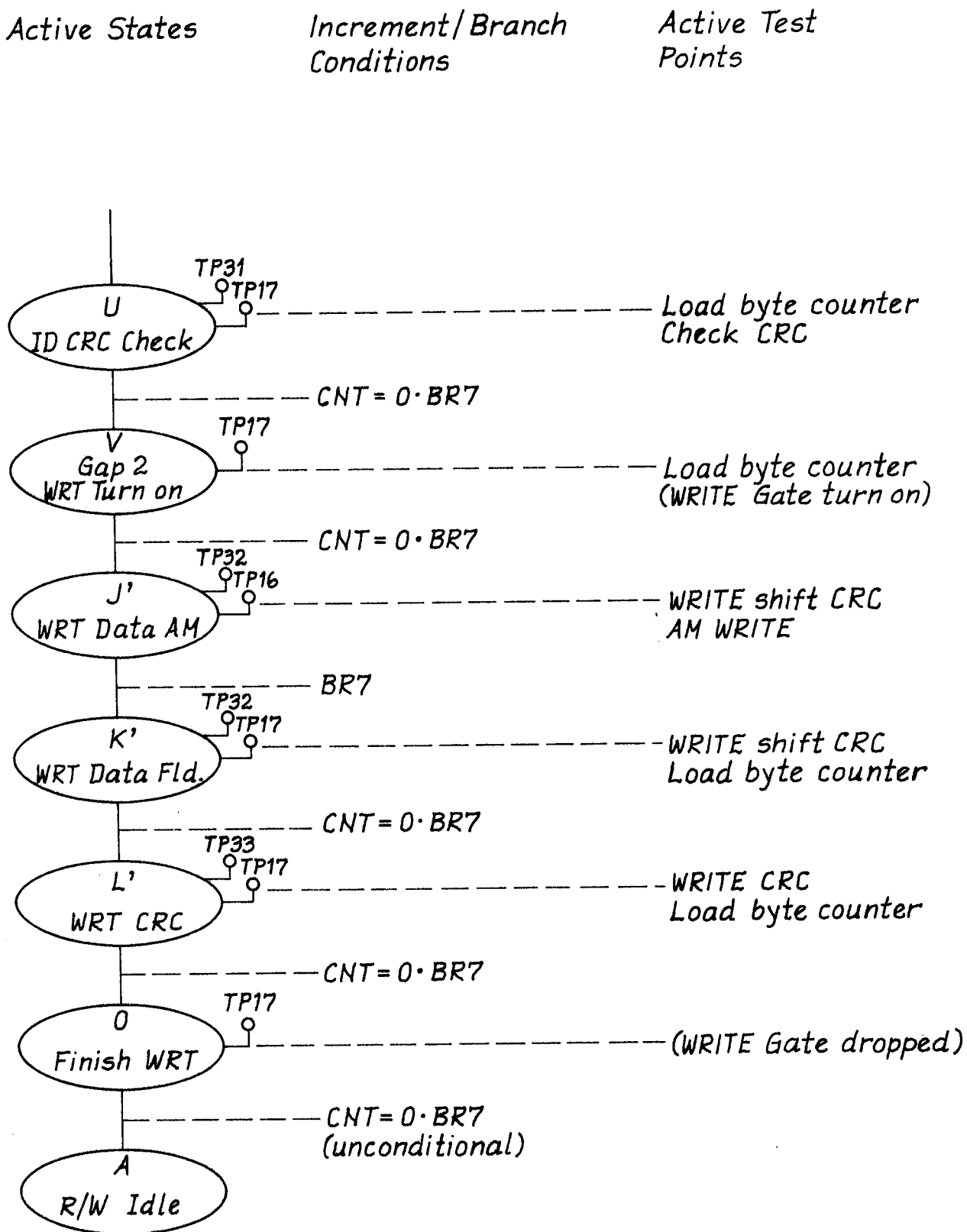


Figure III-6-3

Note: For more detailed study, ref. fig. III-6-6 and appendix D

**III.6.5**     *WRITE DELETED DATA*

The WRITE DELETED DATA command is operationally identical to the WRITE DATA command, but results in the Formatter writing a *deleted data address mark* byte in front of *data field*.



# WRITE Deleted Data - State Diagram

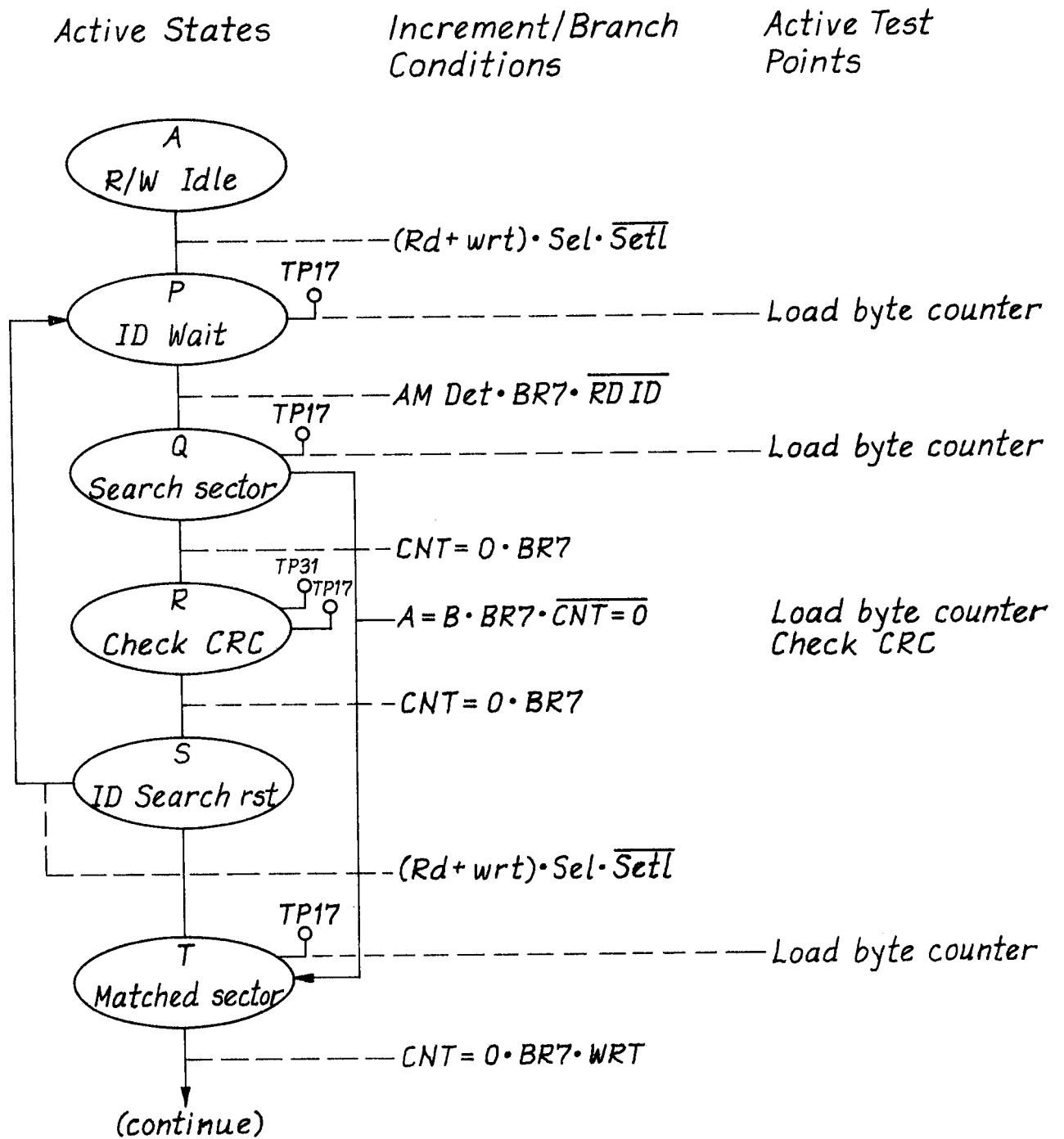


Figure III.6.4, continued on next page

WRITE Deleted Data - continued

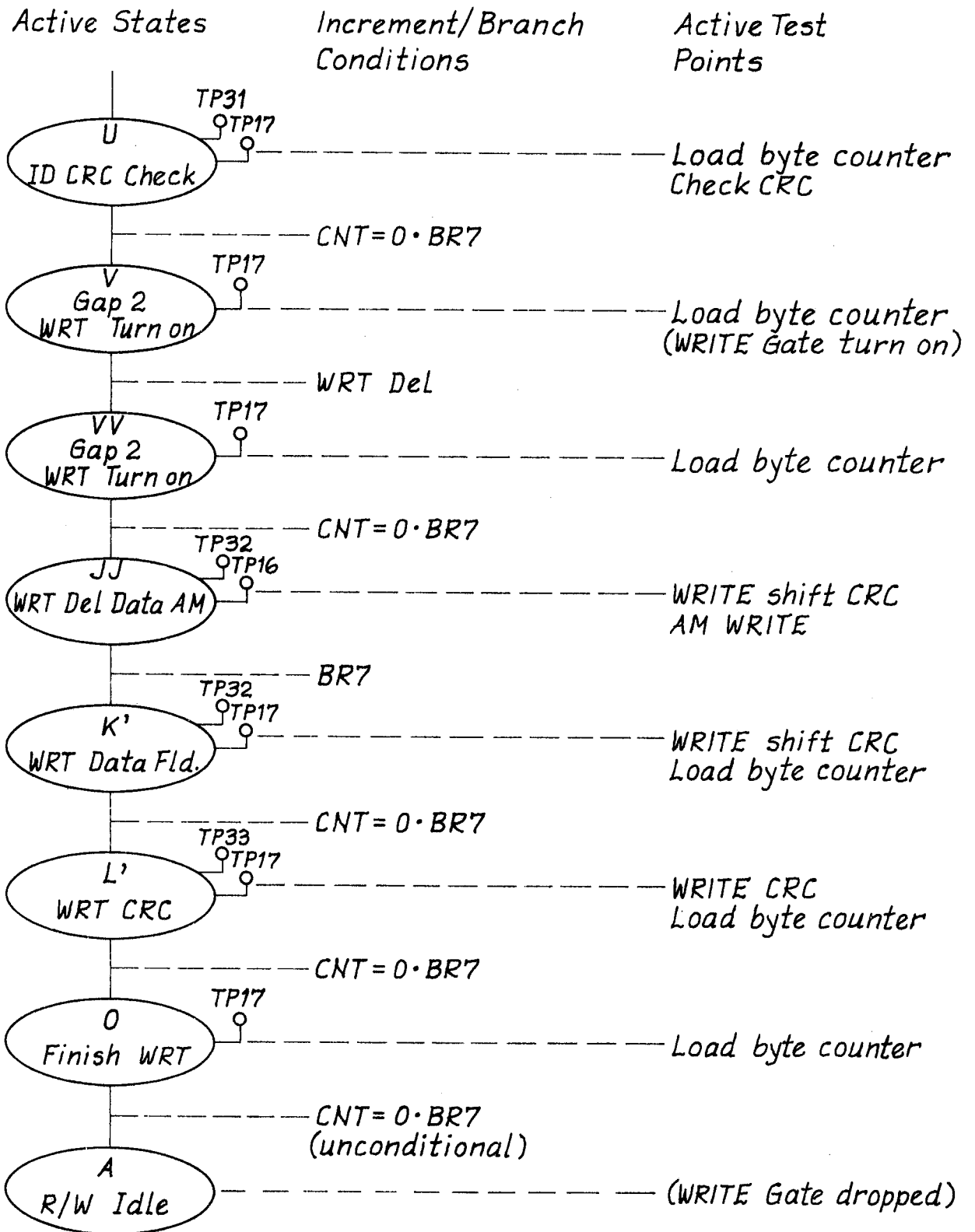


Figure III-6-4

Note: For more detailed study, ref. fig. III-6-6 and appendix D

### III.6.6 *FORMAT TRACK*

The *FORMAT TRACK* command provides the function of writing an entire track in the format illustration in Figure III.3.2.

This provides full diskette initialization capabilities. In the execution of this command, the Formatter provides all *Gap*, *Address Mark*, and *CRC bytes* while the Interface provides the 4 *ID bytes* and all *data bytes* for each record (under Formatter transfer control).

When the Formatter receives the *FORMAT TRACK* command it waits for the Index pulse from the selected drive, then writes:

- *"1" bytes until the end of Gap 1*
- *the Index Address Mark*
- *"1" bytes for Gap 1*
- *the "ID address mark" for the first "ID field", and requests the first byte from the Interface. It continues from this point, to write ID and data bytes (received from the interface) and formatting bytes (generated from the Formatter) (Gaps, Address Marks, CRC) until the last data field is written. At this point, the Formatter starts writing*
- *"1" bytes for Gap 4 and continues writing until the Unit's Index signal is detected again (one full revolution)*

All address marks are preceded by six bytes of "zero" in the gap.

Data transference from the Interface is controlled in the same manner as described for the *WRITE DATA* command. At detection of the second Index pulse, the Formatter presents the end status *INTERRUPT*, *R/W COMPLETE*. The *DATA OVERRUN* error is defined as described for the *WRITE DATA* command. If *DATA OVERRUN* is detected, the Formatter finishes writing the record which it was writing (using X-fer bus data), then starts writing Gap 4 (all one bytes) until detection of Index. At this point it presents an *INTERRUPT* status of *R/W COMPLETE* and *UNIT CHECK*. The *DATA OVERRUN* sense bit indicates to the Interface that all records of the current track were not formatted.

A special consideration for the *FORMAT TRACK* command is that the Formatter writes only *data address marks* at the beginning of each *data field*. If the user desires *deleted data address marks* for certain records, the Interface must follow the *FORMAT TRACK* command with a *WRITE DELETED DATA* command for each record to be deleted.

## Format Track - State Diagram

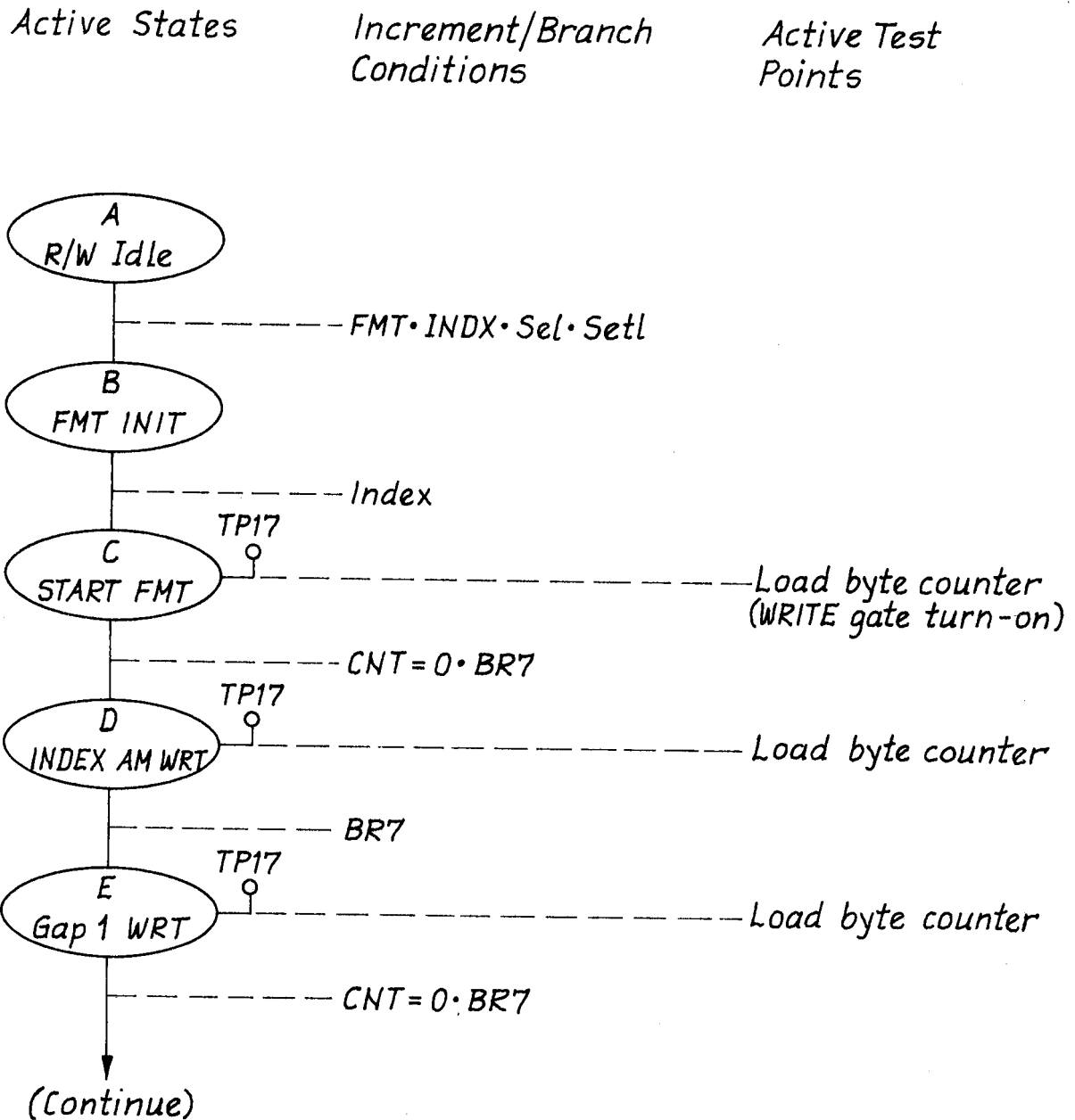


Figure III.6.5, continued on next page

Format Track - continued

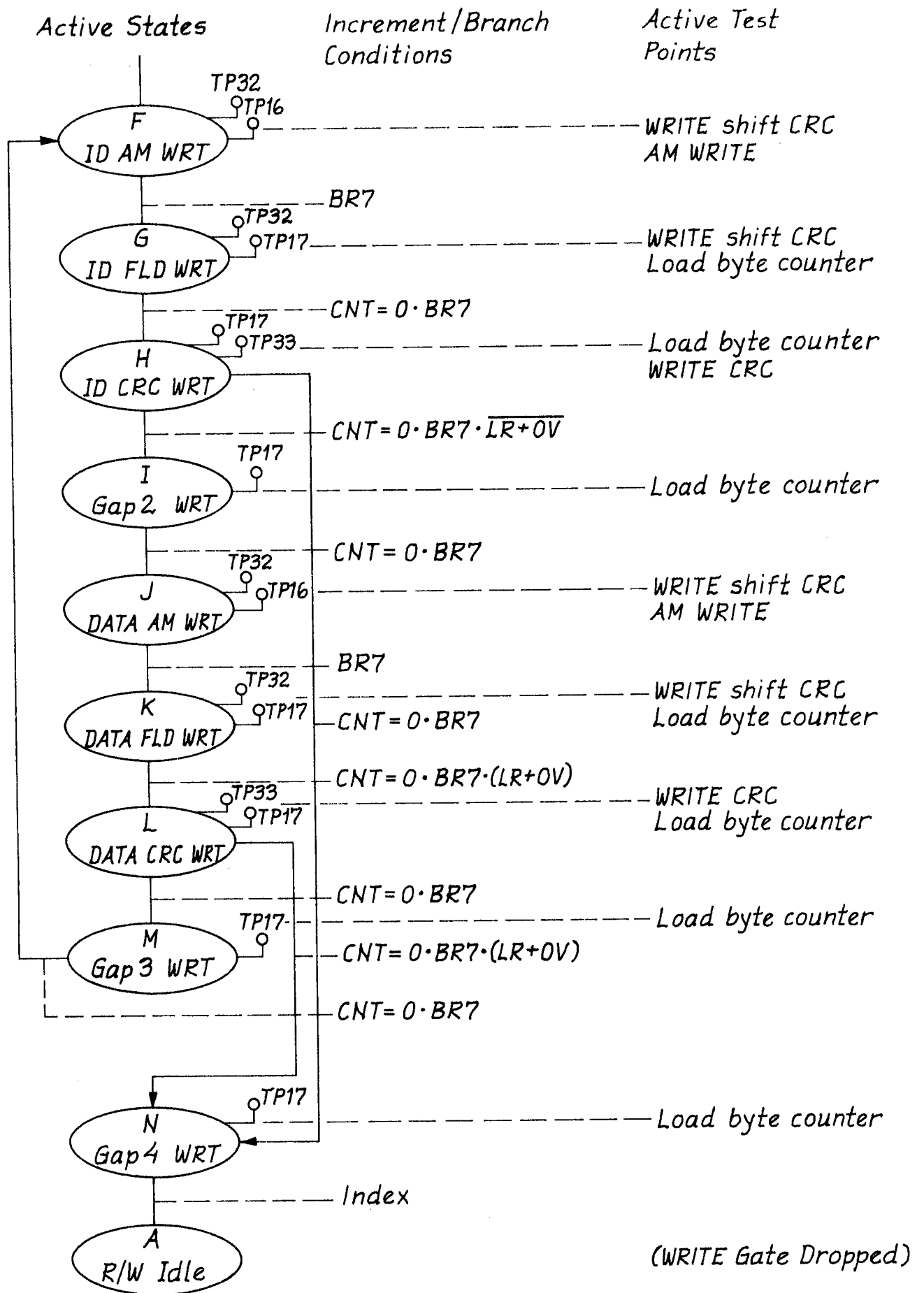


Figure III-6-5



PROM 5 PATTERN.

	IBM SYS 32 (512) FORMAT (512)	0 0 0	<u>SYS 32 (512)</u> OPTIONAL FMT = 1 512 256 = 1									
			7	6	5	4	3	2	1	0		
ID LENGTH	4	0 0 0	1	1	1	1	1	1	1	1		
GAP 4 LENGTH	46	0 0 1	1	1		1				1		
GAP 1 LENGTH	32	0 1 0	1	1		1	1	1	1	1	1	
NO. OF RECORDS	8	0 1 1	1	1	1			1	1	1	1	
CRC LENGTH	2	1 0 0	1	1	1	1	1	1	1	1		
GAP 2 LENGTH	17	1 0 1	1	1	1			1	1	1	1	
GAP 3 LENGTH	80	1 1 0	1			1	1					
DATA LENGTH	512	1 1 1										
SYNC.UPLength	6											

Ref. sys. 32 sector format.

**NOTE:**

Only the pattern related to sys 32 is illustrated.

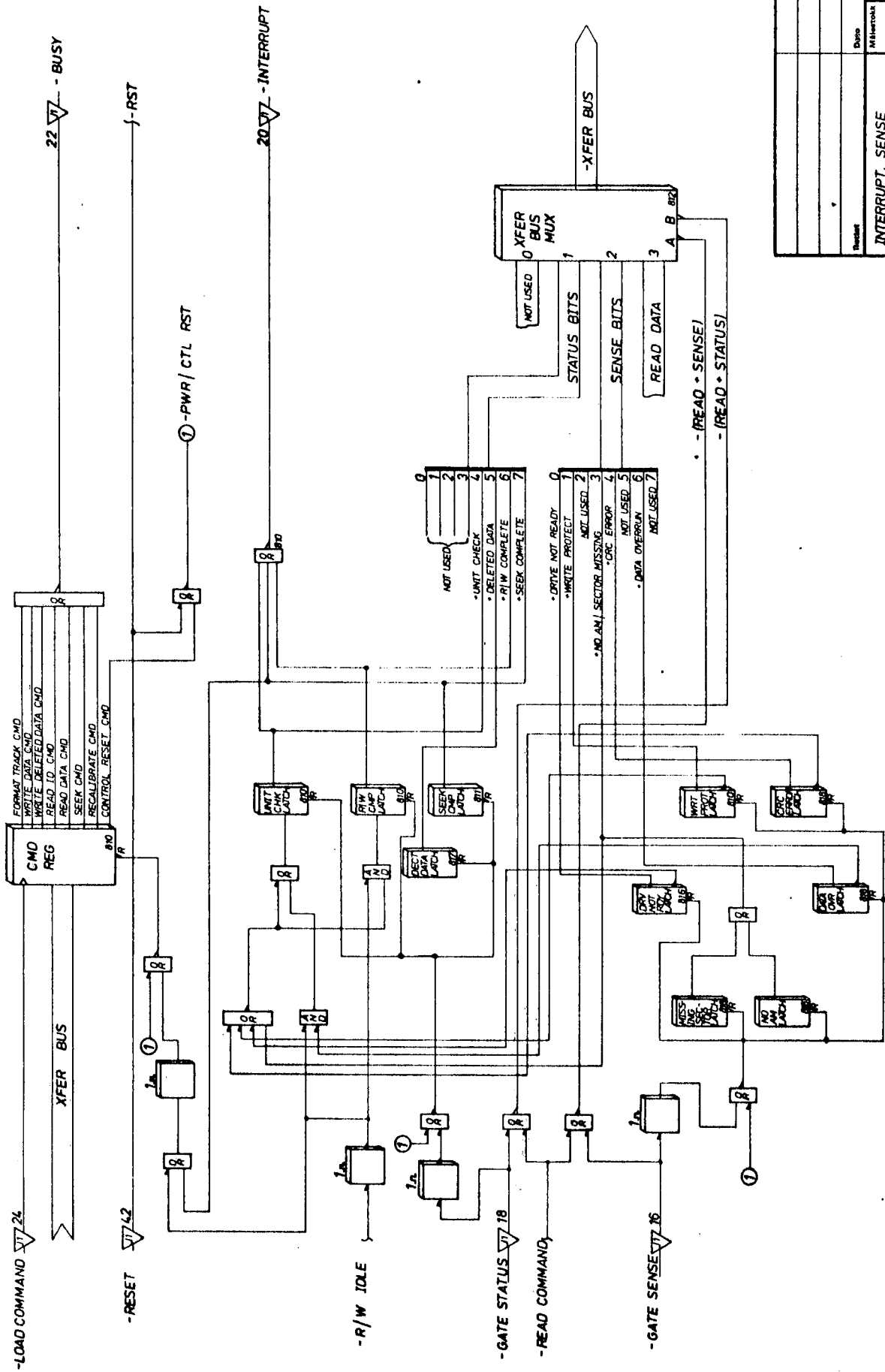
Figure III.6.7.





### III.7 INTERRUPT, SENSE AND STATUS

For explanation of the above heading refer to: Section II.2 (General Command Sequence – Interface/Formatter) and Section II.3 (Interrupt Generation and Handling). Refer also to Figure III.7.1. Also, the description of the INTERFACE Lines involved in the above mentioned figure, may be reviewed in Section II.1. Status and Sense bits descriptions are also described in Section II.1.



Sheet	Microchips	Rev. 3.8.76
Interrupt, Sense and Status	Microchips	Rev. 3.8.76
A/S NORSEK DATA-ELEKTRONIKK		

Figure III.7.1.

**III.8 ANY SEEK OPERATION**

**III.8.1 GENERAL**

For the following study, refer to Figure III.8.1. Refer also to Section III.1 for description of DIRECTION SELECT, STEP and TRACK 00. The remaining INTERFACE signals are described in Section II.1.

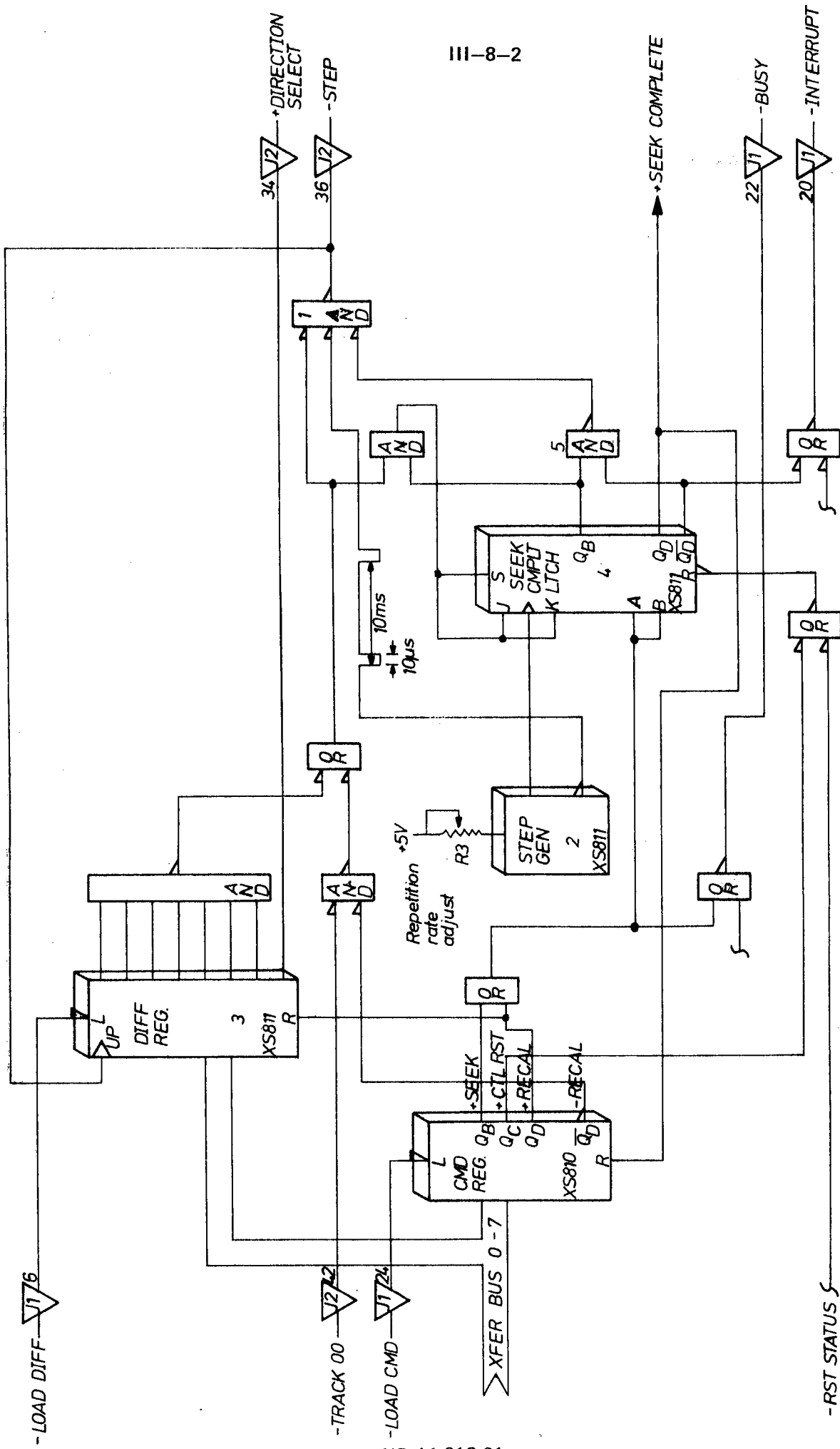


Fig. III - 8 - 1

SEEK / RECALIBRATE

### III.8.2 SEEK OPERATION

Prior to a seek operation, the actual track number will be loaded into the Difference Register. Since the bits on the X-fer bus are active when low, the Difference Register will hold the desired track number in its 1's complemented form. The DIRECTION is given by X-fer bus No. 7.

Three conditions must be met ① in order to send STEP pulses to the Unit:

1. STEP pulses ② (always present)

The step pulses are generated from a free running RC oscillator with adjustable repetition rate. (Pulse with  $10\mu\text{s}$ , nominal repetition rate 100Hz.)

2. Difference Register ③ different from all 1s (non-zero difference). A LOAD DIFFERENCE has been executed.

3. SEEK command issued.

This command will parallel load the SEEK Complete Latch ④ with  $1100_2$  giving  $Q_B = Q_D = 1$ . ⑤.

As the STEP pulses are sent to the Stepper Control Logic in the selected unit, the pulses will also increment the Difference Register ③.

Reaching a count of all 1s, no more STEP pulses will be sent to the unit.

At this point in time, the unit has not performed the last STEP (10ms) and additional 10ms *head settling time* should elapse before generating SEEK COMPLETE, drop BUSY and send an INTERRUPT to the Interface.

The 20ms delay is introduced by SEEK Complete Latch now working as a shift register. After performing two shifts SEEK COMPLETE is generated.

**III.8.3 RECALIBRATE**

Specifying a recalibrate will set the Difference Register to all zeros, i.e., tracks to go will be 127, and the DIRECTION will indicate a reverse seek.

In order to send the STEP pulses to the unit, the following three conditions must be met:

1. *STEP pulses ② (always present)*
2. *Difference Register ③ different from all 1s.  
("Recalibrate" will set it to all 0s.)*
3. *A "Recalibrate" is specified. This command will parallel load the SEEK Complete Latch with 1100<sub>2</sub>.*

The termination condition occurs when doing a Recalibration by receiving a "TRACK 00" indication from the unit (described in Section IV.3.3.3). The SEEK Complete Latch will now be changed from being a latch to a shift register, thus, allowing 20ms from reception of TRACK 00 until SEEK COMPLETE is generated. This is to allow time to perform the last step (10ms) plus *head settling time* (10ms).

As SEEK COMPLETE is activated, BUSY will drop and INTERRUPT generated.

**SECTION IV**

**UNIT**





## DETAILED CONTENTS

+ + +

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IV.1 DISKETTE STORAGE DRIVE

IV.1.1 GENERAL

The SA800 Diskette Drive consists of Read/Write and Control Electronics, Drive Mechanism, Read/Write head, Track Positioning Mechanism and the removable Diskette. These components perform the following functions:

- Interpret and generate control signals
- Move Read/Write head to the desired track
- Read and Write data

The relationship and INTERFACE SIGNALS for the internal functions of the SA800 are shown in Figure IV.1.1.

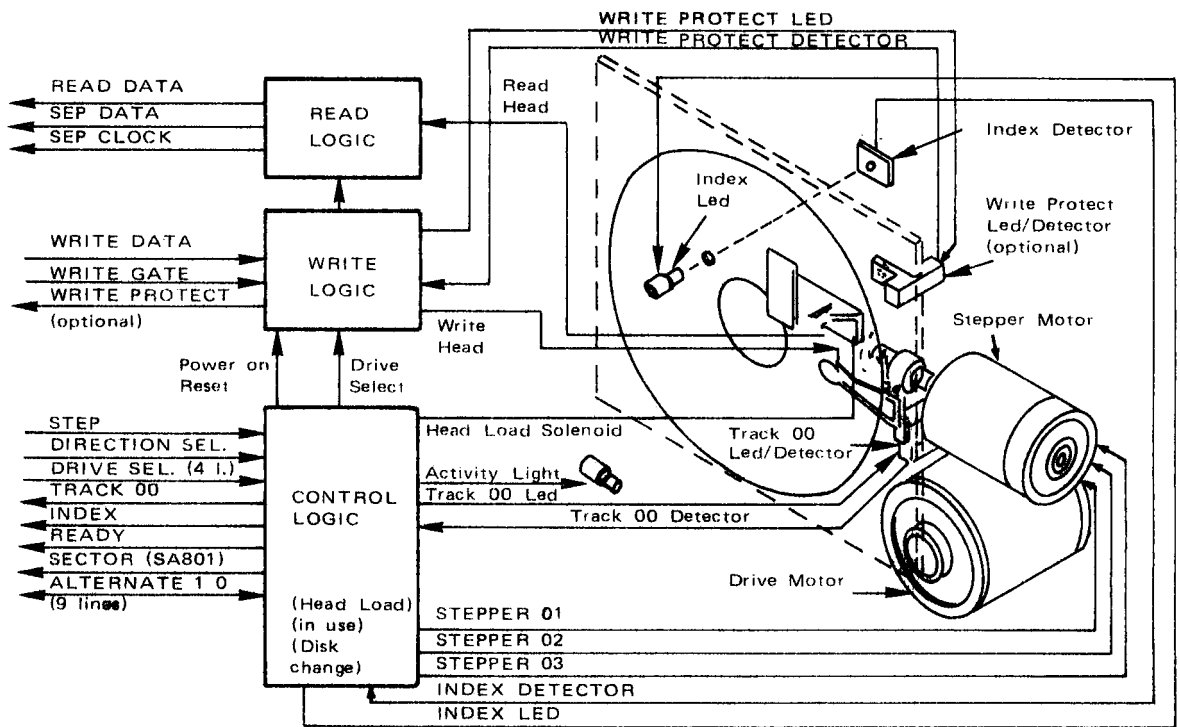


Figure IV.1.1: SA800 Functional Diagram

The Head Positioning Actuator positions the Read/Write head to the desired track on the Diskette. The Head Load Actuator loads the Diskette against the Read/Write head and data may then be recorded or read from the Diskette.

The electronics are packed on one PCB. The PCB contains:

- *Index Detector Circuits (Sector/Index for 801)*
- *Head Position Actuator Driver*
- *Head Load Actuator Driver*
- *Read/Write Amplifier and Transition Detector*
- *Safety Sensing Circuits*

IV.1.2 HEAD POSITIONING

An electrical stepping motor (Head Positioning Actuator) and lead screw positions the Read/Write head. The stepping motor rotates the Lead Screw clockwise or counter clockwise in 15° increments. A 15° rotation of the Lead Screw moves the Read/Write head one track position. The Formatter increments the stepping motor to the desired track.

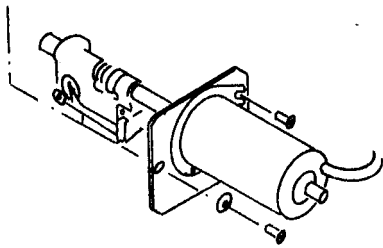


Figure IV.1.2: Head Positioning Actuator

Figure IV.1.3a shows the R/W head in *loaded* position while Figure IV.1.3b shows the R/W head in *unloaded* position.

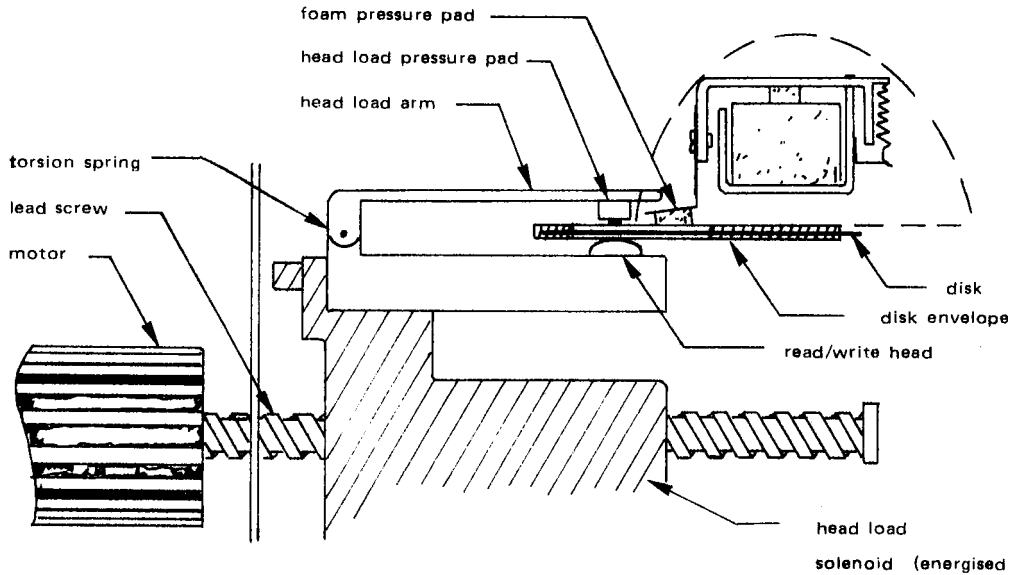


Figure IV.1.3a: Read/Write Head – Loaded

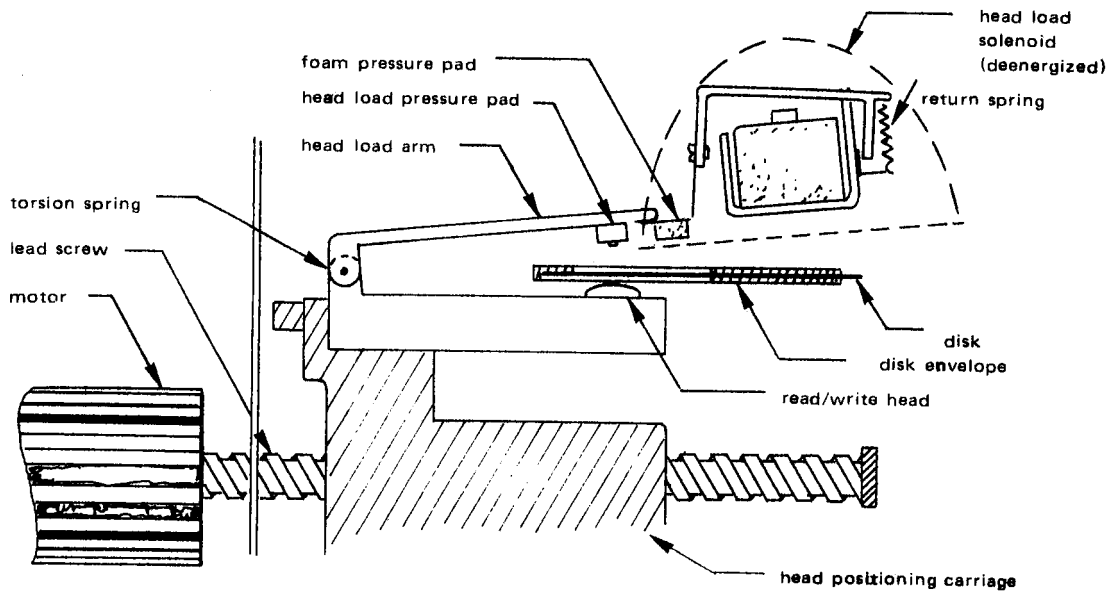
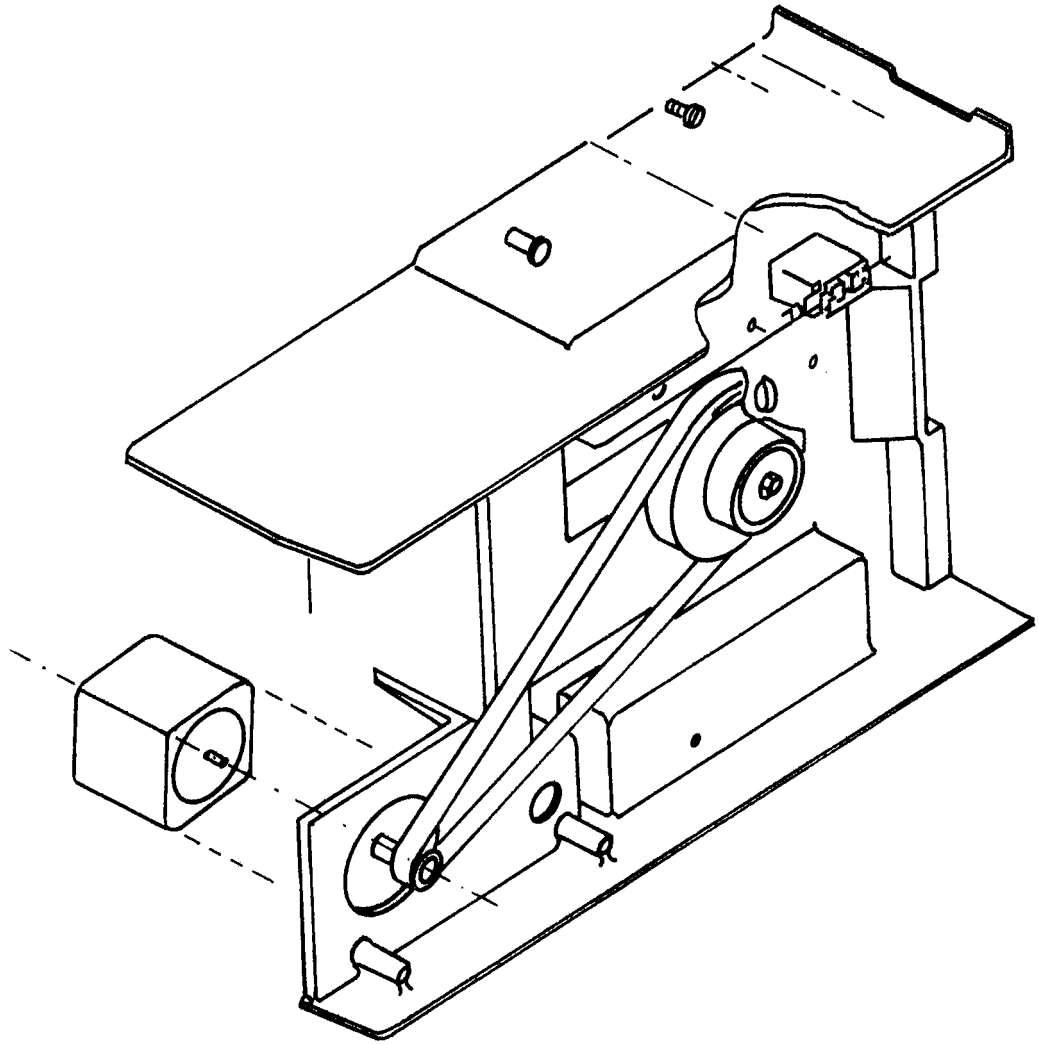


Figure IV.1.3b: *Read/Write Head – Unloaded*

**IV.1.3**     *DISKETTE DRIVE SPINDLE*

The Diskette Drive Motor rotates the spindle at 360 rpm through a belt-drive system. 50 or 60 Hz power is accommodated by changing the drive pulley. A Registration Hub, centered on the face of the Spindle, positions the Diskette. A clamp that moves in conjunction with the Latch Handle fixes the Diskette to the Registration Hub. Refer to Figure IV.1.3.



**Figure IV.1.3:** *Diskette Drive Spindle*

#### IV.1.4 READ/WRITE HEAD ASSEMBLY

The Read/Write head is a ceramic head and is in direct contact with the Diskette. The head surface has been designed to obtain maximum signal transfer to and from the magnetic surface of the Diskette with minimum head/Diskette wear.

The SA800 ceramic head is a single element Read/Write head with *straddle erase* elements to provide erased areas between data tracks. Thus, normal tolerance between media and drives will not degrade the signal to noise ratio and insures Diskette interchangeability.

The Read/Write head is mounted on a Carriage which is located on the Head Position Actuator Lead Screw. The Diskette is held in a place perpendicular to the Read/Write head by one platen located on the Base Casting. The Diskette is loaded against the head with a Load Pad actuated by the Head Load Solenoid.

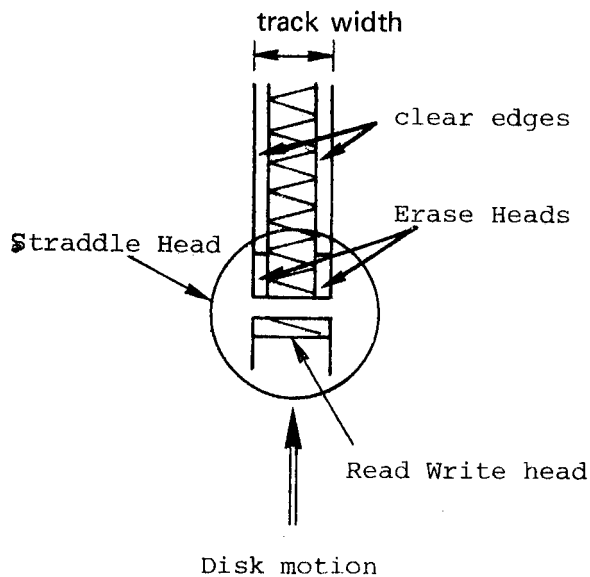


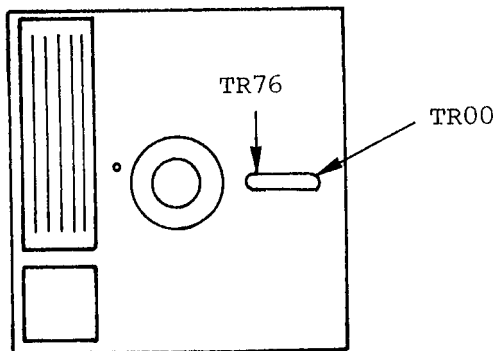
Figure IV.1.4: Straddle Head – Recording Principle



**IV.2 TRACK ACCESSING****IV.2.1 GENERAL**

The recording area is divided into 77 tracks, i.e., the Read/Write head can be moved onto 77 distinct positions.

Track no. 0 is the closest to the edge, while track no. 76 is closest to the center of the Diskette. Refer to Figure IV.2.1.



**Figure IV.2.1: Track Locations**

## IV.2.2 SEEK OPERATION – GENERAL

The carriage is driven forth or back by means of a rotating Lead Screw driven by a Stepper Motor.

The Stepper Motor used on the SA800 is a three-phase, fifteen degree, *variable reluctance* Stepper Motor. Figure IV.2.2 shows the logic diagram of the motor.

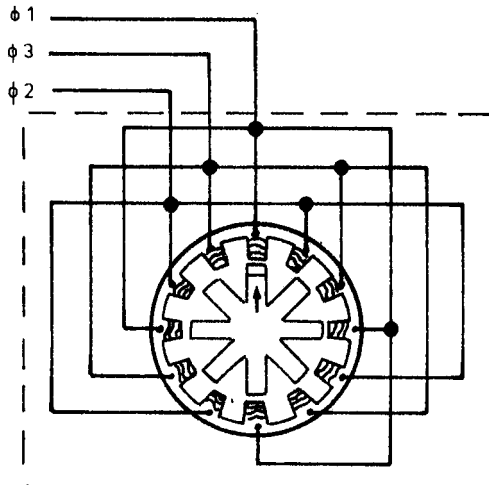


Figure IV.2.2: Stepper Motor

The Stepper Motor has 12 stator windings and a rotor with 8 teeth. The 12 stator windings are wired together in groups of four,  $90^\circ$  apart. Each group of four stator windings is wired to one phase of the Stepper Control Logic. The rotor has its 8 teeth spaced  $45^\circ$  apart.

Figure IV.2.3 shows the Stepper Motor (rear view) with phase 1 of the Stepper Control Logic Active. Phase 1 is applied to the four stator windings at  $0^\circ$ ,  $90^\circ$ ,  $180^\circ$  and  $270^\circ$ . This causes the four rotor teeth closest to those windings to move and line up with the stator windings.

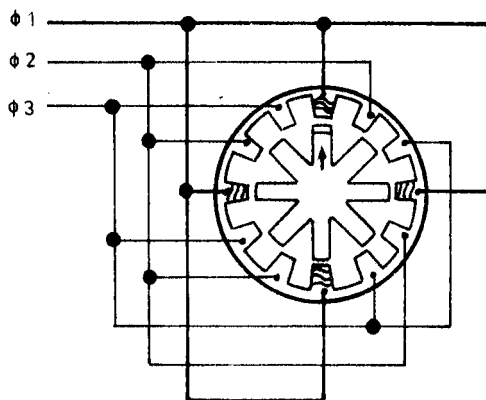


Figure IV.2.3: Position 1 (TRK 00)

Figure IV.2.4 shows the Stepper Motor with phase 2 of the Stepper Control Logic Active. Phase 2 is applied to the stator windings at  $30^\circ$ ,  $120^\circ$ ,  $210^\circ$  and  $300^\circ$ . This causes the four rotor teeth closest to those windings to move and line up with the stator windings. The result is a  $15^\circ$  turn of the Stepper Motor Lead Screw.

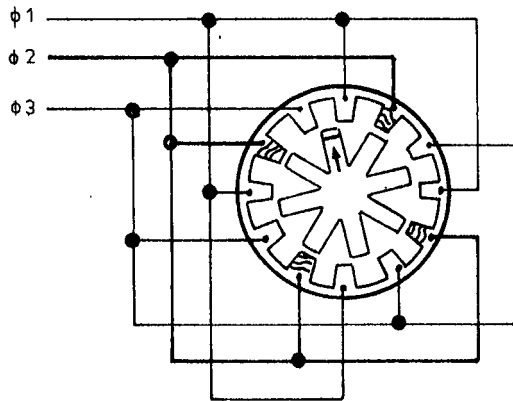


Figure IV.2.4: Position 2 (TRK 01)

Figure IV.2.5 shows the Stepper Motor with phase 3 of the Stepper Control Logic Active. Result is another  $15^\circ$  turn of the Stepper Motor Lead Screw.

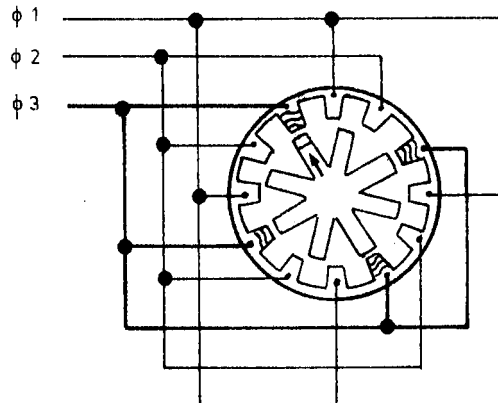


Figure IV.2.5: Position 3 (TRK 02)



### IV.3 STEPPER MOTOR CONTROL LOGIC

#### IV.3.1 GENERAL

The Stepper Motor Control Logic is functioned by the following lines from the Formatter:

- *Direction<sub>0</sub> (Interactive = Rev; Active = FWD)*
- *Step<sub>0</sub>*
- *Write Gate<sub>0</sub>*
- *Door Closed<sub>0</sub>*
- *Heads Loaded<sub>0</sub>*

The output is 01, 02, or 03, only one output active at the time (refer to Figure IV.2.1 and description of the Stepper Motor).

**IV.3.2**     *POWER ON RESET*

At power on, FF1 and FF2 are reset and O1 will be the active output. The Stepper Motor will be aligned up to position 1 as indicated in Figure IV.2.3.

**IV.3.3**     *SEEK OPERATIONS*

Seeking the Read/Write head from one track to another is accomplished by selecting the desired direction utilizing the Direction Select INTERFACE Line, loading the Read/Write head, and then pulsing the STEP line. Multiple track accessing is accomplished by repeating pulsing of the Step line until the desired track has been reached. Each pulse on the Step line will cause the Read/Write head to move one track either in or out depending on the DIRECTION SELECT line. Refer to Figure IV.3.1.

TO STEPPER MOTOR  
(See previous illustrations)

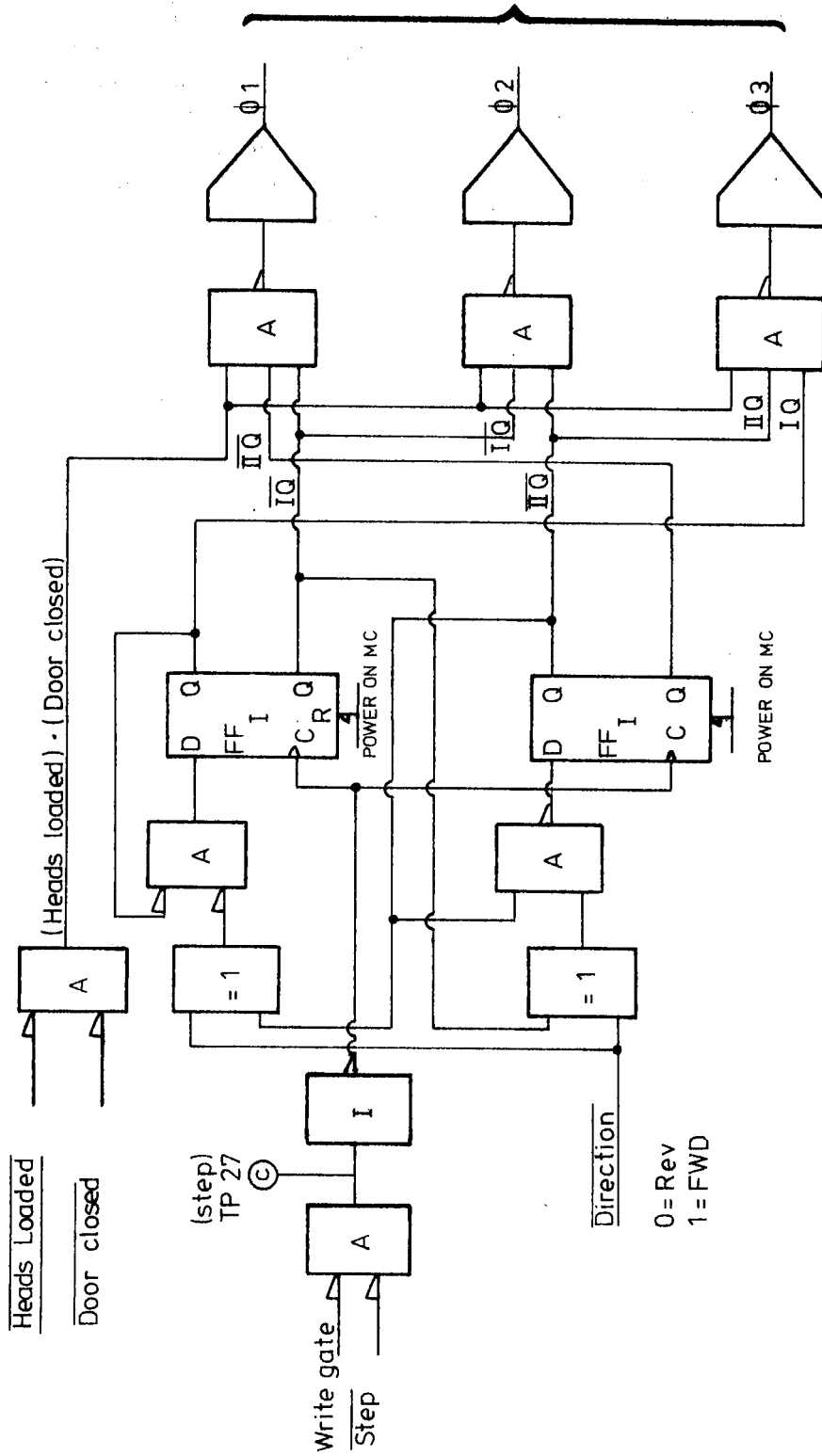


Figure IV.3.1: Stepper Control Logic



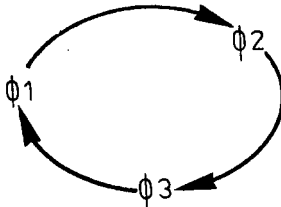
IV.3.3.1 *Forward Seek*

Let us assume this is the first **SEEK operation** after a Power On Reset. As outlined from Figure IV.3.1, 01 is then the active phase. We also see that

- *the Head must be loaded*
- *the Door closed*
- *the Write Gate not active*

in order to perform a SEEK operation. The DIRECTION line must be inactive (high) to direct a forward SEEK.

Let us assume a forward SEEK of five tracks from track zero. As depicted in Figure IV.3.2, the STEP<sub>0</sub> line will be pulsed 5 times at a repetition rate of 10<sup>0</sup>ms. The Stepper Motor will step forward 15<sup>0</sup> for each step pulse. During a Forward Seek, the phases will be activated in the following sequence:



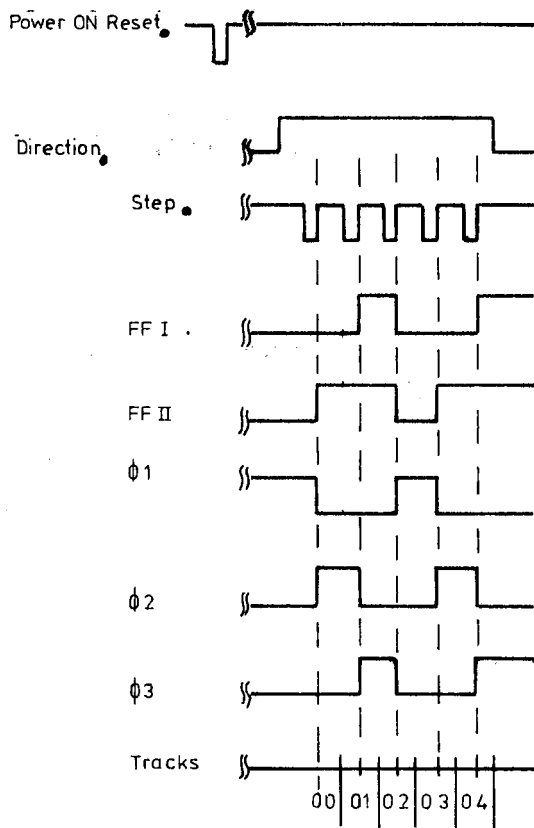
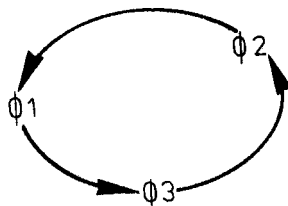


Figure IV.3.2: Stepper Control Logic – Timing Diagram

IV.3.3.2 Reverse Seek Operation

The DIRECTION line in active state (low) will define a reverse seek operation. As the STEP<sub>0</sub> line is pulsed, the phases will be activated in the sequence indicated below.

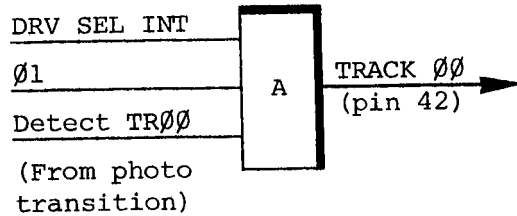


The Stepper Motor will now turn in 15° increments in the opposite direction, moving the Read/Write head to a lower recording track.

**IV.3.3.3** *Track Zero Indicator*

Pin 42 labelled Track 00 is activated to indicate to the Formatter that the Read/Write head is located on track zero.

Figures IV.3.3 and IV.3.4 will show the logic and timing diagram for track zero indication.



**Figure IV.3.3:** *Track 00 – Logic Illustration*

The track zero flag on the Carriage Assembly is adjusted so that the flag covers the photo transistor at track one. When the FF1 and FF2 are set off and the stepper moves to track zero, phase 1 is ANDed with DRV Sel Int and TRACK ZERO detect. TRACK ZERO indication is sent to the Formatter on pin 42, labelled TRACK 00.

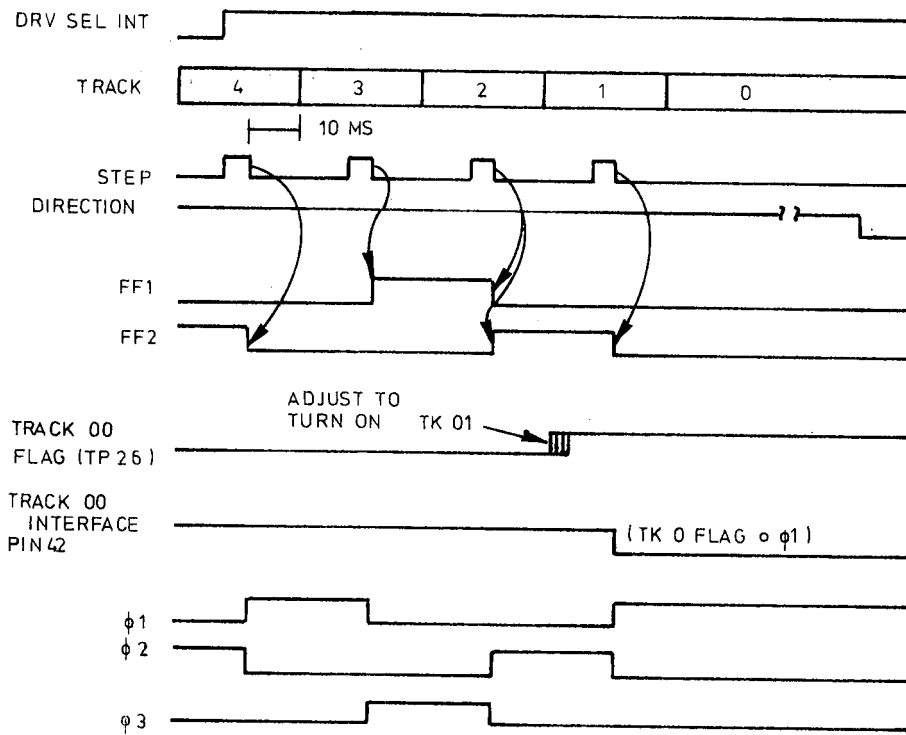


Figure IV.3.4: Track 00 – Timing Diagram

IV.4 READ/WRITE OPERATIONS

IV.4.1 RECORDING TECHNIQUE (SINGLE DENSITY)

The format of the data recorded on the diskette is totally under CPU control. Data is recorded on the diskette using frequency modulation as the recording mode, i.e., each data bit recorded on the diskette has an associated clock recorded with it, referred to as FM. Data written on and read back from the diskette takes the form as shown in Figure IV.4.1. The binary data pattern shown represents a  $101_2$ .

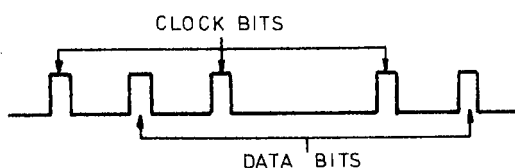


Figure IV.4.1: Data Pattern

IV.4.1.1 Bit Cell

As shown in Figure IV.4.2, the clock bits and the data bits (if present) are *interleaved*. By definition, a Bit Cell is the period between the leading edge of one clock bit and the leading edge of the next clock bit.

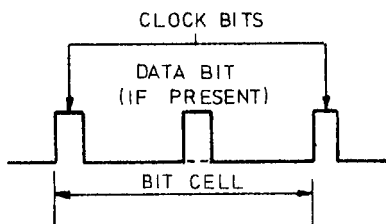


Figure IV.4.2: Bit Cell

IV.4.1.2 *Byte*

A Byte, when referring to serial data (being written onto or read from the disk drive), is defined as eight (8) consecutive bit cells. The most significant bit cell is defined as bit cell 0, and the least significant bit cell is defined as bit cell 7. When reference is made to a specific data bit (i.e., data bit 3), it is with respect to the corresponding bit cell (bit cell 3).

During a write operation, bit cell 0 of each byte is transferred to the disk drive first with bit cell 7 being transferred last. Correspondingly, the most significant byte of data is transferred to the disk first and the least significant byte is transferred last.

When data is being read back from the drive, bit cell 0 of each byte will be transferred first with bit cell 7 last. As with reading, the most significant byte will be transferred first from the drive to the Formatter.

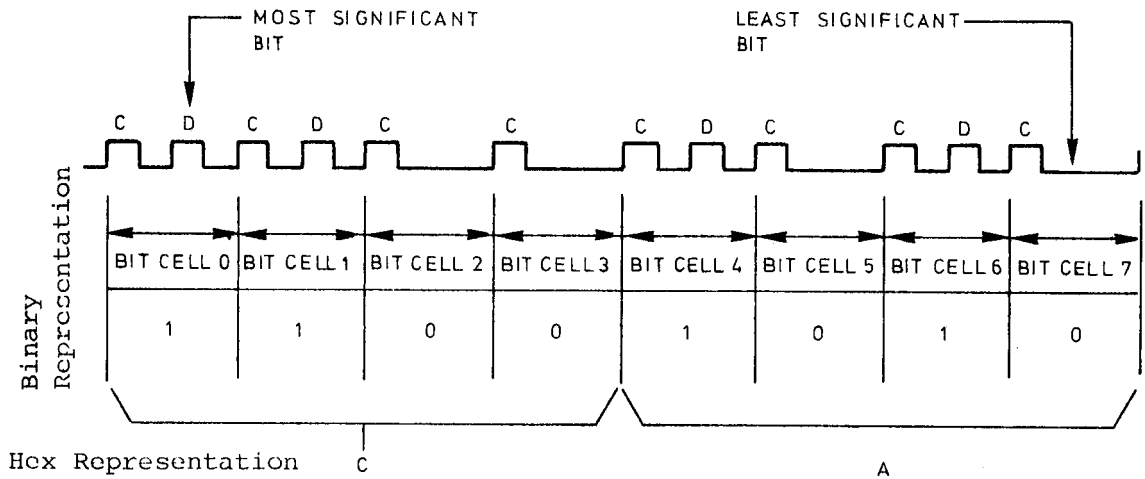


Figure IV.4.3: *Byte Format*

The SA800 drive uses the double-frequency (2F) horizontal non-return-to-zero (NRZ) method of recording. Double frequency is the term given to the recording system that inserts a clock bit at the beginning of each bit cell time, thereby doubling the frequency of recorded bits. This clock bit, as well as the data bit, are provided by the Formatter.

IV.4.1.3 *Writing a Bit*

The Read/Write head is a ring with a gap and a coil wound some point on the ring. When current flows through the coil, the flux induced in the ring fringes at the gap. As the diskette recording surface passes by the gap, the fringe flux magnetizes the surface in a horizontal direction. See Figure IV.4.4.

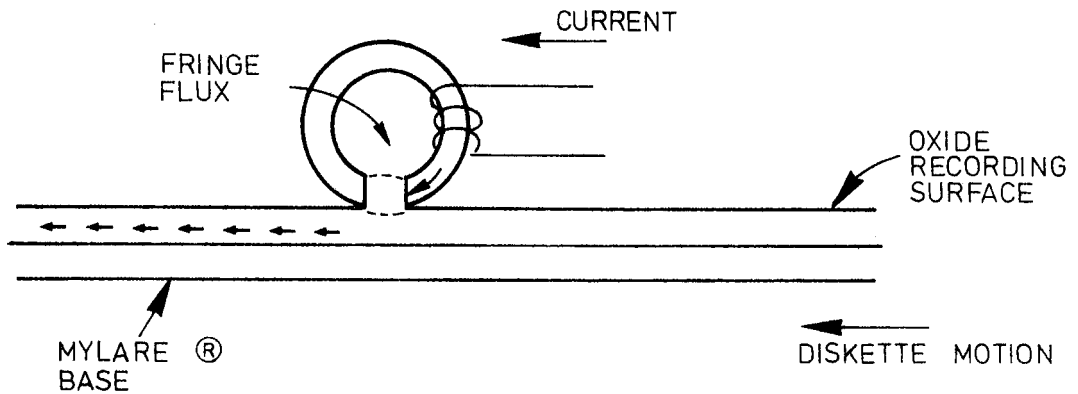


Figure IV.4.4: *Basic Read/Write Head*

During a WRITE operation, a bit is recorded when the flux direction in the ring is reversed by rapidly reversing the current in the coil. The fringe flux is reversed in the gap and hence the portion of the flux flowing through the oxide recording surface is reversed. If the flux reversal is instantaneous in comparison to the motion of the diskette, it can be seen that the portion of the diskette surface that just passed under the gap is magnetized in one direction, while the portion under the gap is magnetized in the opposite direction. *This flux reversal represents a bit.* See Figure IV.4.5.

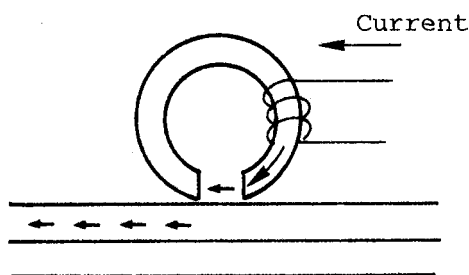


Figure IV.4.5a.

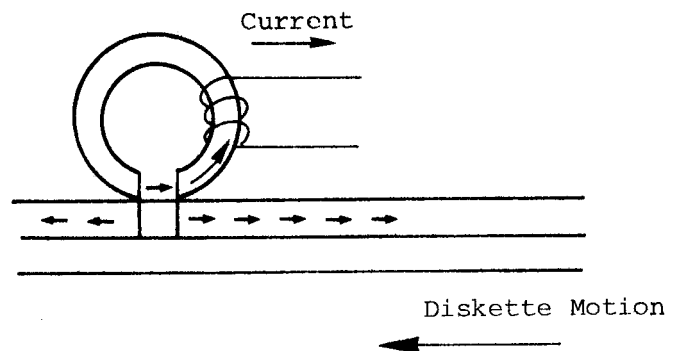


Figure IV.4.5b.

*A Recorded Bit – Illustration*

IV.4.1.4 *Reading a Bit*

During a READ operation, a bit is read when the flux direction in the ring is reversed as a result of a flux reversal on the disk surface. The gap first passes over an area that is magnetized in one direction, and a constant flux flows through the ring and coil. The coil registers no output voltage at this point. When a recorded bit passes under the gap, the flux flowing through the ring and coil will make a 180° reversal. This means that the flux reversal in the coil will cause a voltage output pulse. See Figure IV.4.6.

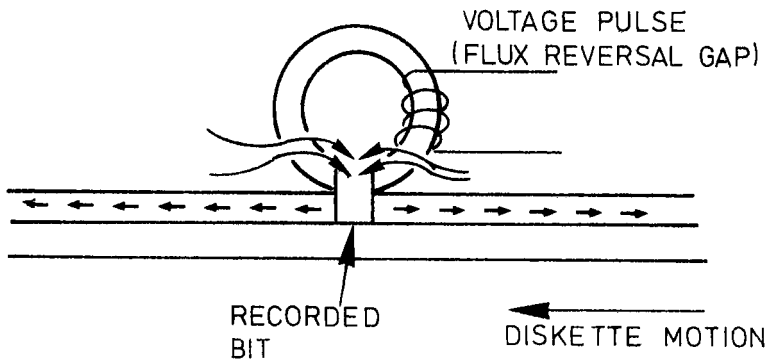


Figure IV.4.6: *Reading a Bit*

Figure IV.4.7 shows the recording flux and pulse relationship.

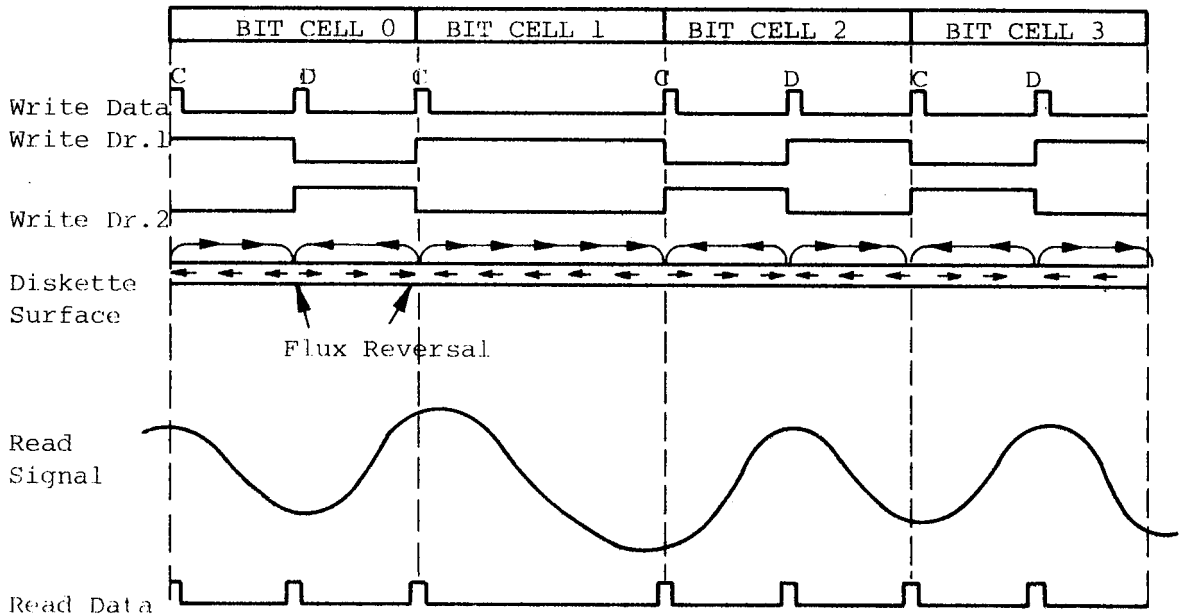


Figure IV.4.7: *Recording Flux to Pulse Relationship*



IV.4.2. READ/WRITE HEAD

The Read/Write head contains three coils. Two Read/Write coils are wound on a single core, center tapped and one erase coil is wound on a yoke that spans the track being written. The Read/Write and Erase coils are connected as shown in Figure IV.4.8.

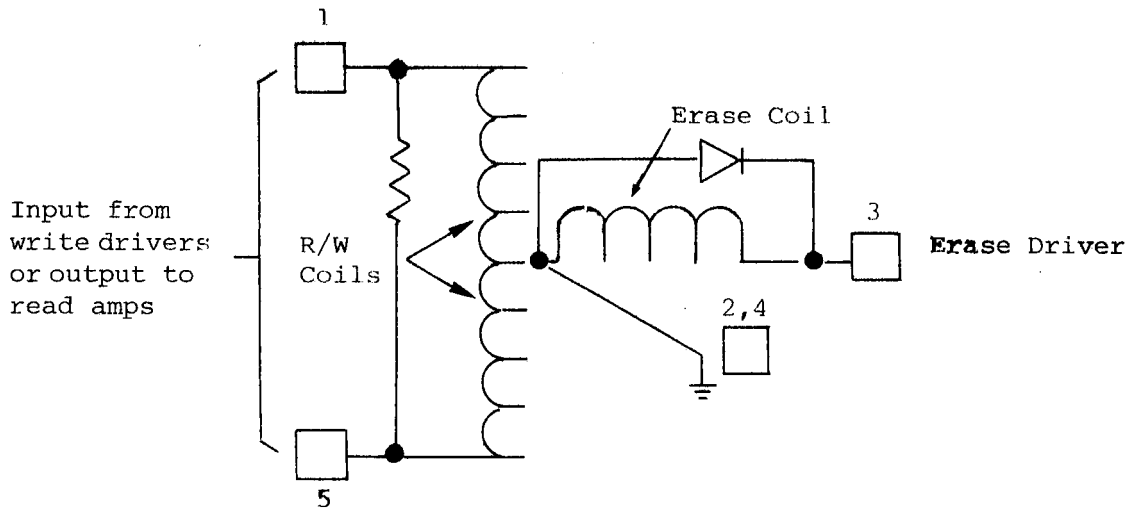


Figure IV.4.8: Read/Write Head

In a WRITE operation, the erase coil is energized. This causes the outer edges of the track to be trim erased so that the track being recorded will not exceed the .012" track width. The *straddle erasing* allows for minor deviations in Read/Write head current so as one track is recorded, it will not "splash over" to adjacent tracks. Refer to Figure IV.4.9.

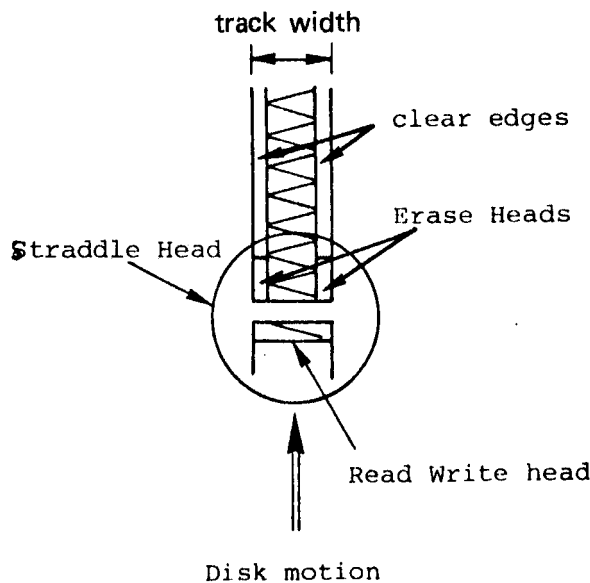


Figure IV.4.9: Straddle Head – Recording Principle

Each bit written will be directed to alternate Read/Write coils, thus, causing a change in the direction of current flow through the Read/Write head. This will cause a change in the flux pattern for each bit. The current through either of the Read/Write coils will cause the old data to be erased as new data is recorded.

In a READ operation, as the direction of flux changes on the diskette surface as it passes under the gap, current will be induced into one of the windings of the Read/Write head. This will result in a voltage output pulse. When the next data bit passes under the gap, another flux change in the recording surface takes place. This will cause the current to be induced in the other coil, causing another voltage output pulse.

IV.4.3 WRITE CIRCUIT OPERATION

WRITE data pulses (clocks and data) are supplied and encoded by the Formatter.

The Write Toggle FF will flip for each pulse. The set and clear output feeds the alternate Write Drivers. Refer to Figure IV.4.10.

The WRITE GATE from the Formatter is ANDed to provide write current.

The output of one of the Write Drivers allows the write current to flow through one half of the Read/Write coil. When the Write Trigger "flips", the other Write Driver provides write current to the other half of the Read/Write coil.

When write current is sensed flowing to the Write Drivers, a signal is generated to provide erase coil current.

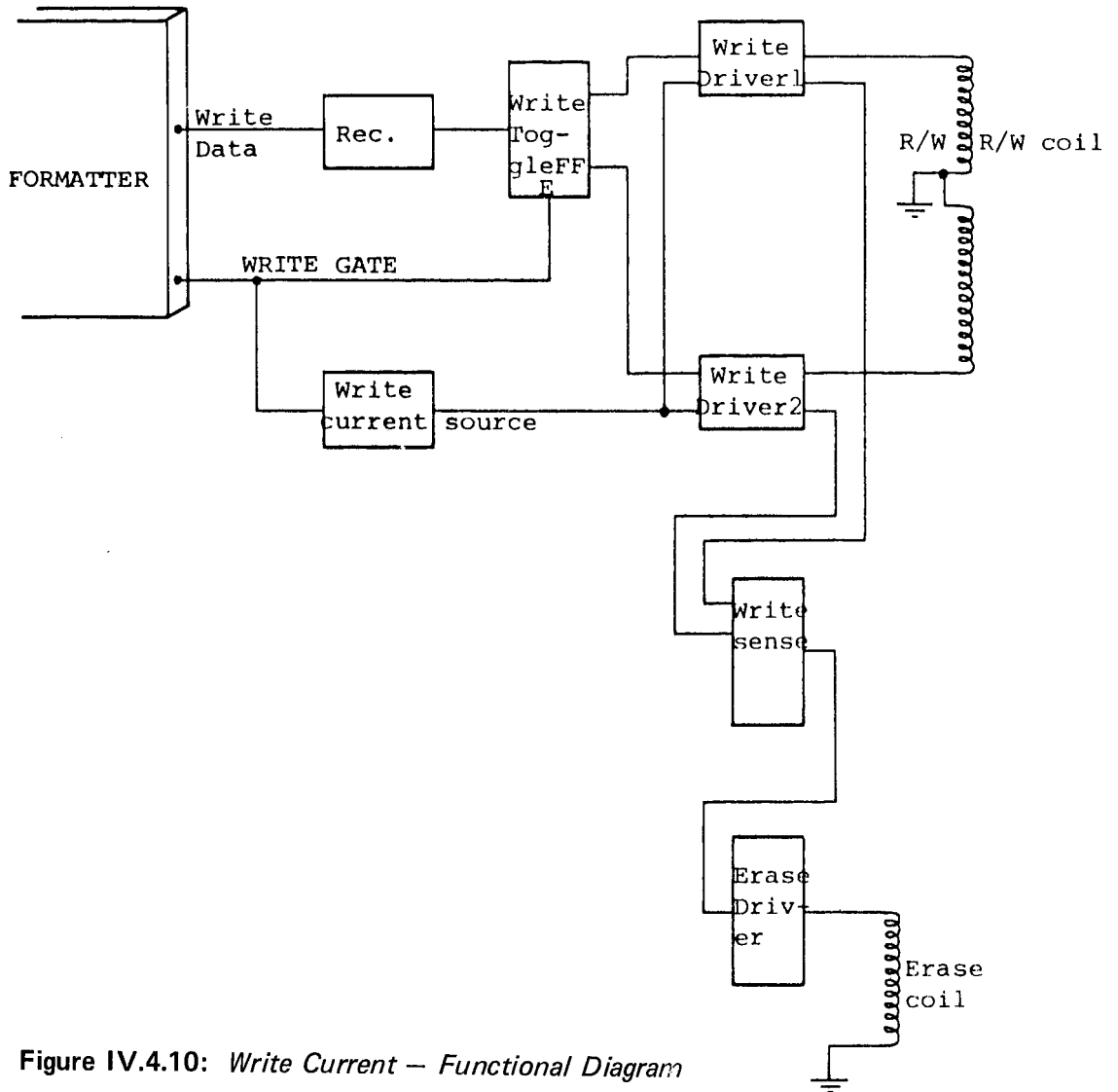


Figure IV.4.10: Write Current – Functional Diagram

#### IV.4.4 READ CIRCUIT OPERATION

When the Formatter requires data from the diskette drive, the Formatter must first load the head. With the head loaded and the write gate inactive, the signal read is fed to the amplifier section of the read circuit. After amplification, this signal is fed to a filter where the noise spikes are removed. The signal is then fed to the differential amplifier.

Since a pulse occurs at least once every  $4\mu\text{s}$ , and data bits are present once every  $2\mu\text{s}$ , the frequency of the read data varies. The read signal amplitude decreases as the frequency increases. Note the signals in Figure IV.4.11. The Differential Amplifier will amplify the read signals to even levels and make square waves out of the read signals (sine waves).

Read data pulses (data and clocks) are sent to the Formatter to be separated in a Data Separation Network (described in Section III.4).

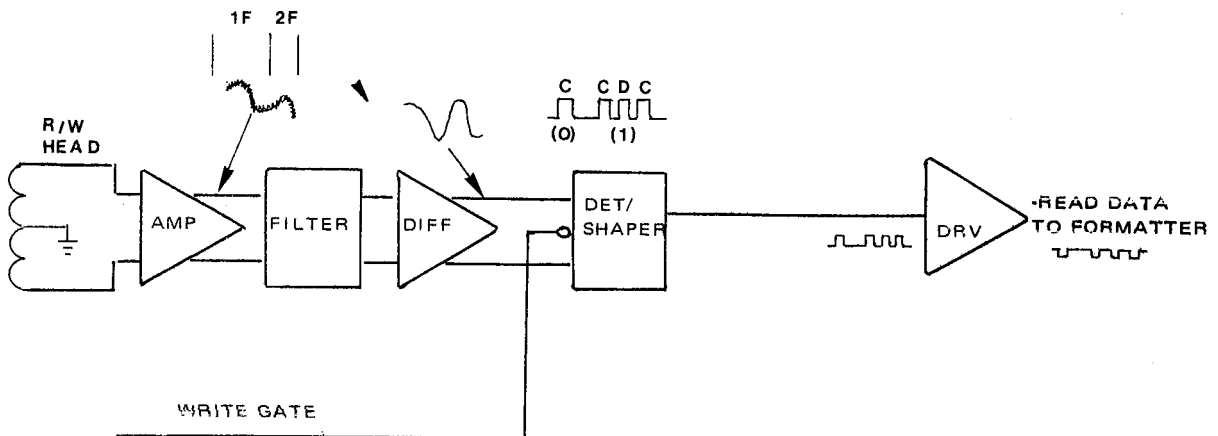


Figure IV.4.11: Read Circuit – Functional Diagram

## APPENDIXES



## DETAILED CONTENTS

+ + +

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**APPENDIX A**

**SPECIFICATION SUMMARY**

*Performance Specifications*

Capacity

Single Density

Unformatted  
Per Disk  
Per Track

3.2 megabits  
41.7 kilobits

Formatted

	FORMAT	SECTORS	CPU WORDS	CPU WORDS	CPU WORDS
		TRACK	(16 bits) SECTOR	(16 bits) TRACK	DISKETTE
				(in K words)	(in K words)
A	3740	26	64	1.664	125
B	SYS 32-I	15	128	1.920	140
C	SYS 32-II	8	256	2.048	150
AA	Double A	32	128	4.096	315

Transfer Rate  
Latency (average)

250 kilobits/sec.  
83 ms

Access Time  
Track to track  
Average  
Settling Time  
Head Load Time

10 ms  
260 ms  
8 ms  
35 ms

*Functional Specifications*

Single Density

Rotational Speed  
Recording Density  
(inside track)  
Flux Density  
Track Density  
Tracks  
Physical Sectors  
SA800  
SA801  
Index  
Encoding Method  
Media Requirements  
SA800  
SA801

360 rpm  
3200 bpi  
6400 fei  
48 tpi  
77  
0  
32/16/8  
1  
FM  
SA100/IBM Diskette  
SA101

*Physical Specifications*

Environment Limits	
Ambient Temperature	=10°C to 38°C
Relative Humidity	=20% to 80%
Maximum Wet Bulb	=25.5°C)
AC Power Requirements	
50/60 Hz $\pm$ 0.5Hz	
100/115 VAC Installations	=90 to 127V @ 4A typical
200/230 VAC Installations	=180 to 253V @ 2A typical
DC Voltage Requirements	
+24VDC $\pm$ 5% 1.3A typical	
+5VDC $\pm$ 5% 0.8A typical	
-5VDC $\pm$ 5% 0.5A typical (option -7 to -16 VDC)	
Mechanical Dimensions	
Width = 11.8 cm	
Height = 24.1 cm	
Depth = 36.2 cm	
Weight = 5.9 kg.	
Heat Dissipation = 72 watt typical	

*Reliability Specifications*

MTBF:	5000 POH* under heavy usage 8000 POH* under typical usage
PM:	Every 5000 POH* under heavy usage Every 15000 POH* under typical usage
MTTR:	30 minutes
Component Life:	15,000 POH*
Error Rates:	
Soft Read Errors:	1 per $10^9$ bits read
Hard Read Errors:	1 per $10^{12}$ bits read
Seek Errors:	1 per $10^6$ seeks
Media Life:	
Passes per Track	$3.5 \times 10^6$
Insertions	30,000+

\* POH = Power on Hours

\* FLOPPY DISK DEBUGGING LOOPS

\* THIS IS A SET OF ROUTINES INTENDED FOR SCOPE DERUCCING OF  
 \* THE FLOPPY DISK SYSTEM .  
 \* EACH ROUTINE IS TERMINATED BY EXIT AD1.  
 \* THIS MAKES IT POSSIBLE FOR THE USER TO BUILD HIS OWN SMALL  
 \* PROGRAMS BY LINKING THESE ROUTINES TOGETHER THE FOLLOWING WAY:

```
* 135001      * JPL I *1
* <ADDR. OF ROUTINE>
* 135001
* <ADDR. OF ROUTINE>
* .
* .
* .
```

DEVNO=1560  
RDAT=DEVNO+0  
WDAT=DEVNO+1  
RSR1=DEVNO+2  
WCWD=DEVNO+3  
RSR2=DEVNO+4  
WDAD=DEVNO+5  
RTST=DEVNO+6  
WSCT=DEVNO+7  
  
INTEN=00  
HUSY=20  
READY=30  
  
EINT=00  
TEST=30  
DVCL=40  
CLBUF=50  
  
FORM=100  
WRDAT=110  
WRDEL=120  
RDID=130  
READ=140  
SEEK=150  
RECAL=160  
RESET=170

100/

% THE FOLLOWING CELLS ARE GLOBAL VARIABLES USED  
% THROUGHOUT THE PROGRAM, AND MUST BE UPDATED MANUALLY

00100	000000	DADR, 0	% DRIVE ADDR. & FORMAT
			%BIT 0-2: DRIVE NO
			% BIT 6-7: FORMAT
00101	000000	TRACK, 0	% BIT 0-7: TRACK NO. (OCTAL)
00102	000000	SECT, 0	% BIT 0-7: SECTOR NO.
00103	000000	DATA, 0	% DATA PATTERN TO BE USED
00104	000000	DIFF, 0	% DIFFERENCE TO BE USED BY SUBSEQUENT SEEK COMMAND
			%BIT 0-6: DIFFERENCE BETWEEN CURRENT & DESIRED TRACK
			% BIT 7= 1: ACCESS "IN" TO A HIGHER TRACK NO.
			% BIT 7 =0: ACCESS "OUT" TO A LOWER TRACK NO.
00105	000000	THYT, 0	% BIT 0-7: BYTE TO BE USED BY TEST INSTRUCTION
00106	000000	WDCNT, 0	% WORDCOUNT FOR READ/WRITE INTERFACE BUFFER (FROM CPU)

%SELECT DRIVE & FORMAT

00107	044	00100	044371	SELDR, LDA	DADR
00110			156410	SHA	ZIN 10
00111	170		172401	AAA	1
00112			165565	IOX	WDAD
00113	000	00113	000000	STZ	*
00114	000	00114	000000	STZ	*
00115			146542	EXIT	AUI

)PCL SELDR

% DRIVE ADDR. & FORMAT  
 % MOVE TO UPPER BYTE  
 % EXECUTE  
 % DELAY

% LOAD DIFFERENCE

00116	044	00104	044366	LDIFF, LDA	DIFF
00117			156410	SHA	ZIN 10
00120			165565	IOX	WDAD
00121			146542	EXIT	AUI

)PCL LDIFF

% DIFF. BETWEEN CURRENT & DESIRED TRACK  
 % MOVE TO UPPER BYTE  
 % EXECUTE

% LOAD SECTOR

00122	044	00102	044360	LSECT, LDA	SECT
00123			156410	SHA	ZIN 10
00124			165567	IOX	WSCCT
00125			146542	EXIT	AUI

)PCL LSECT

% SECTOR  
 % MOVE TO UPPER BYTE  
 % EXECUTE

% CONTROL RESET

00126	170		170400	CNTRS, SAA	0
00127			174375	BSET	ONE RESET DA
00130			165563	IOX	WCWD
00131	170		171773	SAX	-3
00132	130	00132	132400	JNC	*
00133			146542	EXIT	AUI

)PCL CNTRS

% "RESET" BIT IN CONTR. WORD  
 % EXECUTE  
 % DELAY

\* RECALIBRATE

00134	170	170400	RCALB, SAA	0	ONE RECAL DA	% RECALIBRATE
00135		174365	BSET	WCWD		
00136		165563	IOX	RSR1		% READ STATUS
00137		165562	IOX	ONE READY DA		% BUSY?
00140		175235	BSKP	*-2		% YES. WAIT UNTIL FINISHED
00141	124	124375	JMP	AUI		
00142		146542	EXIT			

\* SHAKE HEAD ARM BETWEEN TRACK 0 AND TRACK NO. IN CELL "TRACK"

00143	170	170400	SHAKE, SAA	0	ONE RECAL DA	% RECALIBRATE
00144		174365	BSET	WCWD		
00145		165563	IOX	RSR1		
00146		165562	IOX	ONE READY DA		
00147		175235	BSKP	*-2		
00150	124	124376	JMP	TRACK		% TRACK NO.
00151	044	044330	LDA	ZIN 10		% MOVE TO UPPER BYTE
00152		156410	SHA	ONE 170 DA		% SEEK "OUT"
00153		174375	BSET	WDAD		
00154		165565	IOX	0		
00155	170	170400	SAA	ONE SEEK DA		% START SEEK OPERATION
00156		174355	BSET	WCWD		
00157		165563	IOX	RSR1		% BUSY?
00160		165562	IOX	ONE READY DA		% YES. WAIT UNTIL FINISHED
00161		175235	BSKP	*-2		% TRACK NO.
00162	124	124376	JMP	TRACK		
00163	044	044316	LDA	ZIN 10		
00164		156410	SHA	WDAD		
00165		165565	IOX	0		
00166	170	170400	SAA	ONE SEEK DA		% START SEEK "IN"
00167		174355	BSET	WCWD		
00170		165563	IOX	RSR1		% BUSY?
00171		165562	IOX	ONE READY DA		% YES. WAIT UNTIL FINISHED
00172		175235	BSKP	*-2		% TRACK NO.
00173	124	124376	JMP	AUI		
00174		146542	EXIT	SHAKE		

)PCL

% READ DISK SECTOR

00175	170	170400	RDISK, SAA	0					
00176		174345	BSET	ONE	READ	DA			% SET READ BIT
00177		174255	BSET	ONE	CLBUF	DA			% BUFFER CLEAR BIT
00200		165563	IOX	WCWD					% START READ
00201		165562	IOX	RSR1					
00202		175235	BSKP	ONE	READY	DA			% BUSY?
00203	124	124376	JMP	*-2					% YES. WAIT UNTIL FINISHED
00204		146542	EXIT	AUI					

)PCL RDISK

% WRITE DISK SECTOR

00205	170	170400	WDISK, SAA	0					
00206		174315	BSET	ONE	WRDAT	DA			% SET WRITE BIT
00207		174255	BSET	ONE	CLBUF	DA			% BUFFER CLEAR BIT
00210		165563	IOX	WCWD					% START WRITE
00211		165562	IOX	RSR1					
00212		175235	BSKP	ONE	READY	DA			
00213	124	124376	JMP	*-2					
00214		146542	EXIT	AUI					

)PCL WDISK

% READ ID (IDENTIFIER)

00215	170	170400	RIDT, SAA	0					
00216		174335	BSET	ONE	KDID	DA			% READ ID BIT
00217		174255	BSET	ONE	CLBUF	DA			
00220		165563	IOX	WCWD					
00221		165562	IOX	RSR1					
00222		175235	BSKP	ONE	READY	DA			
00223	124	124376	JMP	*-2					
00224		146542	EXIT	AUI					

)PCL RIDT



```

% WRITE DELETED DATA SECTOR
00225 170          170400  WDEL R, SAA      0
00226          174325  BSET ONE WRDEL DA
00227          174255  BSET ONE CLBUF DA
00230          165563  IOX WCWD
00231          165562  IOX RSRI
00232          175235  BSKP ONE READY DA
00233 124          124376  JMP *-2
00234          146542  EXIT AU1
)PCL WDEL R

```

ND-11.012.01

```

% SEEK TO SPECIFIED TRACK (GIVEN IN CELL "TRACK")
00235 044 I 00250 045013 HSEEK, LDA I (TRACK
00236          156410  SHA ZIN 10
00237          174375  BSET ONE 170 DA
00240          165565  IOX WUAD
00241 170          170400  SAA 0
00242          174355  BSET ONE SEEK DA
00243          165563  IOX WCWD
00244          165562  IOX RSRI
00245          175235  BSKP ONE READY DA
00246 124          124376  JMP *-2
00247          146542  EXIT AU1
00250          000101  )FILL
)PCL HSEEK
% TRACK
% START SEEK "OUT"

```

% READ DATA BUFFER (FROM CPU)

```

00251 170      170400  SAA      0
00252      174255  BSET    ONE CLBUF DA
00253      165563  IOX     WCWD
00254 054      00265 054011  LDX     (BUFR
00255 050      00266 051011  LUT I  (WDCNT
00256      146076  RADU   SX DT
00257      165580  IOX     WDAT
00260 004 X    000     006000  STA     *X
00261 170      173401  AAX     I
00262      140067  SKP    DA EQL ST
00263 124      00257 124374  JMP     *-4
00264      146542  EXIT   AUI
00265      002500  )FILL
00266      000106  )PCL  RDBUF

```

```

% CLEAR BUFFER
% START ADDR. OF READ BUFFER IN MEMORY
% WORDCOUNT
% HEAD DATA WORD
% STRE IN MEMORY BUFFER
% INCR. BUFFER ADDR.
% FINISHED?
% NO. ONCE MORE

```

% WRITE DATA BUFFER (FROM CPU)

```

00267 170      170400  WRBUF, SAA 0
00270      174255  BSET    ONE CLBUF DA
00271      165563  IOX     WCWD
00272 054      00304 054012  LDX     (BUFV
00273 050      00305 051012  LDT I  (WDCNT
00274      146076  RADU   SX DT
00275 044      00303 045006  LDA I  DATAI
00276      165561  IOX     WDAT
00277 170      173401  AAX     I
00300      140067  SKP    DX EQL ST
00301 124      00275 124374  JMP     *-4
00302      146542  EXIT   AUI
00303      000103  DATAI,DATA
00304      000500  )FILL
00305      000106  )PCL  WRBUF

```

```

% CLEAR INTERFACE BUFFER
% START ADDRESS OF WRITE BUFFER IN MEMORY
% WRITE DATA
% INCK. MEMORY BUFFER ADDR.

```



% READ TEST IN TESTMODE

00325	170	170420	TST,	SAA	20	% CLEAR DEVICE
00326		165563	IOX	IOX	WCWD	
00327	170	170410	SAA	SAA	10	% SET IN TEST MODE
00330		165563	IOX	IOX	WCWD	% TEST BYTE
00331	044	045017	I	LDA I	(TBYT	
00332		156410		SMA	ZIN 10	
00333		165567	IOX	IOX	WDCNT	% DEPOSIT TEST BYTE
00334	170	171400	SAX	SAX	0	% NO. OF BYTES TO BE TRANSFERED
00335	050	051014	I	LDT I	(WDCNT	% SIMULATION OF ONE READ TRANSFER (ONE BYTE)
00336		165566	IOX	IOX	RTST	
00337		000000	U			
00340	170	173401	AAX	AAX	1	
00341		140067	SKP	SKP	DA EQL ST	
00342	124	124374	JMP	JMP	*-4	
00343	170	170400	SAA	SAA	0	
00344		165563	IOX	IOX	WCWD	% RESET TEST MODE
00345	170	170420	SAA	SAA	20	% CLEAR DEVICE
00346		165563	IOX	IOX	WCWD	
00347		146542	EXIT	EXIT	AUI	
00350		000105	)FILL			
00351		000106	)PCL TST			

\* FORMATTING FOR IBM SYS-32-II FORMAT. PATCHES FOR OTHER FORMATS

00352	000	00425	000053	FORMA, STZ	CHCNT	* CLEAR CHECK COUNTER
00353	000	00426	000053	STZ	FLAG	* CLEAR FLAG FOR 1. ST SECTOR
00354	000	00416	001042	STZ I	(SECT	* CLEAR SECTOR NO.
00355	040	00417	041042	MIN I	(SECT	* INCREMENT SECTOR
00356	170		170400	SAA	0	
00357			174255	BSET	ONE CLBUF DA	* CLEAR INTERFACE BUFFER
00360			165563	IOX	WCWD	
00361	044	00420	045037	LDA I	(TRACK	
00362			156410	SHA	ZIN 10	
00363			165561	IOX	WDAT	* WRITE ID BYTE 1 & 2 IN INTERFACE BUFFER
00364	044	00421	045035	LDA I	(SECT	
00365			156410	SHA	ZIN 10	
00366	060	00423	060035	ADD	IUS	
00367			165561	IOX	WDAT	* WRITE ID BYTE 3 & 4 IN INTERFACE BUFFER
00370	044	00426	044036	LDA	FLAG	
00371	130	00403	131412	JAF	CUNT	* IF FLAG SET, DO NOT ACTIVATE FORMATTING
00372	170		170400	SAA	0	
00373			174255	BSET	ONE CLBUF DA	
00374			174305	BSET	ONE FORM DA	
00375			165563	IOX	WCWD	* CLEAR INTERFACE BUFFER & START FORMATTING
00376	170		170777	SAA	-1	* SET FLAG
00377	004	00426	004027	STA	FLAG	
00400	170		170400	SAA	0	
00401			174255	BSET	ONE CLBUF DA	
00402			165563	IOX	WCWD	
00403			165562	IOX	RSRI	* SHOULD BE 175315 FOR 3740,175325 FOR
00404			175335	BSKP	ONE 130 DA	* 3600 FORMATN
00405	124	00403	124376	JMP	*-2	* INCR. CHECK COUNTER
00406	040	00425	040017	MIN	CHCNT	

00407	044	I	00422	045013	LDA I (SECT		
00410	064		00424	064014	SUB MSECT		
00411	130		00355	131744	JAF LFORM		* JUMP BACK IF NOT ALL SECTORS FORMATTED
00412				165562	IOX RSM1		
00413				175235	BSKP ONE READY DA		
00414	124		00412	124376	JMP *-2		* WAIT UNTIL NOT BUSY
00415				146542	EXIT AD1		
00416				000102	)FILL		
00417				000102			
00420				000101			
00421				000102			
00422				000102			
00423				000002	IDS, 2		* SHOULD BE 0 FOR 3740 , 1 FOR 3600 FORMAT
00424				000010	MSECT, 10		* SHOULD BE 32 FOR 3740 , 17 FOR 3600 FORMAT
00425				000000	CHCNT, 0		
00426				000000	FLAG, 0		
					)PCL LFORM		

\* CHECK INT. & IDENT  
\* IF OK. THIS LOOP STOPS ON LEVEL 11 WITH ID. CODE IN A (11)

00427	170			INT,	SAA	0		% CLEAR PID
00430					TRK	PID		
00431	044				LDA	(LEVI3		% INITIALIZE PC ON LEVEL 11
00432		00446			IHW	130 RP		
00433	044				LDA	(4000		% ENABLE LEVEL 11
00434		00447			TRK	PIE		
00435					ION			
00436	170				SAA	2		% INTERRUPT SHOULD OCCUR NOW.
00437					IOX	WCWD		
00440					0			
00441					IUF			% WRONG. NO INTERRUPT
00442					WAIT			

\* THE FOLLOWING INSTRUCTIONS RUNS ON LEVEL 11

00443				LEVI3, IDENT PL11				% HEAD IDENT
00444				IUF				% STOP ON LEVEL 11
00445				WAIT				
00446				)FILL				
00447				)PCL INT				

```

% ,//0 6/2 $%15% . , /!$ 3%15% . #%
LL00P, SAA      20      %CLEAR DEVICE
      IUX      W0WD      % DELAY COUNTER
      LDX      COUNT
      COPY     SA DX CM2
      SAA      4
      IUX      W0WD      % START AUTOLOAD
      0
      0
      JNC     *-2      % DELAY
      EXIT   ADI
COUNT, 0
)PCL LL00P
00450 170      170420
00451      165563
00452 054      00462 054010
00453      146777
00454 170      170404
00455      165563
00456      000000
00457      000000
00460 130      00456 132776
00461      146542
00462      000000

```



BUFV=500  
BUFR=BUFV+2000

DADR:000100  
TRACK:000101  
SECT:000102  
DATA:000103  
DIFF:000104  
TRVT:000105  
WDCNT:000106

SELDL:000107  
LDIFF:000116  
LSECT:000122  
CNTRS:000126  
RCALB:000134  
SHAKE:000143  
RDISK:000175  
WDISK:000205  
RIDT:000215  
WDELK:000225  
HSEK:000235  
RDBUF:000251  
WRBUF:000267  
WRADR:000306  
TST:000325  
FORMA:000352  
INT:000427  
LLOOP:000450  
RUFV:000500  
BUFR:000500



**APPENDIX C/I**

***INTERFACE HARDWARE DIAGRAMS***







## APPENDIX C/II

## INTERNAL INTERFACE SIGNAL LIST

<i>Signal</i>	<i>Polarity</i>	<i>Origin</i>	<i>Description</i>
ACLR	H	1111	Clear buffer address during autoloading
ACOUNT	L	1111	Increment buffer address
ADRCL	L	1111	Clear buffer address
AUTO	H	1111	Autoloading sequence running
AX (0-9)	H	1118	Interface buffer address, bits
BAXX (0-15)	L	CPU	Main I/O bus address
BBUSY	L	1111	Device busy (status)
BDIN	L	1111	Enable data or status to BD
BDOUT	L	1111	Enable BD to interface
BDXX (0-15)	L	---	Main I/O bus data
BRQ		1111	19.2 KHZ osc.
BUSXX (0-15)	L	1118	Internal 3 state bus (16 bits)
CE1	L	1111	Enable least significant half of buffer
CE2	L	1111	Enable most significant half of buffer
CL	L	1111	DVCL + MCL
CLSTP	L	1111	Clear autoloading steps
CON	L	1111	Connect to CPU on main I/O bus
DBUSY	L	Floppy	Busy line from floppy disk
DEVNO	L	1111	Selects device number
DIN	L	1111	Enable data from floppy to interface
DINT	L	Floppy	Interrupt from floppy disk
DLCON	H	1111	Programmed device output active
DLYINP	H	1111	Delayed version of input
DOXX (0-15)	L	1118	Data out points on interface buffer
DUT	L	1111	Enable data byte to floppy disk
DVCL	L	1111	Programmed device clear
EN	L	1118	Enable commands on bus during autoloading
ENLO	L	1118	Enable DO 0-7 on bus 8-15
ENUL	L	1118	Enable bus 8-15 on bus 0-7
ENUP	L	1118	Enable DO 8-15 on bus 8-15
FDIN	L	1118	Enable data or status from floppy disk
FDOUT	L	1118	Enable data or commands to floppy disk
GSENS	L	1111	Gate sense strobe
GSTAT	L	1111	Gate status strobe
IDCOD1	L	1111	ID, code 21
IDCOND2	L	1111	ID, code 22
IDENT	H	1111	Ident PL11 active (if interrupt)
INCOM	H	1111	Programmed device input (IOX) active
INP	L	1111	Input to CPU on main I/O bus
INPUT	H	1111	Programmed input active (IOX + IDENT)
INT11	L	1111	Interrupt to CPU
INTEN	L	1111	Interrupt enabled (status)
INTRPT	H	1111	Interrupt to be sent to CPU

<i>Signal</i>	<i>Polarity</i>	<i>Origin</i>	<i>Description</i>
LDOM	L	1111	Load command strobe
LDADR	L	1111	Load drive address, strobe
LDCLK	L	1111	Trailing edge steps the autoload sequence
LDFIN	H	1111	Autoload sequence finished
LDIFF	L	1111	Load difference strobe
LSECT	L	1111	Load sector strobe
MATCH	L	1111	Match for device IOX
MOL	L	CPU	Master clear (push button)
NORDY	L	1111	Drive select caused interrupt
PULS	H	1111	PULS used to generate strobes to floppy
RDAT	L	1111	IOX RDAT active
RDDLY	H	1111	Delay to look for interrupt in step 0
READY	L	1111	Device ready for transfer (status)
RESET	L	1111	Reset to floppy disk
RSR1	L	1111	IOX RSR1 active
RSR2	L	1111,1118	IOX RSR2 active
RSTAT	L	1118	Enable status bits 4-7 on BD
RTST	L	1111	IOX RTST active
SSTAT	L	1111	Strobe status bits 4-7
STEP0	H	1111	First step of autoload sequence (load addr.)
STEP1	H	1111	Second step of autoload sequence (recalibrate)
STEP2	H	1111	Third step of autoload sequence (load sector)
STEP3	H	1111	Fourth step of autoload sequence (read data)
STEP4	H	1111	Fifth step of autoload sequence
STLD	L	1111	Trailing edge starts autoload sequence
STR01	L	1118	Step 0 + step 1
TBUSX (0, 7)	L	1118	Bi-directional transfer bus to floppy
TDIR	L	Floppy	Direction of floppy disk data transfer
TEST	L	1111	Test mode active
TGRANT		1111	Data grant to floppy disk
TIMOUT	L	1111	Timeout (status)
TREQ	L	Floppy	Floppy disk request for data
WCWD	L	1111	IOX WCWD active
WDAD	L	1111	IOX WDAD active
WDAT	L	1111	IOX WDAT active
WRAM	L	1111	Write pulse to interface buffer
WSCT	L	1111,1118	IOX WSCT active



## APPENDIX C/III

*1111/1118 SIGNAL COMMUNICATION*

Signal communication between 1111 and 1118 card through 1:1 berg connection in the backwiring.

All signals are in 0 polarity.

<i>Terminal</i>	<i>Signal Name</i>
56	BDOUT
57	BDIN
58	
59	PULS
60	WRAM
61	CE1
62	CE2
63	LDADR
64	RESET
65	STEP0
66	STEP1
67	STEP2
68	STEP3
69	TEST
70	ACOUNT
71	MATCH
72	DIN
73	DUT
74	ADRCL
75	SSTAT



## APPENDIX C/IV

## FLOPPY DISK CABLES

*N-10 INTERNAL CABLE	*DEVICE	*FLOPPY
*	*CABLE	*DISK
*	*1:1	*INTERNAL
*	*	*CABLE

## 1111 CARD

<i>Term</i>	<i>Signal</i>	<i>Burdny</i>	<i>Burdny</i>	<i>Amp</i>
95	TDIR	Y	Y	D
94	GND	AA	AA	4
93	TREQ	Z	Z	F
92	GND	BB	BB	6
91	DINT	CC	CC	L
90	GND	EE	EE	10
89	DBUSY	DD	DD	M
88	GND	FF	FF	11
87	TGRANT	HH	HH	H
86	GND	KK	KK	7
85	GSENS	JJ	JJ	J
84	GND	LL	LL	8
83	GSTAT	MM	MM	K
82	GND	PP	PP	9
81	LCOM	NN	NN	N
80	GND	RR	RR	12
79	LSECT	SS	SS	E
78	GND	UU	UU	5
77	LDIFF	TT	TT	C
76	GND	VV	VV	3

## 1118 CARD

<i>Term</i>	<i>Signal</i>	<i>Burdny</i>	<i>Burdny</i>	<i>Amp</i>
95	TBUS7	A	A	W
94	GND	C	C	19
93	TBUS6	B	B	X
92	GND	D	D	20
91	TBUS5	E	E	U
90	GND	H	H	17
89	TBUS4	F	F	V
88	GND	J	J	18
87	TBUS3	K	K	S
86	GND	M	M	15
85	TBUS2	L	L	T

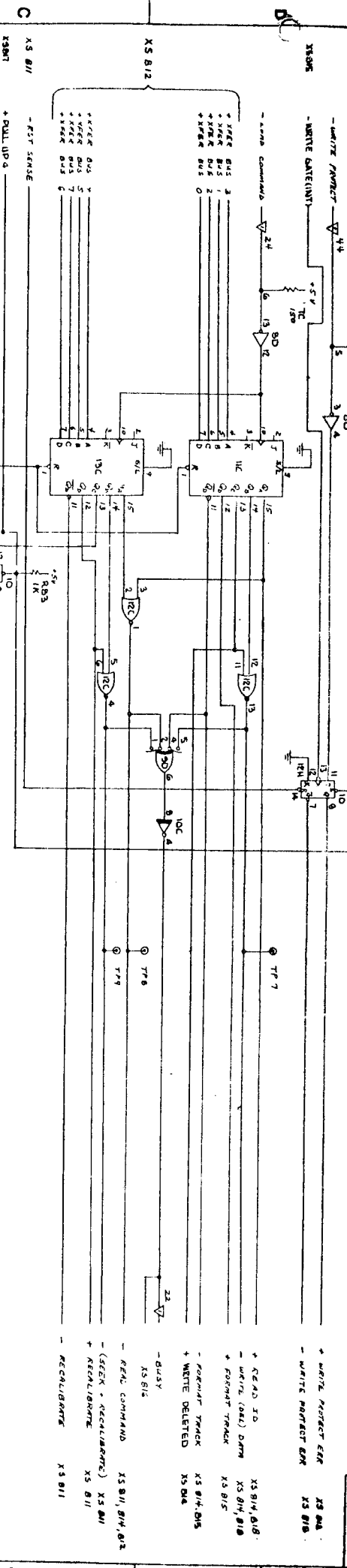
C-IV-2

<i>Term</i>	<i>Signal</i>	<i>Burdny</i>	<i>Burdny</i>	<i>Amp</i>
84	GND	N	N	16
83	TBUS1	P	P	P
82	GND	S	S	13
81	TBUS0	R	R	R
80	GND	T	T	14
79	RESET	U	U	Y
78	GND	W	W	21
77	LDADR	V	V	B
76	GND	X	X	2

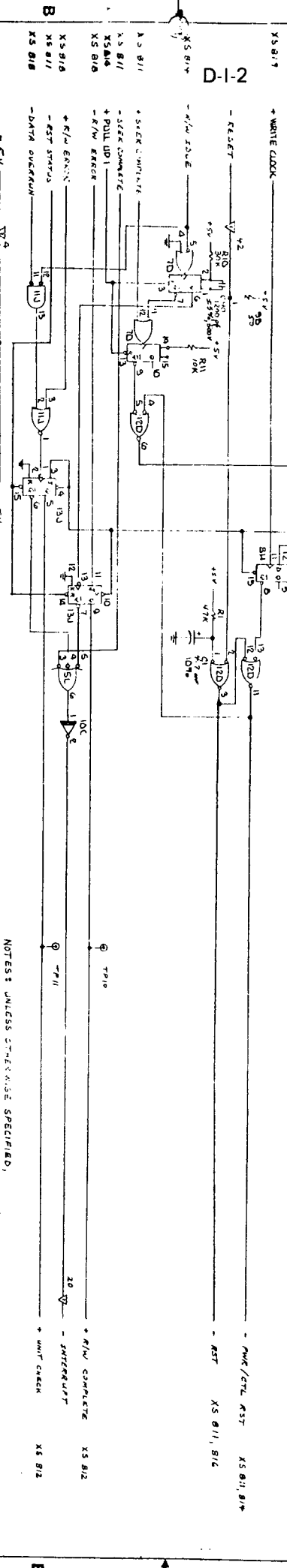
**APPENDIX D/I**

***FORMATTER LOGIC DIAGRAMS***

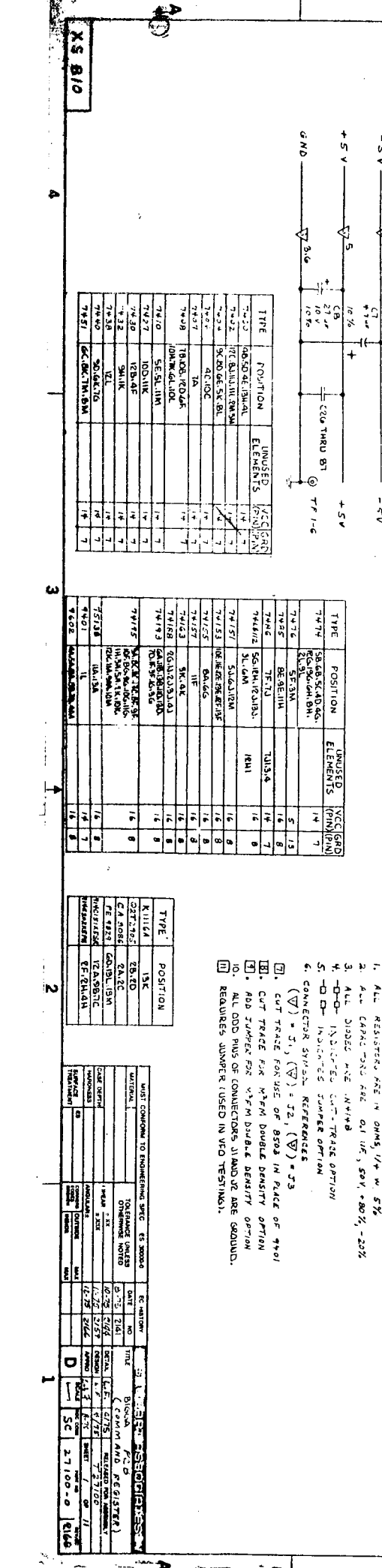
27100-0



+ WRITE PROTECT ERR X5 B11, B12  
 + WRITE PROTECT ENR X5 B11, B12  
 + READ ID X5 B11, B12  
 - WRITE (DEL) DATA X5 B11, B12  
 + FORMAT TRACK X5 B11, B12  
 + WRITE DELETED X5 B11, B12  
 - BUSY X5 B12  
 - RECALIBRATE X5 B11, B12  
 - (SEEK + RECALIBRATE) X5 B11  
 + RECALIBRATE X5 B11



+ R/W COMPLETE X5 B12  
 + INTERLUPT X5 B12  
 + DATA OVERFLOW X5 B12  
 - R/W CHECK X5 B12



+ R/W CHECK X5 B12  
 + DATA OVERFLOW X5 B12  
 + R/W COMPLETE X5 B12  
 + INTERLUPT X5 B12  
 + DATA OVERFLOW X5 B12

TYPE	POSITION	UNUSED ELEMENTS	NC (GRID PIN)
7400	AND	1	1
7401	NOT	1	1
7402	OR	1	1
7403	NAND	1	1
7404	INVERTER	1	1
7405	OR-AND	1	1
7406	AND-OR	1	1
7407	OR-AND-NOT	1	1
7408	AND-OR-NOT	1	1
7409	OR-AND-NOT-NOT	1	1
7410	AND-OR-NOT-NOT	1	1
7411	AND-OR-NOT-NOT-NOT	1	1
7412	OR-AND-NOT-NOT-NOT	1	1
7413	OR-AND-NOT-NOT-NOT-NOT	1	1
7414	AND-OR-NOT-NOT-NOT-NOT	1	1
7415	AND-OR-NOT-NOT-NOT-NOT-NOT	1	1
7416	OR-AND-NOT-NOT-NOT-NOT-NOT	1	1
7417	OR-AND-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7418	AND-OR-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7419	AND-OR-NOT-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7420	OR-AND-NOT-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7421	OR-AND-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7422	OR-AND-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7423	OR-AND-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7424	OR-AND-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7425	OR-AND-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7426	OR-AND-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7427	OR-AND-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7428	OR-AND-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7429	OR-AND-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7430	OR-AND-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7431	OR-AND-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7432	OR-AND-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7433	OR-AND-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7434	OR-AND-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7435	OR-AND-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7436	OR-AND-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7437	OR-AND-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7438	OR-AND-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7439	OR-AND-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7440	OR-AND-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT	1	1

TYPE	POSITION	UNUSED ELEMENTS	NC (GRID PIN)
7441	AND	1	1
7442	NOT	1	1
7443	OR	1	1
7444	NAND	1	1
7445	INVERTER	1	1
7446	OR-AND	1	1
7447	AND-OR	1	1
7448	OR-AND-NOT	1	1
7449	AND-OR-NOT	1	1
7450	OR-AND-NOT-NOT	1	1
7451	AND-OR-NOT-NOT	1	1
7452	OR-AND-NOT-NOT-NOT	1	1
7453	AND-OR-NOT-NOT-NOT	1	1
7454	OR-AND-NOT-NOT-NOT-NOT	1	1
7455	AND-OR-NOT-NOT-NOT-NOT	1	1
7456	OR-AND-NOT-NOT-NOT-NOT-NOT	1	1
7457	AND-OR-NOT-NOT-NOT-NOT-NOT	1	1
7458	OR-AND-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7459	AND-OR-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7460	OR-AND-NOT-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7461	AND-OR-NOT-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7462	OR-AND-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7463	AND-OR-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7464	OR-AND-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7465	AND-OR-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7466	OR-AND-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7467	AND-OR-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7468	OR-AND-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7469	AND-OR-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7470	OR-AND-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7471	AND-OR-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7472	OR-AND-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7473	AND-OR-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7474	OR-AND-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7475	AND-OR-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7476	OR-AND-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7477	AND-OR-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7478	OR-AND-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7479	AND-OR-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT	1	1
7480	OR-AND-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT	1	1

TYPE	POSITION
7481	AND
7482	NOT
7483	OR
7484	NAND
7485	INVERTER
7486	OR-AND
7487	AND-OR
7488	OR-AND-NOT
7489	AND-OR-NOT
7490	OR-AND-NOT-NOT
7491	AND-OR-NOT-NOT
7492	OR-AND-NOT-NOT-NOT
7493	AND-OR-NOT-NOT-NOT
7494	OR-AND-NOT-NOT-NOT-NOT
7495	AND-OR-NOT-NOT-NOT-NOT
7496	OR-AND-NOT-NOT-NOT-NOT-NOT
7497	AND-OR-NOT-NOT-NOT-NOT-NOT
7498	OR-AND-NOT-NOT-NOT-NOT-NOT-NOT
7499	AND-OR-NOT-NOT-NOT-NOT-NOT-NOT
7500	OR-AND-NOT-NOT-NOT-NOT-NOT-NOT-NOT
7501	AND-OR-NOT-NOT-NOT-NOT-NOT-NOT-NOT
7502	OR-AND-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT
7503	AND-OR-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT
7504	OR-AND-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT
7505	AND-OR-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT
7506	OR-AND-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT
7507	AND-OR-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT
7508	OR-AND-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT
7509	AND-OR-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT
7510	OR-AND-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT-NOT

DATE	BY	REVISION	DESCRIPTION
10/25/77	WJG	1	INITIAL DESIGN
11/15/77	WJG	2	REVISED FOR MANUFACTURING
12/15/77	WJG	3	REVISED FOR MANUFACTURING
01/15/78	WJG	4	REVISED FOR MANUFACTURING
02/15/78	WJG	5	REVISED FOR MANUFACTURING
03/15/78	WJG	6	REVISED FOR MANUFACTURING
04/15/78	WJG	7	REVISED FOR MANUFACTURING
05/15/78	WJG	8	REVISED FOR MANUFACTURING
06/15/78	WJG	9	REVISED FOR MANUFACTURING
07/15/78	WJG	10	REVISED FOR MANUFACTURING
08/15/78	WJG	11	REVISED FOR MANUFACTURING
09/15/78	WJG	12	REVISED FOR MANUFACTURING
10/15/78	WJG	13	REVISED FOR MANUFACTURING
11/15/78	WJG	14	REVISED FOR MANUFACTURING
12/15/78	WJG	15	REVISED FOR MANUFACTURING
01/15/79	WJG	16	REVISED FOR MANUFACTURING
02/15/79	WJG	17	REVISED FOR MANUFACTURING
03/15/79	WJG	18	REVISED FOR MANUFACTURING
04/15/79	WJG	19	REVISED FOR MANUFACTURING
05/15/79	WJG	20	REVISED FOR MANUFACTURING

27100-0  
 27100-0  
 27100-0





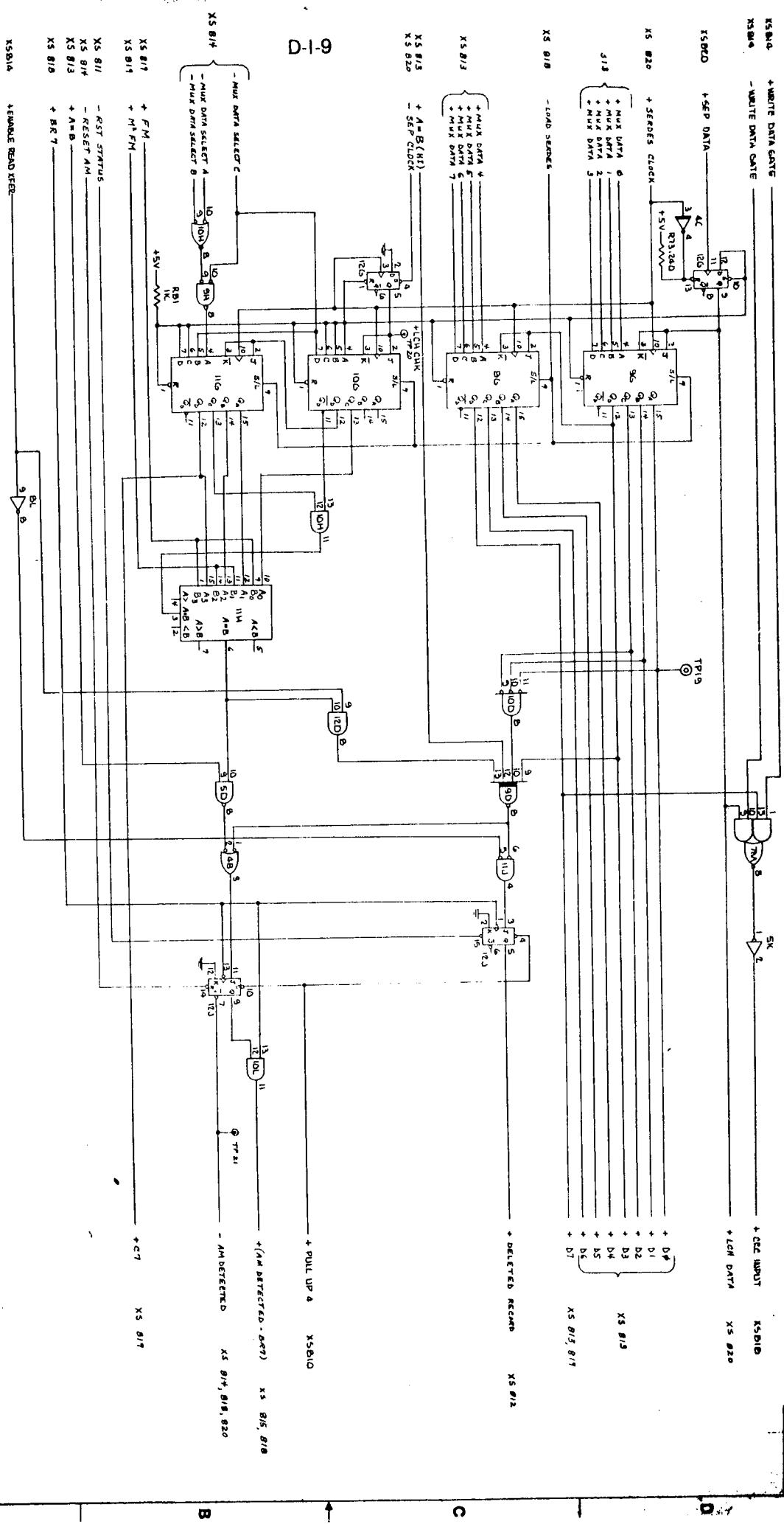












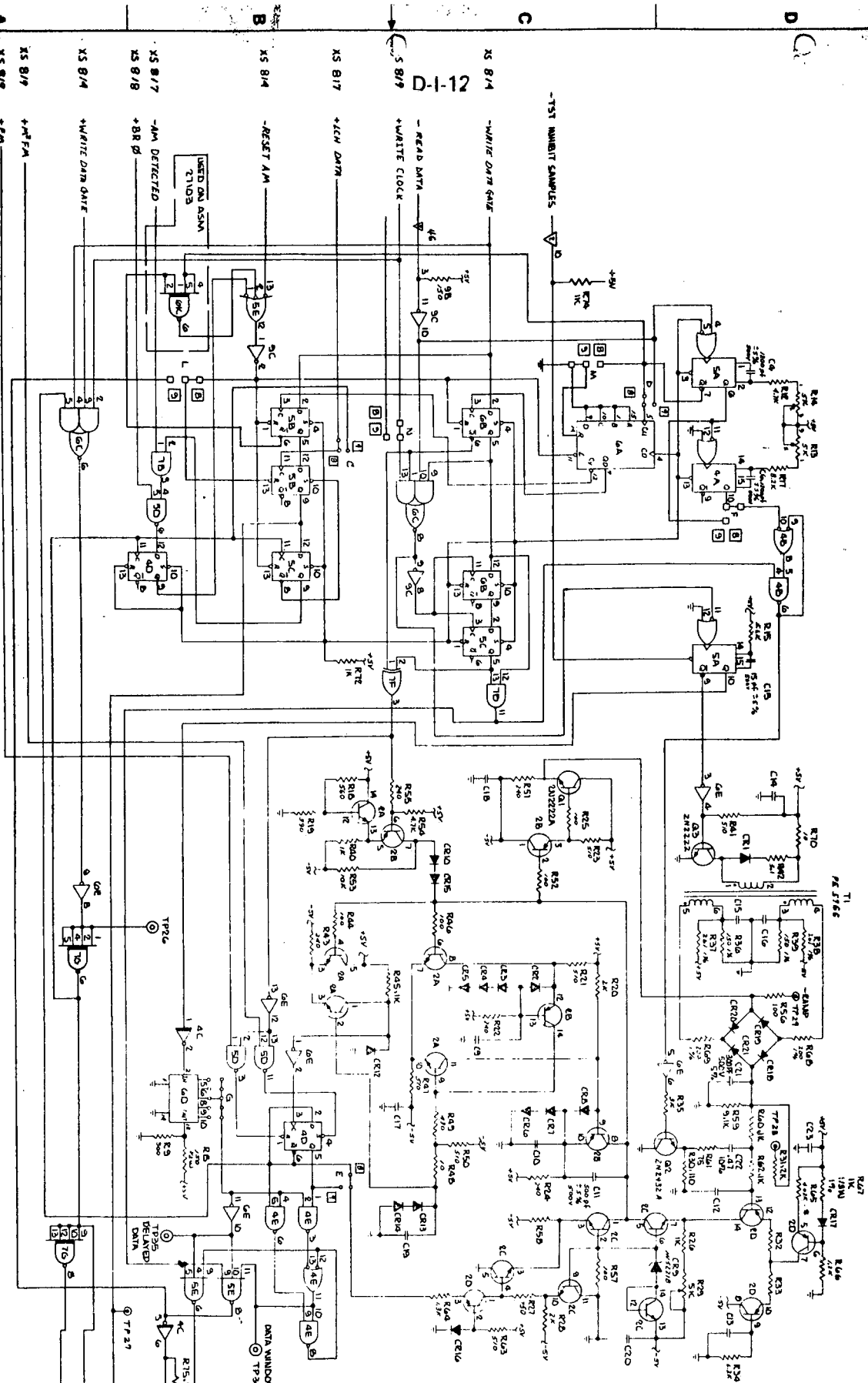
SHIBURA ELECTRONICS	
DATE	NO.
TITLE	(SUSAKA / AM SELECTOR)
DESIGN	27100-0
DRW	27100-0
CHECK	27100-0
APPROVE	27100-0
SCALE	SC
REV	27100-0
DATE	NO.
TITLE	(SUSAKA / AM SELECTOR)
DESIGN	27100-0
DRW	27100-0
CHECK	27100-0
APPROVE	27100-0
SCALE	SC
REV	27100-0

XS 817

XS 817







Callout	Value	Part	Quantity
R27	271K	RES	1
C12	0.05µF	COND	1
R32	200	RES	1
R33	100	RES	1
R34	5.1K	RES	1
R35	20K	RES	1
R36	5.1K	RES	1
R37	10K	RES	1
R38	10K	RES	1
R39	10K	RES	1
R40	10K	RES	1
R41	10K	RES	1
R42	10K	RES	1
R43	10K	RES	1
R44	10K	RES	1
R45	10K	RES	1
R46	10K	RES	1
R47	10K	RES	1
R48	10K	RES	1
R49	10K	RES	1
R50	10K	RES	1
R51	10K	RES	1
R52	10K	RES	1
R53	10K	RES	1
R54	10K	RES	1
R55	10K	RES	1
R56	10K	RES	1
R57	10K	RES	1
R58	10K	RES	1
R59	10K	RES	1
R60	10K	RES	1
R61	10K	RES	1
R62	10K	RES	1
R63	10K	RES	1
R64	10K	RES	1
R65	10K	RES	1
R66	10K	RES	1
R67	10K	RES	1
R68	10K	RES	1
R69	10K	RES	1
R70	10K	RES	1
R71	10K	RES	1
R72	10K	RES	1
R73	10K	RES	1
R74	10K	RES	1
R75	10K	RES	1
R76	10K	RES	1
R77	10K	RES	1
R78	10K	RES	1
R79	10K	RES	1
R80	10K	RES	1
R81	10K	RES	1
R82	10K	RES	1
R83	10K	RES	1
R84	10K	RES	1
R85	10K	RES	1
R86	10K	RES	1
R87	10K	RES	1
R88	10K	RES	1
R89	10K	RES	1
R90	10K	RES	1
R91	10K	RES	1
R92	10K	RES	1
R93	10K	RES	1
R94	10K	RES	1
R95	10K	RES	1
R96	10K	RES	1
R97	10K	RES	1
R98	10K	RES	1
R99	10K	RES	1
R100	10K	RES	1

PARTS LIST		REV. HISTORY		DATE		BY	
Q1	74180	1	1	11/15/70	1	1	1
Q2	74181	1	1	11/15/70	1	1	1
Q3	74182	1	1	11/15/70	1	1	1
Q4	74183	1	1	11/15/70	1	1	1
Q5	74184	1	1	11/15/70	1	1	1
Q6	74185	1	1	11/15/70	1	1	1
Q7	74186	1	1	11/15/70	1	1	1
Q8	74187	1	1	11/15/70	1	1	1
Q9	74188	1	1	11/15/70	1	1	1
Q10	74189	1	1	11/15/70	1	1	1
Q11	74190	1	1	11/15/70	1	1	1
Q12	74191	1	1	11/15/70	1	1	1
Q13	74192	1	1	11/15/70	1	1	1
Q14	74193	1	1	11/15/70	1	1	1
Q15	74194	1	1	11/15/70	1	1	1
Q16	74195	1	1	11/15/70	1	1	1
Q17	74196	1	1	11/15/70	1	1	1
Q18	74197	1	1	11/15/70	1	1	1
Q19	74198	1	1	11/15/70	1	1	1
Q20	74199	1	1	11/15/70	1	1	1
Q21	74200	1	1	11/15/70	1	1	1
Q22	74201	1	1	11/15/70	1	1	1
Q23	74202	1	1	11/15/70	1	1	1
Q24	74203	1	1	11/15/70	1	1	1
Q25	74204	1	1	11/15/70	1	1	1
Q26	74205	1	1	11/15/70	1	1	1
Q27	74206	1	1	11/15/70	1	1	1
Q28	74207	1	1	11/15/70	1	1	1
Q29	74208	1	1	11/15/70	1	1	1
Q30	74209	1	1	11/15/70	1	1	1
Q31	74210	1	1	11/15/70	1	1	1
Q32	74211	1	1	11/15/70	1	1	1
Q33	74212	1	1	11/15/70	1	1	1
Q34	74213	1	1	11/15/70	1	1	1
Q35	74214	1	1	11/15/70	1	1	1
Q36	74215	1	1	11/15/70	1	1	1
Q37	74216	1	1	11/15/70	1	1	1
Q38	74217	1	1	11/15/70	1	1	1
Q39	74218	1	1	11/15/70	1	1	1
Q40	74219	1	1	11/15/70	1	1	1
Q41	74220	1	1	11/15/70	1	1	1
Q42	74221	1	1	11/15/70	1	1	1
Q43	74222	1	1	11/15/70	1	1	1
Q44	74223	1	1	11/15/70	1	1	1
Q45	74224	1	1	11/15/70	1	1	1
Q46	74225	1	1	11/15/70	1	1	1
Q47	74226	1	1	11/15/70	1	1	1
Q48	74227	1	1	11/15/70	1	1	1
Q49	74228	1	1	11/15/70	1	1	1
Q50	74229	1	1	11/15/70	1	1	1
Q51	74230	1	1	11/15/70	1	1	1
Q52	74231	1	1	11/15/70	1	1	1
Q53	74232	1	1	11/15/70	1	1	1
Q54	74233	1	1	11/15/70	1	1	1
Q55	74234	1	1	11/15/70	1	1	1
Q56	74235	1	1	11/15/70	1	1	1
Q57	74236	1	1	11/15/70	1	1	1
Q58	74237	1	1	11/15/70	1	1	1
Q59	74238	1	1	11/15/70	1	1	1
Q60	74239	1	1	11/15/70	1	1	1
Q61	74240	1	1	11/15/70	1	1	1
Q62	74241	1	1	11/15/70	1	1	1
Q63	74242	1	1	11/15/70	1	1	1
Q64	74243	1	1	11/15/70	1	1	1
Q65	74244	1	1	11/15/70	1	1	1
Q66	74245	1	1	11/15/70	1	1	1
Q67	74246	1	1	11/15/70	1	1	1
Q68	74247	1	1	11/15/70	1	1	1
Q69	74248	1	1	11/15/70	1	1	1
Q70	74249	1	1	11/15/70	1	1	1
Q71	74250	1	1	11/15/70	1	1	1
Q72	74251	1	1	11/15/70	1	1	1
Q73	74252	1	1	11/15/70	1	1	1
Q74	74253	1	1	11/15/70	1	1	1
Q75	74254	1	1	11/15/70	1	1	1
Q76	74255	1	1	11/15/70	1	1	1
Q77	74256	1	1	11/15/70	1	1	1
Q78	74257	1	1	11/15/70	1	1	1
Q79	74258	1	1	11/15/70	1	1	1
Q80	74259	1	1	11/15/70	1	1	1
Q81	74260	1	1	11/15/70	1	1	1
Q82	74261	1	1	11/15/70	1	1	1
Q83	74262	1	1	11/15/70	1	1	1
Q84	74263	1	1	11/15/70	1	1	1
Q85	74264	1	1	11/15/70	1	1	1
Q86	74265	1	1	11/15/70	1	1	1
Q87	74266	1	1	11/15/70	1	1	1
Q88	74267	1	1	11/15/70	1	1	1
Q89	74268	1	1	11/15/70	1	1	1
Q90	74269	1	1	11/15/70	1	1	1
Q91	74270	1	1	11/15/70	1	1	1
Q92	74271	1	1	11/15/70	1	1	1
Q93	74272	1	1	11/15/70	1	1	1
Q94	74273	1	1	11/15/70	1	1	1
Q95	74274	1	1	11/15/70	1	1	1
Q96	74275	1	1	11/15/70	1	1	1
Q97	74276	1	1	11/15/70	1	1	1
Q98	74277	1	1	11/15/70	1	1	1
Q99	74278	1	1	11/15/70	1	1	1
Q100	74279	1	1	11/15/70	1	1	1
Q101	74280	1	1	11/15/70	1	1	1
Q102	74281	1	1	11/15/70	1	1	1
Q103	74282	1	1	11/15/70	1	1	1
Q104	74283	1	1	11/15/70	1	1	1
Q105	74284	1	1	11/15/70	1	1	1
Q106	74285	1	1	11/15/70	1	1	1
Q107	74286	1	1	11/15/70	1	1	1
Q108	74287	1	1	11/15/70	1	1	1
Q109	74288	1	1	11/15/70	1	1	1
Q110	74289	1	1	11/15/70	1	1	1
Q111	74290	1	1	11/15/70	1	1	1
Q112	74291	1	1	11/15/70	1	1	1
Q113	74292	1	1	11/15/70	1	1	1
Q114	74293	1	1	11/15/70	1	1	1
Q115	74294	1	1	11/15/70	1	1	1
Q116	74295	1	1	11/15/70	1	1	1
Q117	74296	1	1	11/15/70	1	1	1
Q118	74297	1	1	11/15/70	1	1	1
Q119	74298	1	1	11/15/70	1	1	1
Q120	74299	1	1	11/15/70	1	1	1
Q121	74300	1	1	11/15/70	1	1	



**APPENDIX D/II**

*FORMATTER COMPONENT – LOCATION CHART (next page)*

A	B	C	D	E	F	G	H	J	K	L	M	
					74193	74193	74195	74188	7432	9401	74195	1
CA3086	Q2T2905	CA3086	Q2T2905		Δ	74188	Δ	74188	74195		7402	2
					74193	74193	74195	74188	74163	74LS112	7476	3
9602	7400	7406		7400	7430		Δ	74188	74163	7400	9602	4
9602			7400	7410	7476	74LS112	74195	74151	7404	7410	7402	5
74193		7451	PE9829	7404	7408	74155		74151	7440	7408	74LS112	6
7407	7408	☆	9602 74193		7486	7440		7486	7408		7451	7
74155	9602	74195	7404	7485	74195	74195		7402	7451	7404	7451	8
74195	☆	7404	7440	7485	74195	74195	7432				74195	9
9602	7408	7406	7427	74153	74195	74195	7408		74195	7408	74195	10
75138	74193	74195	74193	74153	74157	74195	7485	7402	7427	7402	7410	11
☆	7430	7402	7408	74153	74153		74LS112	74LS112	74195	7438	74151	12
75138	74193	74195	74193	74153	74153		7400	74LS112	K1116A	PE9829	PE9829	13

Formatter Component-Location Chart

☆ 914C151X5SR

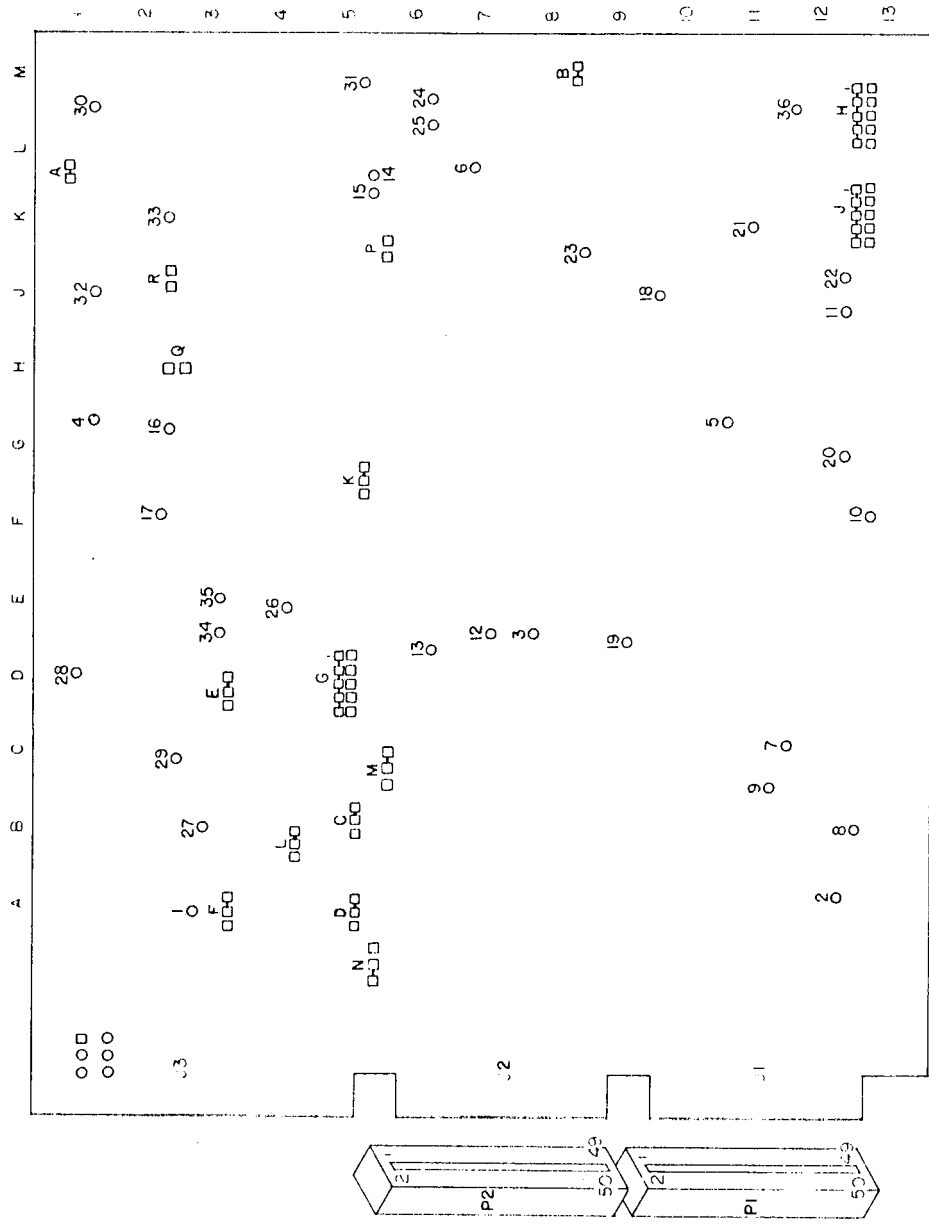
Δ 914C202X5PE

APPENDIX D/III

TEST POINTS	
TPI-6	GND
7	- WRITE (DEL) DATA
8	- READ COMMAND
9	- (SEEK + RECALIBRATE)
10	- R/W COMPLETE
11	+ UNIT CHECK
12	+ SEEK COMPLETE
13	- A=B
14	- BRANCH
15	+ INC
16	+ AM WRITE
17	- LOAD BYTE COUNTER
18	- SELECTED
19	+ D $\emptyset$
20	+ LCH CLK
21	- AM DETECTED
22	+ CRC ERROR
23	- BR 7
24	+ (NO 4V - MISSING SECTOR)
25	+ INDEX
26	+ SERDES CLOCK
27	+ ENABLE BR
28	+ ERROR VOLTAGE
29	- RAMP
30	- SERIAL DATA
31	- CHECK CRC
32	+ ARTE SHIFT CRC
33	+ WRITE CRC
34	+ DATA WINDOW
35	+ DELAYED DATA
36	+ DELAYED SERIAL DATA

TRACE OPTIONS	
TRACES	DESCRIPTION
A	CRC IC
B	FORMAT
G	DATA WINDOW ADJUST
H	EARLY ADJUST (M <sup>2</sup> FM)
J	LATE ADJUST (M <sup>2</sup> FM)
K,L,M,N	FORMAT
P,Q,R	VFO TEST

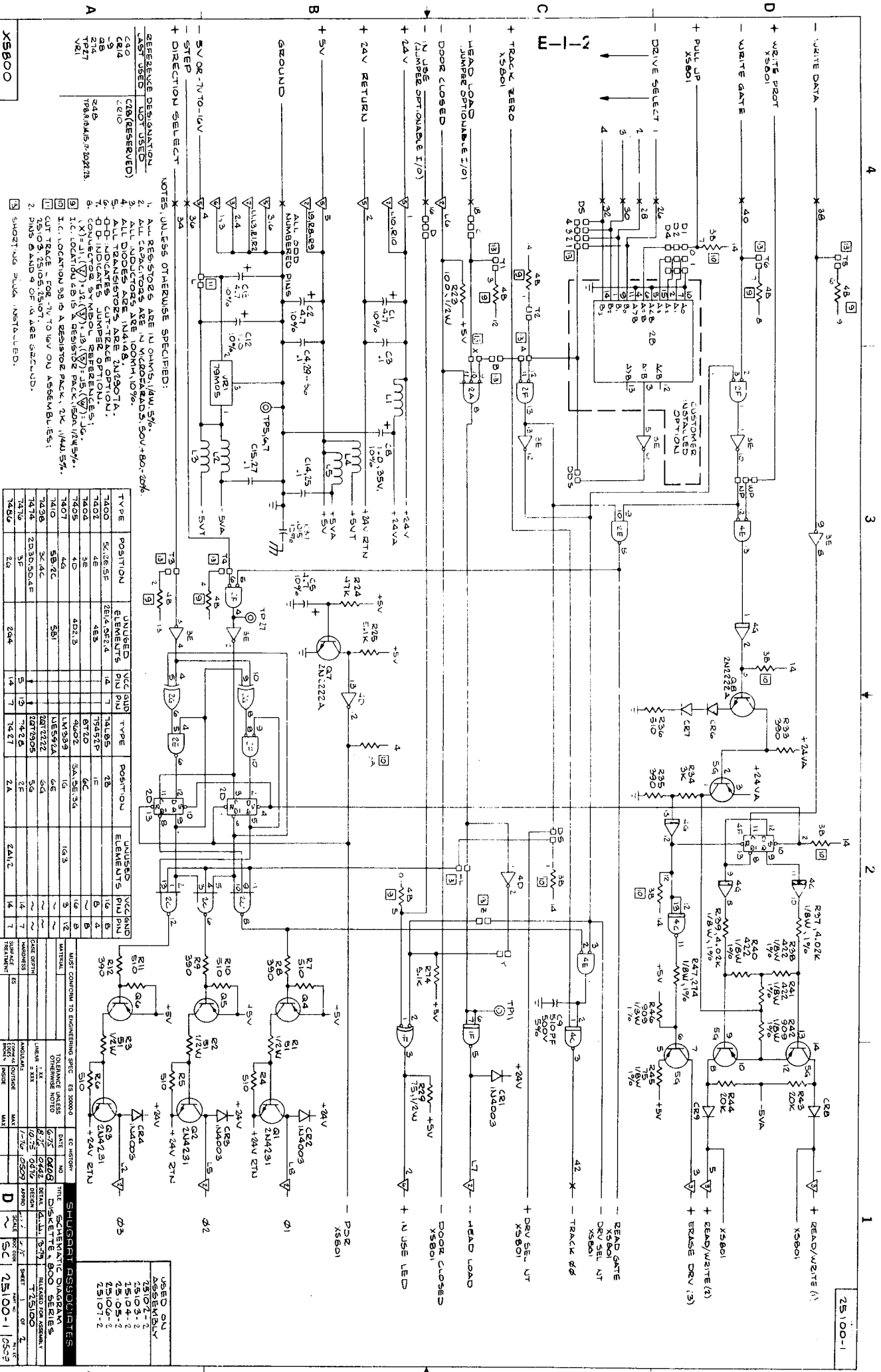


Formatter Test Points/Track Options - Locations chart



**APPENDIX E/I**

***UNIT LOGIC DIAGRAMS***



**REVERSE DESIGNATION**

LAST USED	NOT USED
C40	C26 (RESERVED)
C8	C20
C2	C10
C24	C25
C27	C28
C29	C29

**NOTES, UNLESS OTHERWISE SPECIFIED:**

- ALL RESISTORS ARE IN OHMS, (1/4W), 5%.
- ALL CAPACITORS ARE IN MICROFARADS, 50V, ±80-20%.
- ALL DIODES ARE IN 1N4001, 100V.
- ALL DIODES ARE IN 1N4148.
- ALL TRANSISTORS ARE IN 2N3904.
- ALL TRANSISTORS ARE CUT-TRAKE OPTION.
- Q-D INDICATES JUMPER OR BOARD OPTION.
- X(1) - (1) 1.2K (1/4W), 5% (1/4W), 5%.
- X(2) - (1) 1.2K (1/4W), 5% (1/4W), 5%.
- I.C. LOCATION 98 IS A RESISTOR PACK, 10K (1/4W), 5%.
- CUT TRACK FOR 74181 ON ASSEMBLY.
- 15103, 25105, 25107.
- 2 PINS 8 AND 9 OF IC ARE SOLDERED.
- SHORTCIRCUIT PINS 8 AND 9 OF IC.

**USED ON ASSEMBLY**

DATE	NO.	REV.	DESCRIPTION
25107-2	0000	1	INITIAL DISCREPANCY
25103-2	0000	1	INITIAL DISCREPANCY
25104-2	0000	1	INITIAL DISCREPANCY
25105-2	0000	1	INITIAL DISCREPANCY
25106-2	0000	1	INITIAL DISCREPANCY
25107-2	0000	1	INITIAL DISCREPANCY

**SHUREPORT DISCREPANCIES**

DATE	NO.	REV.	DESCRIPTION
25107-2	0000	1	INITIAL DISCREPANCY
25103-2	0000	1	INITIAL DISCREPANCY
25104-2	0000	1	INITIAL DISCREPANCY
25105-2	0000	1	INITIAL DISCREPANCY
25106-2	0000	1	INITIAL DISCREPANCY
25107-2	0000	1	INITIAL DISCREPANCY

**UNUSUED VCC AND GND PINS**

TYPE	POSITION	UNUSED ELEMENTS	VCC AND GND PINS	UNUSED ELEMENTS
7400	5C, 2E, 5F	2E, 1A, 5E, 2, 4	16	6
7402	4E	4E, 5	6	4
7404	3E	3E, 4	6	4
7405	4D	4D, 3	6	4
7407	4A	4A, 2	6	4
7408	5B, 2C	5B, 2C	6	4
7438	5C, 4C	5C, 4C	6	4
7474	2D, 3D, 5D, 4F	2D, 3D, 5D, 4F	6	4
7476	3F	3F	6	4
7486	2G	2G	6	4

**MARKET COMPACT TO ENGINEERING SPEC. IS 30000**

DATE	NO.	REV.	DESCRIPTION
25107-2	0000	1	INITIAL DISCREPANCY
25103-2	0000	1	INITIAL DISCREPANCY
25104-2	0000	1	INITIAL DISCREPANCY
25105-2	0000	1	INITIAL DISCREPANCY
25106-2	0000	1	INITIAL DISCREPANCY
25107-2	0000	1	INITIAL DISCREPANCY

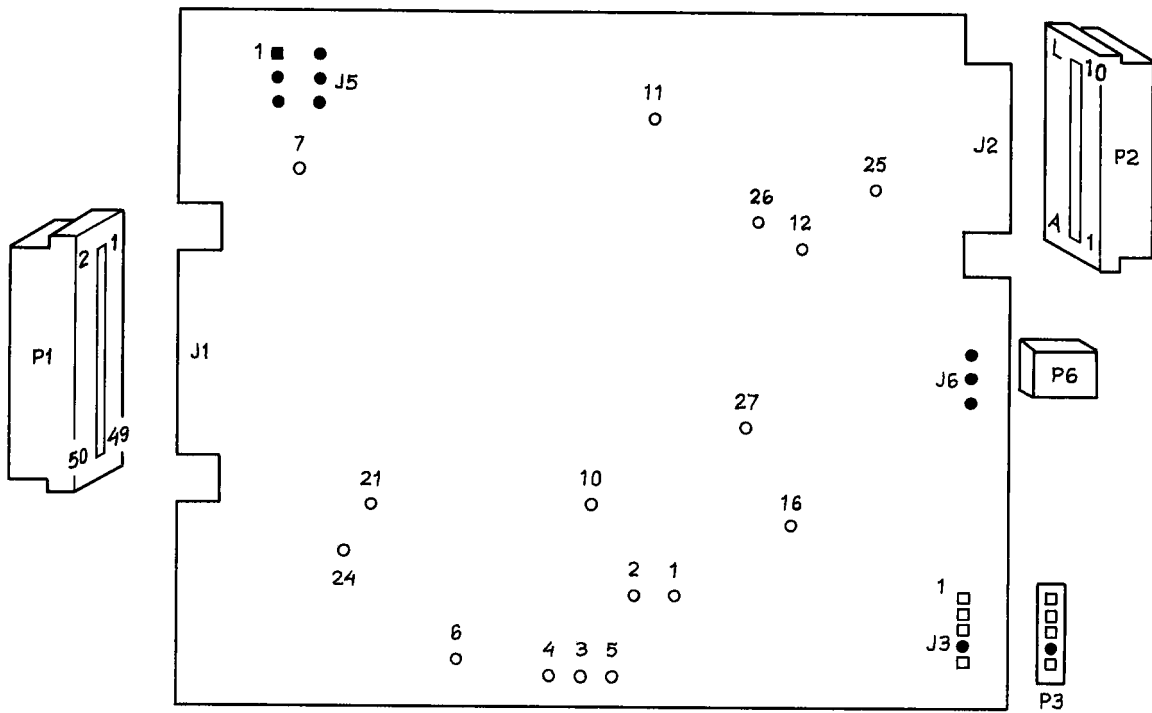
**DATE** 25100-1 **REV.** 1







UNIT PCB TEST POINT LOCATIONS

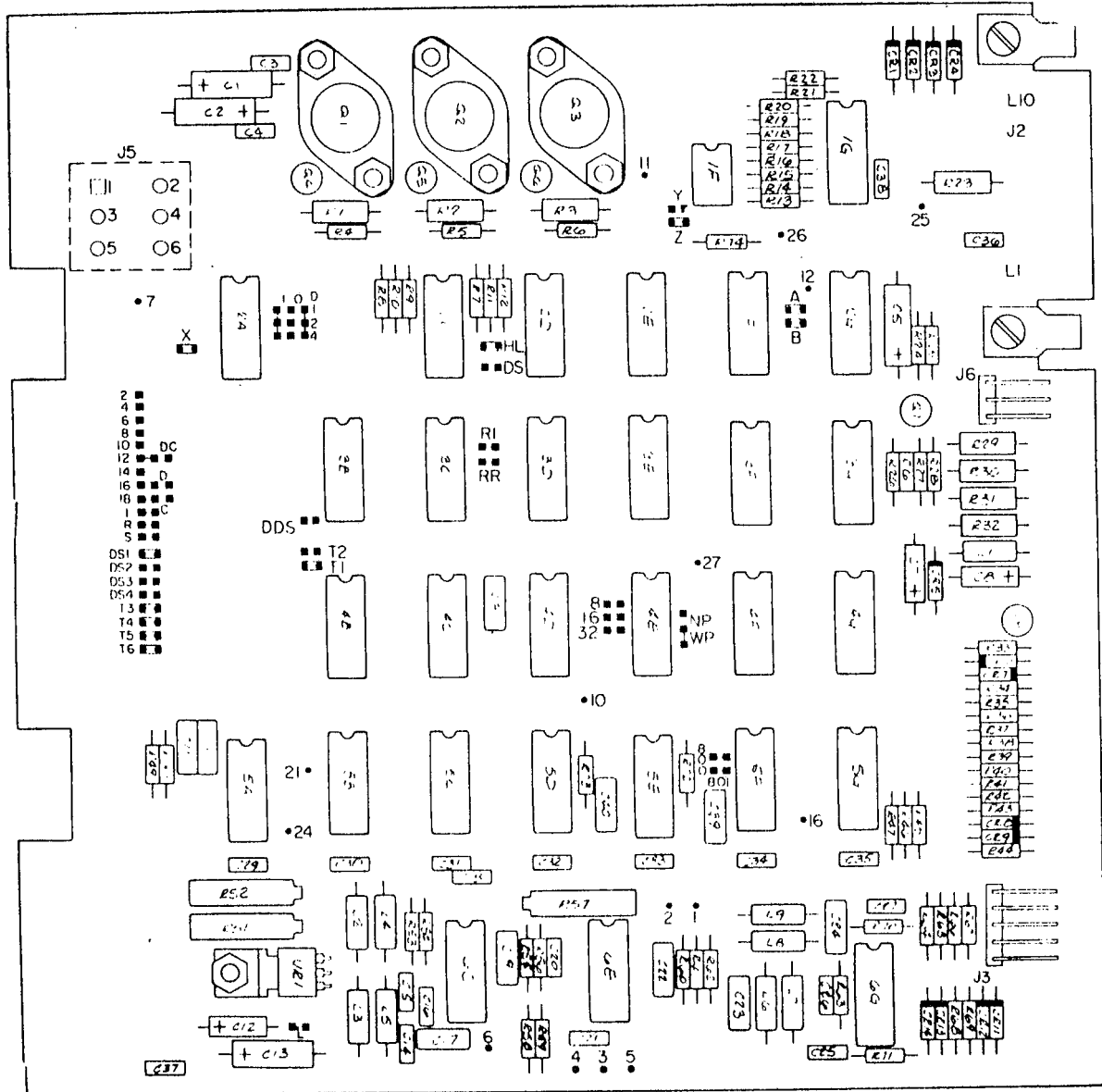


Test Point Assignment

- 1 Read Data Signal
- 2 Read Data Signal
- 3 Read Data (Differentiated)
- 4 Read Data (Differentiated)
- 5 Signal Ground
- 6 Signal Ground
- 7 Signal Ground
- 10 -Index
- 11 +Head Load
- 12 -Index and 801 Sector Pulses
- 16 +Read Data
- 21 -Data Separator Time +1
- 24 -Data Separator Time +2
- 25 +Write Protect
- 26 +Detect Track 00
- 27 +Gated Step Pulses



APPENDIX E/III

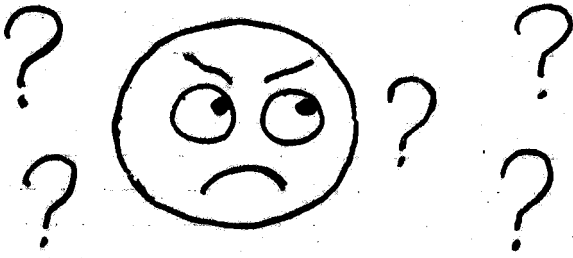


- Jumper Plug Installed as Shipped
- Test Point

Unit PCB Component Location



\*\*\*\*\* SEND US YOUR COMMENTS!!! \*\*\*\*\*

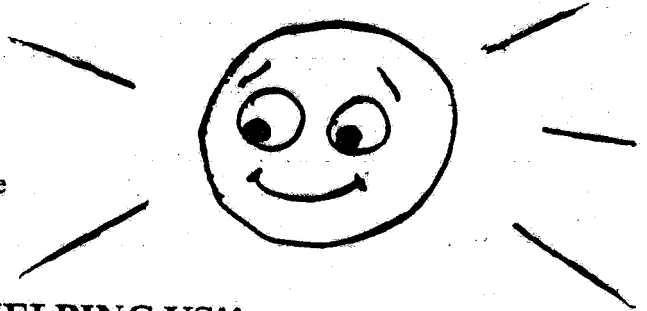


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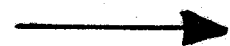
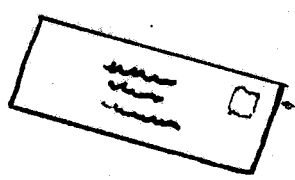
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