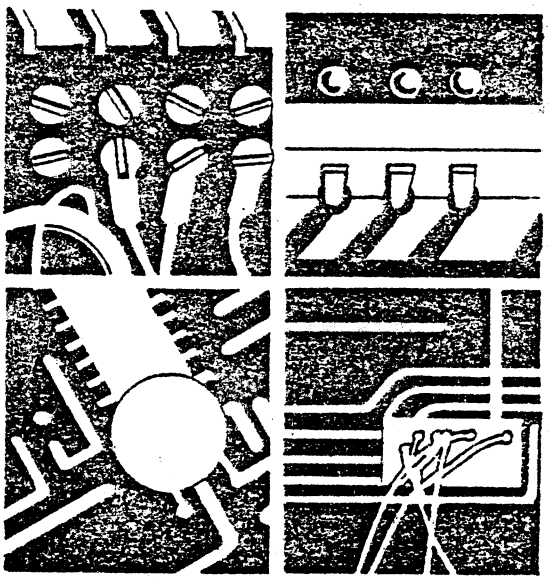
altair



8800b

DOCUMENTATION

mits

ALTAIR 8800b
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2450 Alamo SE
Albuquerque, NM 87106

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SECTION I

INTRODUCTION

1-1. SCOPE

This ALTAIR™ 8800b Documentation provides a general description of the various printed circuit cards contained in the ALTAIR 8800b and detailed theory of their operation. Included in the documentation is an operator's guide which familiarizes the operator with the various switches and indicators on the ALTAIR 8800b front panel. Detailed assembly instructions are also provided.

1-2. ARRANGEMENT

This manual contains five sections as follows:

1. Section I contains a general description of the ALTAIR 8800b computer and associated printed circuit cards.

2. Section II contains information on the controls and indicators which are located on the ALTAIR 8800b front panel.

3. Section III contains a detailed theory explanation of the ALTAIR 8800b circuit operation.

4. Section IV contains troubleshooting information for the ALTAIR 8800b.

5. Section V contains the detailed assembly instructions for the ALTAIR 8800b.

1-3. DESCRIPTION

The ALTAIR 8800b computer (Figure 1-1) is a general purpose, byte-oriented machine (8-bit word). It uses a common 100-pin bus structure that allows for expansion of either standard or custom plug-in modules. It supports up to 64K of directly addressable memory and can address 256 separate input and output devices. The ALTAIR 8800b computer has 78 basic machine language instructions and consists of a power supply board, an interface board, a central processing unit (CPU) board, and a display/control board.

1-4. POWER SUPPLY BOARD (Figure 1-2)

The Power Supply Board provides two of the three output voltages to the ALTAIR 8800b computer bus, a positive and negative 18 volts. It includes a bridge rectifier circuit and associated filter capacitors, a 10-pin terminal block connector, and the regulating transistors for the positive and negative 18 volt supplies.

1-5. INTERFACE BOARD (Figure 1-3)

The Interface Board buffers all signals between the display/control board and the ALTAIR 8800b bus. It also contains eight parallel data lines which transfer data to the CPU from the Display/Control board.

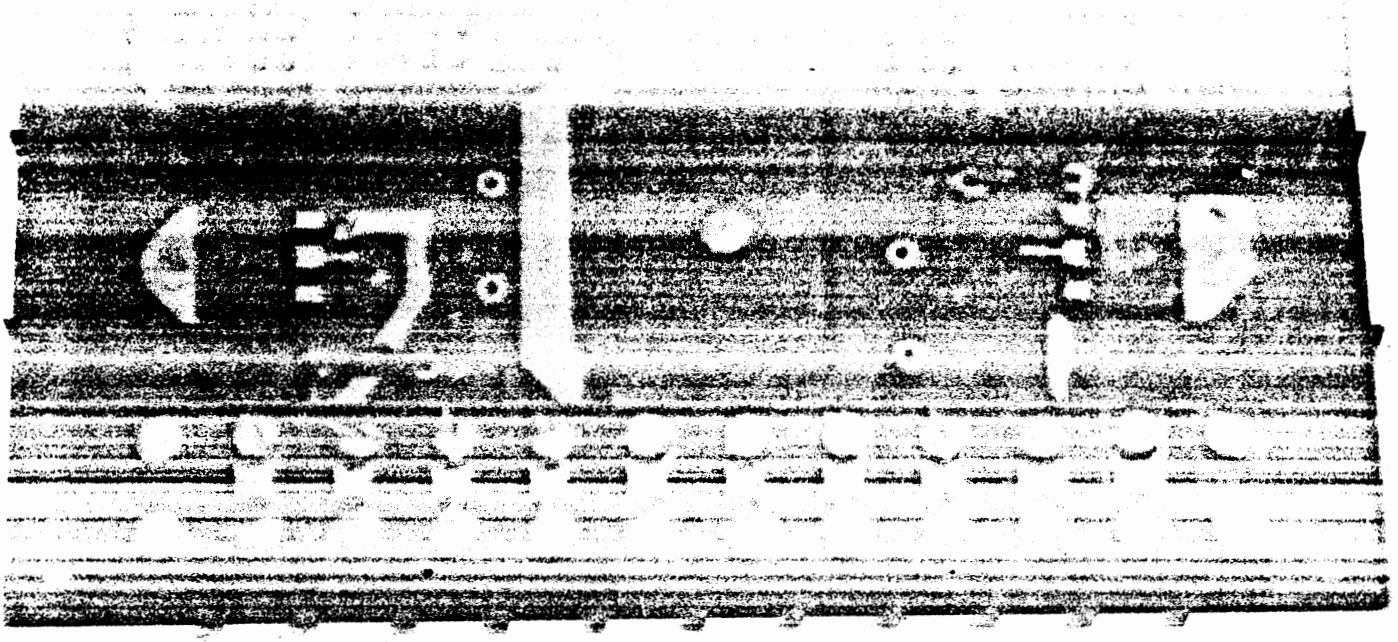


Figure 1-2. Power Supply Board

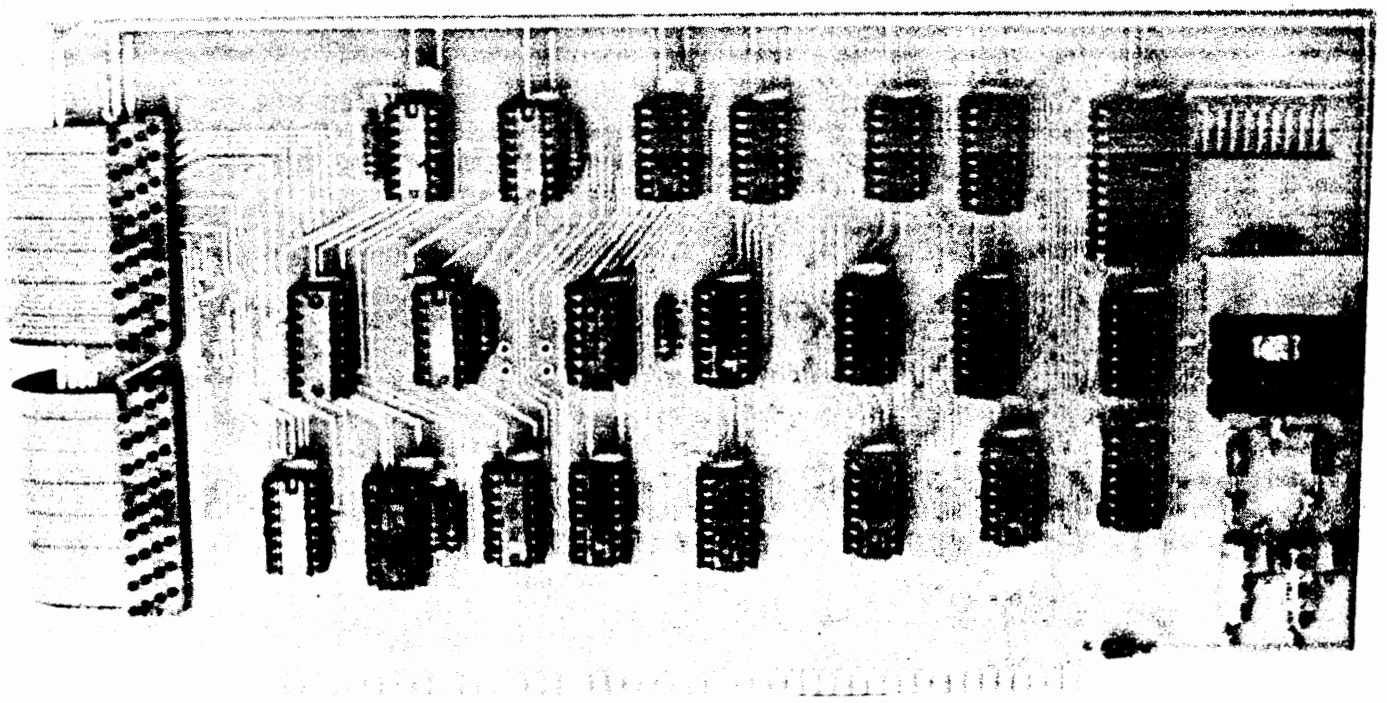


Figure 1-3. Interface Board

1-6. CPU BOARD (Figure 1-4)

The CPU board controls and processes all instructions and data within the ALTAIR 8800b computer. It contains the Intel Corporation model 8080A microprocessor circuit, the master timing circuit, eight input and eight output data lines to the ALTAIR bus control circuits.

1-7. DISPLAY/CONTROL BOARD (Figure 1-5)

The Display/Control Board conditions all ALTAIR 8800b front panel switches and receives information to be displayed on the front panel. It contains a programmable read only memory (PROM), switch and display control circuits, and control circuits to condition the CPU.

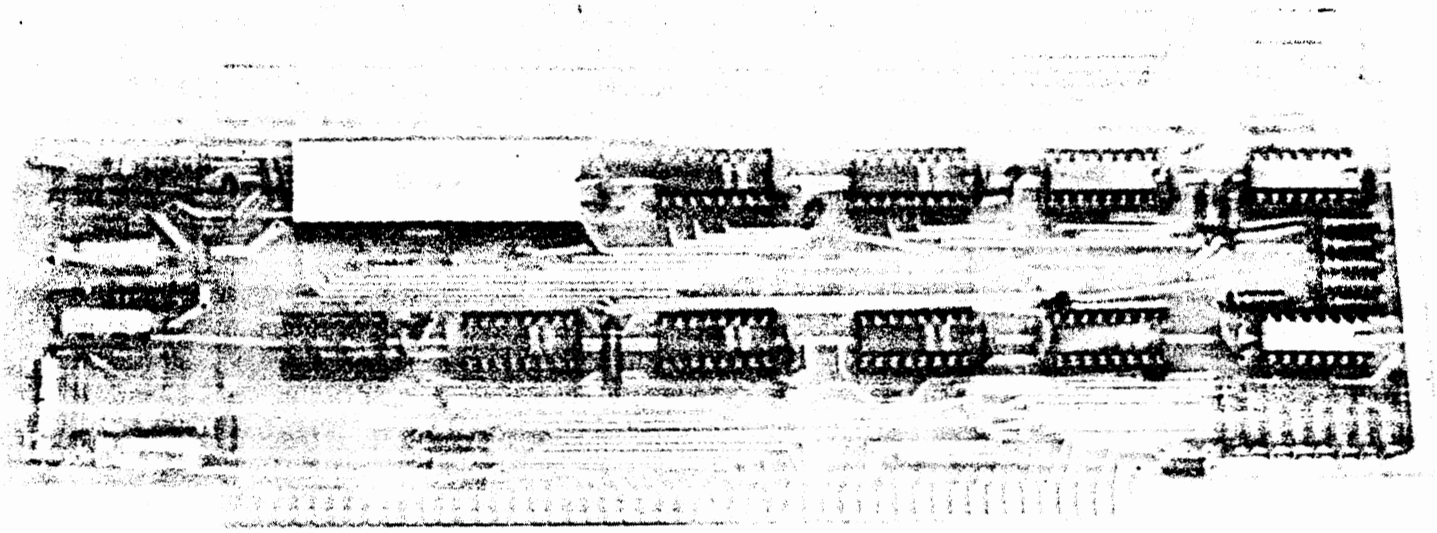


Figure 1-4. CPU Board

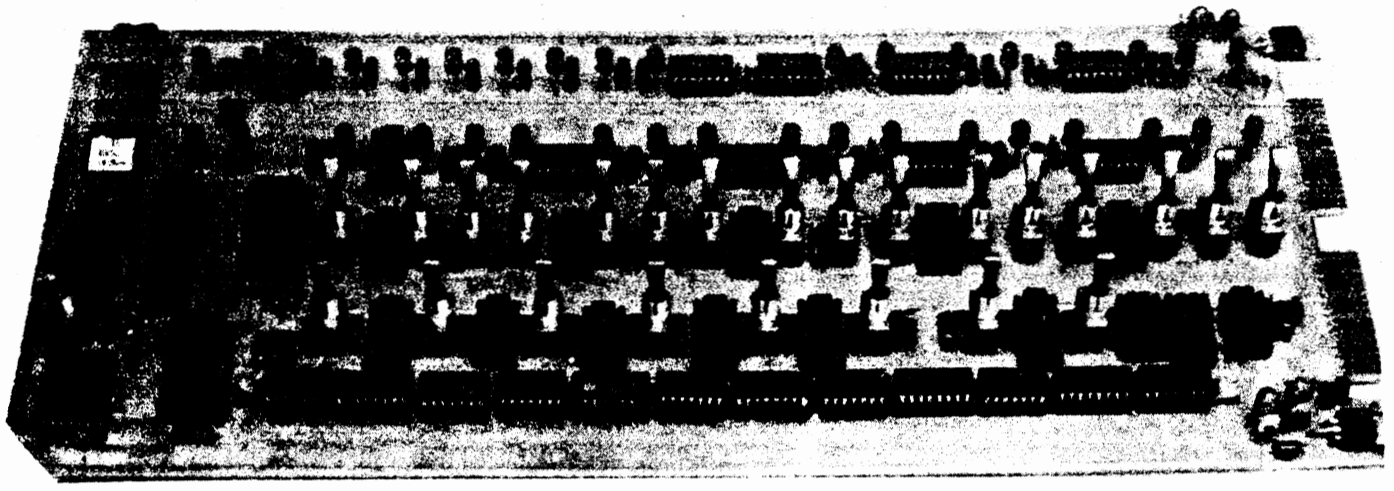
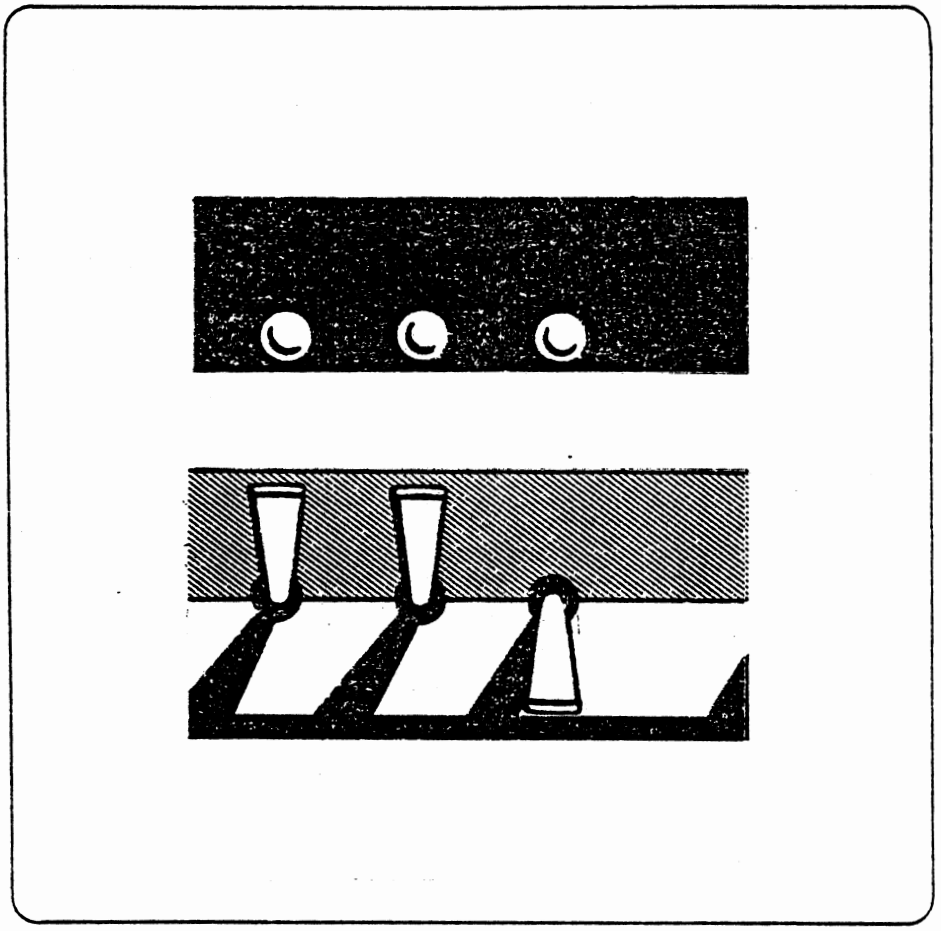


Figure 1-5. Display/Control Board

SECTION II



OPERATORS GUIDE

2-1. GENERAL

The Operators Guide contains information on the ALTAIR 8800b computer (8800b) front panel controls and indicators. It includes general switch operation exercises and a sample program which is intended to familiarize the operator with the various front panel operations. This section does not contain specific information on the 8800b software; but the Intel 8080 Microcomputer Systems Users Manual is provided for this purpose. Also, additional programs available to the user are described in the ALTAIR Software Library. Update information is contained with your unit.

2-2. FRONT PANEL SWITCHES AND INDICATORS

The Front Panel switches permit the operator to perform various ALTAIR 8800b operations, and the indicators display address information, data information, and primary status control line information. Refer to Figure 2-1 for the location of the switches and indicators and Table 2-1 for an explanation of each.

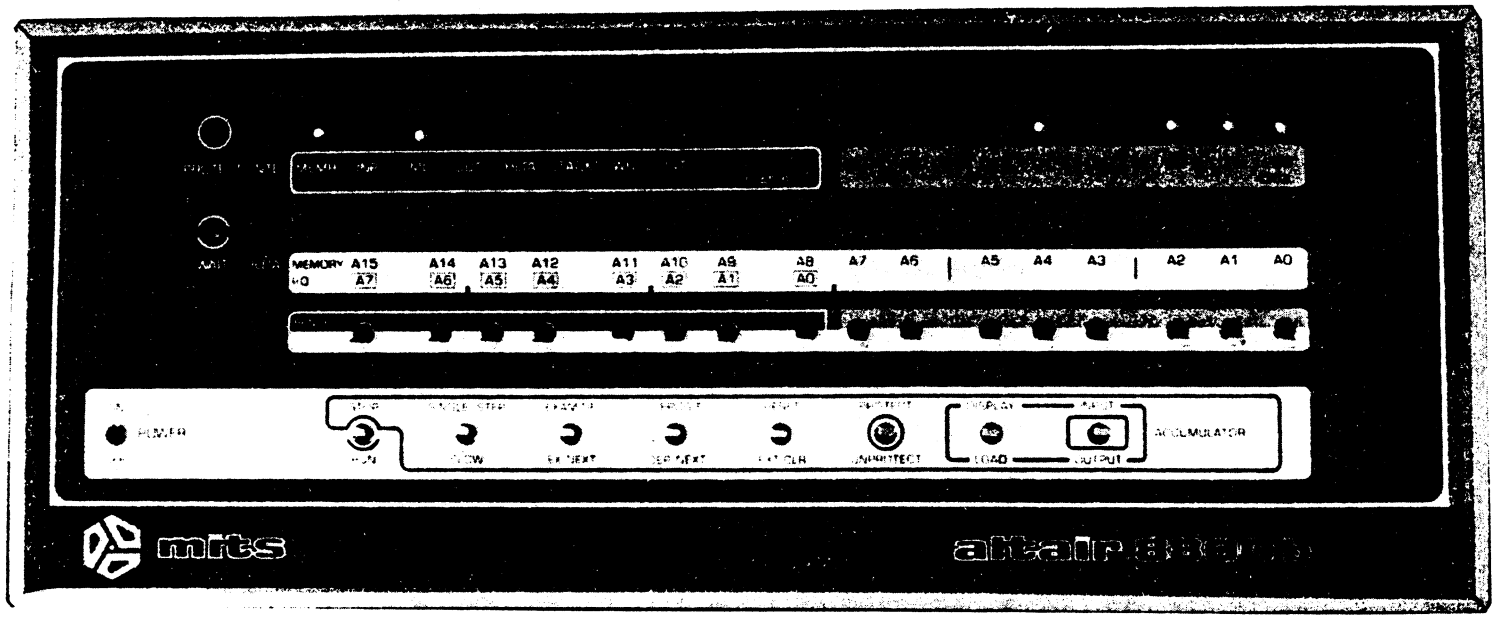


Figure 2-1. Altair 8800b Front Panel

Table 2-1. ALTAIR 8800b Switches and Indicators

Switch	Function or Indication
POWER ON/OFF	Applies power to the ALTAIR 8800b
STOP/RUN	The RUN position allows the CPU to process data and disables all functions on the front panel except reset. The STOP position conditions the CPU to a wait state and enables all functions on the front panel.
SINGLE STEP/ SLOW	The SINGLE STEP position allows execution of one machine cycle or one instruction cycle (depending upon the option selected). SLOW position allows execution of machine or instruction cycles at a rate of approximately 2 cycles per second. (Normal speed is approximately 500,000 machine cycles per second.) The CPU will execute the cycles as long as the SLOW position is maintained.
EXAMINE/ EX NEXT	The EXAMINE position allows the operator to examine the memory address selected on the A0-A15 MEMORY switches. The contents at that address are displayed on the DATA D0-D7 indicators. The EX NEXT position allows the operator to examine the next sequential memory address. Each time EX NEXT is actuated, the contents of the next sequential memory address are displayed.

Table 2-1. ALTAIR 8800b Switches and Indicators - Continued

Switch	Function or Indication
DEPOSIT/ DEP NEXT	The DEPOSIT position stores the contents of the lower address switches (A0-A7) into the memory address that is displayed on the MEMORY address A0-A15 indicators. The DEP NEXT position stores the contents of the lower address switches (A0-A7) into the next successive memory address.
RESET/ EXT CLR	The RESET position resets the program counter to zero and the interrupt enable flag in the CPU. The EXT CLR position produces an external clear signal on the system bus which generally clears an input/output.
PROTECT/ UNPROTECT*	The PROTECT position conditions the write protect circuits on the currently addressed memory board, preventing data in that block of memory from being changed. The front panel or the CPU cannot affect the memory when protected. UNPROTECT position allows the contents of memory to be changed.
ACCUMULATOR DISPLAY/LOAD	The DISPLAY position allows the contents of the CPU accumulator register to be displayed on the DATA D0-D7 indicators. The LOAD position allows the lower eight address switch (A0-A7) information to be stored in the CPU accumulator register.

*Protect switch only applies to memory boards with a protect circuit.

Table 2-1. ALTAIR 8800b Switches and Indicators - Continued

Switch or Indicator	Function or Indication
INPUT/ OUTPUT	The INPUT position allows an external device, selected on the I/O A0-A7 switches (upper eight address switches), to input data into the CPU accumulator. The OUTPUT position allows an external device, selected on the I/O A0-A7 switches, to receive data from the CPU accumulator register.
Address Switches A0-A15	These switches are used to select an address in memory or to enter data. The up position denotes a one bit and the down position denotes a zero bit.
SENSE switches A8-A15	The upper eight address switches (A8-A15) also function as SENSE switches. The data present on these switches is stored in the accumulator if an input from channel 377_8 (front panel) is executed.
MEMORY A0-A15	Display the memory address being examined or loaded with data.
PROTECT	Memory is protected.
INTE	Interrupts are enabled.
MEMR	The CPU is reading data from memory.
INP	An external device is inputting data to the CPU.
M1	The CPU is in machine cycle one of an instruction cycle.
OUT	The CPU is outputting data to an external device.

Table 2-1. ALTAIR 8800b Switches and Indicators - Continued

Indicator	Function or Indication
HLTA	The CPU is in a halt condition.
STACK	The address bus contains the address of the stack pointer.
WO	The CPU is writing out data to an external device or memory.
INT	The CPU has acknowledged an interrupt request.
DATA D0-D7	Data from memory, an external device, or the CPU
WAIT	The CPU is in a wait condition.
HLDA	The CPU has acknowledged a hold signal.

2-3. FRONT PANEL SWITCH APPLICATIONS

The following switch applications are intended to familiarize the operator with the ALTAIR 8800b front panel switches and indicators. Perform the operations in a sequential manner as shown in the following tables.

2-4. POWER ON SEQUENCE (Table 2-2)

The power on sequence resets the CPU program counter to the first memory address and places the CPU in a wait condition at the beginning of an instruction cycle.

Table 2-2. Power On Sequence

Step	Function	Indication
1	Position the POWER ON/ OFF switch to ON.	MEMR, M1, and WAIT indicators are on. Some DATA D0-D7 indicators may also be on. All other indicators are off.

2-5. RUN OPERATION (Table 2-3)

The run operation releases the CPU from a wait condition, and allows it to execute a program. When the run operation is enabled, all other front panel switches are inactive except the RESET switch.

Table 2-3. Run Operation

Step	Function	Indication
1	Momentarily position the STOP/RUN switch to RUN.	WAIT indicator is off (or may be dimly lit). The machine can now execute a program.

2-6. STOP OPERATION (Table 2-4)

The stop operation places the CPU in a wait condition and allows the operator to use the switches on the 8800b front panel.

Table 2-4. Stop Operation

Step	Function	Indication
1	Position the STOP/RUN switch to STOP.	WAIT, MEMR, and M1 indicators are on. The operator now has control of the front panel.

2-7. EXAMINE MEMORY OPERATION (Table 2-5)

This procedure allows the operator to select a memory address and examine its contents.

Table 2-5. Examine Memory Operation

Step	Function	Indication
1	Position the address switches A0-A15 down.	
2	Position the EXAMINE/ EX NEXT switch to EXAMINE.	A0 through A15 indicators are off, indicating memory address location 000_8 is being examined. DATA D0 through D7 indicators are displaying the contents of location 000_8.
3	Position address switches A1 and A2 up.	
4	Position the EXAMINE/ EX NEXT switch to EXAMINE.	A1 and A2 indicators are on, indicating memory address 006_8 is being examined. DATA D0 through D7 indicators are displaying the contents of location 006_8.

2-8. ALTERING MEMORY CONTENTS (Table 2-6)

This procedure allows the operator to select a memory address and change its contents.

Table 2-6. Altering Memory Contents

Step	Function	Indication
1	Position address switch A5 up and the remaining switches down.	
2	Position the EXAMINE/EX NEXT switch to EXAMINE	A5 indicator is on, indicating memory address 040_8. DATA D0 through D7 indicators are displaying the contents of location 040_8.
3	Position the A0 through A7 address switches up.	
4	Position the DEPOSIT/DEP NEXT to DEPOSIT	DATA D0 through D7 indicators are on, indicating the new data that has been placed in address location 040_8.

2-9. EXAMINE NEXT MEMORY LOCATION (Table 2-7)

This procedure allows the operator to examine the next sequential memory location, as determined by the address switches.

Table 2-7. Examine Next Memory Location

Step	Function	Indication
1	Position address switches A0 and A5 up, and the remaining switches down.	
2	Position the EXAMINE/EX NEXT switch to EXAMINE	A0 and A5 indicators are on, indicating memory address 041_8.

Table 2-7. Examine Next Memory Location - Continued

Step	Function	Indication
3	Position address switches A1, A4, and A6 up, and the remaining switches down.	
4	Position the DEPOSIT/DEP NEXT switch to DEPOSIT	DATA D1, D4, and D6 indicators are on.
5	Position address switch A5 up, and the remaining switches down.	
6	Position the EXAMINE/EX NEXT switch to EX NEXT	A5 indicator is on, indicating memory address 040_8. DATA D0 through D7 indicators are on.
7	Position the EXAMINE/EX NEXT switch to EX NEXT	A5 and A0 indicators are on, indicating address 041_8. DATA D1, D4, and D6 indicators are on.

2-10. ALTER NEXT MEMORY LOCATION CONTENTS (Table 2-8)

This procedure allows the operator to select a memory address and change the contents of the address that immediately follows.

Table 2-8. Altering Next Memory Contents

Step	Function	Indication
1	Position address switches A0 and A5 up, and the remaining switches down.	
2	Position the EXAMINE/EX NEXT switch to EXAMINE	A0 and A5 indicators are on.
3	Position address switches A0 through A7 up	

Table 2-8. Altering Next Memory Contents - Continued

Step	Function	Indication
4	Position the DEPOSIT/ DEP NEXT switch to DEP NEXT	A1 and A5 indicators are on, indicating 042_8. DATA D0 through D7 are on, displaying the new contents of location 042_8.
5	To verify, position address switches A5 and A1 up, and the remaining switches down.	
6	Position the EXAMINE/ EX NEXT switch to EXAMINE	A1 and A5 indicators are on, and DATA D0 through D7 are on.

2-11. LOADING AND DISPLAYING ACCUMULATOR DATA (Table 2-9)

This procedure allows the operator to load new data into the accumulator or check the contents of the accumulator.

Table 2-9. Loading and Displaying Accumulator Data

Step	Function	Indication
1	Position address switches A0, A1, and A2 up, and the remaining switches down.	
2	Position the ACCUMULATOR DISPLAY/LOAD switch to LOAD	
3	Position the ACCUMULATOR DISPLAY/LOAD switch to DISPLAY	DATA D0, D1, and D2 indicators are on while "DISPLAY" is activated.

2-12. LOADING A SAMPLE PROGRAM

The sample program is designed to retrieve two numbers from memory, add them together, and store the result in memory. The exact program in mnemonic form can be written as follows:

0. LDA
1. MOV B,A
2. LDA
3. ADD B
4. STA
5. JMP

The mnemonics for all 78 8800b instructions are explained in detail in the Intel 8080 Microcomputer System User's Manual. However, the instructions used in this program are explained as follows:

1. LDA--Load the accumulator with the contents of a specified memory address.
2. MOV B,A--Move the contents of the accumulator into register B.
3. ADD B--Add the contents of register B to the contents of the accumulator and store the result in the accumulator.
4. STA--Store the contents of the accumulator in a specified memory address.
5. JMP--Jump to the first step in the program.

Step 5, the JMP instruction (followed by the memory address of the first instruction), causes the CPU to "jump" back to the beginning of the sample program and execute the program repeatedly until the CPU is halted. Without a JMP instruction, the CPU would continue to run randomly through memory.

2-13. LOADING THE PROGRAM

To load the program into the 8800b, first determine the memory addresses for the two numbers to be added and where the result is to be stored. Store the program instructions in successive memory addresses, beginning at the first memory address, 000_8. In this example, the first number to be added will be located at memory address 200_8 (10 000 000), the second at memory address 201_8 (10 000 001), and the sum will be stored in memory address 202_8 (10 000 010). Now that the memory addresses have been specified, the program can be converted into its machine language bit patterns (Table 2-10).

Table 2-10. Machine Language Bit Patterns

MNEMONIC	BIT PATTERN	EXPLANATION
LDA 200	00 111 010	Load Accumulator in the CPU with con-
	10 000 000	tents of Memory address 200_8 (2 bytes
	00 000 000	required for memory addresses)
MOV B,A	01 000 111	Move Accumulator data to Register B
LDA 201	00 111 010	Load Accumulator with the contents
	10 000 001	of Memory address 201_8
	00 000 000	
ADD B	10 000 000	Add Register B to Accumulator
STA 202	00 110 010	Store the Accumulator contents
	10 000 010	in Memory address 202_8
	00 000 000	
JMP 000	11 000 011	Jump to Memory location 0.
	00 000 000	
	00 000 000	

The octal equivalent of each bit pattern is also frequently included in the program listing. It is easy to load octal numbers on the front panel switches, since it is only necessary to know the binary equivalents for the numbers 0-7. The resulting program, including octal equivalents, may be written as shown in Table 2-11:

Table 2-11. Addition Program

MEMORY ADDRESS	MNEMONIC	BIT PATTERN	OCTAL EQUIVALENT
000	LDA 200	00 111 010	0 7 2
001	(address)	10 000 000	2 0 0
002	(address)	00 000 000	0 0 0
003	MOV B,A	01 000 111	1 0 7
004	LDA 201	00 111 010	0 7 2
005	(address)	10 000 001	2 0 1
006	(address)	00 000 000	0 0 0
007	ADD B	10 000 000	2 0 0
010	STA 202	00 011 010	0 6 2
011	(address)	10 000 010	2 0 2
012	(address)	00 000 000	0 0 0
013	JMP 000	11 000 011	3 0 3
014	(address)	00 000 000	0 0 0
015	(address)	00 000 000	0 0 0

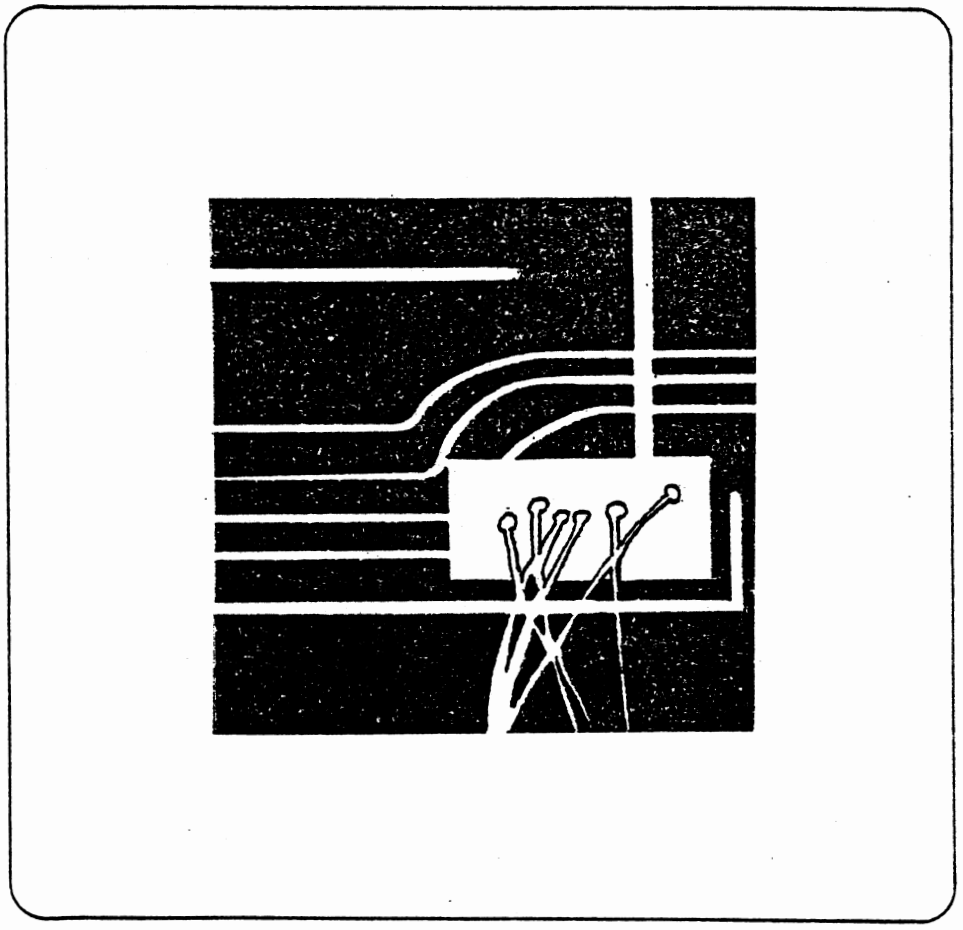
Using the front panel switches, the program may now be entered into the computer. To begin loading the program at the first memory address 000, position the RESET/CLR switch to RESET. The data to be stored in address 000 is entered on address switches A0 through A7. After the address switches are set, position the DEPOSIT/DEP NEXT switch to DEPOSIT to enter the A0-A7 bit pattern into memory address 000. Enter the second byte of data on the address switches and position the DEPOSIT/DEP NEXT switch to DEP NEXT. The bit pattern will be loaded automatically into the next sequential memory address (001). Continue loading the data into memory for the remainder of the program. The complete program loading procedure is shown in Table 2-12:

Table 2-12. Addition Program Loading

MEMORY ADDRESS	ADDRESS SWITCHES DATA 0-7	CONTROL SWITCH
		RESET
000	00 111 010	DEPOSIT
001	10 000 000	DEPOSIT NEXT
002	00 000 000	DEPOSIT NEXT
003	01 000 111	DEPOSIT NEXT
004	00 111 010	DEPOSIT NEXT
005	10 000 001	DEPOSIT NEXT
006	00 000 000	DEPOSIT NEXT
007	10 000 000	DEPOSIT NEXT
010	00 110 010	DEPOSIT NEXT
011	10 000 010	DEPOSIT NEXT
012	00 000 000	DEPOSIT NEXT
013	11 000 011	DEPOSIT NEXT
014	00 000 000	DEPOSIT NEXT
015	00 000 000	DEPOSIT NEXT

The program is now ready to be run, but first it is necessary to store data at each of the two memory addresses (200_8 and 201_8) to be added together. To load the first address, set address switches A0-A7 to 10 000 000_2 and position the EXAMINE/EX NEXT switch to EXAMINE. Now load any desired number into this address by using address switches A0-A7. When the number has been loaded onto the switches, position the DEPOSIT/DEP NEXT to DEPOSIT to load the data into memory. To load the next address, enter a second number on the address switches A0-A7 and position the DEPOSIT/DEP NEXT switch to DEP NEXT. Since sequential memory addresses were selected, the number will be loaded automatically into the proper address (10 000 001_2). Once the program has been loaded and the two numbers have been stored in memory locations 200_8 and 201_8, the program can be run. Return to address 000 by positioning all A0-A7 address switches down and positioning the EXAMINE/EX NEXT switch to EXAMINE. Then position the STOP/RUN switch to RUN. Wait a moment and position the STOP/RUN switch to STOP. Check the answer of your addition program by selecting memory location 202_8 on the address switches and positioning the EXAMINE/EX NEXT switch to EXAMINE. The result is displayed on the DATA D0-D7 indicators.

SECTION III



THEORY OF OPERATION

3-1. GENERAL

This section contains information needed to understand the operation of the MITS Altair 8800b computer (8800b). It contains a basic description of the logic symbols used in the 8800b schematics and detailed theory of the 8800b Central Processing Unit, Interface and Front Panel circuits.

3-2. LOGIC CIRCUITS

The logic circuits used in the 8800b drawings are presented as a tabular listing in Table 3-1. The table is constructed to present the functional name, symbolic representation, and a brief description of each logic circuit. Where applicable, a truth table is provided to aid in understanding circuit operation. Although Table 3-1 does not include every logic circuit used in the drawings, all unmentioned circuits (and their symbolic representations) are variations of the circuits presented with their functional descriptions basically the same. The active state of the inputs and outputs of the logic circuits is graphically displayed by small circles. A small circle, at an input to a logic circuit, indicates that the input is an active LOW; that is, a LOW signal will enable the input. A small circle, at the output of a logic circuit, indicates that the output is an active LOW; that is, the output is low in the actuated state. Conversely, the absence of a small circle indicates that the input or output is active HIGH.

After studying Table 3-1, refer to the "Intel 8800 Microcomputer Systems User's Manual" for information on the 8212, 8216, 8224 and 8080 integrated circuits (ICs). It is recommended that a good understanding of the IC operations be developed before continuing this section.

3-3. ALTAIR 8800b OPERATION

The Altair 8800b operation is explained from a system standpoint. The 8800b system operation is dependent upon the following four circuits: an Interface circuit, a Central Processing Unit (CPU) circuit, a Display/Control circuit, and a Power Supply circuit.

Table 3-1. Symbol Definitions

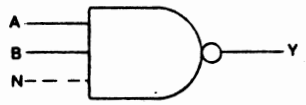
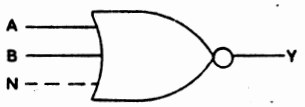
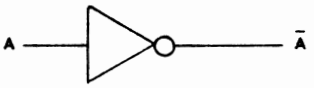
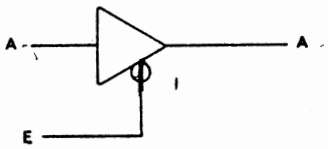
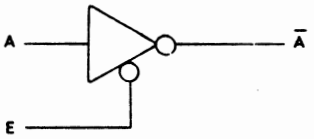
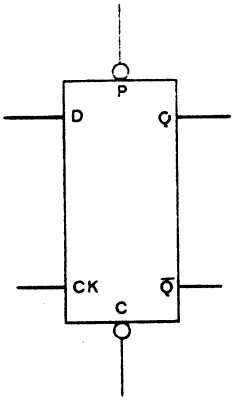
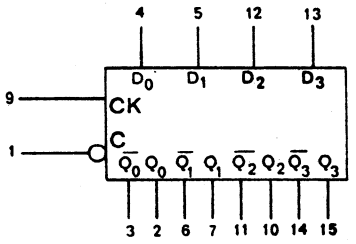
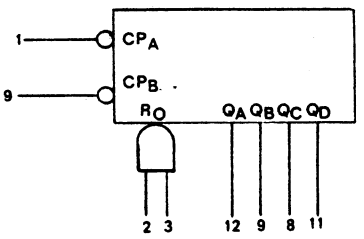
NAME	LOGIC SYMBOL	DESCRIPTION
NAND gate	 $Y = \overline{AB \ldots N}$	The NAND gate performs one of the basic logic functions. All of the inputs have to be enabled (HIGH) to produce the desired (LOW) output.
NOR gate	 $Y = \overline{A + B \ldots + N}$	The NOR gate performs one of the basic logic functions. Any of the inputs need be enabled (HIGH) to produce the desired (LOW) output.
Inverter		The inverter is an amplifier whose output is the opposite state of the input.
Non-Inverting Bus Driver		The non-inverting bus driver is an amplifier whose output is the same state as the input. Data is enabled through the device by applying a (LOW) signal to the E input.
Inverting Bus Driver		The inverting bus driver is an amplifier whose output is the opposite state of the input. Data is enabled through the driver by applying a (LOW) signal to the E input.

Table 3-1. Symbol Definitions - Continued

NAME	LOGIC SYMBOL	DESCRIPTION
Edge triggered D type flip-flop	 **Truth Table**	Applying a LOW signal to the preset input (P) sets the flip-flop with output Q HIGH and output $\overline{Q}$ LOW. Applying a LOW signal to the clear input (C) resets the flip-flop with Q LOW and $\overline{Q}$ HIGH. This method of setting and resetting the flip-flop is independent of the clock (asynchronous). If a signal is applied to the D input, the flip-flop Q output is directly affected on the positive edge of the clock (truth table).
QUAD D flip-flop		The information on the D inputs is stored during the positive edge of the clock (CK). The clear (C) input, when LOW, resets all flip-flops independent of the clock or D inputs.
4-Bit Binary Ripple Counter		The 4-bit binary ripple counter operation requires that the QA output be externally connected to input CP_B. The input count pulses (negative edge) are applied to input CP_A enabling a divide by 2, 4, 8, and 16 at the QA, QB, QC, and QD outputs. The reset (RO) input resets the counter regardless of the clock input (CP_A) when both inputs are HIGH.

Truth Table

T_n	T_{n+1}	
D	Q	$\overline{Q}$
L	L	H
H	H	L

Table 3-1. Symbol Definitions - Continued

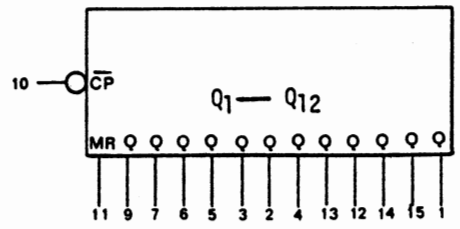
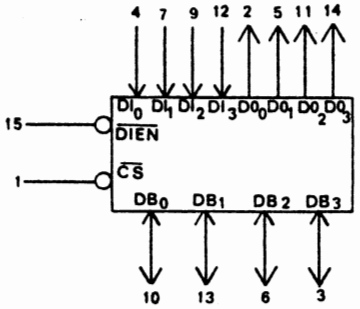
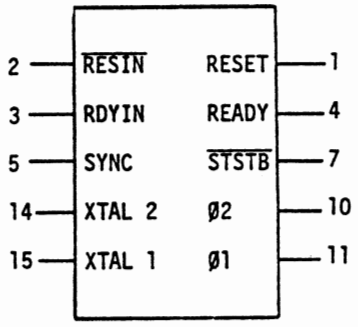
NAME	LOGIC SYMBOL	DESCRIPTION
12-Bit Binary Counter		The 12-bit counter advances on the negative edge of the clock input (CP). A HIGH on the master reset input (MR) clears all counter stages and forces all outputs (Q0-Q11) LOW which is independent of the clock input.
Bi-Directional Device		Output data from a device is present on the DI_0-DI_3 lines and is enabled when $\overline{DIEN}$ and $\overline{CS}$ are LOW. Lines DB_0-DB_3 transfer the data to the receiving unit. Input data to the device is present on the DB_0-DB_3 lines and is enabled when $\overline{DIEN}$ is HIGH and $\overline{CS}$ is LOW. Input data is transferred to the device on the DO_0-DO_3 lines.
Clock Generator		The XTAL 1 and 2 inputs allow for an external crystal connection which produces a Ø1 and Ø2 master clock for the 8800b. The SYNC input from the 8080 (CPU) and internal timing generate a LOW status strobe ($\overline{STSTB}$) signal. The reset in ($\overline{RESIN}$) input generates a RESET output to condition the 8080 (CPU). A HIGH ready in (RDYIN) input generates a READY output to enable the CPU.

Table 3-1. Symbol Definitions - Continued

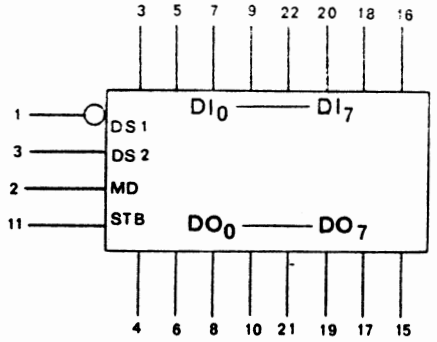
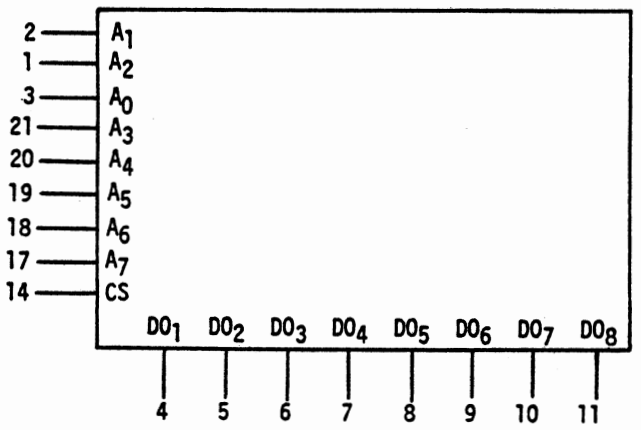
NAME	LOGIC SYMBOL	DESCRIPTION
Data Latch		The data latch is used to store or transfer data on the DO_0-DO_7 outputs by affecting the data latch control inputs. There are several different ways used to store data or transfer it to the data latch. When data is presented to the DI_0-DI_7 inputs and the device selection 2 (DS2), mode MD, and strobe (STB) are HIGH, a LOW device selection 1 ($\overline{DS1}$) allows the input data to be present on the DO_0-DO_7 outputs. When data is presented to the DI_0-DI_7 inputs and MD and STB are HIGH, a HIGH DS2 and LOW $\overline{DS1}$ allow the input data to be present on the DO_0-DO_7 outputs. When data is presented to the DI_0-DI_7 inputs and $\overline{DS1}$ and MD are LOW, a HIGH DS2 and STB allow the input data to be present on the DO_0-DO_7 outputs. When data is presented to the DI_0-DI_7 inputs, and MD and DS2 are HIGH with $\overline{DS1}$ LOW, the input data is directly transferred to the DO_0-DO_7 outputs as long as these states are present.

Table 3-1. Symbol Definitions - Continued

NAME	LOGIC SYMBOL	DESCRIPTION
PROM (programmable read only memory)		When the chip select input (CS) is LOW, the binary address at input A_0 through A_7 is decoded to select one of 256 address locations. The data is present on the DO_1 through DO_8 outputs.

These circuits comprise the basis of the 8800b and control the operation that allows communication with memory and/or external devices. The following paragraphs explain how these four circuits function as a system to accomplish master timing, data transfers to and from memory or external devices, and instigation of front panel functions.

3-4. SCHEMATIC REFERENCING

The detailed schematics of the Interface circuit, CPU circuit, and Display/Control panel are provided to aid in determining signal direction and tracing. A solid arrow (⟶) on the signal line indicates direction, and the tracing of the signal through the schematics is referenced as it leaves the page. The reference is shown as a number - letter number (e.g. 2-A3), indicating sheet 2 and schematic zone A3. The reference may be shown alone or in a bracket. If the reference is bracketed, the signal is going to another schematic which is referenced outside the bracket. If the reference is shown alone, the signal is going to another page of the multisheet schematic.

3-5. 8800b BLOCK DIAGRAM DESCRIPTION (Figure 3-1)

The 8800b computer contains four basic circuits; the Central Processing Unit (CPU), Memory, an Input/Output (I/O) section, and the Front Panel. The CPU controls the interpretation and execution of software instructions, and Memory stores the software information to be used by the CPU. The I/O section provides a communication link between the CPU and external devices. The Front Panel allows the operator to manually perform various operations with the 8800b. The 8800b basic block diagram and accompanying text (paragraphs 3-6 and 3-7) explain the CPU's communication with the memory (and I/O) circuits and with the front panel. The system clock, power-on operation and run operation are explained in paragraphs 3-8 through 3-10.

3-6. CPU TO MEMORY OR I/O OPERATION

The Memory or I/O section operation repuires several signals that allow transfer of data to and from the CPU. The ADDRESS bus (AØ-A15) consists of sixteen individual lines from the CPU to Memory and I/O devices. The signals on this bus represent a particular

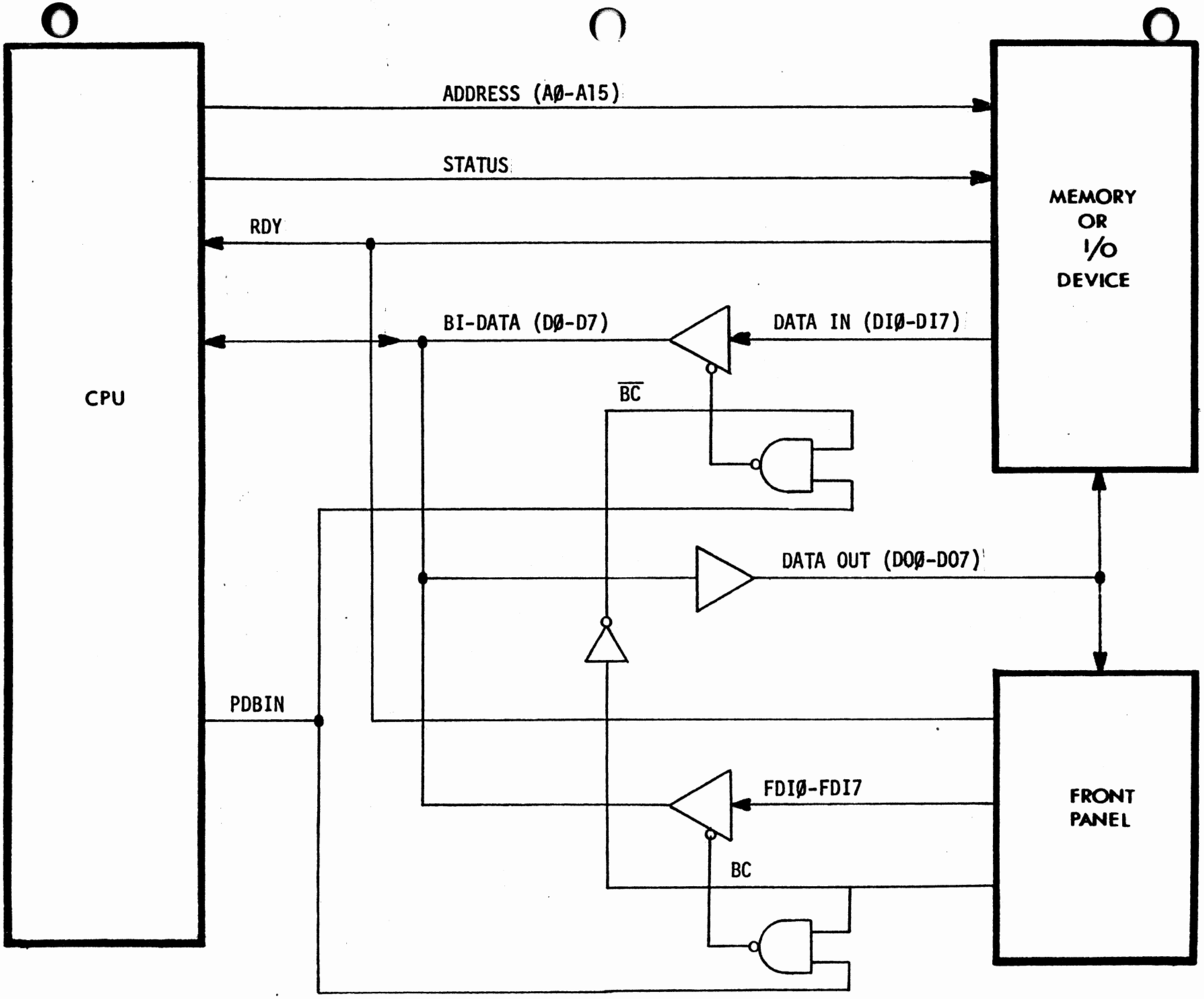


Figure 3-1. 8800b Basic Block.

memory address location or external device number that is needed to establish communications with Memory or I/O devices. Once the address data (A0-A15) is presented to Memory or I/O devices, the CPU generates various STATUS signals. The STATUS signals enable decoding of a memory address or conditions the I/O device card to send or receive data from the CPU

Data from Memory or I/O devices is presented on the DATA IN lines (DIØ-DI7) and applied to eight non-inverting bus drivers. The drivers are enabled by a PDBIN signal from the CPU and a $\overline{BC}$ (bus control) signal. The BC signal is LOW when the Front Panel is not in operation. The eight non-inverting bus drivers, when enabled, present the input data to BI-DATA lines (DØ-D7) which input the data to the CPU.

Data outputted to Memory or I/O devices is presented to the DATA OUT lines (DOØ-DO7) from the CPU. The RDY (ready) line either forces the CPU to a wait state while data is being transferred or allows the CPU to process data.

3-7. FRONT PANEL OPERATION

The Front Panel Operation is very similar to Memory or I/O section operation. The Front Panel gains control of the CPU by producing a HIGH BC signal. The BC signal disables the DATA IN (DIØ-DI7) lines from a Memory or I/O Device and enables the FDIØ-FDI7 lines. The FDIØ-FDI7 lines contain Front Panel data which is transferred to the CPU upon the occurence of the PDBIN signal. All data from the CPU to the Front Panel is applied to the DATA OUT (DOØ-DO7) lines and displayed on the Front Panel.

3-8. SYSTEM CLOCK

The system clock (F) for the 8800b is located on the CPU circuit card (Figure 3-14, zone B7). The system clock generates phase 1 and phase 2 outputs derived from the external crystal (XTAL 1). The Ø1 and Ø2 outputs operate at a frequency of 2 MHz, which determines the speed at which the 8080 (M) will operate. The Ø1 and Ø2 clock signals are presented to the bus (zone A7) through inverter A and inverter bus driver J, respectively. The Ø1 clock is used by memory and external I/O cards, and the Ø2 clock is applied to the 24-bit counter on the Display/Control card (Figure

3-16, sheet 1, zone D2) through the Interface card (Figure 3-15, sheet 2, zone B3).

3-9. POWER ON CLEAR OPERATION

Positioning the ON/OFF switch to ON causes a power on clear (POC) operation to be performed, resetting the 8800b circuitry. The POC signal is generated on the CPU card (Figure 3-14, zone A3) when VCC is applied. With VCC present, capacitor C4 will charge to the VCC potential in 100 milliseconds because of the RC time constant of C4 and resistor R17. The 100 millisecond delay disables (turns off) transistor Q3, producing a LOW $\overline{POC}$ signal to the bus (pin 99) through inverters S and J (zone A2). The $\overline{POC}$ signal is inverted by U on the Interface card (Figure 3-15, sheet 2, zone B2) and presented to the Display/Control card as a HIGH POC signal (Figure 3-16, sheet 2, zone D6). The POC input is inverted LOW by T1 (zone C6) and applied to three circuits on the Display/Control Card. It clears the M1 flip-flops (zone C7) through NOR gate T1 and inverter J1 (zone C6), insuring that single step operation is disabled. It presets the M1 flip-flop (zone C9) and disables NAND gate P1 (zone B8) to insure that the 8800b is not running. The $\overline{POC}$ signal (zone D9) is also present at NOR gate R1 which inverts it HIGH to reset the PROM counter. The $\overline{POC}$ signal is present to the external input/output (I/O) cards and memory for similar initialization operations. During the POC operation, two other functions are being performed.

On the Display/Control card (Figure 3-16, sheet 1, zone D2), a 24-bit counter is being clocked by Ø2 which will condition circuits on the Display/Control card. The $\overline{C13}$ output (zone D1) from the counter is applied to the clock (CK) input of quad latches C1, F1, H1, G1, N1, U1, Y1, and W1 (zones B9-B1) through non-inverting bus driver K1 (zones A1 and D1) and inverter J1 (zone C1). The $\overline{C13}$ signal clears the quad latches in the following manner to insure all latches are conditioned after POC. The inputs to quad latches C1, F1, H1, and G1 are HIGH because no switches are activated. After the first $\overline{C13}$ clock, all the $\overline{Q}$ outputs are LOW and applied to the inputs of quad latches N1, U1, Y1, and W1 (zones B9-B1).

The occurrence of the next C13 clock latches the Q outputs LOW and the $\overline{Q}$ outputs HIGH during the POC operation.

When VCC is present in the CPU circuits, another RC time constant affects the clock generator F (Figure 3-14, zone B7). Capacitor C2 will charge to the VCC potential in 33 microseconds which is the time constant of C2 and resistor R10. The 33 microsecond delay allows the RESET output from F (zone B7) to clear the 8080 M internal circuits. The 8080 remains in this state because the READY output (zone B7) is LOW from F. The READY output from F will be affected during the run operation.

3-10. RUN OPERATION

The Run Operation allows the 8080 on the CPU Board to start processing data to and from memory and external devices. The Run Operation is activated when the RUN/STOP switch on the 8800b front panel is momentarily depressed to RUN.

The RUN/STOP circuits are located on the Display/Control card (Figure 3-16, sheet 2, zone A9). When the RUN/STOP switch is momentarily depressed, a LOW is applied to quad latch C1, input D2. The occurrence of the next C13 clock (zone A1) causes the $\overline{Q}$ output at pin 6 of C1 (zone B9) to go HIGH. This HIGH is applied to quad latch N1, input D2. The next C13 clock causes the Q output at pin 2 of N1 (zone B9) to go HIGH and allows NAND gate P1 to clear M1 (zone C9). The Q output of M1 generates a LOW $\overline{RUN}$ signal and LOW $\overline{FRDY}$ signal through NOR gate P1 and inverter R1 (zone D9).

The $\overline{RUN}$ signal is applied to the Interface Card (Figure 3-15, sheet 2, zone D2) to condition the MD input of data latch G (sheet 3, zone A6). With MD enabled, output data from the CPU can be displayed on the 8800b front panel if a STB input is present to G (discussed in Paragraph 3-40).

The $\overline{FRDY}$ signal is applied to the Interface Card (Figure 3-15, sheet 2) to allow the 8080 to start processing data. The FRDY output is applied to pin 58 of the bus through inverter R and non-inverting bus driver H as a HIGH (zone A1). The HIGH on pin 58 of the bus enables NAND gate C, pin 8, LOW on the CPU (Figure 3-14, zone A7) which is inverted HIGH by B (zone B7) and applied

to the clock generator F RYDIN input. The RYDIN signal enables the READY output at F HIGH (zone B7) which allows the 8080 M (zone A8) to start processing data.

3-11. 8800b DATA PROCESSING OPERATION

The 8800b data processing begins when the 8080 IC is enabled (Paragraph 3-10). With the 8080 IC enabled, the program (P) counter in the 8080 starts to increment or begins at a predetermined count established by the operator. The count in the P counter represents a location in memory which is examined by the CPU before the P counter increments to the next location. To examine each memory location, the CPU initiates an instruction cycle operation. Every instruction cycle consists of one, two, three, four, or five machine cycles. In order to perform a data processing operation, basic machine cycles are required.

The Instruction Fetch Machine cycle is a basic machine cycle needed to allow the CPU to fetch an instruction from memory. A memory read machine cycle is also a basic machine cycle that enables the CPU to communicate with a memory or external device for data transfer operations.

The following paragraphs discuss data transfers from an external device to the CPU, from the CPU to memory, from memory to the CPU, and from the CPU to an external device. However, the instruction fetch and memory read machine cycles used in the data transfers are discussed first because their operation is identical in all of the data transfers. It is important to note that there are many variations of data transfer which are dependent on the programmer.

3-12. INSTRUCTION FETCH CYCLE

The Instruction Fetch Cycle is the first machine cycle (M1) to be performed by the CPU in any data transfer operation. The memory location specified by the P counter contains data that the CPU interprets as an instruction. The first cycle must be a fetch cycle because, during the fetch cycle, the CPU is informed as to what operation will be performed next.

3-13. INSTRUCTION FETCH CYCLE OPERATION (Figure 3-2)

The Instruction Fetch Cycle is initiated whenever the P counter is incremented to a new memory address location (e.g. 000 100_8) where an instruction (e.g. 072_8) is stored. In order to fetch the 072_8 data from memory during machine cycle one, several signals are generated by the CPU.

A PSYNC output from the CPU is applied to memory to condition for address decoding. Next the ADDRESS (000 100_8), consisting of sixteen parallel outputs (AØ-A15) from the CPU, is presented to the Display/Control Card and memory. The AØ through A15 signals drive the appropriate address buffers, illuminating the light emitting diodes (LEDs) on the Display/Control Card. The ADDRESS and PSYNC signals present at the memory from the CPU initiate decoding of the memory address (000 100_8).

The CPU then generates three signals, SM1, SMEMR, and Ø1 CLOCK to complete the Instruction Fetch Cycle. The SM1 output is applied to the Display/Control Card through the Interface Card to light the M1 (machine cycle 1) LED on the 8800b front panel. The SMEMR and Ø1 CLOCK outputs are applied to memory to allow decoding of the memory address (000 100_8). With the memory address decoded, the 072_8 data present in that location is transferred to the CPU on the eight DATA IN (DIØ-DI7) lines. The DIG 1 input to the CPU from the Interface Card is enabled when the 8800b is in the run mode (see paragraph 3-10). This permits the memory data to be transferred to the CPU. The SMEMR output is applied to the Display/Control Card through the Interface Card to light the MEMR (memory read) LED on the 8800b front panel. This operation is performed when the P counter is incremented, indicating a new memory address.

3-14. INSTRUCTION FETCH CYCLE DETAILED OPERATION

The following paragraphs describe the Instruction Fetch Cycle operation in detail. Refer to Figure 3-3, Instruction Fetch Cycle Timing, during the explanation. The Instruction Fetch Cycle operation (M1) requires four Ø1 and Ø2 clock pulses. Each clock period performs a particular operation as described in the following paragraphs.

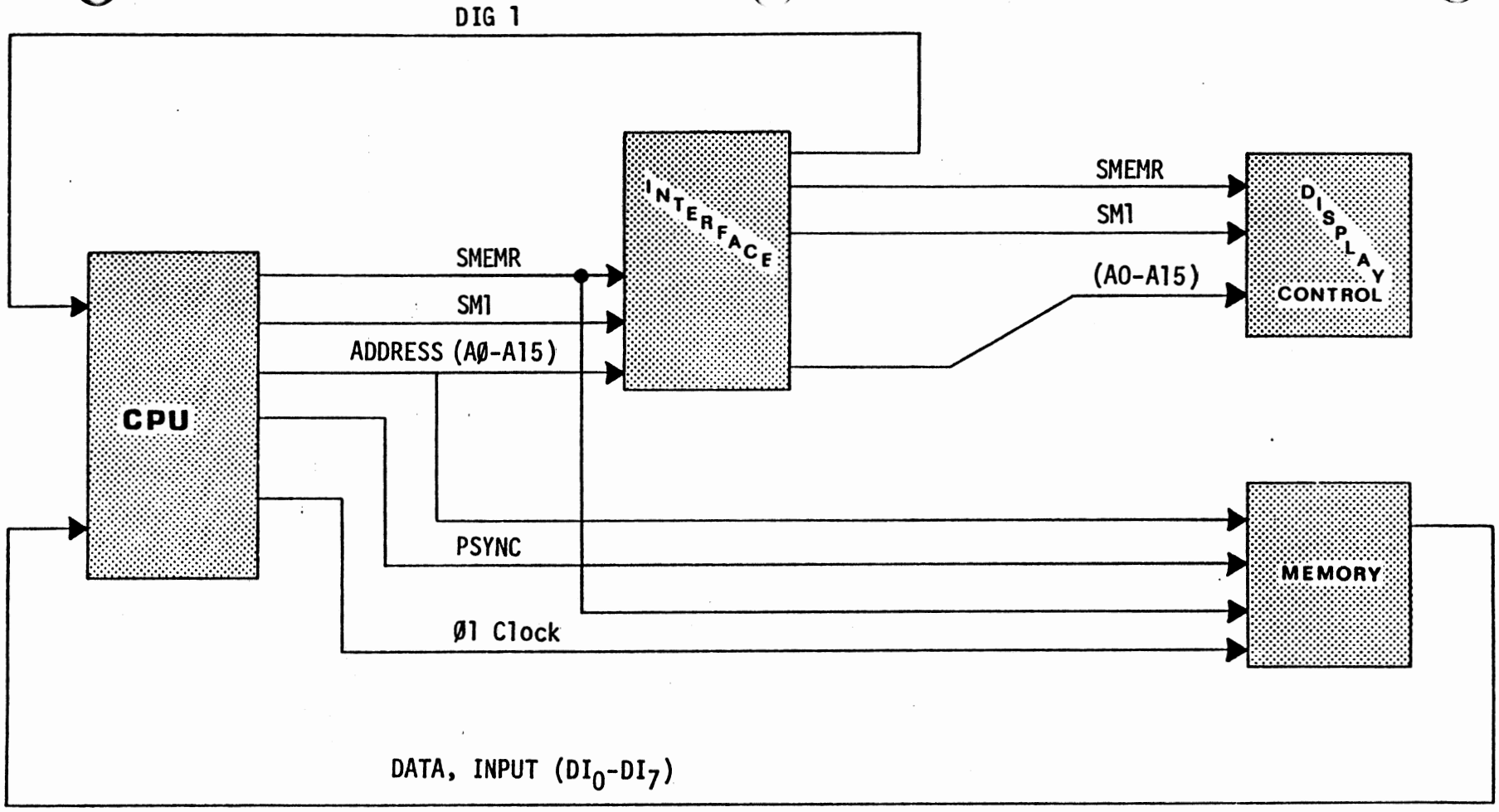


Figure 3-2. Instruction Fetch Cycle Block Digaram

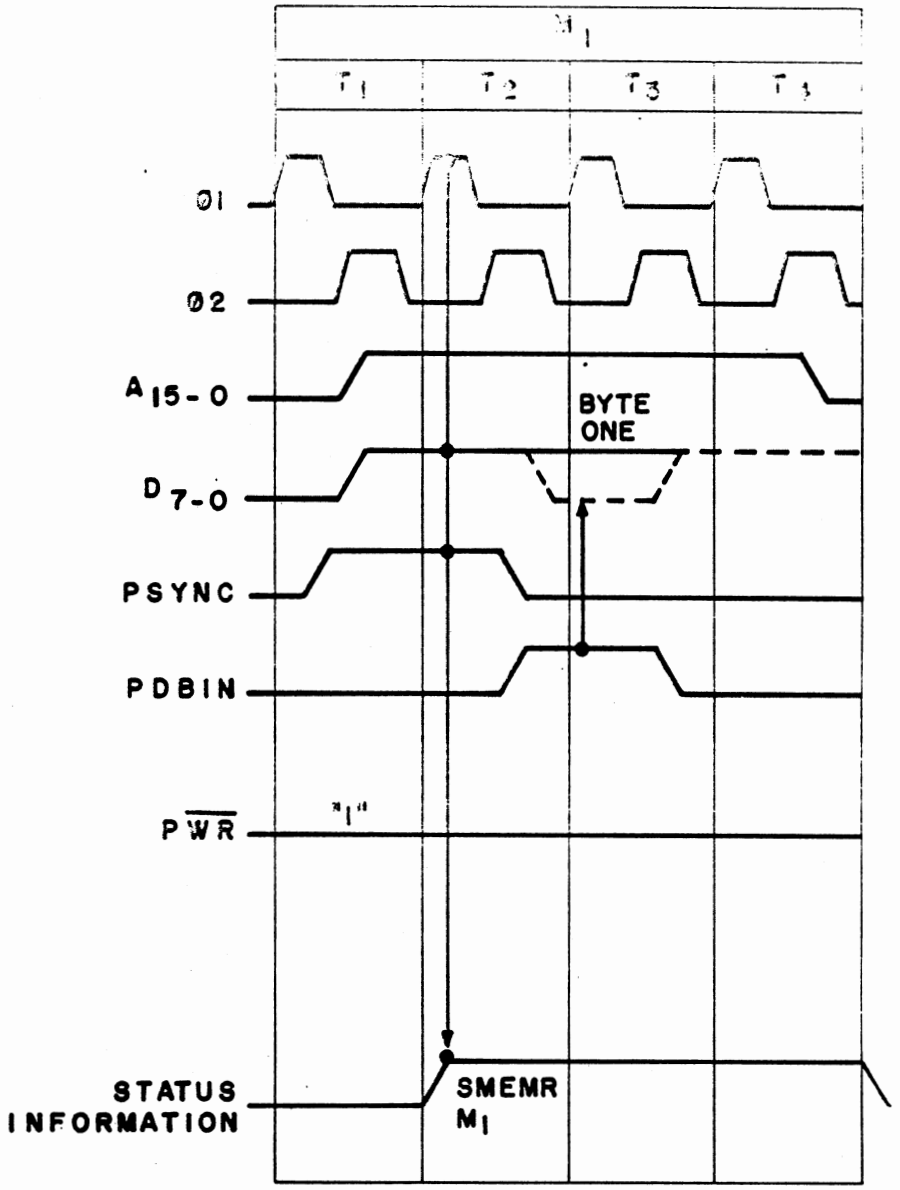


Figure 3-3. Instruction Fetch Cycle Timing.

During the latter portion of T1, several outputs are generated by the CPU (M) (Figure 3-14): address data AØ through A15 (zone B8). status data DØ through D7, and a SYNC signal (zone C8). The AØ through A15 data is applied to memory via the bus through non-inverting bus drivers, U, P, and N (zone B9) on the CPU. The address data (AØ-A15) is also applied through inverters P, N, and X on the Interface card (Figure 3-15, sheet 1, zone B5) and presented to the Display/Control card. The AØ through A15 signals present on the Display/Control card light the appropriate AØ through A15 LEDs, indicating the memory address.
The DØ through D7 data is applied to K (zone B5) on the CPU through the bi-directional circuits D and E. The status data is enabled through D and E at this time because $\overline{CS}$ and $\overline{DIEN}$ are LOW. The SYNC output is applied to the clock generator F (zone B7) and memory as PSYNC via pin 76 (zone D1) on the bus through the non-inverting bus driver V (zone D8). The PSYNC signal conditions memory to decode the address data. The SYNC input at F will enable a signal during T2.

During the beginning of T2, a low $\overline{STSTB}$ (zone B7) is generated from F as a result of the HIGH SYNC input and internal timing of F. The $\overline{STSTB}$ is applied to the data latch K (zone B5), allowing the status data DØ through D7 to be stored in K. The status data present at the output of K conditions the memory to fetch the instruction (072_8) from its addressed memory location (e.g. 000 100_8) by enabling the following signals.

A SM1 and SMEMR HIGH output from K is presented on pins 44 and 47 of the bus (zone A5) through non-inverting bus drivers X and R. The SM1 and SMEMR signals are applied through inverter V on the Interface card (Figure 3-15, sheet 2, zone B5) and presented to the Display/Control card as $\overline{SM1}$ and $\overline{SMEMR}$. The $\overline{SM1}$ and $\overline{SMEMR}$ signals present on the Display/Control card light the M1 and MEMR LEDs (Figure 3-16, sheet 3, zone C3) on the front panel of the 8800b, indicating machine cycle one is performing a memory read operation. The SMEMR output from the CPU (Figure 3-14, zone A5) is applied to memory, initiating a data transfer to the CPU during T3.

At the beginning of T3, the instruction (072_8) data is transferred from memory to M on the CPU. The memory data (DI0 through DI7) is supplied to the CPU card (Figure 3-14, zone B1) from the bus. The data is presented to M through bi-directional gates D and E (zone C7), inverter bus drivers L and J (zone B4), and inverters Y and S (zone B3) by the DBIN signal.

At the latter portion of T2 and the beginning of T3, a high DBIN output (zone C8) is generated by M. The DBIN output is applied to the $\overline{\text{DIEN}}$ inputs (zone C7) of D and E and pin 4 of NAND gate C (zone B4) as PDBIN. This signal enables pin 6 of NAND gate C LOW (DIG1 is high when the front panel is not used). This allows data input from memory (DIØ-DI7) to be enabled through inverting bus drivers L and J (zone B4) and applied through bi-directional gates D and E to M (zone C7).

Clock period T4 of machine cycle one allows for 8080 processing of the received instruction data from memory. If the instruction data present in the CPU requires a data transfer to or from an external device, a memory read cycle (M2) is initiated. However, if the instruction data present in the CPU requires a data transfer to or from memory, two memory read cycles (M2 and M3) are initiated.

3-15. MEMORY READ CYCLE

The Memory Read Cycle (M2) follows the Instruction Fetch Cycle (M1). During a Memory Read Cycle, an address is transferred to the CPU from memory. This address is either an external device number or a memory location (depending upon the instructions received during M1).

3-16. MEMORY READ CYCLE OPERATION (Figure 3-4)

The CPU performs one or two Memory Read Cycle operations. If the CPU is to communicate with an external device, one Memory Read Cycle is required because the external device number consists of 8 data

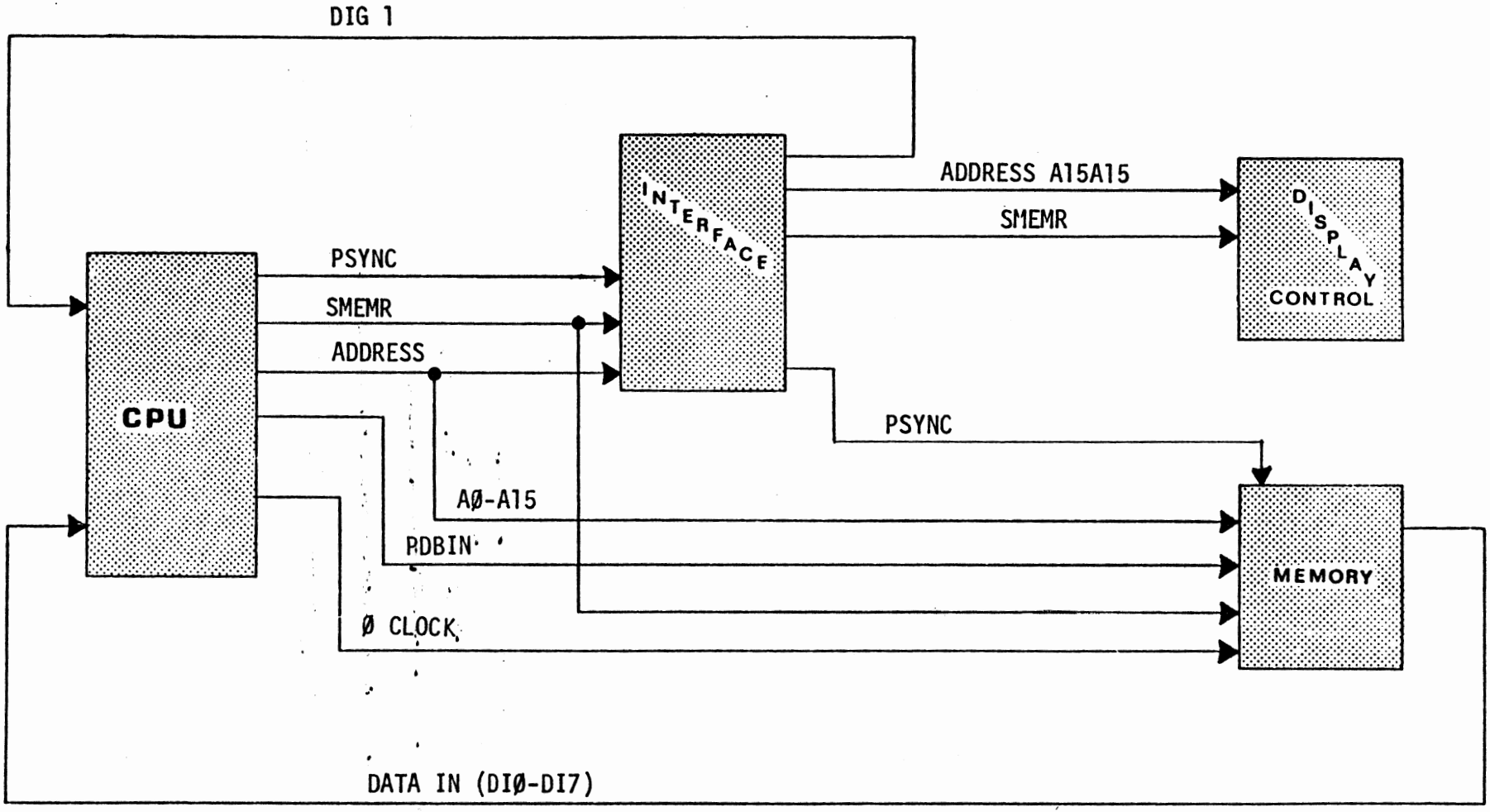


Figure 3-4. Memory Read Cycle Block Diagram

bits (1 byte). However, if the CPU is instructed to communicate with memory, two Memory Read Cycles are required because the memory address consists of 16 data bits (2 bytes).

The two Memory Read Cycles obtain the memory address (e.g. 000 200_8) that is required by the CPU to complete the instruction. Since one byte (8 bits) of the two byte address is transferred during one Memory Read Cycle, two cycles are required. The first Memory Read Cycle obtains the least significant bits (LSBs) of the address (200_8) from memory and stores them in the CPU. The second cycle obtains the most significant bits (MSBs) of the address (000_8) from memory and stores them in the CPU.

The Memory Read Cycles are very similar to the Instruction Fetch Cycle. They require a memory address location (e.g. 000 101_8 and 000 102_8) that indicates where the LSBs and MSBs of the address (000 200_8) are stored. After completion of the Instruction Fetch Cycle, the program counter in the CPU is incremented to 000 101_8 and the first Memory Read Cycle is initiated. Several signals are generated by the CPU in order to read the LSBs of the address (200_8) from memory.

A PSYNC output from the CPU is applied to memory through the Interface Card to condition the memory for address decoding. Next the ADDRESS (000 101_8), consisting of sixteen parallel outputs (AØ-A15) from the CPU, is presented to the Display/Control Card and memory. The AØ through A15 signals light the appropriate address light emitting diodes (LEDs) on the Display/Control Card. The ADDRESS and PSYNC signals present at the memory from the CPU initiate decoding of the address (000 101_8).

The CPU then generates three signals, SMEMR, PDBIN, and Ø1 to complete the Memory Read Cycle. The SMEMR, PDBIN, and Ø1 outputs are presented to memory to enable decoding of the address (000 101_8). With the address decoded, the 200_8 data present in that location is transferred to the CPU on the eight DATA IN (DIØ-DI7) lines. The DIG1 input to the CPU from the Interface Card is enabled when the 8800b is in the run mode, permitting memory data to be transferred to the CPU.

The SMEMR output is presented to the Display/Control Card through the Interface Card to light the MEMR (memory read) LED on the 8800b front panel. The second Memory Read Cycle operation is identical to the first. It transfers the MSBs of the address (000_8) to the CPU.

3-17. MEMORY READ CYCLE DETAILED OPERATION

The following paragraphs describe the Memory Read Cycle operation in detail. Refer to Figure 3-5, Memory Read Cycle Timing, during the explanation.

The two Memory Read Cycle operations (M2 and M3) obtain the memory address (e.g. 000 200_8) required by the CPU to complete an instruction. As stated previously, the LSBs of the address (200_8) are transferred to the CPU during M2, and the MSBs of the address (000_8) are transferred to the CPU during M3. There are three clock periods (T1-T3) required for each Memory Read Cycle operation.

During the latter portion of T1, several outputs are generated by the CPU (Figure 3-14); Address data AØ through A15 (zone B8), status data DØ through D7, and a SYNC signal (zone C8). The AØ through A15 data is presented to memory and the 8800b front panel via the bus through non-inverting bus drivers U, P, and N (zone B9) on the CPU. The DØ through D7 data is applied to K (zone B5) on the CPU through the bi-directional circuits D and E. The status data is enabled through D and E at this time because $\overline{CS}$ and $\overline{DIEN}$ are LOW. The SYNC output is applied to the clock generator F (zone B7) and memory as PSYNC via pin 76 (zone D1) on the bus through non-inverting bus driver V (zone D8). The PSYNC signal conditions memory to decode the address data.

During the beginning of T2, a $\overline{STSTB}$ (zone B7) is generated (LOW) from F as a result of the HIGH SYNC input and internal timing of F. The $\overline{STSTB}$ is applied to the data latch K (zone B5), allowing the status data DØ through D7 to be stored in K. The status data present at the output of K allows the CPU to read the LSBs of the memory address

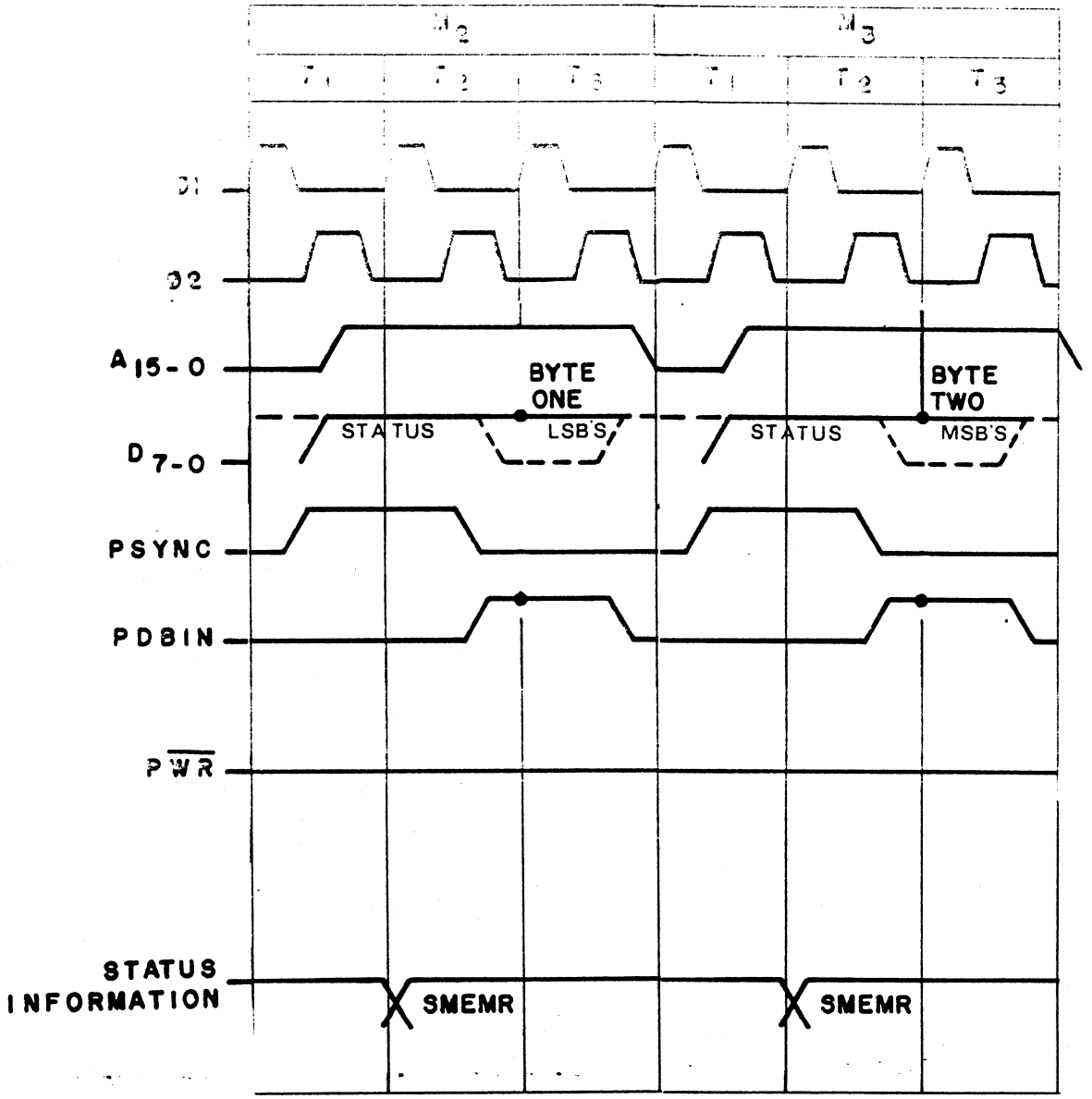


Figure 3-5. Memory Read Cycle Timing.

location (ex. 000 101_8) by enabling the SMEMR signal.

A SMEMR output (HIGH) from K is presented on pin 47 of the bus (zone A4) through non-inverting bus drivers X and R. The SMEMR signal is applied through inverter V on the Interface Card (Figure 3-15, zone B4) and presented to the Display/Control card as $\overline{\text{SMEMR}}$. The $\overline{\text{SMEMR}}$ signal present on the Display/Control card lights the MEMR LED (Figure 3-16, zone C3) on the front panel of the 8800b, indicating a memory read operation is occurring. The SMEMR output from the CPU (Figure 3-14, zone A5) is applied to memory in order to initiate a data transfer to the CPU during T3.

At the beginning of T3, the LSBs of the memory storage location (200_8) are transferred from memory to the 8080 (M) on the CPU. The memory data in (DIØ through DI7) is applied to the CPU card (Figure 3-14, zone B1) from the bus. The data is presented to M through bi-directional gates D and E (zone C7), inverter bus drivers L and J (zone B4), and inverters Y and S (zone B3) by the PDBIN signal.

At the latter portion of T2 and the beginning of T3, a DBIN output (zone C8) HIGH is generated by M. The DBIN output is applied to the $\overline{\text{DIEN}}$ inputs (zone C7) of D and E and pin 4 of NAND gate C (zone B4) as PDBIN. This signal enables pin 6 of NAND gate C LOW (DIG 1 is high when front panel is not used). This allows the data in from memory (DIØ - DI7) to be enabled through inverting bus drivers L and J (zone B4) and applied through bi-directional gates D and E to M (zone C7). The second Memory Read Cycle operation (M3) transfers the contents of memory address (000 102_8) which contain the MSBs of the memory address number to the CPU. It is important to note that only one Memory Read Cycle operation is required if the CPU is to communicate with an external device.

3-18. EXTERNAL DEVICE TO CPU DATA TRANSFER

An External Device to CPU data transfer is accomplished when an input instruction (333_8) is fetched from a memory location during M1, and the external device number (XXX_8) is read from a memory location during M2 by the CPU. The data from the external device is transferred to the CPU by an Input Read Cycle operation (M3).

3-19. INPUT READ CYCLE OPERATION (Figure 3-6)

The Input Read Cycle operation will allow the CPU to obtain data from an external device. After the completion of the Memory Read Cycle (M2), the program counter is not incremented until the completion of the Input Read Cycle. Several signals are generated by the CPU in order to obtain data from the external device.

The SINP output and external device ADDRESS (XXX_8) number, consisting of the first eight individual outputs (AØ-A7) from the CPU, is presented to the external device input/output channel, thereby enabling the I/O card. With the I/O enabled, a PDBIN signal from the CPU allows the I/O to transfer the external device data to the CPU on the eight DATA IN (DIØ-DI7) lines for storage. The DIG 1 input to the CPU from the Interface is enabled during the 8800b run mode and allows the external device data to be stored in the CPU. The SINP and AØ through A15 outputs are supplied to the Display/Control Card through the Interface Card to illuminate the INP (input) and ADDRESS LEDs on the 8800b front panel.

3-20. INPUT READ CYCLE DETAILED OPERATION

The following paragraphs describe the Input Read Cycle operation in detail. Refer to Figure 3-7, Input Read Cycle Timing, during the explanation. The Input Read Cycle operation (M3) requires three Ø1 and Ø2 clock pulses. During each clock period, a specific operation is performed as described in the following paragraphs.

During the latter portion of T1, several outputs are generated by the CPU (Figure 3-14); address data AØ through A15 (zone B8), status data DØ through D7, and a SYNC signal (zone C8). The AØ through A15 data contains the external device number (AØ-A7 and A8-A15 contain identical data) and is applied to the I/O card via the bus through non-inverting bus drivers U, P, and N (zone B9) on the CPU in order to enable the I/O card. The address data (AØ-A15) is also applied through inverters P, W, and X on the Interface Card (Figure 3-15, sheet 1, zone B5) and

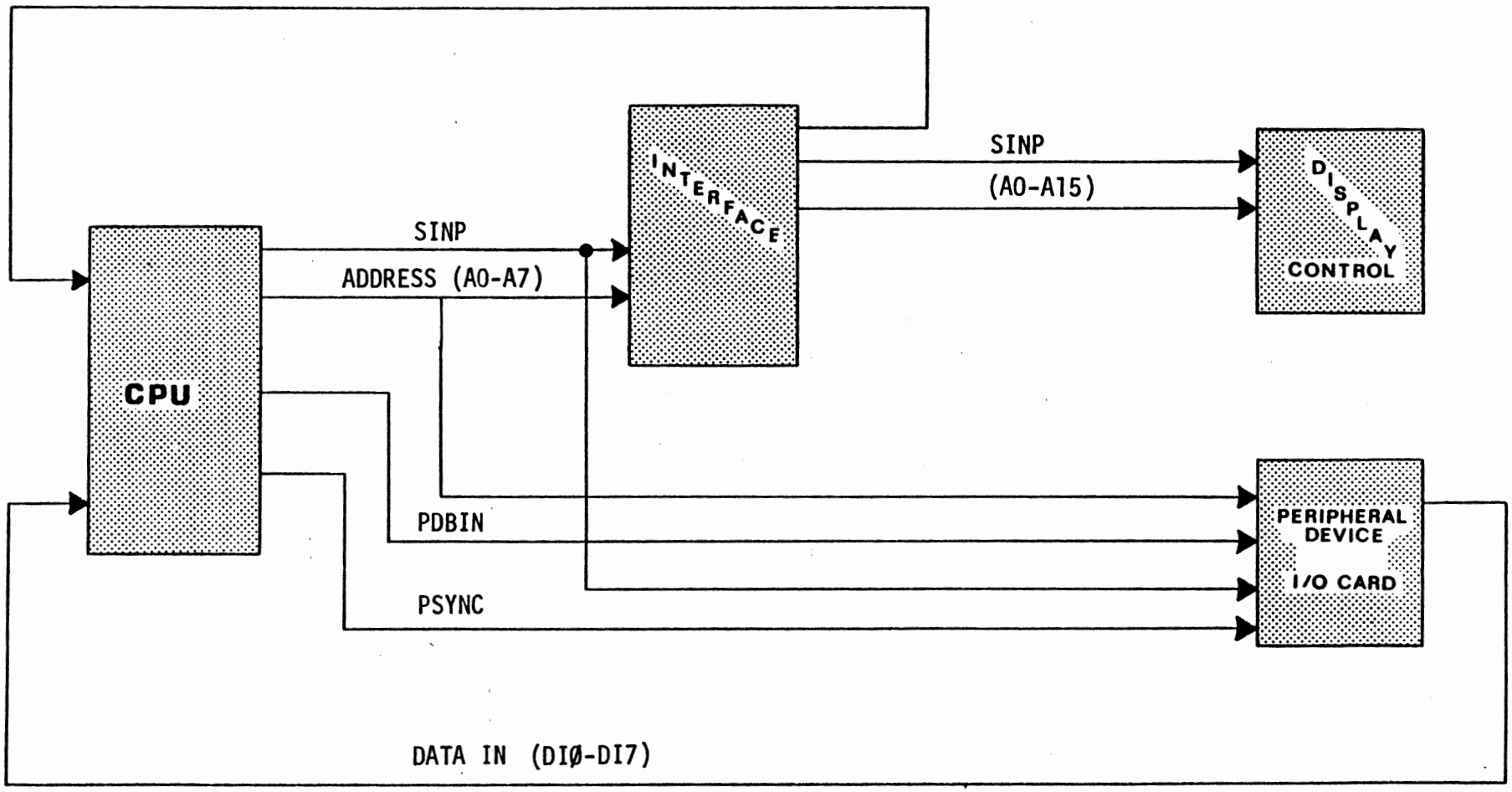


Figure 3-6. Input Read Cycle Block Diagram

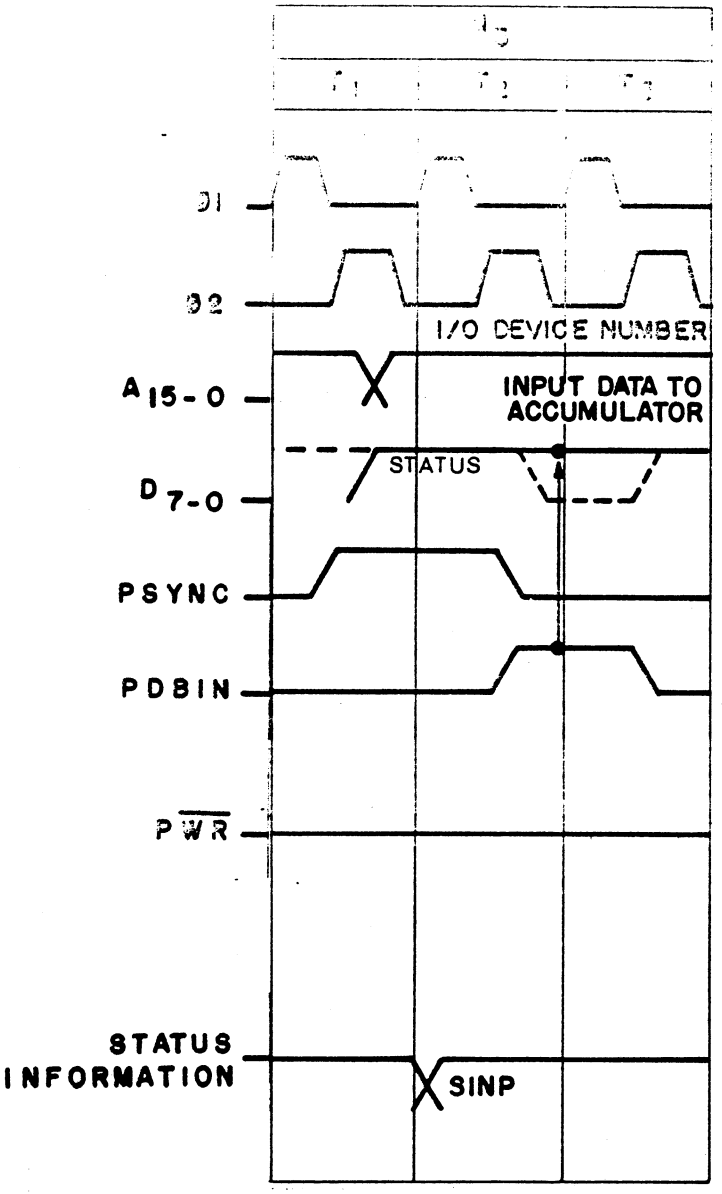


Figure 3-7. Input Read Cycle Timing.

presented to the Display/Control card. The AØ through A15 signals present on the Display/Control card (Figure 3-16, sheet 3, zone A9-A4) light the appropriate AØ through A15 LEDs, indicating the address of the external device. (Recall that when addressing an I/O device, the address is repeated on the upper eight and lower eight address LEDs.) The DØ through D7 data is applied to K (Figure 3-14, zone B5) on the CPU through the bi-directional circuits D and E. The status data is enabled through D and E at this time because $\overline{CS}$ and $\overline{DIEN}$ are LOW. The SYNC output is applied to the clock generator F (zone B7), conditioning F to generate a signal during T2.

At the beginning of T2, a $\overline{STSTB}$ (zone B7) is generated LOW from F as a result of the HIGH SYNC input and internal timing of F. The $\overline{STSTB}$ is applied to the data latch K (zone B5), allowing the status data DØ through D7 to be stored into K. The status data present at the output of K conditions the I/O card to send data to the CPU by enabling the SINP signal.

A SINP output from K is presented HIGH on pin 46 of the bus (zone A4) through non-inverting bus driver R. The SINP signal is applied through inverter V on the Interface Card (Figure 3-15, sheet 2, zone B5) and presented to the Display/Control card as $\overline{SINP}$. The $\overline{SINP}$ signal present on the Display/Control card lights the INP LED (Figure 3-16, sheet 3, zone C3) on the front panel of the 8800b, indicating data is being received from an external device. The SINP output from the CPU is applied to the external device I/O card in order to initiate a data transfer to the CPU during T3.

At the beginning of T3, the external device data is transferred to M on the CPU via the bus. The external device data in (DIØ through DI7) is applied to the CPU card (Figure 3-14, zone B1) from the bus. The data is presented to the 8080 (M) through bi-directional gates D and E (zone C7), inverter bus drivers L and J (zone B4), and inverters Y and S (zone B3) by the PDBIN signal.

At the latter portion of T2 and the beginning of T3, a DBIN output (zone C8) HIGH is generated by M. The DBIN output is applied to the $\overline{DIEN}$ inputs (zone C7) of D and E, pin 4 of NAND gate C (zone B4) and the bus pin 78 (zone D1) as PDBIN. This

signal enables pin 6 of NAND gate C LOW (DIG 1 is HIGH when the front panel is not used), allowing the data input from the I/O card (DIØ-DI7) to be enabled through inverting bus drivers L and J (zone B4) and applied through bi-directional gates D and E to M (zone C7). The data at the external device is presented on the bus by the occurrence of PDBIN. After the external device data is stored in the CPU, the P counter is incremented, thus ending the Input Read Cycle operation.

3-21. CPU TO MEMORY DATA TRANSFER

A CPU to Memory data transfer is accomplished whenever an instruction is encountered to perform this operation. For example, a store accumulator STA (062_8) instruction requires the accumulator in the CPU to transfer its contents to memory. The STA instruction is fetched during M1 and its storage location determined in memory read cycles M2 and M3. The accumulator data is transferred to memory by a Memory Write Cycle operation (M4).

3-22. MEMORY WRITE CYCLE BASIC OPERATION (Figure 3-8)

The Memory Write Cycle operation will allow the CPU to transfer data to the memory. Several signals are generated by the CPU in order to transfer data to the memory.

The $\overline{\text{SWO}}$ output from the CPU is applied to the Display/Control through the Interface to light the WO (write out) LED on the 8800b front panel. The ADDRESS (XXX XXX_8), consisting of fifteen individual outputs (AØ-A15) from the CPU, is presented to the Display/Control and memory. The AØ through A15 signals light the appropriate address LEDs on the Display/Control. The ADDRESS and PSYNC signals present at the memory from the CPU can also initiate decoding of the memory address. With the memory conditioned, eight DATA OUT lines (DOØ-DO7) transfer the CPU data to the memory for storage. The $\overline{\text{PWR}}$ and $\overline{\text{SOUT}}$ outputs from the CPU are applied to the Interface to produce a MWRITE signal which allows the memory to store the data.

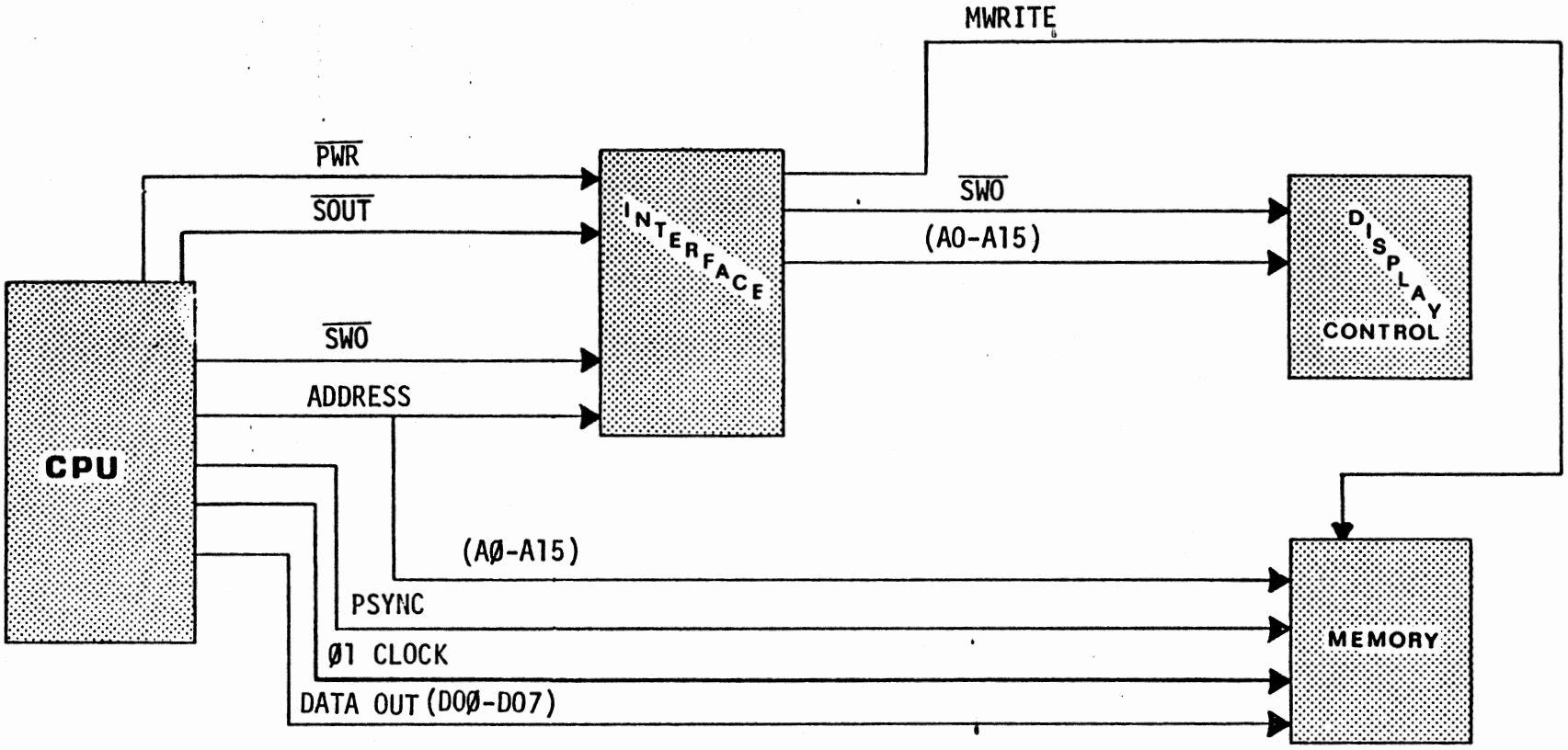


Figure 3-8. Memory Write Cycle Block Diagram

3-23. MEMORY WRITE CYCLE DETAILED OPERATION

The following paragraphs describe the Memory Write Cycle operation in detail. Refer to Figure 3-9, Memory Write Cycle Timing, during the explanation. The Memory Write Cycle operation (M4) requires three Ø1 and Ø2 clock pulses. Each period performs a certain operation as described in the following paragraphs.

During the latter portion of T1, several outputs are generated by the CPU 8080 IC (Figure 3-14); Address data AØ through A15 (zone B8), status data DØ through D7, and a SYNC signal (zone C8). The AØ through A15 data contains the memory storage location address (ex. 000 200_8) which is applied to the memory card via the bus through non-inverting bus drivers U, P, and N (zone B9) on the CPU in order to enable the memory. The address data (AØ-A15) is also applied through inverters P, W, and X on the Interface Card (Figure 3-15, sheet 1, zone B5) and presented to the Display/Control card. The AØ through A15 signals present on the Display/Control card (Figure 3-16, sheet 3, zones A9-A5) light the appropriate AØ through A15 LEDs, indicating the memory location address. The DØ through D7 data is applied to K on the CPU (Figure 3-14, zone B5) through the bi-directional circuits D and E. The status data is enabled through D and E at this time because $\overline{CS}$ and $\overline{DIEN}$ are LOW. The SYNC output is applied to the clock generator F (zone B7), conditioning F to generate a signal during T2.

During the beginning of T2, a LOW $\overline{STSTB}$ (zone B7) is generated from F as a result of the HIGH SYNC input and internal timing of F. The $\overline{STSTB}$ is applied to the data latch K (zone B5) allowing the status data DØ through D7 to be stored into K. The status data present at the output of K indicates a write output operation is being performed. However, the distinction of whether the data from the CPU is being transferred to a memory or an external device is determined by the status of the SOUT signal (zone A5). During a Memory Write Cycle, the SOUT signal is LOW and applied to the Interface Card (Figure 3-15, sheet 2). The SOUT signal is inverted HIGH by V and applied to pin 2 of NAND gate A (zone C3).

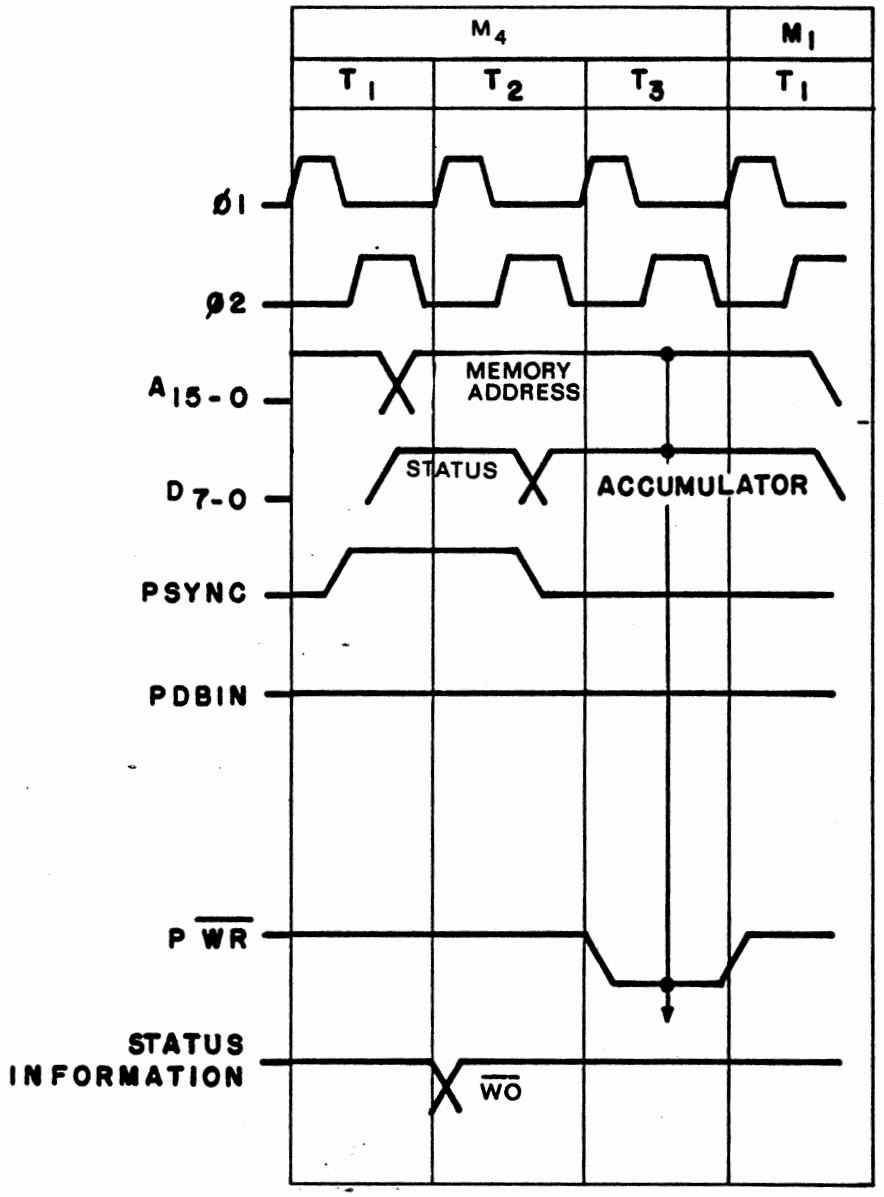


Figure 3-9. Memory Write Cycle Timing.

The $\overline{SWO}$ output from K is presented on pin 97 of the bus (zone A4) through non-inverting bus driver X as a LOW. The SWO signal is applied through inverter M on the Interface Card (Figure 3-15, sheet 2, zone B6) and presented to the Display/ Control card as SWO. The SWO signal present on the Display/ Control card lights the WO LED (Figure 3-16, zone C3) on the front panel of the 8800b, indicating data is being transferred to memory from the CPU.

At the beginning of T3, the CPU data is transferred to the memory via the bus. The CPU data out (DOØ through DO7) is applied to the bus (zone C1) through bi-directional gates D and E ($\overline{CS}$ and $\overline{DIEN}$ are LOW) and non-inverting bus drivers M and W (zones C7 and C3). The bus data is presented to memory and written in by the MWRITE signal.

After the CPU data is settled on the bus and presented to memory, a $\overline{WR}$ signal (zone C8) is generated LOW by M. The $\overline{WR}$ signal is applied to pin 77 (zone D1) of the bus through non-inverting bus driver V (zone D8) as $\overline{PWR}$. The $\overline{PWR}$ signal is inverted HIGH by U on the Interface Card (Figure 3-15, sheet 2, zone B3) and applied to pin 1 of NAND gate A (zone C3), enabling pin 6 LOW ($\overline{SOUT}$ is HIGH on pin 2). The LOW at pin 6 forces the output of NOR gate A (zone C2) HIGH which is applied to pin 68 of the bus through non-inverting bus driver H (zone B2) as MWRITE. The MWRITE signal allows the memory to store the CPU data in the addressed memory location, thus completing the CPU to memory data transfer.

3-24. MEMORY TO CPU DATA TRANSFER

A Memory to CPU data transfer is accomplished whenever an instruction is encountered to perform this operation. For example, a load accumulator LDA (072_8) instruction requires the specified addressed memory location to transfer its contents to the accumulator in the CPU. The LDA instruction was fetched during M1 and the specified memory location determined during the memory read cycles, M2 and M3. The memory data is transferred to the CPU by an additional Memory Read Cycle operation (M4). The M4 operation

requires the CPU to output the specified addressed memory location to memory, allowing the data in the specified addressed memory location to be transferred to the CPU in an identical manner as M2.

For a detailed operation description of the M2 cycle, refer to Paragraph 3-17. Note as you read the description that the specified memory address location is presented to memory on the fifteen individual address lines, allowing that location to transfer its data to the CPU.

3-25. CPU TO EXTERNAL DEVICE DATA TRANSFER

A CPU to External Device data transfer is accomplished when an output instruction (323_8) is fetched from a memory location during M1, and the external device number (XXX_8) is read from a memory location during M2 by the CPU. The data from the CPU is transferred to the external device by an Output Write Cycle operation (M3).

3-26. OUTPUT WRITE CYCLE BASIC OPERATION (Figure 3-10)

The Output Write Cycle operation will allow the CPU to output data to an external device. After completion of the Memory Read Cycle (M2), the program counter is not incremented until the completion of the Output Write Cycle. Several signals are generated by the CPU in order to transfer the data to the external device.

The SOUT and PSYNC external device ADDRESS (XXX_8) number, consisting of sixteen individual outputs (AØ-A7) from the CPU, is presented to the external device (I/O) to condition the I/O card. With the I/O conditioned, a $\overline{PWR}$ signal from the CPU allows the I/O to transfer the CPU data via the DATA OUT (DOØ-DO7) lines to the external device. The $\overline{SWO}$ output from the CPU is presented to the Display/Control through the Interface to light the WO (write output) LED on the 8800b front panel. The SOUT and AØ through A15 outputs are applied to the Display/Control through the Interface to light the OUT output and ADDRESS LEDs on the 8800b front panel.

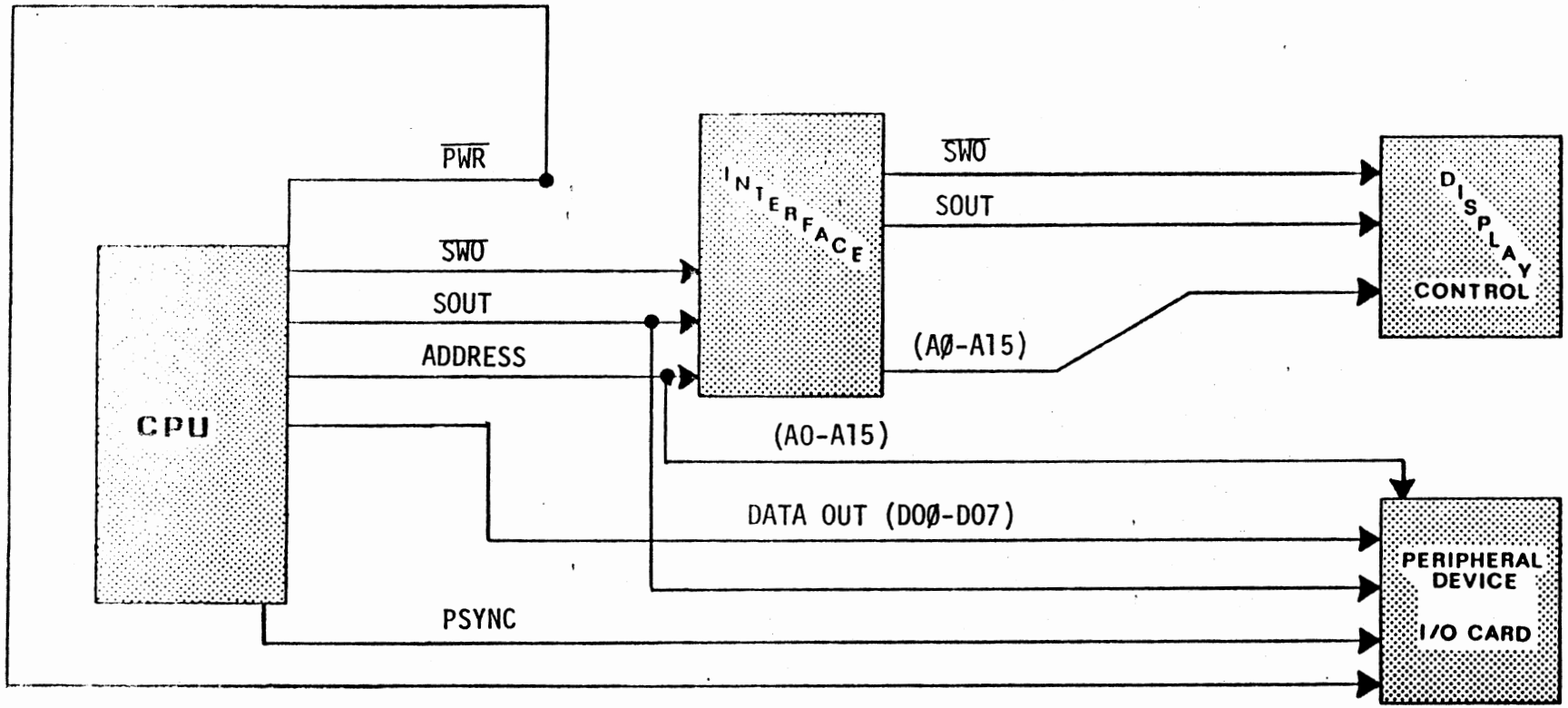


Figure 3-10. Output Write Cycle Block Diagram

3-27. OUTPUT WRITE CYCLE DETAILED OPERATION

The following paragraphs describe the Output Write Cycle operation in detail. Refer to Figure 3-11, Output Write Cycle Timing, during the explanation. The Output Write Cycle operation (M3) requires three Ø1 and Ø2 clock pulses. Each clock period performs a certain operation as described in the following paragraphs.

During the latter portion of T1, several outputs are generated by the CPU 8080 IC (Figure 3-14); Address data AØ through A15 (zone B8), status data DØ through D7, and a SYNC signal (zone C8). The AØ through A15 data contains the external device number and is applied to the I/O card via the bus through non-inverting bus drivers U, P, and N (zone B9) on the CPU in order to enable the I/O card. The address data (AØ-A15) is also applied through inverters P, W, and X on the Interface Card (Figure 3-15, sheet 1, zone B5) and presented to the Display/ Control card. The AØ through A15 signals present on the Display/ Control card light the appropriate AØ through A15 LEDs, indicating the address of the external device. The DØ through D7 data is applied to K (zone B5) on the CPU through bi-directional circuits D and E. The status data is enabled through D and E at this time because $\overline{CS}$ and $\overline{DIEN}$ are LOW. The SYNC output is applied to the clock generator F (zone B7) which conditions F to generate a signal during T2.

At the beginning of T2, a $\overline{STSTB}$ (zone B7) is generated LOW from F as a result of the HIGH SYNC input and internal timing of F. The $\overline{STSTB}$ is applied to the data latch K (zone B5), allowing the status data DØ through D7 to be stored into K. The status data present at the output of K conditions the I/O card to receive data from the CPU by enabling the SOUT and $\overline{SWO}$ signals.

A SOUT output from K is presented HIGH on pin 45 of the bus (zone A4) through non-inverting bus driver X. The SOUT signal is applied through inverter V on the Interface Card (Figure 3-15, zone B5) and presented to NAND gate A (zone C3) and the Display/Control card as SOUT. The $\overline{SOUT}$ signal disables NAND gate A to insure that a MWRITE output is not produced when writing data to an external

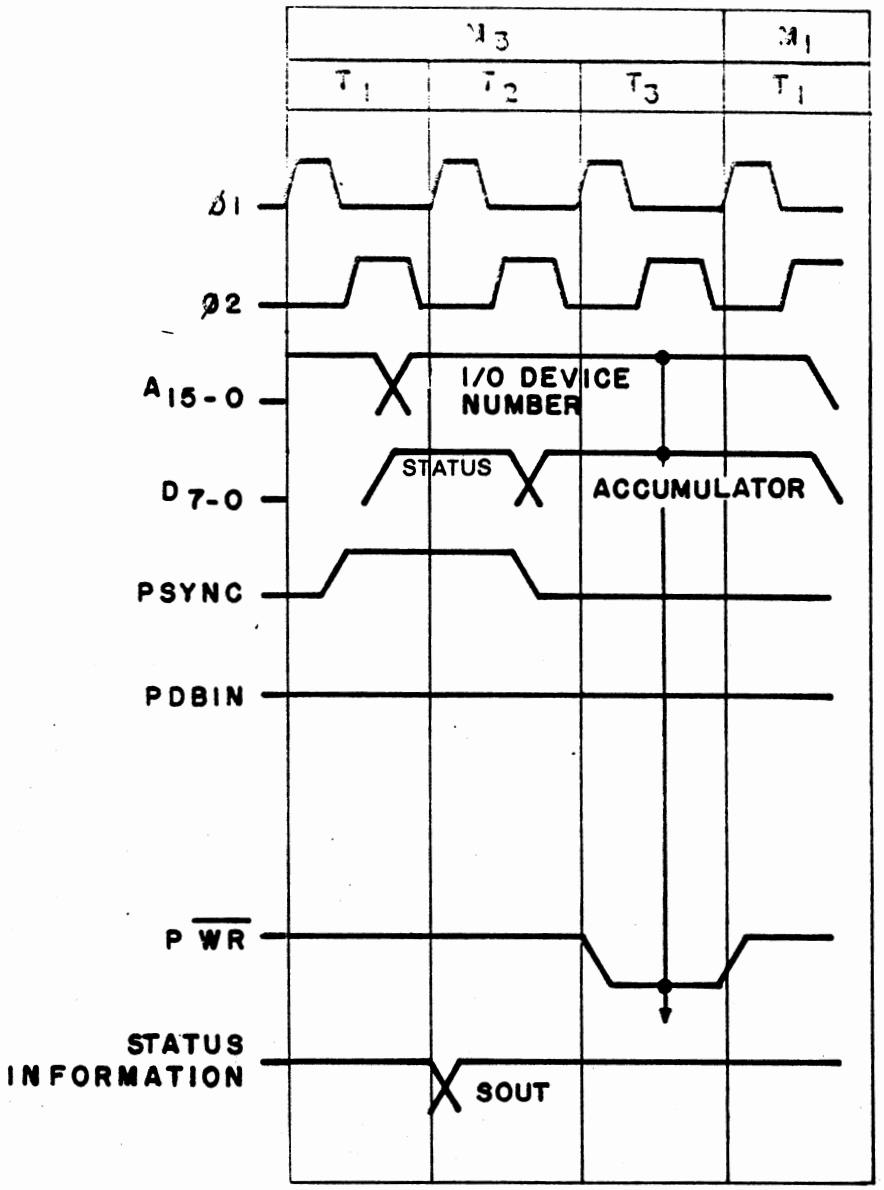


Figure 3-11. Output Write Cycle Timing.

device. It is applied to the Display/Control to light the "OUT" LED (Figure 3-16, sheet 3, zone B3), indicating data is being transferred from the CPU to an external device. The SOUT output from the CPU (Figure 3-14, zone A5) is applied to the external device I/O card in order to initiate a data transfer from the CPU during T3.

At the beginning of T3, the CPU data is transferred to the external device via the bus. The CPU data out (DOØ through DO7) is applied to the bus (zone C1) through bi-directional gates D and E ($\overline{CS}$ and $\overline{DIEN}$ are LOW) and non-inverting bus drivers M and W (zones C7 and C3). The bus data is presented to the external device and written in by the $\overline{PWR}$ signal.

After the CPU data is settled on the bus, a $\overline{WR}$ signal (zone C8) is generated LOW by M. The $\overline{WR}$ signal is applied to pin 77 (zone D1) of the bus through non-inverting bus driver V (zone D8) as $\overline{PWR}$. The $\overline{PWR}$ signal allows the external device to store the CPU data, thus completing the CPU to external device data transfer.

3-28. FRONT PANEL OPERATION

A variety of functions may be performed through the operation of the front panel: e.g. selecting a starting location for a program, examining memory locations, single stepping through a program, depositing and displaying CPU accumulator data, and depositing data into a specified memory location. Each of the functions performed on the 8800b front panel are discussed in the following paragraphs. The run operation was discussed in Paragraph 3-10.

3-29. FRONT PANEL BLOCK DIAGRAM (Figure 3-12)

The front panel switches allow the operator to assume control of the CPU. The CPU is controlled by a FRDY signal which is generated from the front panel display control circuits. The FRDY signal places the CPU in either a wait condition or a run operation.

The CPU is placed in a wait condition when the Switches and Decoding circuits sense that the RUN/STOP switch on the front panel is positioned to STOP. A STOP signal is applied to the Stop/Run

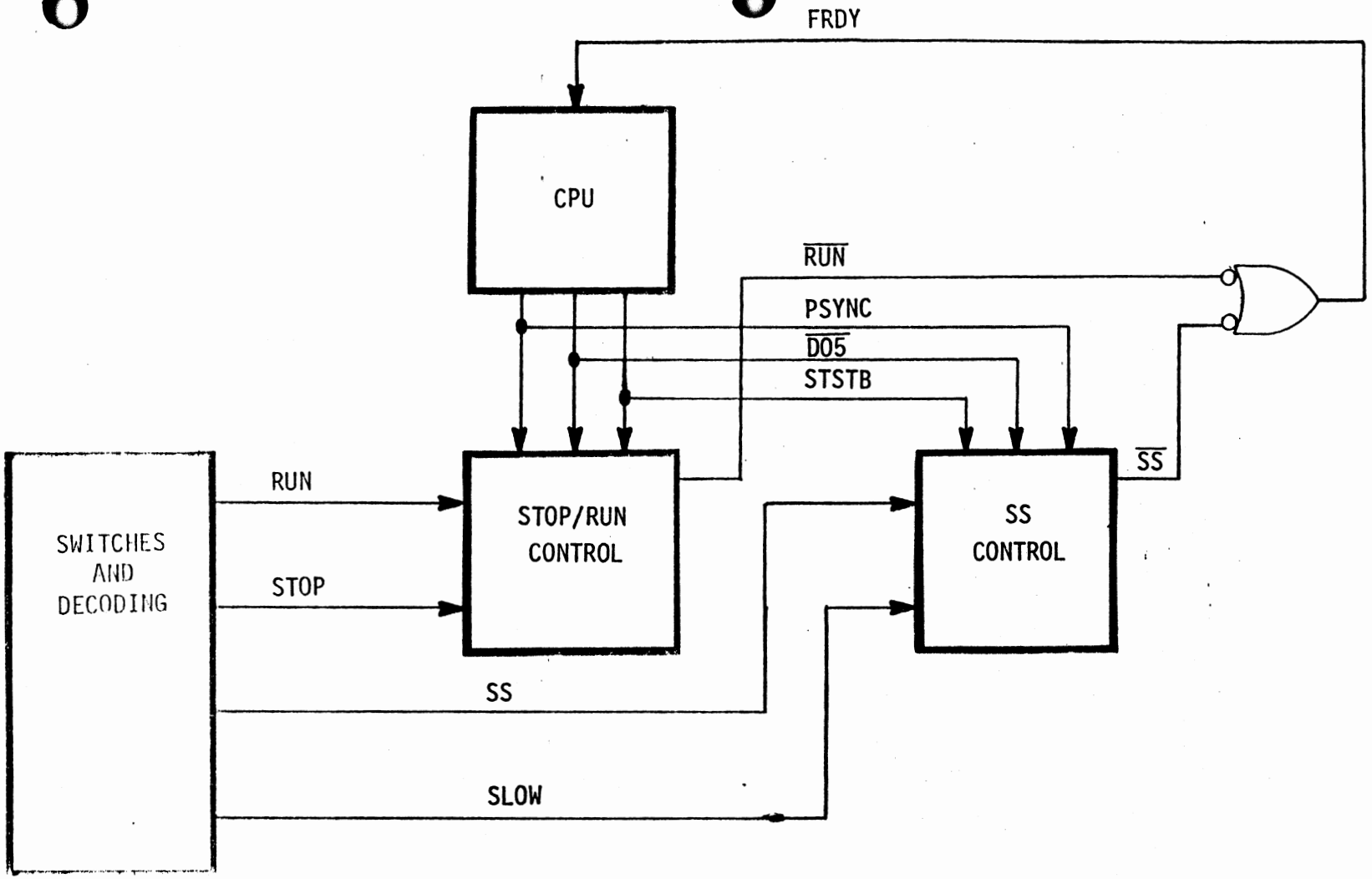


Figure 3-12. Front Panel Block Diagram

Control circuits to disable (HIGH) the $\overline{RUN}$ signal. The $\overline{RUN}$ signal forces the CPU to a wait condition by disabling (LOW) the FRDY line. The CPU will not enter a wait condition until the PSYNC, $\overline{DO5}$, and STSTB signals are presented to the Stop/Run Control circuits. The presence of these signals insures that the CPU will stop during the first machine cycle of an instruction cycle.

The CPU is placed in a single step (SS) or slow run operation by the generation of an SS or SLOW signal from the Switches and Decoding circuits. The SS or SLOW run operation allows the CPU to perform one instruction cycle. The SS signal is applied to the SS Control circuit, enabling (LOW) the $\overline{SS}$ signal. The $\overline{SS}$ signal allows the CPU to execute one instruction cycle by enabling the FRDY signal. Upon the completion of the instruction cycle, the CPU attempts to perform another instruction cycle, but the PSYNC, $\overline{DO5}$, and STSTB signals reset the SS Control circuits forcing the CPU to a wait condition.

3-30. STOP OPERATION

The stop operation allows the operator to use the switches on the 8800b front panel. The stop operation is activated when the RUN/STOP switch on the 8800b front panel is momentarily depressed to STOP.

The RUN/STOP circuits are located on the Display/Control card (Figure 3-16, sheet 2, zone A9). With the RUN/STOP switch momentarily depressed, a LOW is applied to quad latch C1, input D1. The occurrence of the next C13 clock (zone A1) causes the $\overline{Q}$ output at pin 3 of C1 (zone B9) to go HIGH which is applied to quad latch N1, input D1. The next C13 clock causes the Q output at pin 7 of N1 (zone B9) to go HIGH which is applied to the D input of M1. A HIGH present at D produces a clock pulse to set M1, stopping the CPU.

The clock pulse that sets M1 is derived from three signals: $\overline{DO5}$, $\overline{PSYNC}$, and $\overline{STSTB}$ (zone D8). The signals are enabled during machine cycle 1 (paragraph 3-14) of an 8800b instruction cycle, and their presence generates a clock to M1 (zone C9). This insures that the 8800b stops during the first machine cycle of an instruc-

tion cycle. The DO5 signal is generated by the CPU (Figure 3-14, zone C1) and presented to pin 39 of the bus as a HIGH through the bi-directional gate E (zone C7) and non-inverting bus driver W (zone C3) and applied to the Interface Card (Figure 3-15, sheet 2, zone C2). The DO5 signal is inverted by Y (zone B2) and inverted again by R1 on the Display/Control Card (Figure 3-16, sheet 2, zone D8) and applied HIGH to pin 3 of NAND gate D1 (zone C8). The PSYNC is generated by the CPU (Figure 3-14, zone D1) on pin 76 of the bus as a HIGH through non-inverting bus driver V (zone D8) and applied to the Interface Card (Figure 3-15, sheet 2, zone A3). PSYNC is inverted by U (zone B3) and R1 on the Display/Control Card (sheet 5, zone B3) and applied HIGH to pin 4 of NAND gate D1 (zone C8).

The $\overline{\text{STSTB}}$ is generated by the CPU (Figure 3-14, zone A4) to pin 56 of the bus as a LOW through non-inverting bus driver R and applied to the Interface Card (Figure 3-15, sheet 2, zone A4). The $\overline{\text{STSTB}}$ is inverted and then inverted again by the Interface Card (sheet 2, zone A4) and applied to pin 5 of NAND gate D1 on the Display/Control Card (Figure 3-16, sheet 2, zone C8) as a HIGH. These signals allow NAND gate D1 to produce a HIGH at gate P1, pin 6 (zone C8), which sets M1. The $\overline{Q}$ output of M1 goes LOW and is applied through K1 (zone A8) to enable all the front panel switches. The $\overline{Q}$ output is also presented to gate P1 which keeps a high on the CK input of M1 (zone C9), insuring that M1 remains set after the stop switch is released.

Because M1 is set, the Q output of M1 (zone C9) is HIGH, disabling the $\overline{\text{RUN}}$ and $\overline{\text{FRDY}}$ signals. The $\overline{\text{FRDY}}$ signal is applied to NAND gate C on the CPU (Figure 3-14, zone A8) through the Interface (Figure 3-15, sheet 2, zone A1) as a LOW. This inhibits the RDYIN signal at F (Figure 3-14, zone B7) which disables the READY signal to M (zone A8), thereby halting the CPU.

3-31. SINGLE STEP OPERATION

The single step operation allows the operator to increment one instruction cycle at a time. The single step operation is activated when the SINGLE STEP/SLOW switch is momentarily positioned to SINGLE STEP.

The SINGLE STEP circuits are located on the Display/Control card (Figure 3-16, sheet 1, zone A8). With the SINGLE STEP/SLOW

switch momentarily positioned to SINGLE STEP, a LOW is presented to pin 1 of gate P1 (zone C8). The LOW input at D1 generates a clock pulse which sets M1 (zone A7), producing a LOW at the $\overline{Q}$ output of M1. The LOW output is applied to pin 13 of gate P1 (zone C9), enabling the $\overline{FRDY}$ signal (zone D9). The CPU performs one instruction cycle with $\overline{FRDY}$ enabled. At the completion of the instruction cycle, the $\overline{DO5}$, $\overline{PSYNC}$, and $\overline{STSTB}$ input (zone D8) enable NAND gate T1, pin 12 (zone C6), LOW which produces a LOW at the output of inverter J1 (zone C6). The LOW clears the M1 flip-flop, thereby ending the first single step operation. Additional single step operations are enabled by momentarily depressing the SINGLE STEP/SLOW switch to SINGLE STEP.

The DO5 input is applied to pin 1 of NAND gate T1 through jumpers JE and JF (zone D7). If this jumper is removed, pin 1 of NAND gate is always HIGH. Under this condition, the PSYNC and $\overline{STSTB}$ signals would reset M1 after each machine cycle.

3-32. SLOW OPERATION

The slow operation is very similar to the single step operation except the slow operation allows the 8800b to execute instruction cycles at a very slow rate (786 milliseconds vs. 3 milliseconds normal operation).

The slow circuits are located on the Display/Control card (Figure 3-16, sheet 2, zone A8). When the SINGLE STEP/SLOW switch is positioned to SLOW, a HIGH is presented to pin 9 of NAND gate P1 (zone B7). The HIGH at pin 9 enables the C18 clock (zone D7) from a 24-bit counter (sheet 1, zone D1) through NAND gate P1 (sheet 2, zone B7). This clock enables pin 12 of gate D1 (zone C8) HIGH, providing a clock pulse to set M1 (zone A7), producing a LOW at the $\overline{Q}$ output, M1. The LOW output is applied to pin 13 of gate P1 (zone C9), enabling the $\overline{FRDY}$ signal (zone D9). With $\overline{FRDY}$ enabled, the CPU performs one instruction cycle. At the completion of the instruction cycle, the $\overline{DO5}$, $\overline{PSYNC}$, and $\overline{STSTB}$ input (zone D8) enable NAND gate T1, pin 12 (zone C6), LOW which produces a LOW at the output of inverter J1 (zone C6). This LOW clears the M1 flip-flop, ending the first single step operation. If the SINGLE STEP/

SLOW switch is still positioned to SLOW, another instruction cycle operation is performed. Otherwise, the machine halts. If jumpers JE and JF (zone C7) are removed, the machine may not stop at the beginning of an instruction cycle.

3-33. RESET OPERATION

The reset operation allows the operator to reset the CPU at anytime during machine operation. The reset is activated when the RESET/EXT CLR switch on the front panel is positioned to RESET.

The reset circuits are located on the Display/Control card (Figure 3-16, sheet 2, zone A2). With the RESET/EXT CLR switch momentarily positioned to RESET, a PRESET signal (zone D3) is applied to the Interface (Figure 3-15, sheet 2, zone D1) as a HIGH. The HIGH is inverted by R and applied to pin 75 (zone A1) of the bus through non-inverting bus driver N (zone B1). The CPU receives the $\overline{\text{PRESET}}$ signal and inverts it twice through G and B (Figure 3-14, zone B6). The output of B is applied to the clock generator F $\overline{\text{RESIN}}$ (reset in) input (zone B7), producing a RESET output to the 8080 (M).

3-34. PROTECT AND UNPROTECT OPERATION

The protect/unprotect operation either prevents any new data from being written into a particular region of memory (protect) or allows new data to be written into a particular region of memory (unprotect). The protect/unprotect operation is controlled by the positioning of the PROTECT/UNPROTECT switch on the front panel.

The protect/unprotect circuits are located on the Display/Control card (Figure 3-16, sheet 2, zone A1). With the PROTECT/UNPROTECT switch positioned to either PROTECT or UNPROTECT, a $\overline{\text{PROTECT}}$ or $\overline{\text{UNPROTECT}}$ signal (zone D3) is applied to the Interface as a LOW. The LOW is inverted by R (Figure 3-15, sheet 2, zone B6) and applied to pin 70 and 20 on the bus to condition the memory. These signals are used to set or reset the protect/unprotect circuits on the addressed memory board.

3-35. PROGRAMMABLE READ ONLY MEMORY (PROM) CIRCUIT

The PROM circuit on the Display/Control Card is used when one of the following operations is performed: Examine, Examine Next, Deposit, Deposit Next, Accumulator Display, Accumulator Load, Accumulator Input and Accumulator Output. Each of the functions requires a program operation that is stored in the PROM. Access to these programs is determined by the type of function to be performed. The PROM operation is similar for each function, therefore two functions are discussed in detail.

3-36. PROM BLOCK DIAGRAM (Figure 3-13)

The PROM circuit contains eight individual programs which are used in conjunction with the following switches: EXAMINE/EX NEXT, DEPOSIT/DEP NEXT, ACCUMULATOR DISPLAY/LOAD, and ACCUMULATOR INPUT/OUTPUT. Activating any of these switches produces a specific binary number on the RA4, RA5, RA6, and RA7 lines (MSBs) from the Switches and Decoding circuit. At the same time the RA4 through RA7 data is generated, a RESET signal is applied to the 4-Bit Counter, conditioning the RAØ, RA1, RA2, and RA3 outputs (LSBs) to zero. The RAØ-RA7 signals are applied to the PROM, and they represent an 8-bit starting address location. There are eight different starting address locations which correspond to the eight different front panel switch settings (refer to Table 3-2). Any of the eight different starting address locations are always even because of the resetting of the 4-Bit Counter.

The PROM circuit outputs a DATA OUT (RDØ-RD7) signal, consisting of eight individual lines, to either the Control Latch or the non-inverting bus driver F. The DATA OUT is transferred to one of these two circuits by the status of the RAØ signal from the 4-Bit Counter. When the RAØ signal is LOW, representing a PROM even address, the Control Latch receives the data. The even addresses of the PROM contain data that is used to enable the Control Latch output lines (S1-S8). After the Control Latch receives the PROM data, a CLOCK signal increments the 4-Bit Counter to an odd PROM address location. During an odd PROM address cycle, the CPU will execute one machine cycle (assuming the S8 bit has been set in the Control Latch). If the cycle is a memory read cycle, an instruction

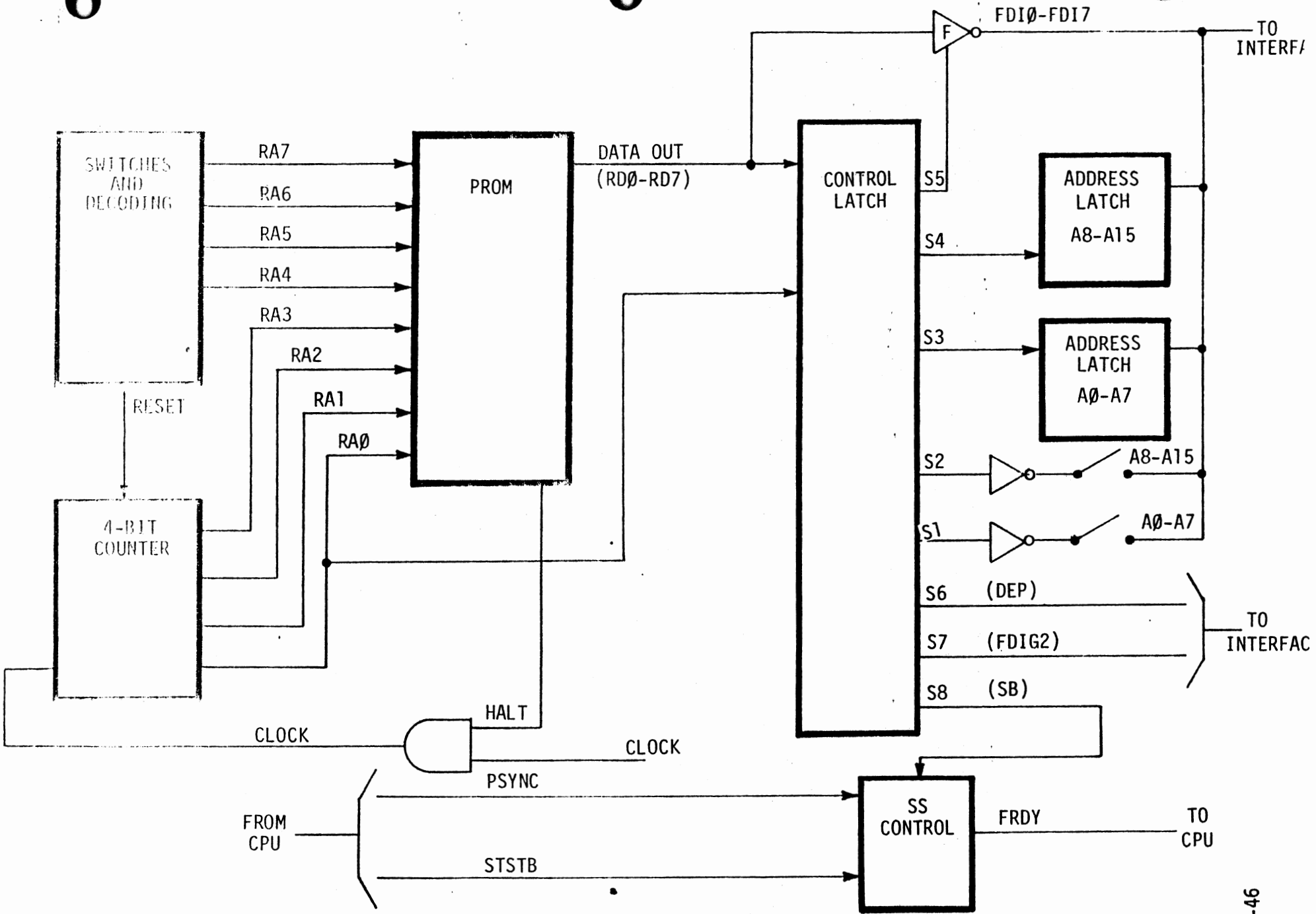


Figure 3-13. PROM Block Diagram

TABLE 3-2. PROM Programs

Front Panel Operations	PROM Address	PROM DATA	Function
Examine	160*	013*	Set S5, S7, S8
	161	303	Jam Jump Instruction to CPU
	162	203	Set S1, S7, S8
	163	000	Jam AØ-A7 switch data to CPU
	164	103	Set S2, S7, S8
	165	000	Jam A8-A15 switch data to CPU
	166	000	Clear control latch
	167	177	Stop
Examine Next	260	013	Set S5, S7, S8
	261	000	Jam NOP instruction to CPU
	262	000	Clear control latch
	263	177	Stop
Deposit	320	206	Set S1, S6, S7
	321	000	Put AØ-A7 switch data and MWRITE pulse on bus
	322	000	Clear control latch
	323	177	Stop
Deposit Next	340	013	Set S5, S7, S8
	341	000	Jam NOP instruction to CPU
	342	206	Set S1, S6, S7
	343	000	Put AØ-A7 switch data and MWRITE pulse on bus
	344	000	Clear control latch
	345	177	Stop
Display Accumulator	060	013	Set S5, S7, S8
	061	323	Output Instruction
	062	013	Set S5, S7, S8

*All PROM address and data information is octal.

TABLE 3-2. PROM Programs - Continued

Front Panel Operations	PROM Address	PROM DATA	Function
	063*	377*	Jam front panel address to CPU
	064	001	Set S8
	065	000	Data in accumulator is transferred to the DØ-D7 LEDs
	066	013	Set S5, S7, S8
	067	303	Jam jump instruction to CPU
	070	043	Set S3, S7, S8
	071	000	Jam AØ-A7 latch data to CPU
	072	023	Set S4, S7, S8
	073	000	Jam A8-A15 latch data to CPU
	074	000	Clear control latch
	075	177	Stop
Accumulator Deposit	220	013	Set S5, S7, S8
	221	333	Jam input instruction to CPU
	222	013	Set S5, S7, S8
	223	377	Jam front panel address to CPU
	224	001	Set S8
	225	000	Data in accumulator is transferred to CPU
	226	013	Set S5, S7, S8
	227	303	Jam jump instruction to CPU
	230	043	Set S3, S7, S8
	231	000	Jam AØ-A7 latch data to CPU
	232	023	Set S4, S7, S8
	233	000	Jam A8-A15 latch data to CPU
	234	000	Clear control latch
	235	177	Stop
Input from external device selected by ADDRESS switches A8-A15	300	013	Set S5, S7, S8
	301	333	Jam input instruction to CPU
	302	103	Set S2, S7, S8
	303	000	Jam A8-A15 switch data to CPU

*All PROM address and data information is octal.

TABLE 3-2. PROM Programs - Continued

Front Panel Operations	PROM Address	PROM DATA	Function
	304*	001*	Set S8
	305	000	Data in accumulator is transferred to specific I/O device
	306	013	Set S5, S7, S8
	307	303	Jam jump instruction to CPU
	310	043	Set S3, S7, S8
	311	000	Jam AØ-A7 latch data to CPU
	312	023	Set S4, S7, S8
	313	000	Jam A8-A15 latch data to CPU
	314	000	Clear control latch
	315	177	Stop
Output from external device selected by ADDRESS switches A8-A15	240	013	Set S5, S7, S8
	241	323	Jam output instruction to CPU
	242	103	Set S2, S7, S8
	243	000	Jam A8-A15 switch data to CPU
	244	001	Set S8
	245	000	Data is transferred from specific I/O device to accumulator
	246	013	Set S5, S7, S8
	247	303	Jam jump instruction to CPU
	250	043	Set S3, S7, S8
	251	000	Jam AØ-A7 latch data to CPU
	252	023	Set S4, S7, S8
	253	Q00	Jam A8-A15 latch data to CPU
	254	000	Clear control latch
	255	177	Stop

*All PROM address and data information is octal.

byte is supplied to the CPU on the FDIØ-FDI7 lines.

The instruction data at the odd PROM address is transferred to the CPU through the interface from five different sources. The source is determined by the output control lines S1 through S5 from the Control Latch.

The S1 and S2 control lines enable the front panel switch data, AØ through A15, to the Interface. The S3 and S4 control lines enable the Address Latch data, AØ through A15, to the Interface. The S5 control line enables the DATA OUT (RDØ-RD7) from the PROM to the Interface.

The data present at the Interface is applied to the CPU by output control lines S7 and S8 from the Control Latch. The S7 control line allows the Interface to apply the instruction data to the CPU, and the S8 control line enables the FRDY signal. The FRDY signal allows the CPU to receive the instruction data and execute one machine cycle. After the completion of the machine cycle, the PSYNC and STSTB signals from the CPU reset the SS Control circuit. The S6 control line is enabled from the Control Latch to allow data to be deposited into memory. Upon the completion of a PROM program, a HALT signal is generated by the PROM, disabling the CLOCK signal to the 4-Bit Counter.

3-37. EXAMINE OPERATION

The examine operation allows the operator to examine a memory location by using the ADDRESS switches on the front panel. Refer to Table 3-2 during the explanation. The examine operation is activated when the EXAMINE/EXAMINE NEXT switch is momintarily positioned to EXAMINE.

The EXAMINE circuit is located on the Display/Control card (Figure 3-16, sheet 2, zone B7). With the EXAMINE/EXAMINE NEXT switch momentarily positioned to EXAMINE, a LOW is generated at pin 6 of inverter V1 (zone B7) and a HIGH at the output of the remaining V1 and Z1 inverters (zones B6 through B3). The LOW output is applied to pin 6 of gate X1 which generates a HIGH to set L1 (zone D4). The $\overline{\text{RC-CLR}}$ (LOW) and AL-STB (HIGH) outputs

from L1 reset a 4-bit binary counter to zero (sheet 2, zone A9) and strobes the current address data into data latches B1 and T1 (zone B6). The L1 latch is cleared by the $\overline{C6}$ signal from the 24-bit binary counter (sheet 1, zone D3). The LOWs and HIGHs from the inverters are presented as RA7 through RA4 inputs to the PROM (sheet 1, zone B9).

The RAØ through RA7 inputs to the PROM (zone B9) represent an address location (160_8). This location is the beginning of the examine program stored in the PROM. The data in address location 160_8 is presented on the RDOØ through RDO7 outputs (013_8) and applied to data latch A (zone D8). After the 4-bit binary counter (zone B9) is LOW during the even addresses (RAØ=0), and a control strobe (CS) to DS2 (zone C8) is generated, the data present at latch A is stored by the A output.

The CS strobe is produced by the 24-bit counter outputs C6, C7, and $\overline{C8}$ (zone D3). When the C6, C7, and $\overline{C8}$ counter outputs are HIGH, NAND gate V (zone D5) is enabled LOW, and CS (zone D6) is applied HIGH to the DS2 input of data latch A (zone C8). With DS2 and $\overline{DS1}$ enabled, the RDØ through RD7 data (013_8) is latched into A. The 013_8 data enables outputs S5, S7, and S8 (zone D7) HIGH. Output S5 is inverted LOW by A1 (zone A6), enabling inverting bus drivers R and S. Outputs S7 and S8 are applied to pins 3 and 13 of NAND gates J (zone D6). With the PROM data stored in latch A and the associated circuits conditioned, NAND gate Z (zone A7) produces a clock pulse to INP A of the 4-bit counter (zone A8). When C8 goes HIGH from the 24-bit counter (zone D3), the 4-bit counter, A output, goes HIGH which addresses PROM location 161_8.

The data in address location 161_8 is present on the RDØ through RD7 outputs 303_8. The 303_8 data is transferred to the Interface on the FDIØ-FDI7 (zone C2) outputs through enabled inverting bus drivers R and S (zone A6). The data is not stored in Latch A because the A output (zone B9) of the 4-bit counter is HIGH (odd address RAØ=1), disabling the $\overline{DS1}$ input (zone C7). The A output is applied to pins 1 and 5 of NAND gates J (zone D6).

The $\overline{FDI0}$ through $\overline{FDI7}$ data presented to the Interface Card (Figure 3-15, sheet 2, zone D8) represents a jump instruction to be stored in the CPU. The CPU cannot receive this instruction and execute it until the $\overline{FDIG2}$ (zone D7) signal is LOW, and the CPU is released from the wait condition generated when the CPU was stopped. The following operation allows the CPU to receive the jump instruction.

When the C6, C7, and $\overline{C8}$ outputs of the 24-bit counter on the Display/Control (Figure 3-16, sheet 1, zone D3) are HIGH, another CS signal (zone D6) is generated. The CS signal allows NAND gate J, pins 6 and 12, to produce $\overline{SB}$ (zone D4) and $\overline{FDIG2}$ (zone C2) signals.

The $\overline{SB}$ signal is applied to pin 13 of gate D1 (sheet 2, zone C8) as a LOW, producing a HIGH clock pulse to set M1 (zone C7). The $\overline{Q}$ output of M1 is applied to pin 13 of NOR gate P1 and inverter R1 (zone D9), allowing the $\overline{FRDY}$ signal to release the CPU from its wait condition.

The $\overline{FDIG2}$ signal is applied to pin 12 of NOR gate B (Figure 3-15, sheet 2, zone C7) on the Interface as a LOW which enables NAND gate B, pin 6, LOW (PDBIN is HIGH because the CPU is in a wait condition). The LOW enables the non-inverting drivers F (zone B7), allowing the PROM data (303_8) to be applied to M on the CPU through bi-directional gates D and E on the CPU (Figure 3-14, zone C7). Because the READY line to M (zone A8) is HIGH, the CPU inputs the 303_8 data which is interpreted by the CPU as a jump instruction. After the completion of the machine cycle, the $\overline{PSYNC}$ and $\overline{DO5}$ signals (sheet 2, zone D8) are inverted by R1 and applied to pins 11 and 10 of NAND gate T1 (zone D6). These signals and $\overline{SB}$ (zone D8) enable T1 which generates a clear to M1 (zone C7), halting the CPU.

The CPU contains a jump instruction but no information as to where to jump. The remaining part of the examine operation allows the ADDRESS switch data to be read into the CPU from the front panel in order for the CPU to jump to that address. NAND gate Z (sheet 1, zone A7) produces another clock pulse to INP A of the 4-bit counter. When C8 goes HIGH and returns LOW (zone D3), the 4-bit counter increments to an even PROM address 162_8.

The data in address location 162_8 is present on the RDØ through RD7 outputs (203_8) and applied to data latch A (zone D8). The data present at latch A is stored by the LOW A output (zone B9) during even addresses (RAØ=0) and the generation of the CS strobe (C6, C7, and $\overline{C8}$ HIGH). The 203_8 data enables outputs S1, S7, and S8 (zone D7) HIGH. Output S1 is applied through inverters Y and W (zone C4) to the AØ through A7 switches (open switch HIGH, closed switch LOW), and the switch information is presented to the Interface as $\overline{FDIØ}$ through $\overline{FDI7}$. Outputs S7 and S8 are applied to pins 3 and 13 of NAND gate J (zone D6) and are used to generate the $\overline{FDIG2}$ and $\overline{SB}$ signals as described in the jump instruction transfer. With the data presented to the Interface Card and the associated circuits conditioned, NAND gate (zone A7) is enabled (C8 HIGH), producing a clock pulse to INP A, incrementing the 4-bit counter (zone A8) to address 163_8.

The data in address 163_8 is not stored in latch A because it is an odd address. However, the A output (zone B9) is applied to pins 1 and 5 of NAND gates J (zone D6) as a HIGH, allowing the CS signal to produce the $\overline{SB}$ and $\overline{FDIG2}$ outputs. The $\overline{SB}$ and $\overline{FDIG2}$ signals allow the transfer of the first eight address data bits (address switches AØ-A7) to the CPU, and the operation is identical to the jump instruction.

After the CPU receives the eight address bits, the 4-bit binary counter is incremented to address 164_8. The data in 164_8 (01000110 - 103_8) is stored in latch A (zone D7) because it is an even address. The 103_8 data enables S2, S7, and S8 (zone D7) HIGH. Output S2 is applied to inverter A1 (zone C6), gate Z (zone C5), and inverters W and U (zone C4) to the A8 through A15 address switches. The switch information is presented to the Interface as $\overline{FDIØ}$ through $\overline{FDI7}$. Outputs S7 and S8 condition NAND gates J (zone D6) and are used to generate $\overline{SB}$ and $\overline{FDIG2}$ during the next address. With the data present to the Interface and the associated circuits conditioned, NAND gate Z (zone A7) is enabled (C8 HIGH), producing a clock pulse to INP A, incrementing the 4-bit counter (zone A8) to address 165_8.

Address 165_8 operation is the same as address 163_8, allowing the A8 through A15 address data to be stored in the CPU. After

the CPU receives the second byte of the address, it executes a jump to that address. Address 166_8 clears the data latch A (zone D7) and allows the CPU to address memory (Figure 3-14, zone B9). The memory presents the addressed memory location data to the CPU via data input lines DI0 through DI7 (zone B1). The data is enabled through inverters Y, S, L, and J (zone B4) and non-inverters P, W (zone C3) to the Interface (Figure 3-15, sheet 1, zone B1). The data is enabled through the G data latch (sheet 3, zone B4) to the Display/Control (Figure 3-16, sheet 3, zone D1) and displayed on the LEDs. The G latch (sheet 3, zone B4) is enabled because the $\overline{\text{RUN}}$ signal (zone A6) is HIGH, producing a HIGH at input MD of the data latch.

While the memory data was being displayed, the 4-bit binary counter (Figure 3-16, sheet 1, zone A9) is incremented to address 167_8. The data in 167_8 (01111111 - 177_8) is applied to NAND gate N (zone B7), producing a HIGH at gate Z (zone B8). The HIGH at gate Z disables NAND gate Z (zone A8), inhibiting any following clock pulses to the 4-bit binary counter, thus ending the examine operation.

3-38. ACCUMULATOR DISPLAY OPERATION

The accumulator (ACC) display operation allows the operator to monitor the contents of the CPU accumulator. Refer to Table 3-1, PROM Programs, during the explanation. The ACC display operation is activated when the ACC DISPLAY/ACC DEPOSIT switch is momentarily positioned to ACC DISPLAY.

The ACC DISPLAY circuit is located on the Display/Control card (Figure 3-16, sheet 2, zone A5). With the ACC DISPLAY/ACC DEPOSIT switch momentarily positioned to ACC DISPLAY, a LOW is generated at pins 8 and 10 of inverter V1 (zone B5), and a HIGH is generated at the output of the remaining V1 and Z1 inverters (zones B7 through B3). The LOW outputs are applied to pins 6 and 5 of gate X1 which generates a HIGH to set L1 (zone D4). The $\overline{\text{RC-CLR}}$ (LOW) and AL-STB (HIGH) outputs from L1 reset a 4-bit binary counter to all zeros (sheet 1, zone A9) and strobe the address in the P counter into data latches B1 and T (zone B6). The P counter address data is stored because the P counter increments during the accumulator display operation. The original P

count is saved and restored in the CPU after the ACC display operation is complete. The L1 latch is cleared by the $\overline{C6}$ signal from the 24-bit binary counter (sheet 1, zone D3). The LOW and HIGHs from the inverters are presented as RA7 through RA4 inputs to the PROM (sheet 1, zone B9). An $\overline{ACC\ DSP}$ signal (zone D3) is also applied LOW to the Interface (Figure 3-15, sheet 3, zone A1), producing a LOW to the MD input of data latch G (zone A4).

The RAØ through RA7 inputs to the PROM (zone B9) represent an address location (060_8). This location is the beginning of the ACC display program stored in the PROM. The data in address location 060_8 is presented on the RDØ through RD7 outputs (013_8) and applied to data latch A (zone D8). The data present at latch A is stored by the LOW A output (zone B9) during the even addresses (RAØ=0) and the generation of a control strobe (CS) to DS2 (zone C8).

The CS strobe is produced by the 24-bit counter outputs C6, C7, and $\overline{C8}$ (zone D3). When the C6, C7, and $\overline{C8}$ counter outputs are HIGH, NAND gate V (zone D5) is enabled LOW, the CS (zone D6) is applied HIGH to the DS2 input (zone C8). The RDØ through RD7 data (013_8) is latched into A with DS2 and $\overline{DS1}$ enabled. The 013_8 data enables outputs S5, S7, and S8 (zone D7) HIGH. Output S5 is inverted LOW by A1 (zone A6), enabling inverting bus drivers R and S. Outputs S7 and S8 are applied to pins 3 and 13 of NAND gates J (zone D6). With the PROM data stored in latch A and the associated circuits conditioned, NAND gate Z (zone A7) is enabled, producing a clock pulse to INP A of the 4-bit counter (zone A8). When C8 goes HIGH from the 24-bit counter (zone D3), the 4-bit counter A output goes HIGH which addresses PROM location 061_8.

The data in address location 061_8 is present on the RDØ through RD7 outputs (323_8). The 323_8 data is transferred to the Interface on the $\overline{FDIØ}$-$\overline{FDI7}$ (zone C2) outputs through enabled inverting bus drivers R and S (zone A6). The data is not stored in latch A because the A output (zone B9) of the 4-bit counter is HIGH (odd address), disabling the $\overline{DS1}$ input (zone C7). The A output is applied to pins 1 and 5 of NAND gates J (zone D6).

The FDIØ through $\overline{FDI7}$ data presented to the Interface (Figure 3-15, sheet 2, zone D8) represents an output instruction to be stored in the CPU. The CPU cannot receive this instruction and

execute it until the FDIG2 (zone D7) signal is LOW, and the CPU is released from the wait condition generated when the CPU was stopped. The following operation allows the CPU to receive the output instruction.

When the C6, C7, and $\overline{C8}$ outputs of the 24-bit counter on the Display/Control (Figure 3-16, sheet 1, zone D3) are HIGH, another CS signal (zone D6) is generated. The CS signal allows NAND gate J, pins 6 and 12, to produce a $\overline{FDIG2}$ (zone C2) and $\overline{SB}$ (zone D4) signal.

The $\overline{SB}$ signal is applied to pin 13 of gate D1 (sheet 2, zone C8) as a LOW which produces a HIGH clock pulse to set M1 (zone C7). The $\overline{Q}$ output of M1 is applied to gate P1 and inverter R1 (zone D9), allowing the $\overline{FRDY}$ signal to release the CPU from its wait condition.

The $\overline{FDIG2}$ signal is applied to pin 12 of gate 13 (Figure 3-15, sheet 2, zone C7) as a LOW which enables NAND gate B, pin 6, LOW. The LOW allows the PROM data (323_8) to be applied to M on the CPU through bi-directional gates D and E on the CPU (Figure 3-14, zone C7). Because the READY line to M (zone A8) is HIGH, the CPU inputs the 323_8 data which is interpreted as an output instruction. After the completion of the machine cycle, the $\overline{PSYNC}$ and $\overline{DO5}$ signals (Figure 3-14, sheet 2, zone D8) are inverted by R1 and applied to pins 11 and 10 of NAND gate T1 (zone D6). These signals and $\overline{SB}$ (zone D8) enable T1 which generates a clear to M1 (zone C7), halting the CPU.

The CPU contains an output instruction but no information as to where to output data. The next part of the ACC display operation allows the CPU to output data to the front panel data LEDs (DØ through D7). NAND gate Z (sheet 1, zone A7) is enabled (C8 HIGH), producing a clock pulse to INP A, incrementing 4-bit counter (zone A8) to address 062_8.

The data in address location 062_8 is present on the RDØ through RD7 outputs (013_8) and stored in data latch A (zone D8) in the same manner as address 060_8. This insures that the S5, S7, and S8 outputs (zone D7) are enabled as in address 060_8. After the completion of this operation, NAND gate Z (zone A7) is enabled, producing a clock pulse to INP A, incrementing the 4-bit counter

(zone A8) to address 063_8.

The data in address location 063_8 is present on the RDØ through RD7 outputs (377_8) which is the I/O channel number for the front panel. The 377_8 data is transferred to the CPU in the same manner as the output instruction at address 061_8. The 377_8 data allows the CPU to address the front panel and output the accumulator data to the DØ through D7 LEDs on the front panel. With the output instruction and front panel address number stored in the CPU, NAND gate Z (zone B7) is enabled, producing a clock pulse to INP A, incrementing the 4-bit binary counter (zone A8) to address 064_8.

The data in address location 064_8 is present to the RDØ through RD7 outputs (001_8) and stored in data latch A (zone D8). The 001_8 data enables output S8 (zone D7) HIGH which is used during address 065_8. After the data in address location 064_8 is stored in data latch A, NAND gate Z (zone B7) is enabled, producing a clock pulse to INP A, incrementing the 4-bit binary counter (zone A8) to address 065_8.

Address 065_8 enables the $\overline{SB}$ signal (zone D4) as described in address 061_8. The CPU performs one machine cycle with $\overline{SB}$ enabled. During the one machine cycle, the CPU outputs address 377_8 on the AØ - A7 and A8 - A15 address lines to the bus (Figure 3-14, zone B9). The CPU also outputs accumulator data through bi-directional gates D and E (zone C7) and non-inverting bus drivers P and W (zone C3) to the data out (DOØ-DO7) bus. The address data (377_8) enables NAND gates L on the Interface board (Figure 3-15, sheet 3, zone C6) LOW. The LOWs enable gate D (zone C4) HIGH which is applied through jumper JE/JF to pin 9 of NAND gate K (zone B4). During an output instruction, the $\overline{SOUT}$ and PWR signals (zone B6) are generated by the CPU which enables NAND gate K (zone B4) output LOW. The LOW is applied through jumper JD/JC and inverted HIGH by gate J (zone C3) and presented to the STB input (zone B4) of latch G.

The data from the CPU is presented to the Interface (sheet 1, zone C1) and stored in data latch G (sheet 3, zone B4) during the output instruction because the STB and MD inputs are enabled.

The outputs of data latch G light the appropriate data LED (DØ-D7) on the Display/Control Panel (Figure 3-16, sheet 3, zone D2). After the machine cycle is complete, NAND gate Z (sheet 1, zone B7) is enabled, producing a clock pulse to INP A, incrementing the 4-bit binary counter to address 066_8.

The data (013_8) in address location 066_8 is stored in data latch A (zone D8) and enables the S5, S7, and S8 outputs (zone D7) HIGH. After the completion of this operation, NAND gate Z is enabled, and the 4-bit binary counter is incremented to address 067_8. Address 067_8 contains a jump instruction (303_8) which is stored in the CPU in the same manner as the previous instructions. The jump instruction will force the CPU back to the original P counter address which was stored in data latches B1 and T (zone B5) at the beginning of the ACC display operation. The remainder of the ACC display operation will transfer the address stored (AØ-A7) in B1 and (A8-A15) in T to the CPU. After the jump instruction is stored in the CPU, the 4-bit binary counter is incremented to address 070_8.

The data in address location 070_8 is present on the RDØ through RD7 outputs (043_8) and applied to data latch A (zone D8). The data present at latch A is stored by the A output of the 4-bit binary counter (zone B9) being LOW during even addresses and the generation of the CS strobe (C6, C7, and $\overline{C8}$ HIGH). The 043_8 data enables outputs S3, S7, and S8 (zone D7) HIGH. Output S3 is applied to the DS2 input of data latch B1 (zone C5), presenting the output data (AØ-A7) to the Interface as $\overline{FDIØ}$ through $\overline{FDI7}$. Outputs S7 and S8 are applied to pins 3 and 13 of NAND gate J (zone D6) and are used to generate the $\overline{SB}$ and $\overline{FDIG2}$ signals as described in the previous instruction transfers. With the data present to the Interface and the associated circuits conditioned, NAND gate Z (zone A7) is enabled, producing a clock pulse to INP A, incrementing the 4-bit counter (zone A8) to address 071_8.

The data in address 071_8 is not stored in latch A because it is an odd address. However, the A output (zone B9) is applied to pins 1 and 5 of NAND gates J (zone D6) as a HIGH, enabling the CS signal to produce the $\overline{SB}$ and $\overline{FDIG2}$ outputs. The $\overline{SB}$ and $\overline{FDIG2}$ signals allow the transfer of the first eight address data latch

bits to the CPU, and the operation is identical to the previous instructions.

After the CPU receives the eight address bits, the 4-bit binary counter increments to address 072_8. The data in 072_8 (023_8) is stored in latch A (zone D7) because it is an even address. The 023_8 data enables S4, S7, and S8 (zone D7) HIGH. Output S4 is applied to the DS2 input of data latch T (zone A6), presenting the output data (A8-A15) to the Interface as $\overline{\text{FDI}\emptyset}$ through $\overline{\text{FDI7}}$. Outputs S7 and S8 condition NAND gates J (zone D6) and are used to generate $\overline{\text{SB}}$ and $\overline{\text{FDIG2}}$ during the next address (073_8). With the data present to the Interface and the associated circuits conditioned, NAND gate Z (zone A7) is enabled (C8 HIGH), producing a clock pulse to INP A, incrementing the 4-bit counter (zone A8) to address 073_8.

Address 073_8 operation is the same as address 071_8, allowing the A8 through A15 address data to be stored in the CPU. Address 074_8 clears the data latch A (zone D7) and allows the CPU to jump to the original P counter address, conditioning the CPU for normal operation.

After conditioning the CPU, the 4-bit binary counter (zone A9) is incremented to address 075_8. The data in 075_8 (177_8) is applied to NAND gate N (zone B7), producing a HIGH at gate Z (zone B8). The HIGH at gate Z disables NAND gate Z (zone A8), inhibiting any following clock pulses to the 4-bit binary counter, thus ending the ACC display operation.

3-39. 8800b OPTIONS

The 8800b has several options which may be selected by the operator. Two options may be used on the Display/Control card, and three options may be used on the Interface card.

3-40. DISPLAY/CONTROL CARD OPTIONS

The Display/Control card options contain a choice of front panel slow operation clock frequencies and a choice of completing one instruction cycle or machine cycle in single step or slow operation. The normal slow operation clock frequency requires a

connection between jumpers JA and JD (Figure 3-16, sheet 1, zone D2). For slower operation, jumpers JB to JD or JC to JD may be connected. The normal single/step or slow operation requires a connection between jumpers JE and JF (sheet 2, zone D7) which allows the 8800b CPU to complete one instruction cycle before resuming a wait condition. However, if the operator wishes to execute one machine cycle after each single/step or slow operation, remove jumpers JE and JF which disables the $\overline{DO5}$ signal (zone D8).

3-41. INTERFACE CARD OPTIONS

One Interface Card option allows the operator to monitor any data from an external device on the DØ through D7 front panel LEDs. Data may be monitored from an external device if jumpers JA and JB are connected (Figure 3-15, sheet 3, zone C3). NAND gate K is enabled LOW when the Ø1, $\overline{PDBIN}$, and $\overline{SINP}$ signals (zone C6) are present during an external device to CPU data transfer. The LOW is presented through JB and JA (zone C3) to gate J which produces a HIGH to the STB input of data latch G (zone B4). The HIGH on STB allows the data present on the DOØ-DO7 line (zone B6) to be displayed on the DØ-D7 LEDs on the front panel.

The remaining Interface card options pertain to jumpers JE and JF (zone C4) and jumpers JD and JC (zone C3). If jumpers JE and JF and JC and JD are connected, only data addressed to the front panel (377_8) is displayed. If jumpers JE and JF are removed, all output data from the CPU is displayed on the front panel.

3-42. 8800b POWER SUPPLIES

The 8800b requires a positive 8 volt, 18 ampere supply, a positive 18 volt, 2 ampere supply, and a -18 volt, 2 ampere supply (Figure 3-17). When the ON/OFF switch on the front panel is positioned to ON, a 110 AC voltage is applied to transformer T1. Two bridge rectifiers on the secondary of T1 produce the positive 8, 18, and negative 18 voltage supplies which are applied to the 8800b circuits. The positive and negative 18 volt supplies are pre-regulated by the Q and Q2 transistor circuits on the power supply board.

The 8800b printed circuit cards receive the supply voltages on the bus. Each printed circuit card contains its own voltage regulator circuits which produce the operating voltage for the particular printed circuit card.

The CPU card (Figure 3-18) requires a regulated positive and negative 5 volt source and a regulated positive 12 volt source. These voltages are produced by VR1, VR2, and D2 circuits.

The Interface card (Figure 3-19) requires a regulated positive 5 volt source which is produced by the VR1 circuit.

The Display/Control card (Figure 3-20) requires an unregulated positive 8 volt source, a regulated positive 5 volt source, and a regulated negative 9 volt source. The regulated voltages are produced by the VR1 and VR2 circuits.

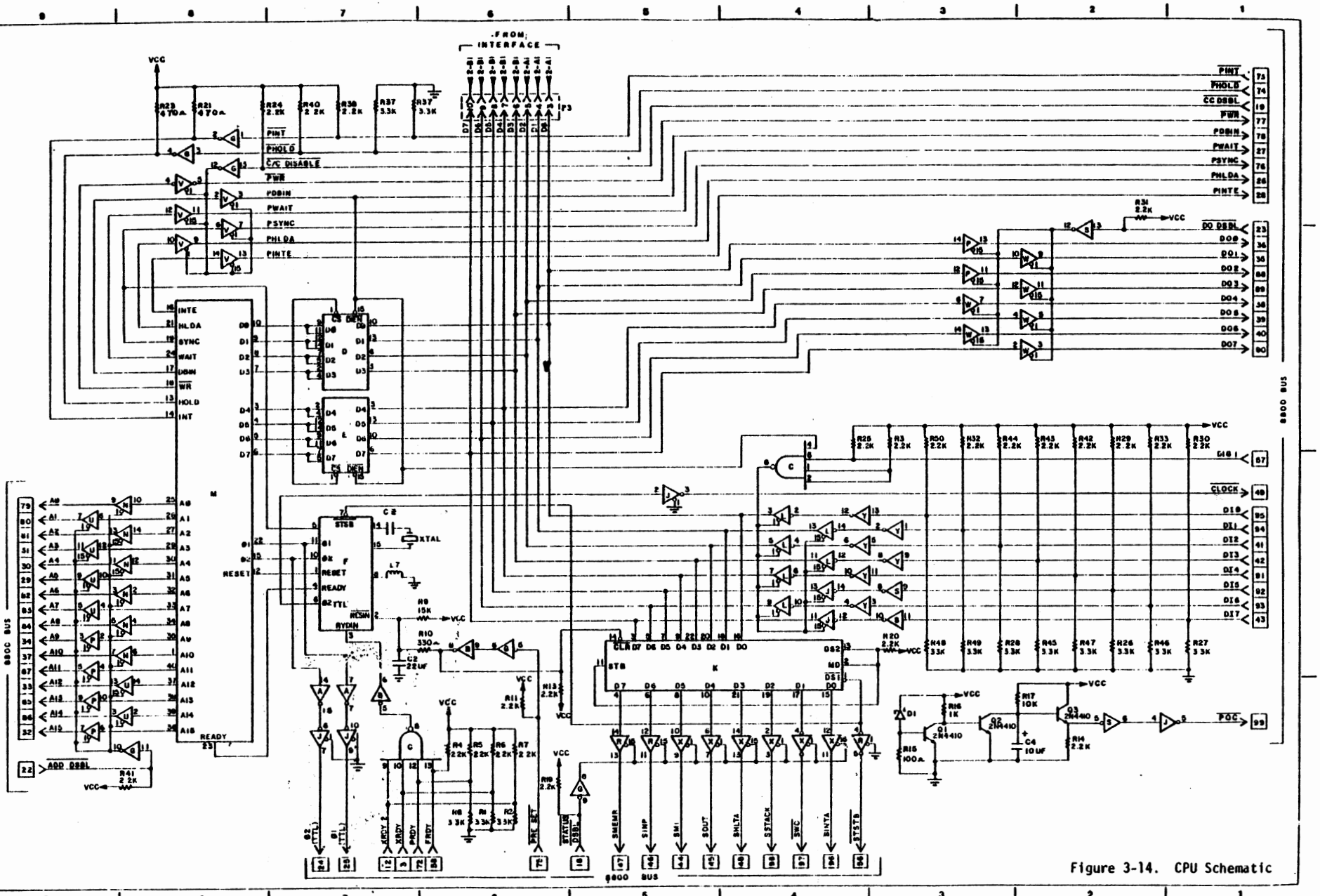


Figure 3-14. CPU Schematic

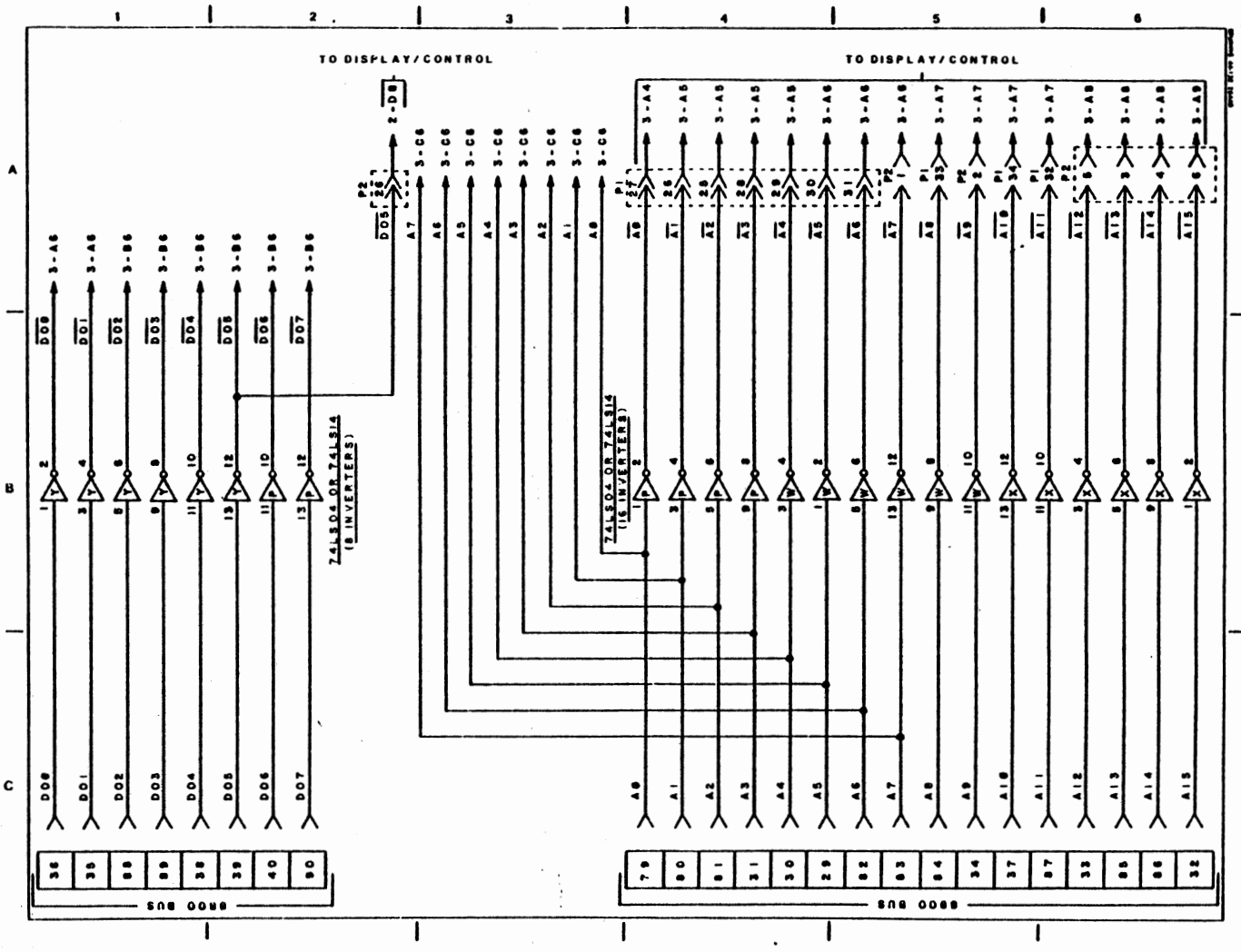


Figure 3-15. Interface Schematic (sheet 1 of 3)

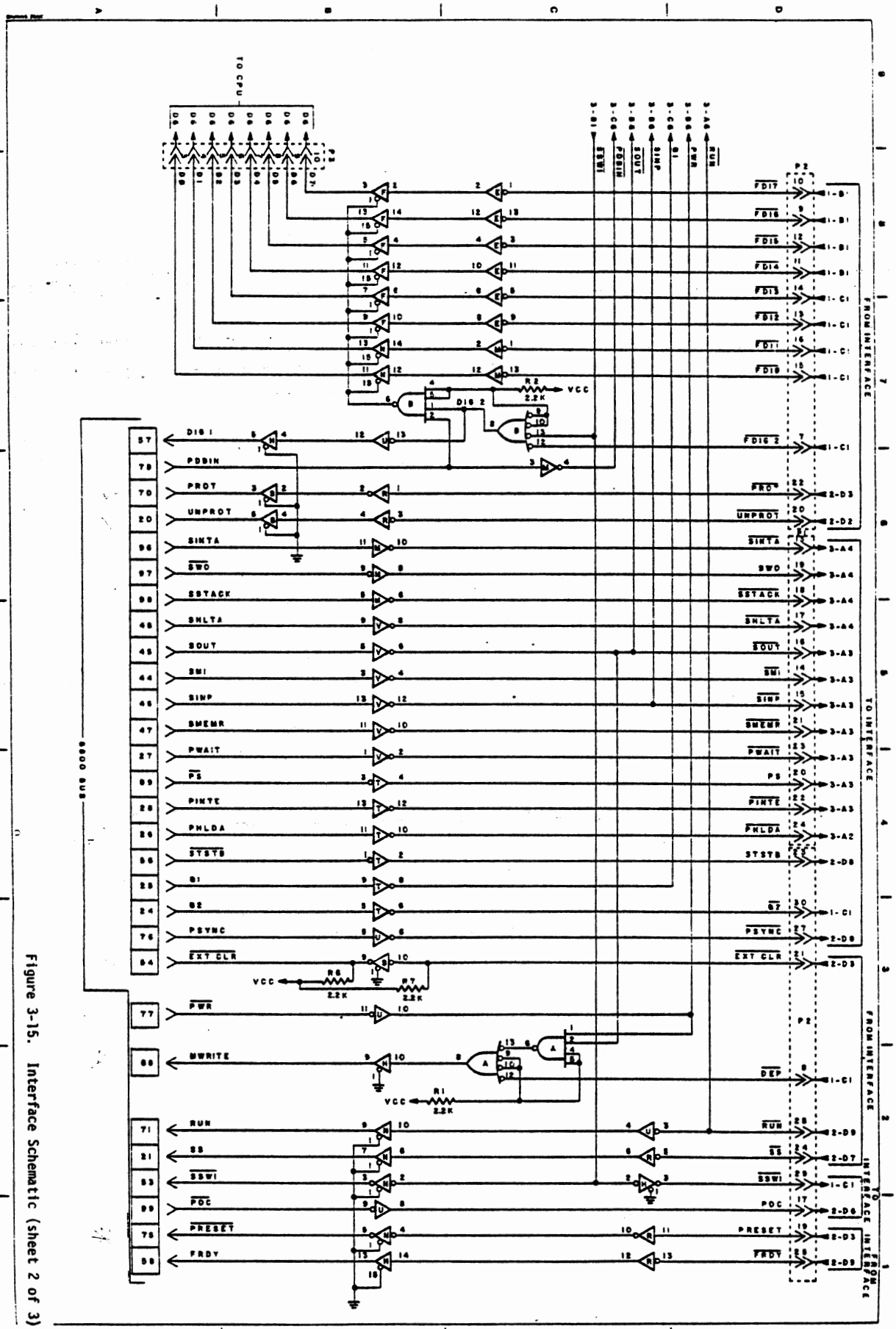


Figure 3-15. Interface Schematic (sheet 2 of 3)

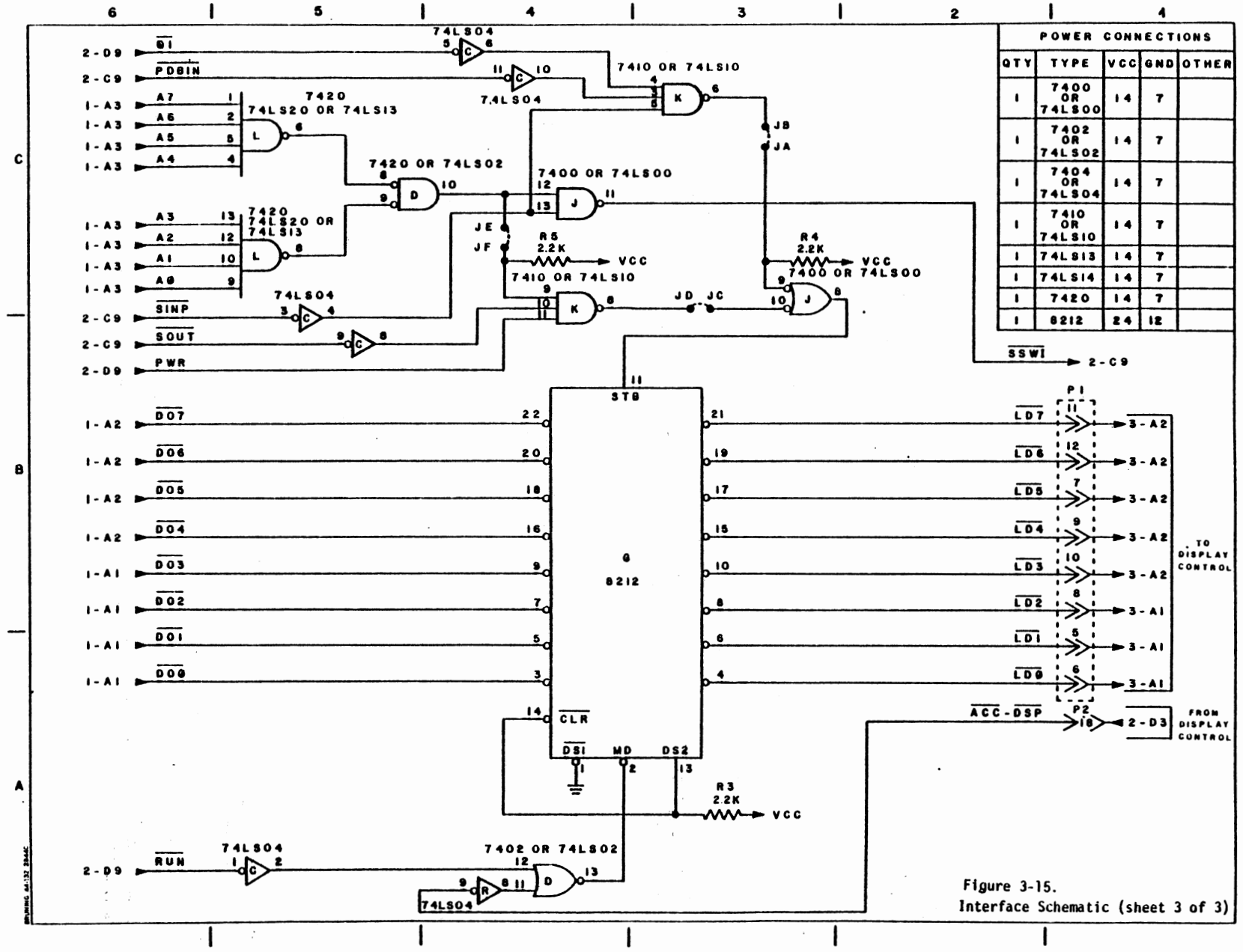


Figure 3-15.
Interface Schematic (sheet 3 of 3)

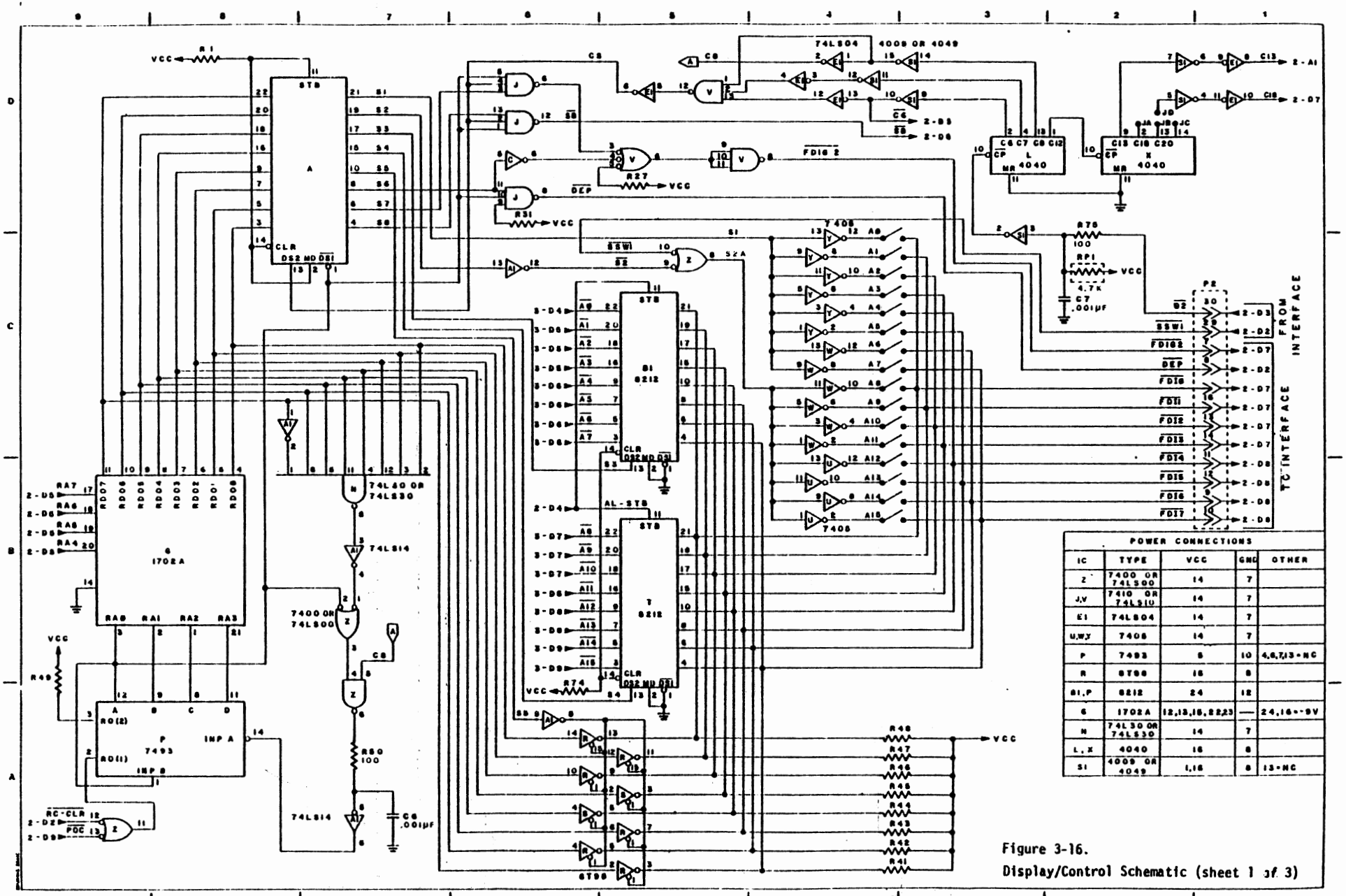


Figure 3-16.
Display/Control Schematic (sheet 1 of 3)

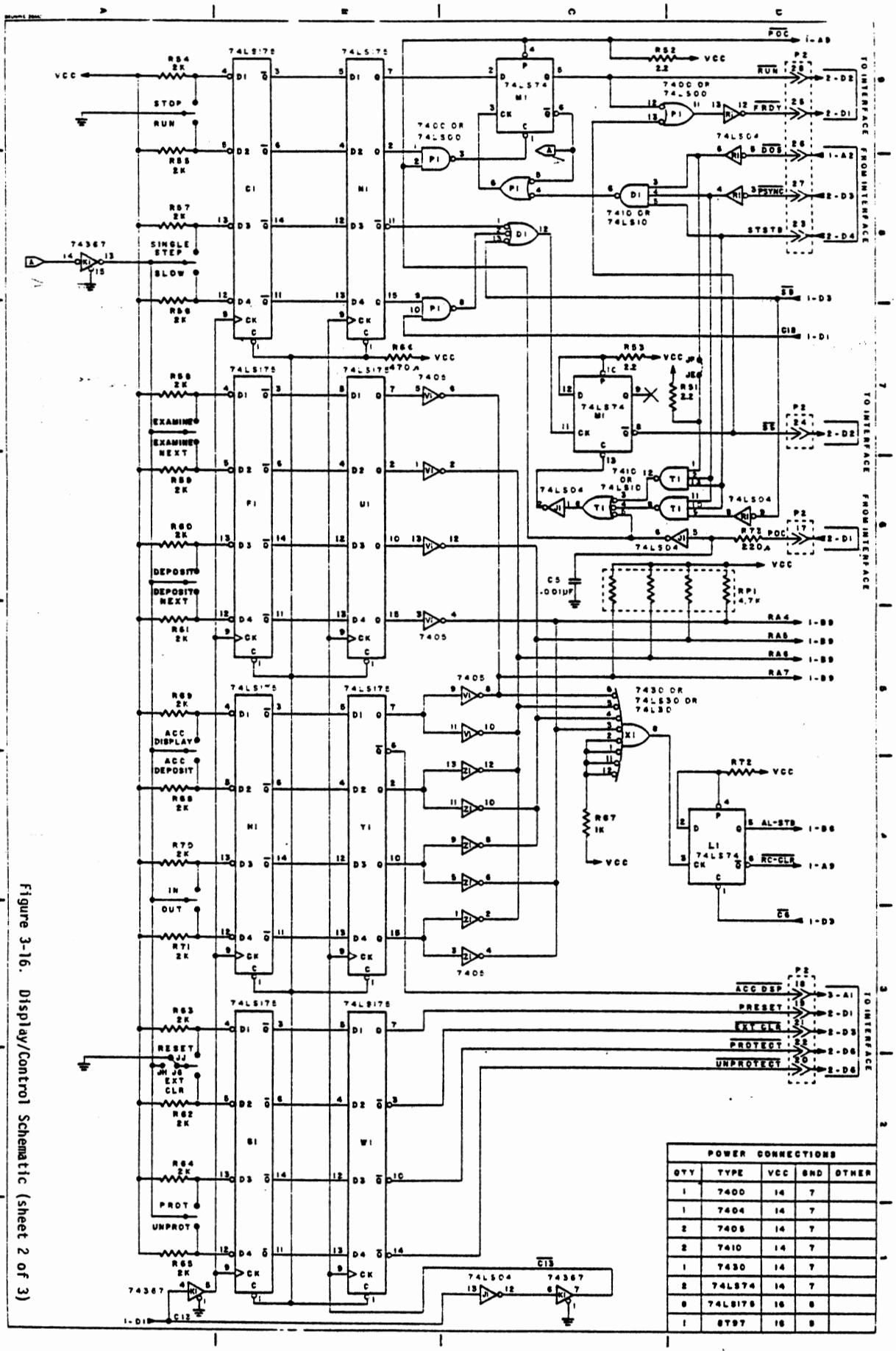


Figure 3-16. Display/Control Schematic (sheet 2 of 3)

POWER CONNECTIONS				
QTY	TYPE	VCC	GND	OTHER
1	7400	14	7	
1	7404	14	7	
2	7405	14	7	
2	7410	14	7	
1	7430	14	7	
2	74LS74	14	7	
8	74LS175	16	8	
1	8T97	16	8	

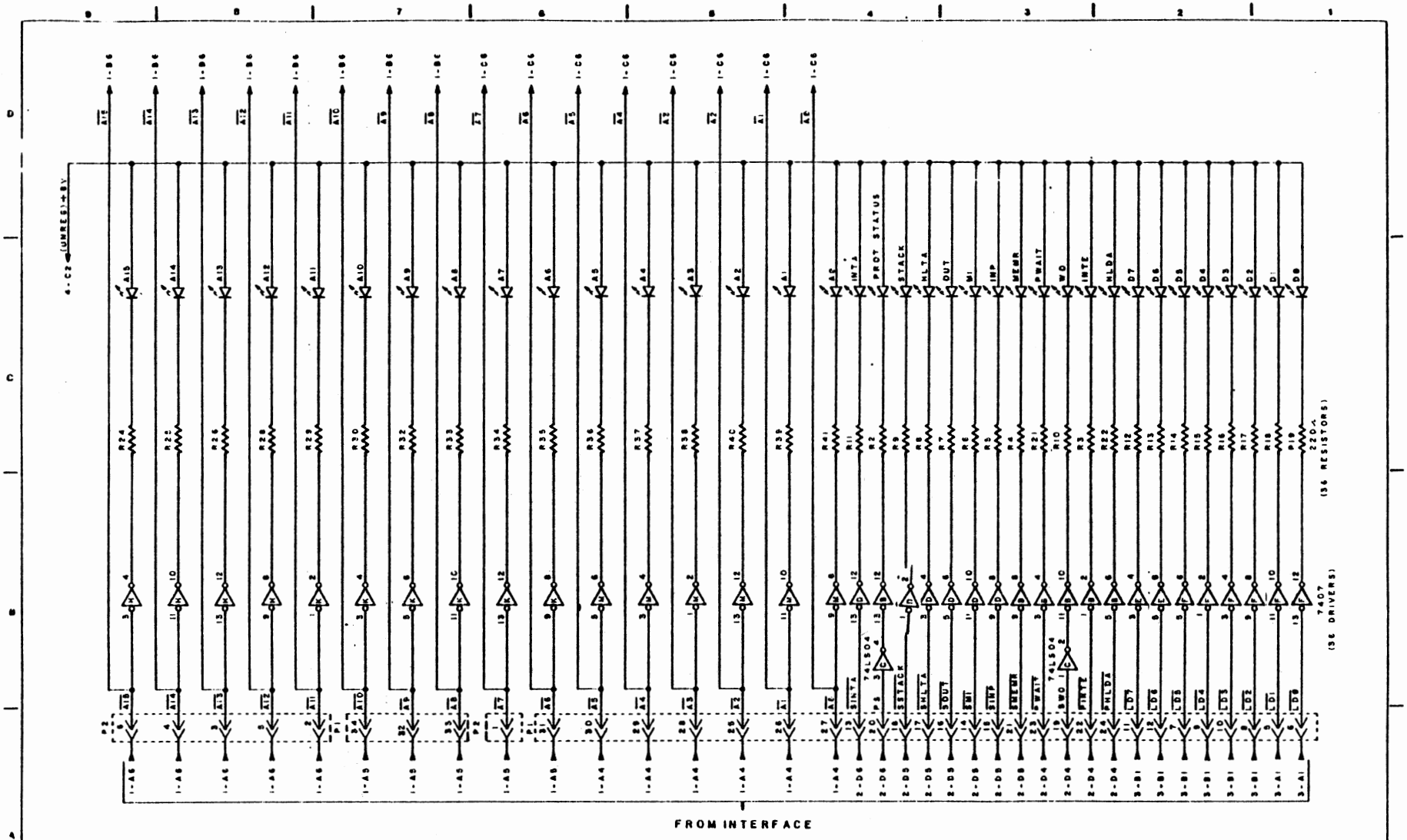
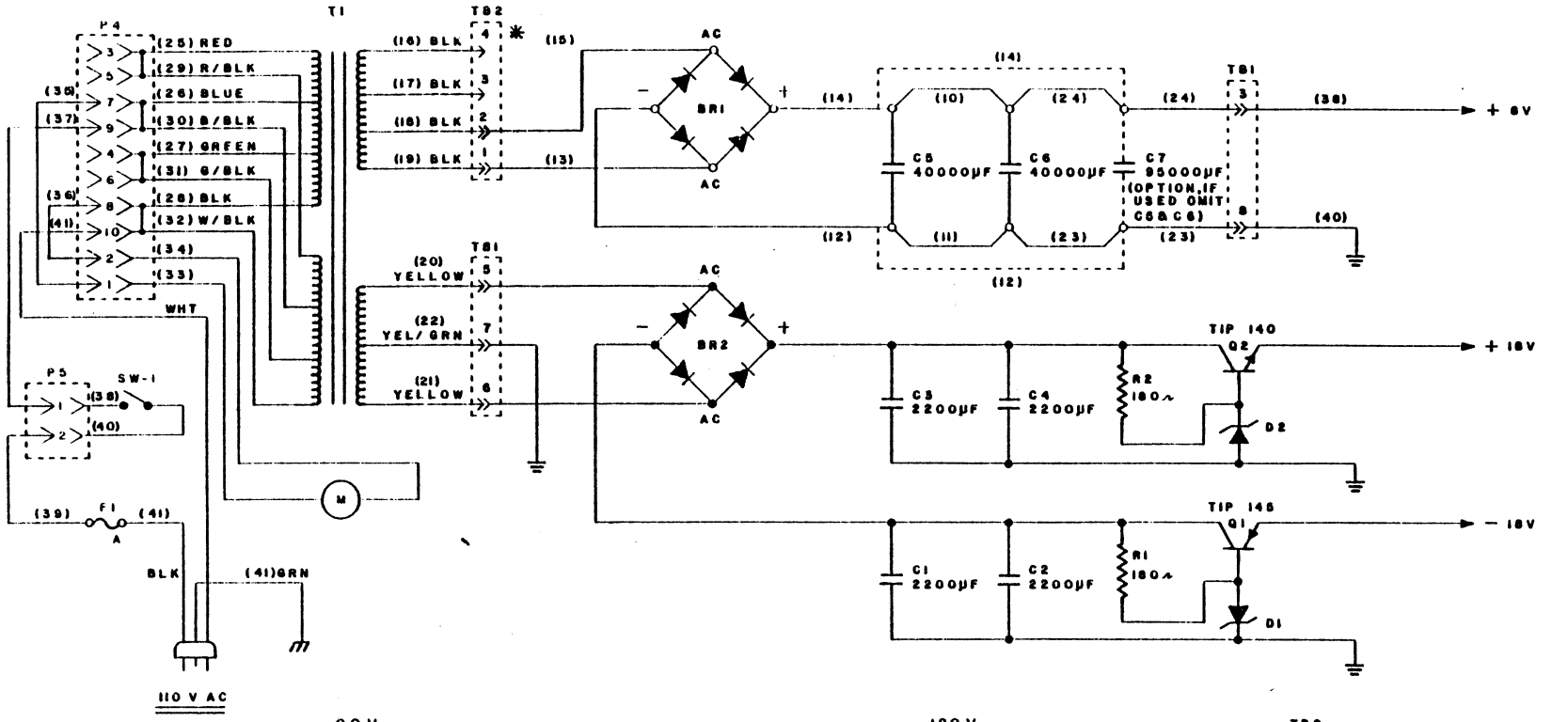


Figure 3-16. Display/Control Schematic (sheet 3 of 3)



90 V
// GREEN & GRN./BLK. TO PIN 1
// BLACK & WHT./BLK. TO PIN 2

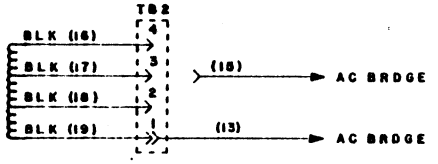
110 V
// BLUE & BLUE/BLK. TO PIN 1
// BLACK & WHT./BLK. TO PIN 2

130 V
// RED & RED/BLK. TO PIN 1
// BLACK & WHT/BLK. TO PIN 2

180 V
IN 1 WHT./BLK.
IN 2 GREEN
JUMP
BLACK & GREEN/BLK.

220 V
IN 1 WHT./BLK.
IN 2 BLUE
JUMP
BLACK & BLUE/BLK.

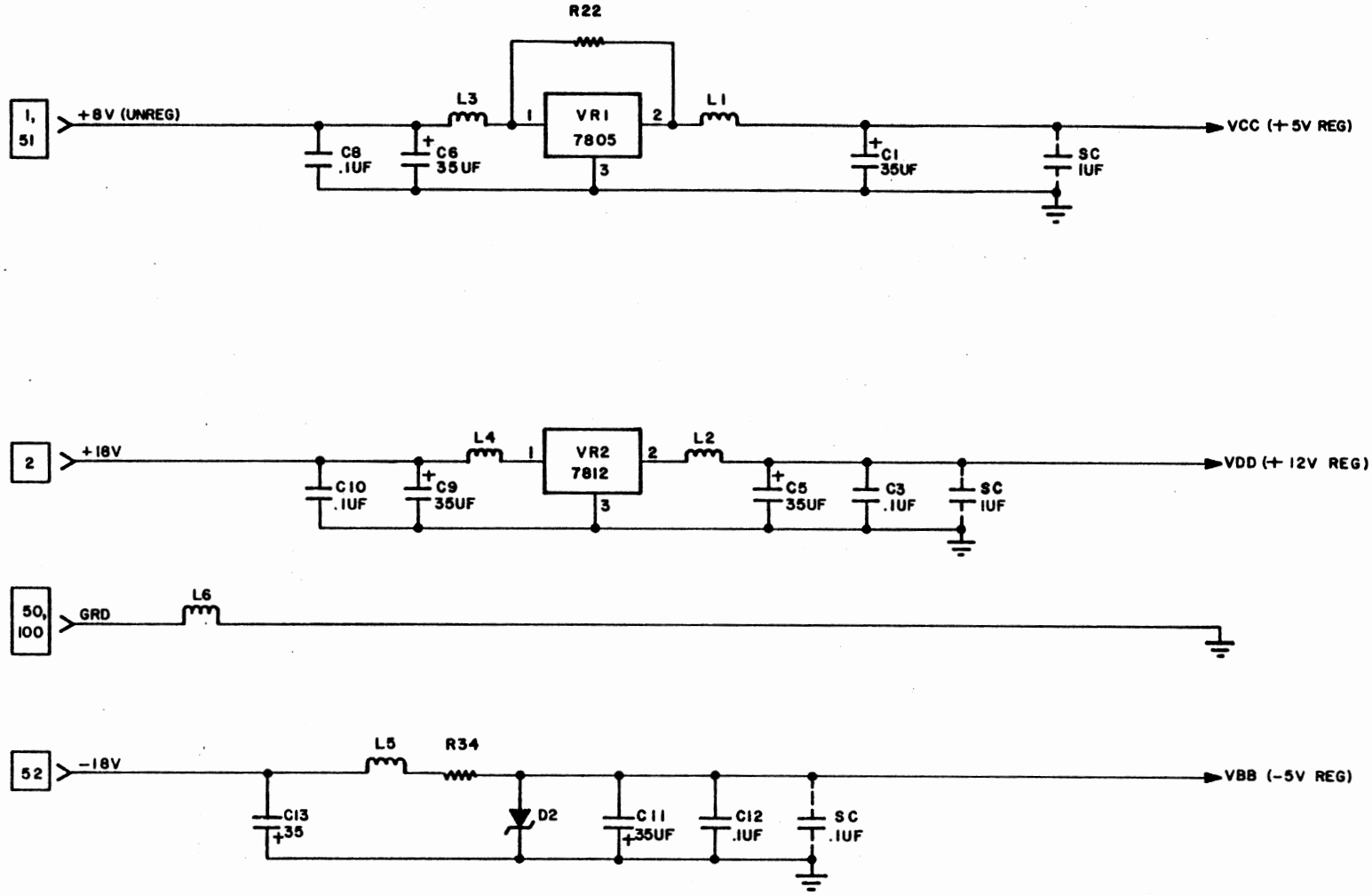
260 V
IN 1 WHT./BLK.
IN 2 RED
JUMP
BLACK & RED/BLACK



*

AMPS	TB2
0 - 4	pin 2
4 - 9	pin 3
9 - 18	pin 4

Figure 3-17. Power Supply Board Schematic



REF DESIG	TYPE	VCC	GRD	OTHER	REF DESIG	TYPE	VCC	GRD	OTHER
					M	8080A	20	2	
G, B	74LS04	14	7		J, X, R, V, N, U, P	74368 OR 8T98	16	8	
C	74LS13 OR 74LS20	14	7		K	8212	24	12	
S, Y	74LS14	14	7		D, E	8216	16	8	
					F	8224	16	8	VDD = 9
P, W	74367	16	8		A	4009	1	8	VDD = 16

Figure 3-18. CPU Voltage Regulator Schematic

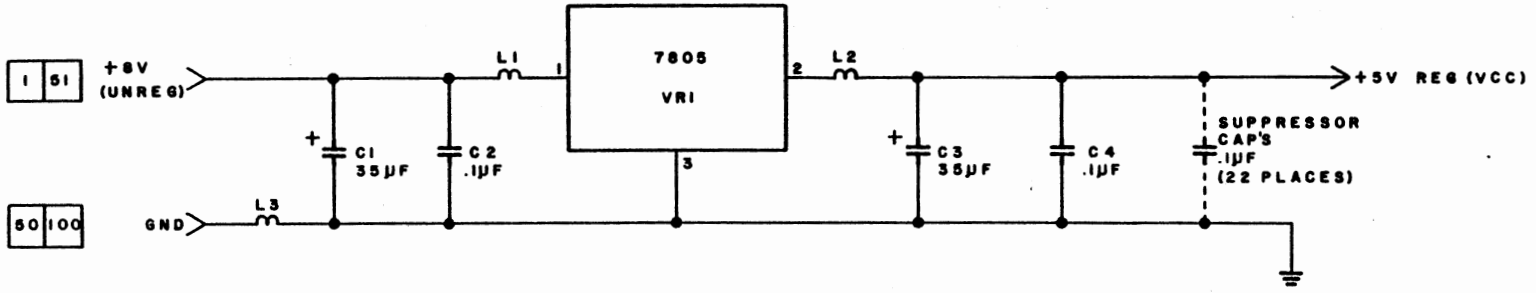


Figure 3-19. Interface Voltage Regulator Schematic

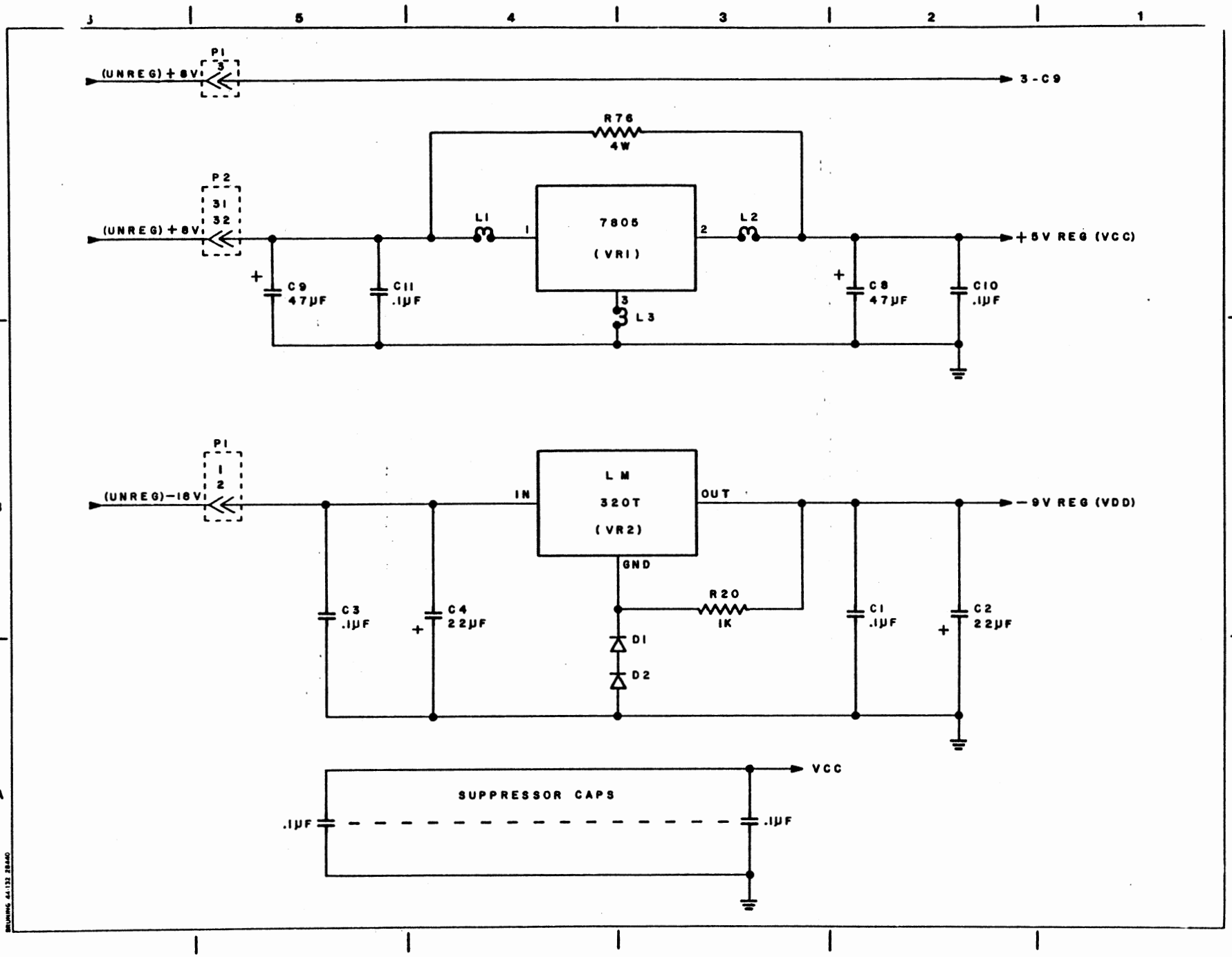


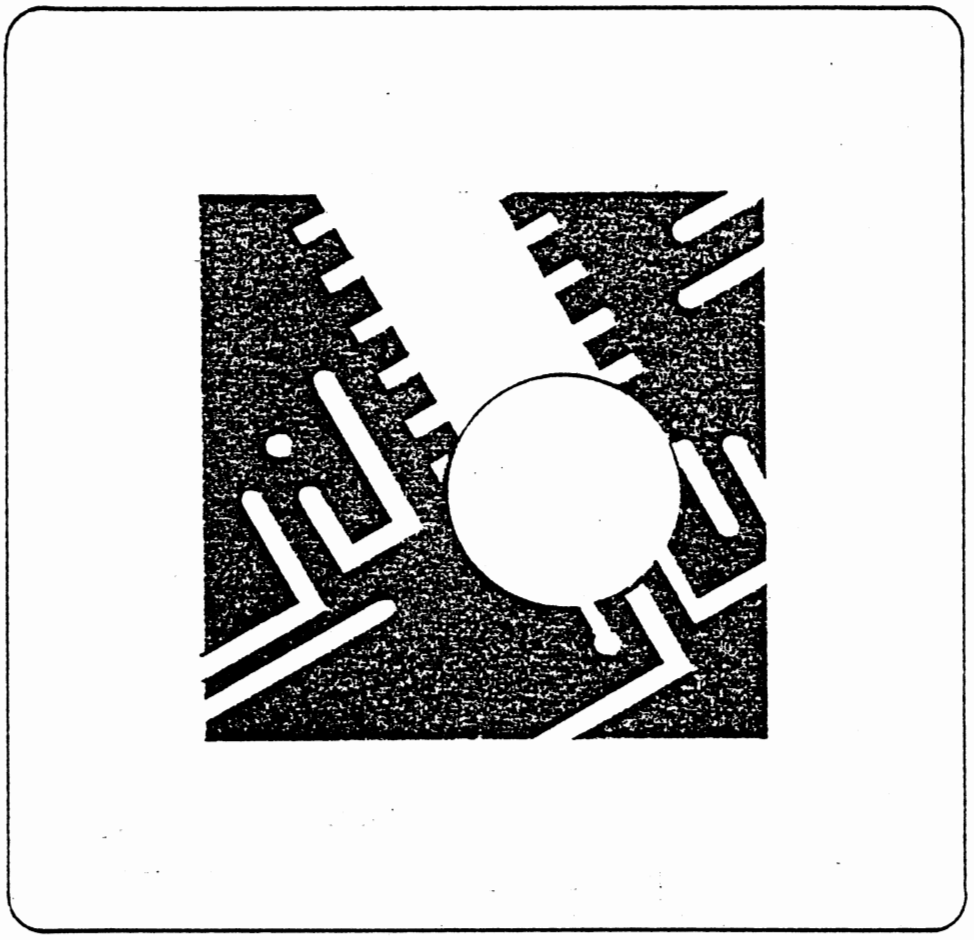
Figure 3-20. Display/Control Voltage Regulator Schematic

2450 Alamo SE
Albuquerque, NM 87106

altair 8800b

SECTION IV
TROUBLESHOOTING

SECTION IV



TROUBLESHOOTING AIDS

ALTAIR 8800b COMPUTER DOCUMENTATION

SECTION IV

TROUBLESHOOTING AIDS

Section IV, Troubleshooting Aids, is currently being printed and will be shipped to you as soon as possible.

MITS, Inc.
August, 1976

PREFACE

Section IV is designed to aid the user in pinpointing trouble areas and correcting problems that may be encountered with the Altair 8800b computer. The text that follows contains detailed instructions that should help in locating and correcting most problems. However, if the malfunction(s) cannot be rectified, send the unit to the MITS Repair Department or your local Altair dealer.

Section IV is divided into five major sections :

4-1) Introduction to Troubleshooting which contains general procedures that should always be followed, and IC static level charts showing the proper indications for the most common trouble areas;

4-2) Visual Inspection which contains procedures for locating problems caused by improper assembly;

4-3) Preliminary Check which contains tests for voltages and waveforms;

4-4) Non-PROM Related Switch Problems which concerns the RUN/STOP, SINGLE STEP/SLOW, RESET/EXTERNAL CLEAR and PROTECT/UNPROTECT switches;

4-5) PROM Related Switch Problems which deals with the EXAMINE/ EXAMINE NEXT, DEPOSIT/DEPOSIT NEXT, ACCUMULATOR DISPLAY/ ACCUMULATOR LOAD and IN/OUT switches.

Sections 4-3, 4-4 and 4-5 are presented in chart form, indicating the testing instructions, the correct indication, the incorrect indication and the procedures for remedying the problem.

Before beginning the actual troubleshooting procedures, the Theory of Operation and Section 4-1 should be reviewed. Refer to these portions of the manual when necessary.

An oscilloscope and an inexpensive multimeter will be needed to perform these troubleshooting procedures. The oscilloscope should be used to detect and measure pulses; the multimeter should be used to check voltage levels and continuity.

4-1. INTRODUCTION TO TROUBLESHOOTING

A. Basic Troubleshooting Procedures

Paragraphs 1, 2, 3 and 4 contain general instructions for testing ICs, diodes, transistors and bridge rectifiers, respectively. These procedures should be followed each time the instructions (in the tables that follow) specify that one of the above mentioned components be checked.

1. ICs
   a. With a voltmeter (or oscilloscope), check the IC pin for the proper voltage level or pulse. Make sure that the voltmeter is touching only one pin at a time; if the voltmeter should come in contact with more than one pin, erroneous readings and shorts may occur. (Note: Because the entire system is based upon the 8080 microprocessor chip, IC M on the CPU board, be especially careful when checking this component.) If the correct voltage is not present at the IC:
      1. Use the schematic to trace the signal back to its original source, checking for proper logic operation at each gate.
      2. Visually inspect the area surrounding the IC for solder bridges or opens.
   b. Never assume that when a signal leaves its source it will always reach its destination. Check for continuity with an ohmmeter (set at X1K ohms or higher to protect the ICs from the ohmmeter's current). If opens in the lands are found, solder over them.
   c. Check for power (Vcc) and Ground at the IC. Several of the schematics (in the Theory of Operation section) contain charts indicating the Vcc and Ground pins for each IC. If Vcc and Ground are present, test the IC according to the steps below.
      1) For ICs with sockets:
         a) Turn power off and remove the IC from its socket.
         b) Bend the suspected output pin up and reinstall the IC into its socket.
         c) Turn power on and check for proper logic operation.

NOTE

Removing an IC pin from its socket or from the board may change the IC's input level. When checking for proper logic, refer to the truth tables (pages 3-5 through 3-8) associated with that type of gate.

d) If the IC does not operate properly, replace it. If it does operate properly, bend the pin back and reinsert it into the socket. Look for a solder short or bridge and repair as necessary.

2) For ICs without sockets:

a) Turn power off and cut the suspected IC pin where it meets the component side of the board.

b) Bend the pin up and turn power on.

c) Check for proper logic operation (as shown in the appropriate truth table).

d) If the IC does not operate properly, replace it. If it does operate properly, resolder the pin to the board and look for a solder short or bridge. Repair as necessary.

NOTE

If an IC without a supplied socket needs to be replaced, you may wish to install a good-quality socket with it. Because sockets don't have to be removed from the board in order to test the IC, installation of sockets will aid in future troubleshooting and will prevent wear and tear on the board.

2. Diodes

Diodes can be easily tested with an ohmmeter set at X100 ohms. Turn power off and unsolder one lead from the board. To forward bias the diode, place the ohmmeter's positive lead on the diode's anode lead and the ohmmeter's negative lead on the diode's cathode lead. (The cathode lead is on the side marked with a bar.) The ohmmeter should show a LOW reading (15-300 ohms). To reverse bias the diode, transpose the ohmmeter's leads and check for a HIGH resistance reading (above 1K ohms). If the diode's readings do not correspond with the readings shown here, the diode should be replaced.

3. Transistors

Transistors can be tested with an ohmmeter set at X100 ohms. The following chart shows the correct readings for transistors with at least two leads removed from the board. Refer to the chart on page 5-9 in the Assembly section of the manual for lead identification, and compare the transistor's resistance to the resistance indicated in the chart below. Q1, Q2 and Q3 on the CPU board and Q2 on the Power Supply board are NPN transistors. Q1 on the Power Supply board is a PNP transistor.

Ohmmeter Lead Placement	Transistor Resistance NPN Transistors	PNP Transistors
Positive lead to emitter Negative lead to base	HIGH resistance	LOW resistance
Positive lead to base Negative lead to emitter	LOW resistance	HIGH resistance
Positive lead to base Negative lead to collector	LOW resistance	HIGH resistance
Positive lead to collector Negative lead to base	HIGH resistance	LOW resistance
HIGH = 2K ohms or higher LOW = 1K ohms or lower		

4. Bridge Rectifiers

Unplug the chassis, remove the AC wires to TB1 and refer to the Diode testing instructions on page 4-6 to test the bridge rectifiers.

B. Normal Output Voltage Levels

1. TTL Gates (7400 Series ICs) and MOS ICs:

Condition	Voltage
Valid LOW	.8v or less
Valid HIGH	2v - 4v

An output in the range of .8v - 2v indicates a problem. (Note: Voltages can vary ±10%.)

2. Open Collector Gates

Open collector outputs, such as those of ICs Y, W, U, F, B and K on the Display/Control board, must be connected to +5v or +8v to operate properly. The outputs of ICs Y, W and U are tied to Vcc through resistors R41-R48 when the corresponding address switch is in the "up" position. When the switch is in the down

position, the output will be disconnected from Vcc and will not allow signals to go through.

3. Tri-State Buffers (when enabled)

Condition	Voltage
Valid LOW	.8v or lower
Valid HIGH	2v or higher

An output in the range of .8v - 2v indicates a problem. (Note: Voltages can vary ±10%.)

When disabled, tri-state buffers will have various voltages at their outputs.

C. Static Levels

1. IC Levels

Table 4-1, starting on page 4-9, shows the proper static levels of the most common problem areas, assuming the computer is in a "stopped" state (M1, MEMR and WAIT).

Table 4-1. Static Levels of the Most Common Problem Areas

Board	Schematic	IC	Pin #	Static Level
Display/Control	3-16, sheet 1 of 3	G	17, 18, 19, 20	HIGH
		P	2, 8, 9, 11, 14	LOW
		P	12	HIGH
		N	8	LOW
		A	4, 6, 8, 10, 15, 17, 19, 21	LOW
		R	15, 1	HIGH
		S	1	HIGH
		Y	1, 3, 5, 11, 9, 13	LOW
		W	13, 9, 11, 5, 3, 1	LOW
		U	1, 9, 11, 13	LOW
		J	8, 12	HIGH
		Z	5	C8 (see waveform #5, page 4-30)
		V	8	HIGH
		J	4, 2	CS
		E1	6	CS
		A	13	CS
	3-16, sheet 2 of 3	C1, F1, H1, G1, N1, U1, Y1, W1	9	C13 (see waveform #4, page 4-29)
		V1	6, 2, 4, 12, 8, 10	HIGH
		Z1	2, 4, 6, 8, 10, 12	HIGH
		K1	13	LOW
		M1	11	LOW
		M1	8, 13	HIGH
		L1	3, 5	LOW

Table 4-1 (continued)

Board	Schematic	IC	Pin #	Static Level
		L1	1	$\overline{C6}$ (see waveform #6, page 4-30)
		R1	12	HIGH
		M1	2	LOW
		M1	1, 3, 5	HIGH
Interface	3-15, sheet 3 of 3	G	2, 13, 14	HIGH
		G	1, 11	LOW
		K	6	HIGH
		D	10	LOW
		J	11	HIGH
		K	8	HIGH
	3-15, sheet 2 of 3	B	6, 2, 12, 13	HIGH
		E	2, 4, 6, 8, 10, 12	LOW
		M	2, 12	LOW
		A	12, 13, 6, 2	HIGH
		A	1, 8	LOW
		N	6, 10	LOW
		N	4, 2	HIGH
		H	14	LOW
CPU	3-14	C	6, 13	LOW
		C	8, 4	HIGH
		M	23, 12	LOW
		D, E	15	HIGH
		F	7, 2	HIGH

2. Mother Board Static Levels

Table 4-2 shows the proper static levels of the mother board, assuming the computer is in a "stopped" state (M1, MEMR and WAIT). Note that the levels on the pins of the 8080a (IC M on the CPU board) are reflected on the mother board as well as the front panel LEDs. For example:

A HIGH level on pin 24 (WAIT) of IC M on the CPU board causes bus pin 27 to go HIGH, which in turn causes the WAIT light on the front panel to light.

HIGH pulses on pin 27 (address line A2) of IC M on the CPU board produce pulses on bus pin 81, which cause A2 on the front panel to light (dimly).

Table 4-2. Mother Board Static Levels

Bus #	Symbol	Name	Static Level
1	+8v	+8 volts	
2	+18v	+18 volts	
3	XRDY	EXTERNAL READY	HIGH
4	VI0	VECTORED INTERRUPT LINE #0	LOW
5	VI1	VECTORED INTERRUPT LINE #1	LOW
6	VI2	VECTORED INTERRUPT LINE #2	LOW
7	VI3	VECTORED INTERRUPT LINE #3	LOW
8	VI4	VECTORED INTERRUPT LINE #4	LOW
9	VI5	VECTORED INTERRUPT LINE #5	LOW
10	VI6	VECTORED INTERRUPT LINE #6	LOW
11	VI7	VECTORED INTERRUPT LINE #7	LOW
12*	XRDY2	Extra READY Line	HIGH
13-17	Not Used		
18	$\overline{\text{STA DSB}}$	$\overline{\text{STATUS DISABLE}}$	HIGH
19	$\overline{\text{C/C DSB}}$	$\overline{\text{COMMAND/CONTROL DISABLE}}$	HIGH
20**	UNPROT	UNPROTECT	LOW
21**	SS	SINGLE STEP	LOW
22	$\overline{\text{ADD DSB}}$	$\overline{\text{ADDRESS DISABLE}}$	HIGH
23	$\overline{\text{DO DSB}}$	$\overline{\text{DATA OUT DISABLE}}$	HIGH
24	Ø2	PHASE 2 CLOCK	See waveforms 2 and 3, page 4-26
25	Ø1	PHASE 1 CLOCK	See waveforms 2 and 3, page 4-26

Bus #	Symbol	Name	Static Level
26	PHLDA	HOLD ACKNOWLEDGE	LOW
27	PWAIT	WAIT	HIGH
28	PINTE	INTERRUPT ENABLE	LOW
29	A5	ADDRESS LINE #5	
30	A4	ADDRESS LINE #4	
31	A3	ADDRESS LINE #3	
32	A15	ADDRESS LINE #15	
33	A12	ADDRESS LINE #12	
34	A9	ADDRESS LINE #9	
35	DO1	DATA OUT LINE #1	
36	DO0	DATA OUT LINE #0	
37	A10	ADDRESS LINE #10	
38	DO4	DATA OUT LINE #4	
39	DO5	DATA OUT LINE #5	
40	DO6	DATA OUT LINE #6	
41	DI2	DATA IN LINE #2	
42	DI3	DATA IN LINE #3	
43	DI7	DATA IN LINE #7	
44	SM1	M1 (Instruction Fetch Cycle)	HIGH
45	SOUT	OUT (Output Write)	LOW
46	SINP	INP (Input Read)	LOW
47	SMEMR	MEMR (Memory Read)	HIGH
48	SHLTA	HLTA (Halt Acknowledge)	LOW
49	$\overline{\text{CLOCK}}$	$\overline{\text{CLOCK}}$	See Waveforms 2 and 3, page 4-28
50	GND	GROUND	
51	+8v	+8 volts	
52	-18v	-18 volts	
53**	$\overline{\text{SSW DSB}}$	$\overline{\text{SENSE SWITCH DISABLE}}$	HIGH
54	$\overline{\text{EXT CLR}}$	$\overline{\text{EXTERNAL CLEAR}}$	HIGH
55	RTC	REAL TIME CLOCK	
56*	$\overline{\text{STSTB}}$	$\overline{\text{STATUS STROBE}}$	HIGH
57**	DIG1	DIGITAL #1	HIGH
58**	FRDY	Front Panel READY	LOW
59-67	Not Used		
68	MWRT	MEMORY WRITE	LOW
69	$\overline{\text{PS}}$	$\overline{\text{PROTECT STATUS}}$	HIGH

Bus #	Symbol	Name	Static Level
70**	PROT	PROTECT	LOW
71**	RUN	RUN	LOW
72	PRDY	READY	HIGH
73	$\overline{\text{PINT}}$	$\overline{\text{INTERRUPT REQUEST}}$	HIGH
74	$\overline{\text{PHOLD}}$	$\overline{\text{HOLD}}$	HIGH
75	$\overline{\text{PRESET}}$	$\overline{\text{RESET}}$	HIGH
76	PSYNC	SYNC	LOW
77	$\overline{\text{PWR}}$	$\overline{\text{WRITE}}$	HIGH
78	PDBIN	DATA BUS IN	HIGH
79	A0	ADDRESS LINE #0	
80	A1	ADDRESS LINE #1	
81	A2	ADDRESS LINE #2	
82	A6	ADDRESS LINE #6	
83	A7	ADDRESS LINE #7	
84	A8	ADDRESS LINE #8	
85	A13	ADDRESS LINE #13	
86	A14	ADDRESS LINE #14	
87	A11	ADDRESS LINE #11	
88	DO2	DATA OUT LINE #2	
89	DO3	DATA OUT LINE #3	
90	DO7	DATA OUT LINE #7	
91	DI4	DATA IN LINE #4	
92	DI5	DATA IN LINE #5	
93	DI6	DATA IN LINE #6	
94	DI1	DATA IN LINE #1	
95	DI0	DATA IN LINE #0	
96	SINTA	INTA (Interrupt Request Acknowledge)	LOW
97	$\overline{\text{SWO}}$	$\overline{\text{WO}}$ (Write Operation)	HIGH
98	SSTACK	STACK	LOW
99	$\overline{\text{POC}}$	POWER ON CLEAR	HIGH
100	GND	GROUND	

* = Not used in 8800a system.

** = Not used in 8800b Turnkey system.

Note: If a static level is not indicated, the signal can be either HIGH or LOW.

4-2. VISUAL INSPECTION

A. Component Inspection

The first step in troubleshooting is to carefully examine each board for solder bridges, open lands, misplaced components, etc. A thorough inspection of this kind will eliminate one possibility for errors and will allow troubleshooting efforts to be concentrated elsewhere. Carefully check each board using the list below:

1. Look for solder bridges.
2. Look for leads that have not been soldered.
3. Look for cold solder connections (cold solder connections do not have a "shiny" appearance).
4. Examine the board's lands for "hairline opens" or bridges."
5. Check the ICs for proper pin placement and good socket connections.
6. Examine the electrolytic and tantalum capacitors for proper polarity.
7. Examine the diodes for proper polarity.
8. Examine the LEDs for proper polarity.
9. Check the color codes on all resistors.

B. Wiring Inspection

> CAUTION
> The computer should be unplugged for this check.

1. Referring to Figure 5-50 on page 5-58 in the Assembly section of the manual, check for incorrect wiring on the mother board.
2. With an ohmmeter, check the power supply wiring on the terminal block (TB1). Check for resistance (about 100 ohms) between pins 2 and 7, 10 and 7, 1 and 7, 2 and 10, 2 and 1 and 1 and 10. If a reading of less than 10 ohms appears, recheck the wiring. Also check continuity from mother board bus pins 1, 2, 52 and 50 to corresponding terminal block pins 2, 10, 1 and 7. If a reading of more than 100 ohms appears, inspect the wiring from the mother board to TB1.

4-3. PRELIMINARY CHECK

The procedures outlined in Section 4-3 are general tests that should be made before going on to the specific problems presented in Sections 4-4 and 4-5. Follow the instructions in the order in which they are given, and always complete each step before going on to the next.

1. Before installing the boards and applying power to the computer, use an ohmmeter to check the resistance of the edge connectors on the mother board. Test the consecutively numbered pins down each row (1, 2, 3 . . . etc.), then cross check the pins (1-51, 2-52 . . . etc.). A LOW resistance reading should appear at pins 1, 50, 51 and 100. If a LOW reading appears at any other location, examine the back of the board for solder bridges or etching errors.
2. Turn the computer on and check for the following voltages on the Power Supply board's terminal block (TB1). See page 5-58 in the Assembly section of the manual for pin locations.

Pin #	Voltage
2, 3, 4	+8v to +10v (unregulated)
10	+16v to +18v (pre-regulated)
1	-16v to -18v (pre-regulated)
7, 8	Ground

WARNING

When testing components on the Power Supply board, be extremely careful not to touch the AC wiring. Always unplug the chassis when testing continuity or replacing components.

a. If the +8 voltage is absent from pins 2, 3 or 4 of TB1, check for AC at pins 1 and 2 of TB2. If absent, unplug the chassis and check continuity and wiring at connector P4. Also check the fuse and the wiring to the AC cord. Plug in the chassis. If AC is present at pins 1 and 2 of TB2, check the wiring from TB2 to BR1 and from BR1 to TB1. If AC is present at BR1, but no output voltage appears across the "+" and "-" pins of BR1, BR1 is probably defective and should be replaced.

b. If the correct voltage does not appear at pin 10 or pin 1 of TB1, check the voltage at the base of transistor Q2 (for pin 10) and Q1 (for pin 1). If the reading is 27 volts, the transistor or diode may have shorted out. Test these components according to the instructions on pages 4-6 and 4-7.

Check for AC at TB1 pins 6 and 5. If absent, unplug the chassis and check the wiring from connector P4 to the AC cord. If AC is present at TB1, check for AC at BR2. If AC is absent at BR2, check the wiring to BR2. If AC is present at BR2, remove the "+" pin from the board and check for voltage across the "+" and "-" pins. If voltage is not present, replace BR2.

c. If Ground does not appear at pins 7 and 8 of TB1, check the wiring from TB1 to the cross member and from the AC cable to the cross member.

3. If the fuse on the back panel blows:
   a. Check for solder bridges on the Power Supply board or the mother board.
   b. Check for proper orientation of BR2 on the Power Supply board and BR1 on the back panel.
   c. Check wiring on:
      1) voltage wires on the mother board
      2) front panel switch
      3) AC power cord
      4) Ground to +8v line
   d. Check for pinched wires and incorrectly installed components.
4. Turn power off, and install the CPU and Interface boards.

> **WARNING**
>
> Always turn power off when removing or installing plug-in boards or when connecting or disconnecting the Display/Control board. Failure to turn power off may cause damage to the board and the computer. Note that capacitor C7 (on the cross member) will retain a +8v charge for a few minutes after power has been turned off.

Connect the Interface board cables (P1 and P2) to the front panel and connect P3 from the CPU board to the Interface board. Turn power on. The computer should be automatically reset and in a stopped state.

If there are no memory boards in the computer at address Ø, the front panel LEDs should appear as follows:

LED	Condition
AØ-A15	OFF
M1, MEMR, WAIT	ON
DØ-D7	ON

If a memory board is present at address Ø, the DØ-D7 LEDs will show the random pattern for that board.

Table 4-3. Voltage and Waveform Check

Note: The following checks should be made with the CPU, Interface and Display/Control boards installed and with power turned on (unless otherwise specified) Voltages may vary ±10%.

Step	Instructions	If Correct	If Incorrect
1	Check the 7805 voltage regulators on the CPU and Interface boards.	Both regulators should read +5v at pin 2. The figure below shows the correct pin locations for all voltage regulators. 	If voltage is incorrect, refer to schematics 3-18 and 3-19. Check pin 3 for Ground. If absent, trace continuity back to bus pin 100 or 50. Pin 1 is the unregulated output--at least 8v. If absent, trace continuity back to bus pins 1 and 51. If Ground and sufficient unregulated voltage are present at these pins, check pin 2 of the voltage regulator for +5v. If voltage is absent, turn power off and remove voltage regulator pin 2 from the board. Turn power on and recheck for +5v. If the voltage is still below +5v, the voltage regulator is defective and should be replaced. If voltage is correct, look for a short on the board. With power off, resolder pin 2 to the board.
2	Check the 7812 voltage regulator on the CPU board.	It should read +12v at pin 2. Proceed to Step 3.	If voltage is incorrect, refer to schematic 3-18 and check pin 3 for Ground. If absent, trace continuity to bus pin 100 or 50. Pin 1 is the unregulated output--at least 16v. If voltage is absent, trace continuity back to bus pin 2. If Ground and sufficient unregulated voltage are present, check pin 2 of the voltage regulator for a +12v signal. If absent, turn power off and disconnect voltage regulator pin 2 from the board.

Step	Instructions	If Correct	If Incorrect
			Turn power on and check again for the +12v signal. If the voltage is below 11v, the voltage regulator should be replaced. If the voltage is correct, look for a short on the board. Resolder pin 2 to the board.
3	Check the anode lead of diode D2 on the CPU board.	It should read -5v. Proceed to Step 4.	If the voltage is incorrect, check D2 for proper polarity. Check for -18v on capacitor C13 (negative side) on the CPU board. If absent, trace continuity to bus pin 52. Turn power off and check diode D2 according to the instructions on page 4-6. Replace, if necessary. With an ohmmeter set at X10K or higher, check the resistance from the negative side of C11 to Ground. A reading of zero ohms indicates a short on the board. Resolder the anode lead of D2 to the board.
4	Check pin 2 of VR2 on the Display/Control board.	It should read -9v. Proceed to Step 5.	If the voltage is incorrect, check for -18v on pin 3 of the voltage regulator. If absent, trace continuity back to bus pin 2. Check for the correct part number on VR2, D1, D2 and R20. Turn power off and remove the anode lead of diodes D1 and D2 from the board. Check both diodes according to the instructions on page 4-6. If the readings are incorrect, replace D1 and/or D2. Remove pin 2 of VR2 from the board. Turn power on and check for a -9v reading at VR2. If incorrect, replace VR2. If correct, look for a short on the board. Resolder the output pin to the board.

Step	Instructions	If Correct	If Incorrect
5	On the CPU board, check the voltage on IC M pins 20, 11 and 28. Be careful not to touch more than one pin at a time.	Pin 20 should read +5v. Pin 11 should read -5v. Pin 28 should read +12v. Proceed to Step 6.	If incorrect, use an ohmmeter set at X10K or higher to trace continuity back to the CPU board's voltage regulators. If opens are found, solder over them.
6	On bus pins 24 and 25, check for proper Ø2 and Ø1 waveforms (see waveforms 2 and 3, page 4-28). On the CPU board, check for Ø2 and Ø1 on corresponding pins, 22 and 15 of IC M. (See waveform #1, page 4-27.)	If present, proceed to Step 7.	If Ø2 and Ø1 waveforms are absent on the bus pins, trace logic through ICs J and A on the CPU board. If Ø2 or Ø1 is present at the inputs of IC J or IC A, but absent at the outputs, check the IC according to the instructions on page 4-5. If there is no Ø1 or Ø2 signal at IC A (pin 14 or 7), trace continuity to pins 10 and 11 of IC F. (Note: Ø1 and Ø2 are 12v in amplitude at pins 10 and 11.) If signals are absent at pins 10 and 11, check for +12v at pin 9 of IC F. If absent, trace continuity to VR2 pin 2 on the CPU board. Check for an 18 MHz signal at pins 14 and 15 of IC F. If absent, check IC F according to the instructions on page 4-5, and replace if necessary.
7	On bus pin 99, check for a HIGH $\overline{\text{POC}}$ level. This signal is usually a 4 VDC level with a small amount of AC ripple voltage.	If present, proceed to Step 8.	Visually inspect transistors Q1, Q2 and Q3 and diode D1 on the CPU board for proper installment. Check the base of Q1 for a 1v level. If absent, check D1 according to the instructions on page 4-6. Replace if necessary. Q1 should be active, causing a 0v level to appear at the base of Q2. If this 0v level is absent, check Q1 according to the instructions on page 4-6. Q2 should cause a 5v signal to appear at

Step	Instructions	If Correct	If Incorrect
			the base of Q3. If the 5v signal is absent, check Q2 according to the instructions on page 4-6. Then turn power off, and wait a moment for C4 to discharge. Remove one of the leads of C4 from the board, and measure C4's resistance with an ohmmeter. (Note: The ohmmeter needle may fluctuate slightly.) If the reading is lower than 10 ohms, replace C4. If C4 is working properly, reinstall C4 and check continuity from the base of Q3 to Vcc. Repair as necessary. The Q3 emitter should be above 2v. If not, check Q3 according to the instructions on page 4-7. Trace this HIGH level through ICs S and J on the CPU board to bus pin 99. If ICs S and J do not invert the signal, test the ICs according to the instructions on page 4-5.
8	Pin 13 (HOLD) of IC M on the CPU board should be LOW.	Proceed to Step 9.	If a LOW is not present at IC M pin 13, check IC G on the CPU board according to the instructions on page 4-5. Check for Vcc at resistors R23 and R40. If absent, check continuity and repair as necessary. Bus pin 74 should be HIGH. If not, look for a short on the mother board.
9	On the Display/Control board check for Ø2 at pin 10 of IC L. If Ø2 is absent, the entire front panel will not operate.	If present, proceed to Step 10.	If Ø2 is absent at IC L pin 10, trace continuity and logic from IC S1 on the Display/Control board through IC T on the Interface board to bus pin 24. Any inverter having a Ø2 input, but no Ø2 output,

Step	Instructions	If Correct	If Incorrect
	(Note: If you received your 8800b computer before January, 1977, an extra capacitor, C7, for the Display/Control board was included in the installation instructions. This capacitor is not needed and should be removed.)		should be checked according to the instructions on page 4-5. If the IC(s) are functioning properly, look for a short and repair as necessary.
10	On the Display/Control board, check for a $\overline{C13}$ signal (see waveform #4, page 4-29) at pin 9 of ICs C1, N1, F1, U1, H1, Y1, G1 and W1. (Note: If no switches are pressed, R54-R65 should produce a signal of approximately 4v at the input pins of these ICs.)	If present, proceed to Step 11.	If absent, trace the $\overline{C13}$ signal through ICs K1, J1, E1 and S1 to IC X pin 9 on the Display/Control board. If any of these ICs have a C13 input, but no C13 output, they should be checked according to the instructions on page 4-5. If IC X pin 9 has no C13 signal, check for a square wave (approximately .1 ms. wide) at pin 10 of IC X. If present, check IC X according to the instructions on page 4-5. If a square wave is not present at pin 10 of IC X, check IC L. If a square wave is not present at pin 1 of IC L when it is removed from the board, replace IC L.
11	Check for a HIGH $\overline{POC}$ level at ICs M1 pin 4, P1 pin 2, T1 pin 5 and Z pin 13 on the Display/Control board.	If present, proceed to Step 12.	If a LOW appears at any of the pins, trace $\overline{POC}$ from the suspected pin to pin 6 of IC J1 on the Display/Control board. If $\overline{POC}$ is absent at pin 6, check IC J1 according to the instructions on page 4-5. Check the Vcc connection at R42. If Vcc is absent, check continuity to VR1 pin 2 on the Display/Control board. Check the logic operation of the

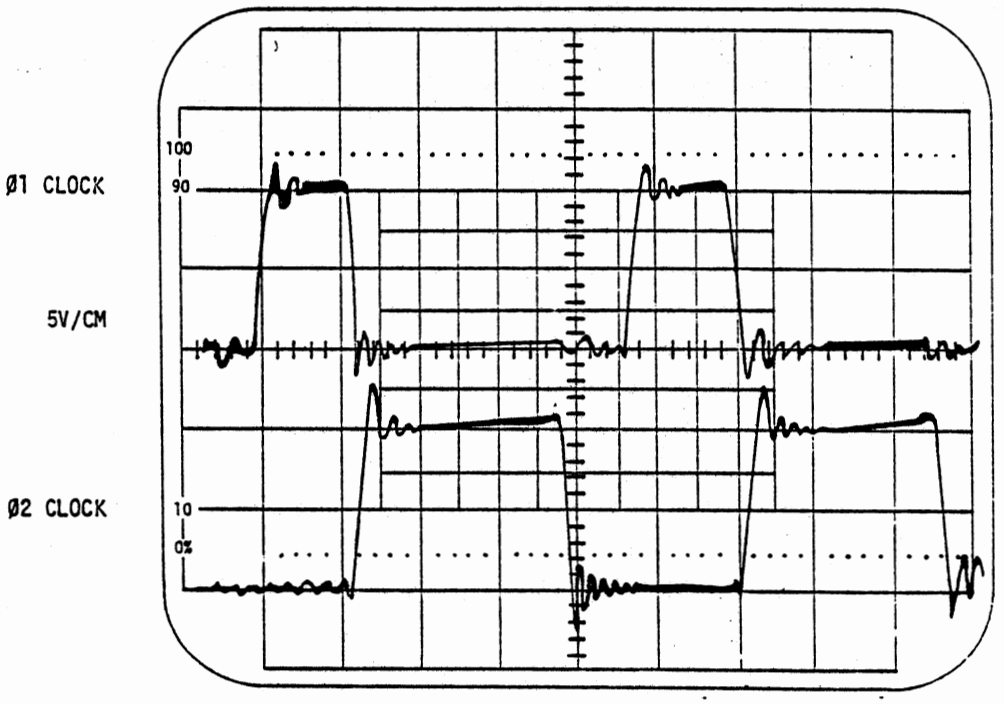
Step	Instructions	If Correct	If Incorrect
			ICs from J1 through U on the Interface board to bus pin 99. Check and replace the ICs if necessary.
12	On the Display/Control board, check for a LOW at pin 13 of IC K1. (Note: If the computer is running, pin 13 will be HIGH and only the RUN/STOP or RESET/EXT CLR switches will work.)	If present, proceed to Step 13.	If the computer is not in a run state and a LOW is not present at pin 13, trace logic from IC K1 to a LOW at IC M1 pin 6. Check any suspected ICs according to the instructions on page 4-5. If lifting the STOP switch does not stop the computer, continue with the remaining steps in this chart and onto Section 4-4.
13	On the Display/Control board, check for a CS signal (see waveform #5, page 4-30) at pin 13 of IC A.	If the proper CS signal is present, proceed to Step 14.	If the CS signal does not match waveform #5, examine IC V pins 1, 2 and 13 on the Display/Control board. Pin 1 should be a 64 µsec. pulse width square wave; pin 2 a 32 µsec. pulse width square wave; and pin 13 a 16 µsec. pulse width square wave. If all of these signals are present, check ICs V and E1 according to the instructions on page 4-5. If any of the signals are absent from pins 1, 2 and 13 of IC V, trace the signal back through ICs E1 and S1 to IC L. Any ICs that have input signals but no output signals should be checked according to the instructions on page 4-5. If all of the ICs are operating properly, check for the corresponding square waves at pins 2, 4 and 13 of IC L. If absent, check IC L according to the instructions on page 4-5.

Step	Instructions	If Correct	If Incorrect
14	On the Display/Control board, check pin 1 of IC L1 for a $\overline{C6}$ signal (see waveform #6, page 4-30).	If present, proceed to Step 15.	If absent or incorrect, check the logic operation from IC S1 to pin 2 of IC L. Check for a 16 µsec. square wave pulse at pin 2 of IC L. If absent, check the IC according to the instructions on page 4-5.
15	On the Display/Control board, check pin 5 of IC Z for a C8 signal (see waveform #5, page 4-30).	If present, proceed to Step 16.	If absent, trace logic through ICs E1 and S1 to pin 13 of IC L on the Display/Control board. If E1 or S1 has an input signal but no output signal, check that IC according to the instructions on page 4-5. If an output is not present at IC L pin 13, check IC L.
16	On the Display/Control board, examine the PROM, IC G. It should be labelled B D/C. If it is <u>not</u> labelled B D/C, contact the MITS Marketing Dept. or your local Altair dealer. Check for Ground at pin 14; for +5v at pins 12, 13, 15, 22 and 23; and for -9v at pins 24 and 16 (of IC G).	If IC G is labelled B D/C and if the voltage levels are correct, proceed to Step 17.	If the +5v signal is absent, use an ohmmeter set at X1K or higher to trace continuity to VR1 pin 2. (Note: If another computer with a PROM board is available, the data in the suspected PROM can be checked by installing it in the other computer's PROM board and examining its output with Table 3-2 in the Theory of Operation section.) If the -9v signal is absent, use the ohmmeter to trace continuity to VR2 pin 2.
17	When the RESET switch is held, all address lights and data lights should be lit. All status lights except WO should be lit if PRESET on the CPU board is connected to pin 14 of	If the correct LEDs are lit, proceed to Section 4-4 (if problems exist with the RUN/STOP, SINGLE STEP/SLOW or PROTECT/UNPROTECT switches). Then proceed to Section 4-5	If pin 2 of IC F on the CPU board does not go LOW with RESET, a problem exists in the RESET circuitry; proceed to Section 4-4. When the RESET switch is pressed and pin 2 goes LOW, pin 1 of IC F should go HIGH. If not, check IC F according to the instructions on page 4-5. A HIGH at pin 1

Step	Instructions	If Correct	If Incorrect
	IC K. (Note: If the pins of IC M on the CPU board are HIGH, the corresponding LEDs on the front panel should be lit.)	If problems exist with the EXAMINE/EXAMINE NEXT, DEPOSIT/DEPOSIT NEXT, ACCUMULATOR DISPLAY/ ACCUMULATOR LOAD, or IN/ OUT switches.	of IC F should cause a HIGH at pin 12 of IC M. If not, check continuity and repair as necessary. If any of the address lights or data lights are not lit when the RESET switch is held, the problem may be due to shorts or defective LEDs. RESET should cause all data lines (DØ-D7) and address lines (AØ-A15) from IC M on the CPU board to go HIGH. If any of these lines fail to go HIGH when pin 12 of IC M is HIGH, check for shorts and repair as necessary. If any of the address or data lights are unlit when RESET is lifted, start at the corresponding pin of IC M on the CPU board and trace the levels through the Interface board to the Display/Control board. The address lights correspond to AØ-A15 (IC M pins 25, 26, 27, 1, 29-40) and the data lights correspond to DØ-D7 (IC M pins 3-10). To trace the data lines (DØ-D7), pins 1 and 15 of both ICs D and E on the CPU board should be LOW. If pin 1 is not LOW, trace continuity to pin 3 of VR1. If pin 15 is not LOW, trace logic to a LOW at pin 17 of IC M on the CPU board. If pin 17 is not LOW, check IC M according to the instructions on page 4-20, step 6. If the inputs of ICs D and E do not match the outputs, D and E should be checked according to the instructions on page 4-5.

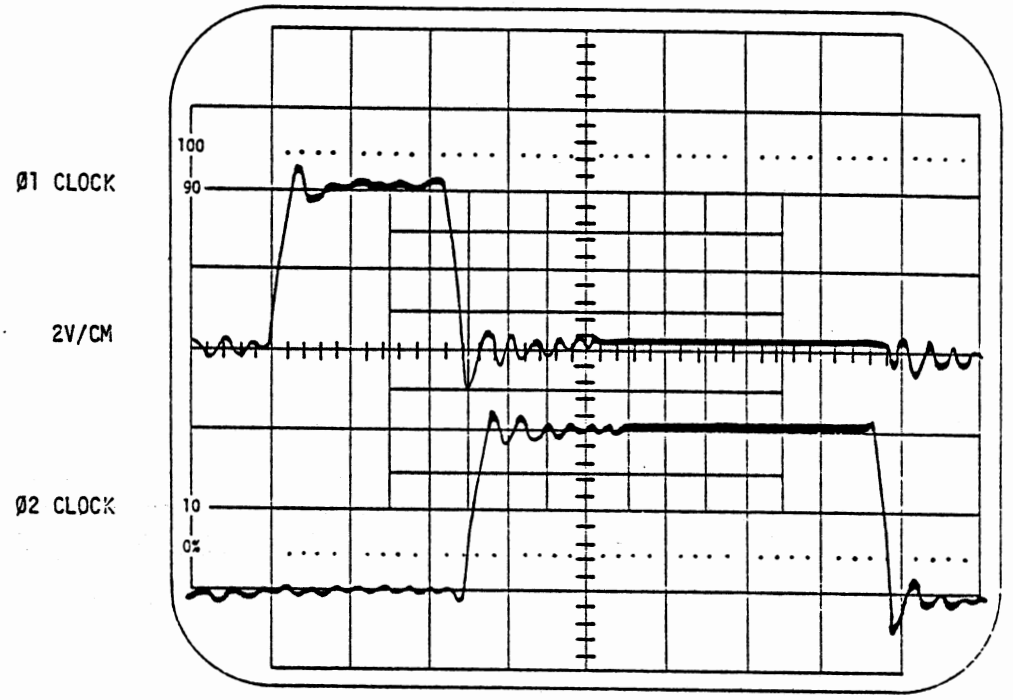
Step	Instructions	If Correct	If Incorrect
			Trace the logic levels of ICs Y and P to IC G on the Interface board. Pins 2, 13 and 14 of IC G should be HIGH to allow data to pass through. Check any suspected ICs according to the instructions on page 4-5. Refer to schematic 3-16 (sheet 3 of 3), and check the anode lead of the suspected LED for +8v. If the voltage is absent, trace continuity to bus pin 1. Repair as necessary. A LOW (less than .8v) output from open collector ICs H, K, M, D, B or F on the Display/Control board should produce a voltage of approximately 5v at the cathode lead of the corresponding LED. If this voltage is absent, check for shorts. Check for Vcc and Ground to the open collector IC. If absent, check continuity. If Vcc and Ground are present, check the LED before replacing the IC. A lower voltage (5v) should cause the LED to light; if the LED remains unlit, turn power off and unsolder the LED. Refer to Figure 5-23 on page 5-34 for orientation and install the LED in place of a working (lit) LED. If the LED does not light when power is returned and the RESET switch is lifted, the LED is defective and should be replaced.

Waveform #1 shows the clock inputs to the 8080A microprocessor chip itself.



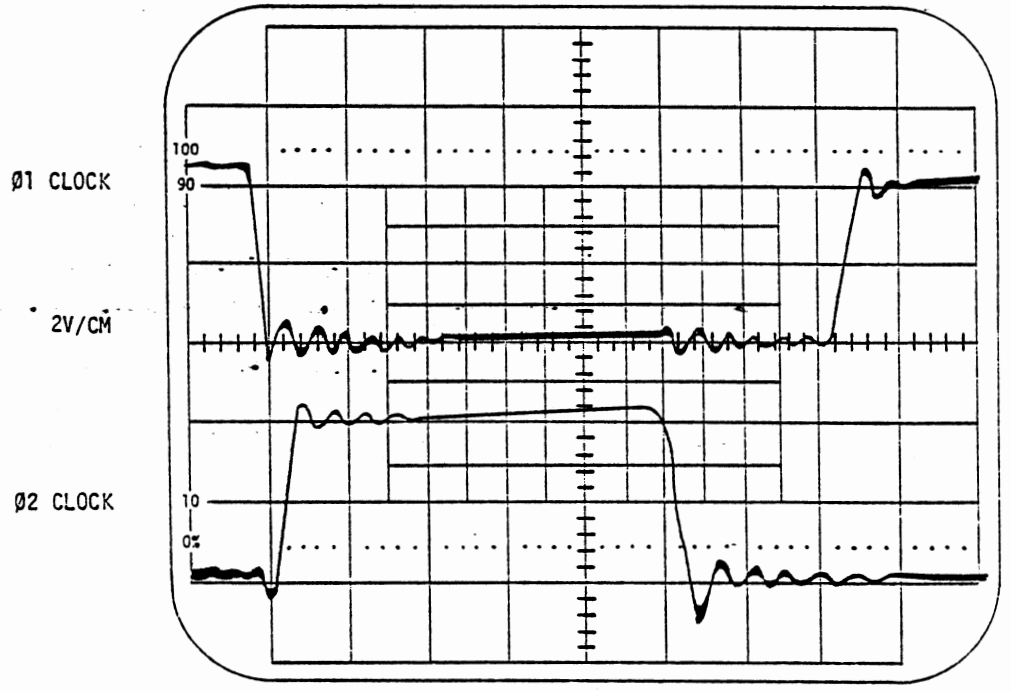
Waveform #1

Waveforms 2 and 3 show Ø1 and Ø2 signals on the bus.



50 MS/CM

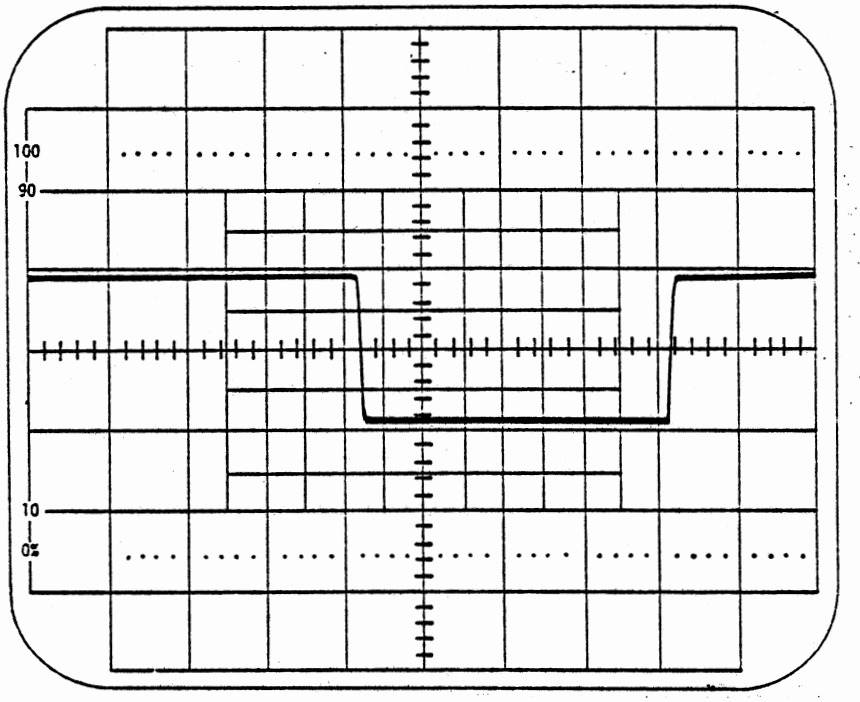
Waveform #2



50 MS/CM

Waveform #3

Waveform #4 shows the $\overline{C13}$ waveform on the D/C board for all conditions.



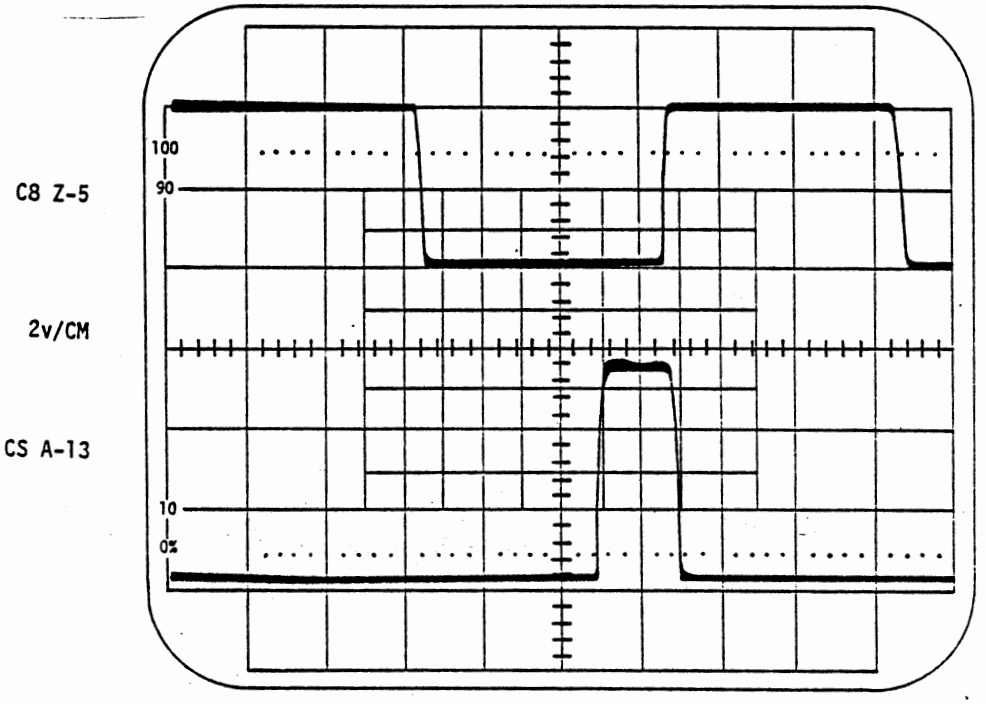
$\overline{C13}$ W 1-9

2v/CM

500 ns/CM

Wave form #4

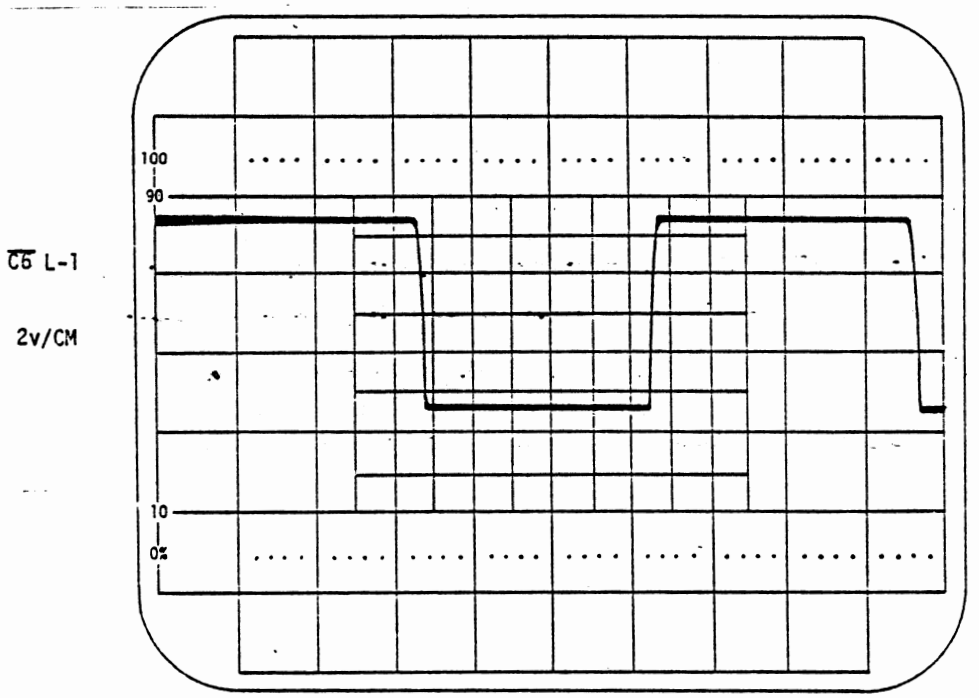
Waveform #5 shows the C8 and CS waveforms on the D/C board for all conditions.



20μs/CM

Waveform #5

Waveform #6 shows the $\overline{C6}$ waveform on the D/C board for all conditions.



5μs/CM

Waveform #6

4-4. NON-PROM RELATED SWITCH PROBLEMS

Section 4-4 contains tests for the RESET, STOP, RUN, SINGLE STEP/SLOW, PROTECT/UNPROTECT, SENSE and STATUS circuitry. If problems involving the PROM related switches also exist, solve the non-PROM related switch problems first.

Table 4-4. Reset Check

Problem Description: During proper operation, lifting the RESET switch should cause all data and address lights to go HIGH whether the computer is running or not. If this does not occur, follow the steps below.

Step	Instructions	If Correct	If Incorrect
1	Press the RESET switch and check IC G1 pin 4 and IC W1 pins 5 and 7 on the Display/Control board.	Pin 4 of IC G1 should go LOW. Pins 5 and 7 of IC W1 should go HIGH. Proceed to Step 2.	If pin 4 fails to go LOW, check the RESET switch with an ohmmeter and replace if necessary. If pins 5 and 7 fail to go HIGH, check ICs W1 and G1 according to the instructions on page 4-5. Trace continuity from pin 1 of ICs W1 and G1 to VR1 pin 2. If absent, repair as necessary.
2	Trace the HIGH level of IC W1 pin 7 through ICs R and N on the Interface board to bus pin 75 (which should be LOW when the RESET switch is lifted).	If proper logic operation is present, proceed to Step 3.	If ICs R and N do not follow their respective truth tables, check them according to the instructions on page 4-5. With an ohmmeter, check continuity from the Display/Control board to the Interface board. If opens are found, repair as necessary.
3	A LOW $\overline{\text{PRESET}}$ signal should produce a LOW at IC F pin 2 on the CPU board.	If present, proceed to Step 4.	If a LOW is not present at IC F pin 2, check for proper logic operation through ICs G and B on the CPU board. Check any IC that does not follow its truth table according to the instructions on page 4-5.
4	A LOW input at IC F pin 2 should produce a HIGH at IC M pin 12 on the CPU board.	If present, proceed to Step 5.	Check IC F for +5v at pin 16, +12v at pin 9 and Ground at pin 8. If absent or incorrect, trace continuity to VR1 pin 2, VR2 pin 2 and bus pin 1, respectively. If continuity is present, check IC F according to the instructions on page 4-5, and replace if necessary.

Step	Instructions	If Correct	If Incorrect
5	A HIGH signal at pin 12 of IC M on the CPU board should cause all address and data lines to go HIGH. (The LEDs corresponding to the address and data lines should light.)	Proceed to Table 4-5.	If any of the address (AØ-A15) or data (DØ-D7) lines fail to go HIGH, check for shorts. If the address and data lights do not light when the corresponding pin of IC M (on the CPU board) is HIGH, refer to Section 4-3, Step17 on page 4-24.

Table 4-5. Stop Check

Problem

Description: Normal Operation--When the computer is running, the Wait light should be off or dim and several address lights should be dim. The Ready line will be HIGH on pin 23 of IC M cn the CPU board. When the computer is stopped, only status lights M1, MEMR and WAIT should be on. Pin 23 of IC M will be LOW. There should be no change in the address lights. If the computer cannot be stopped, proceed with the steps below.

Step	Instructions	If Correct	If Incorrect
1	Check the logic operation from IC R1 on the Display/Control board to IC M on the CPU board. A LOW signal at IC R1 pin 12 should cause a HIGH at pin 23 of IC M on the CPU board. Check for proper logic operation at IC P1 on the Display/Control board.	If logic to the Display/Control board is correct, the problem lies in either one of two areas: the RUN/STOP circuitry or the SS Control circuitry. Check pins 12 and 13 of IC P1 on the Display/Control board. A constant LOW on pin 12 indicates a problem in the RUN/STOP circuitry. Irregular LOW going pulses at pin 13 of IC P1 indicate a problem in the SS Control circuitry. To test for RUN/STOP problems, proceed to Step 2 on page 4-35. To test for SS Control problems, proceed to Step 3 on page 4-39.	Trace the logic levels from IC R1 on the Display/Control board through ICs R and H on the Interface board. Pin 12 of IC R1 should be LOW and bus pin 58 should be HIGH. If not, check ICs R and H according to the instructions on page 4-5. A LOW at bus pin 58 should produce a HIGH at IC F pin 3 on the CPU board. If this HIGH signal is absent at pin 3, check ICs C and B on the CPU board according to the instructions on page 4-5. The HIGH at IC F pin 3 should produce a HIGH at IC M pin 23. If not, check IC F pins 16, 9 and 8. Pin 16 should read +5v; pin 9, +12v; and pin 8, Ground. If the procedures on this page have solved the problem, proceed to Table 4-5 on page 4-43. If the problem still exists, proceed to Step 2 on page 4-35.

Step	Instructions	If Correct	If Incorrect
2	RUN/STOP Circuitry.		
	A. If a board was pulled out with power on, proceed with the steps below:	Proceed to Step B.	
	1) Turn the computer off and remove all boards. Test the mother board pins with an ohmmeter as described in Step 1 on page 4-15.		Repair according to the instructions on page 4-15.
	2) Inspect the mother board for opens along the lands corresponding to bus pins 1, 2 and 52.		Repair as necessary.
	3) Turn power on and check for proper voltages on the bus as described on page 4-15, step 2.		If voltages are incorrect, repair according to the instructions on page 4-15.
	4) Pulling a board out while power is on usually damages the ICs connected to bus pins 3 and 53 which are shorted to bus pins 2 and 52. Check these ICs according to the instructions on page 4-15.		Replace IC C on the CPU board and IC N on the Interface board if necessary.

Step	Instructions	If Correct	If Incorrect
B.	Incorrect installation of Interface cables P1 and P2 can cause damage to several components. Refer to page 5-19 to check for improper cable assembly and repair if necessary. Then follow the steps below:	If P1 and P2 were correctly installed, proceed to Step C.	
	1) Check ICs H, K, B1 and T on the Display/Control board according to the instructions on page 4-5.		Replace as necessary.
	2) Turn power off and unsolder one lead of R74 on the Display/Control board. Test for a resistance reading of 2.2K ohms. Resolder the lead to the board.		Replace as necessary.
	3) Turn power on and check the +5v voltage regulator and the -9v voltage regulator on the Display/Control board as described on page 4-18, step 1.		Repair according to the instructions on page 4-18.

Step	Instructions	If Correct	If Incorrect
	C. Electrical Problem.		
	1) With the computer in a Run state, check for irregular HIGH pulses at IC M1 pin 3 on the Display/Control board.	If pulses are present, proceed to Step 2) on page 4-38.	If pulses are not present, check the logic from IC M1 to IC D1 on the Display/Control board. HIGH pulses should be present at pins 3, 4 and 5 of IC D1. a. If pulses are missing from pin 3 (of IC D1), check pin 4 of IC M on the CPU board for positive pulses. If absent, check ICs M and F according to the instructions on page 4-20, Step 6. If pulses are present at IC M pin 4, check IC E pin 1 on the CPU board for a constant LOW signal. If absent, check continuity from pin 1 to Ground. Check pin 15 (of IC E) for a LOW PDBIN pulse. If pin 15 is HIGH, check IC V on the CPU board according to the instructions on page 4-5. If IC V is working properly, check pin 17 of IC M for LOW pulses. If absent, again check ICs M and F according to the instructions on page 4-20, step 6. Check pin 13 of IC E for a HIGH DO5 signal. If present, trace continuity and logic to IC D1 on the Display/Control board. Repair as necessary. b. If the PSYNC pulse is missing at pin 4 of IC D1, check for a HIGH pulse at pin 19 of IC M on the CPU board. If absent, check ICs F and M according to the instructions on page 4-5,

Step	Instructions	If Correct	If Incorrect
			step 6. If the HIGH pulse is present at pin 19, check continuity and logic from pin 19 to pin 4 of IC D1. Check ICs, if necessary, according to the instructions on page 4-5.
			c. If the HIGH pulse (STSTB) is absent at pin 5 of IC D1 on the Display/Control board, check for a LOW pulse at pin 7 of IC F on the CPU board. If absent, check for a HIGH PSYNC signal at pin 5 of IC F. If absent, trace continuity to IC M pin 19. If continuity is present, check ICs F and M according to the instructions on page 4-20, step 6. If the LOW pulse is present at pin 7 of IC F, trace logic and continuity to pin 5 of IC D1 on the Display/Control board, and repair as necessary.
2)	Lift the STOP switch and check pin 4 of IC C1, pin 5 of IC N1 and pin 2 of IC M1 on the Display/Control board.	C1 pin 4 should be LOW. N1 pin 5 should be HIGH. M1 pin 2 should be HIGH. Proceed to Step 3).	Pin 1 of ICs C1 and N1 should be HIGH. If not, trace continuity to Vcc, and repair as necessary. Check ICs C1, N1 and M1 according to the instructions on page 4-5. (Note: M1 pin 2 is HIGH only when the STOP switch is lifted and held.)
3)	Lift the STOP switch and check pins 4, 1 and 5 of IC M1.	Pins 4 and 1 should be HIGH; pin 5 should be HIGH. Proceed to Step 3 on page 4-39.	If pin 4 is LOW, check $\overline{POC}$ according to the instructions on page 4-22, step 11. If pin 1 of IC M1 is LOW, check IC P1 according to the instructions on page 4-5. Pin 1 of IC P1 should be LOW when the STOP switch is pressed. If not, check logic at pins 2 and 4 of IC N1 and at pins 5 and 6 of IC C1. If pin 5 of IC M1 is LOW, check pin

Step	Instructions	If Correct	If Incorrect
			2 for a HIGH. If absent, check the logic of ICs C1 and N1. If pin 2 is HIGH, check IC M1 according to the instructions on page 4-5.
3	SS Circuitry.		
	A. (Note: If the JE to JF jumper is present on the Display/Control board, it should be removed for this check.) Check for LOW going clear pulses on IC M1 pin 13 on the Display/Control board while the chassis is in a Run state. A LOW at IC T1 pin 8 on the Display/Control board should produce the LOW clearing pulse at IC M1 pin 13.	If clear pulses are present on IC M, the trouble lies in the $\overline{SB}$ circuitry. Proceed to Step B.	If pulses are absent at M1 pin 13, check for proper logic at ICs J1 and T1 on the Display/Control board. If the PSYNC and/or STSTB signals are absent at the inputs of IC T1, refer to Step C on page 4-37.
	B. If LOW $\overline{SB}$ pulses are present, follow the steps below:		
	1) Check pin 2 of IC J on the Display/Control board for a CS waveform (see waveform #5 on page 4-30).	If present, proceed to Step 2).	If absent, refer to Section 4-3, Step 13, page 4-23.
	2) Check pin 13 of IC J for a constant LOW level.	If absent, check pin 13 of IC A for a CS signal. If the signal is absent	If a constant HIGH level is present at IC J pin 13, check continuity to pin 4 of IC A. Check IC A according to the instructions on page 4-5.

Step	Instructions	If Correct	If Incorrect
		at IC A, refer to Section 4-3, Step 13, page 4-23.	
	3) Check pins 2, 11 and 14 of IC A on the Display/Control board for HIGH signals.	If present, proceed to Step 4).	If absent, trace continuity to VR1 pin 2 and repair as necessary.
	4) Trace continuity from pin 1 of IC J to pin 1 of IC A and to pins 12 and 1 of IC P.	If continuity is present, proceed to Step C.	Repair as necessary.
C.	Check pin 14 of IC P on the Display/Control board for a C8 signal.	If present, proceed to Step D.	If absent, refer to Section 4-3, Step 15, page 4-24. Check the logic operation of IC Z.
D.	Check for a HIGH at IC P pin 3 on the Display/Control board.	If present, proceed to Step E.	If absent, trace continuity through R49 to VR1 pin 2 (on the Display/Control board). Repair as necessary.
E.	Check pin 2 of IC P for a LOW level. Pin 2 should pulse HIGH only when a PROM related switch is pressed.	If present, proceed to Step F.	If absent, check for HIGH $\overline{\text{RC-CLR}}$ and $\overline{\text{POC}}$ levels at pins 12 and 13 of IC Z. If $\overline{\text{POC}}$ is LOW, refer to Section 4-3, Step 7, page 4-20. A LOW signal at $\overline{\text{RC-CLR}}$ indicates either no $\overline{\text{C6}}$ signal at IC L1 pin 1 on the Display/Control board (refer to Section 4-3, Step 14, page 4-24) or LOW going pulses on pin 3 of IC L1. LOW pulses at IC L1 pin 3 should occur only when a PROM related switch is pressed. Check for HIGHs at IC L1 pins 2 and 4. If absent, trace continuity to VR1 pin 2 and

Step	Instructions	If Correct	If Incorrect
			repair as necessary.
F.	A C8 signal at IC P pin 14 should cause HIGH going pulses to appear at pins 8, 9, 11 and 12 of IC P (RAØ-RA13) on the Display/Control board. (Note: The C8 signal will occur only briefly when a PROM related switch is pressed.)	If HIGH pulses are present, proceed to Step G.	If HIGH pulses are not present, check continuity from pin 1 to pin 12 of IC P. Check power and Ground at IC P. If present, turn power off and remove IC G. Turn power on and check again for pulses at pins 8, 9, 11 or 12. If absent, check IC P according to the instructions on page 4-5. Turn power off and reinstall IC G.
G.	Check pins 17, 18, 19 and 20 of IC G on the Display/Control board for HIGHs. (LOWs should occur only when the appropriate PROM related switches are pressed.)	If present, proceed to Step H.	If any LOW levels are present (but no PROM related switches are pressed), trace logic through ICs V1, Z1, U1, F1, Y1 and H1. Pin 1 of ICs F1, U1, H1 and Y1 should be LOW. If not, trace continuity to Vcc. Check and replace ICs if necessary.
H.	Check pins 1, 2, 3, 4, 5, 6, 11 and 12 of IC N on the Display/Control board for pulses.	If present, proceed to Step I.	If constant levels rather than pulses are present, refer to Section 4-3, step 16 on page 4-24. Also check for shorts and bad socket connections.
I.	Check IC A1 pins 1 and 2 on the Display/Control board for proper inverting logic.	If IC A1 is working properly, proceed to Step J.	If proper inverting logic is not present, check IC A1 according to the instructions on page 4-5.
J.	On the Display/Control board, compare the signal at IC A pin 1 to that of IC P pin 12.	If the signals match, proceed to Step K.	If the signals do not match, trace continuity to Vcc and repair as necessary.

Step	Instructions	If Correct	If Incorrect
K.	Check for pulses at pins 3 and 4 of IC A.	If present, proceed to Step L.	If pulses are absent at pin 3, trace continuity to pin 4 of IC G and repair as necessary. If the pulse is absent at pin 4 of IC A, turn power off and remove pin 4 from the board. Trace logic to pin 12 of IC J. If the pulse is present while pin 4 is removed from the board, trace continuity and look for shorts. If the pulse is absent while pin 4 is removed from the board, turn power off and replace IC A with either IC B1 or IC T. If pulses are now present at pins 3 and 4, IC A is defective and should be replaced.
L.	Check for a LOW at IC N pin 8 and trace logic to pin 4 of IC Z on the Display/ Control board. A LOW at Z pin 4 should prevent the C8 signal from appearing at pin 6 of IC Z and pin 14 of IC P and should keep IC P from incrementing. (Note: Pin 4 of IC Z should be LOW when the computer is stopped. Pin 4 should pulse HIGH only when a PROM related switch is pressed.)	If a LOW is present at pin 8 of IC N and if proper logic is present, proceed to Table 4-6.	Check any ICs that do not follow their respective truth tables according to the instructions on page 4-5. Check for continuity and shorts from pin 12 of IC P to pin 2 of IC Z and repair as necessary.

Table 4-6. Run Check

Problem

Description: When the computer is running, the WAIT light on the front panel should be dim or off, and a HIGH should be present at pin 23 of IC M on the CPU board. If the computer will not run when the RUN switch is pressed, follow the steps below.

Step	Instructions	If Correct	If Incorrect
1	Press and hold the RUN switch and check for LOWs at ICs C1 pin 5 and M1 pin 2 on the Display/Control board. Check for HIGHs at ICs N1 pin 4 and P1 pin 1 (on the Display/Control board).	If present, proceed to Step 2.	If absent, trace logic to the RUN/STOP switch. Check ICs C1 and N1 according to the instructions on page 4-5.
2	The HIGH at pin 1 of IC P1 should produce a LOW at pin 1 of IC M1, causing a LOW at pin 5. A LOW at M1 pin 5 should produce a LOW at IC R1 pin 12. Trace this active LOW $\overline{\text{FRDY}}$ level through the Interface board to IC C pin 13 on the CPU board. (IC C pin 13 should be HIGH when the RUN switch is pressed.) The resulting HIGH at pin 3 of IC F should cause a HIGH at pin 23 of IC M (on the CPU board).	If proper logic operation is present, proceed to Table 4-7.	If a LOW is not present at pin 5 of IC M1, check the logic of IC P1 and, if necessary, check the ICs according to the instructions on page 4-5. Check for Ø2, Vcc and Ground at IC F. If IC F or IC M appears defective, refer to Section 4-3, Step 6, page 4-20.

Table 4-7. Single Step/Slow Check

Problem

Description: If JE is jumpered to JF on the Display/Control board, SINGLE STEP/SLOW can be misleading. For example, when SINGLE STEP/SLOW is pressed for a JMP, a change cannot be detected in the LEDs. Activity can only be detected by monitoring pulses on IC M pin 23 (READY) on the CPU board. If pulses are not present at IC M, a problem exists in the SINGLE STEP/SLOW circuitry. Follow the steps below.

Step	Instructions	If Correct	If Incorrect
1	If SINGLE STEP will not function, follow steps A and B below:		
	A. While pressing the SINGLE STEP switch, check for LOWs at ICs C1 pin 13 and D1 pin 1 on the Display/Control board.	If present, proceed to Step B.	If absent, check for HIGH signals at pin 1 of ICs C1 and N1 on the Display/Control board. If absent, trace continuity to VR1 pin 2. If the HIGH signal is present, check ICs C1 and N1 according to the instructions on page 4-5. If IC D1 pin 2 is LOW, check pin 15 of IC N1 for a LOW. If absent, check pin 9 of ICs C1 and N1 for a $\overline{C13}$ waveform. If the waveform is absent, refer to Section 4-3, Step 13, page 4-23. If pin 15 is HIGH, recheck the logic of ICs N1 and C1. Pin 13 of IC N1 should be HIGH. If not, trace continuity from pin 13 of IC D1 to pin 12 of IC J and repair as necessary.
	B. When the SINGLE STEP switch is pressed and held, IC M1 pin 11 on the Display/Control board should go HIGH. Check	If HIGH signals and proper logic are present, proceed to Step 2.	Check IC D1 according to the instructions on page 4-5. Check the logic from pin 8 of IC M1 on the Display/Control board to pin 23 of IC M on the CPU board. Check any suspected ICs according to

Step	Instructions	If Correct	If Incorrect
	for HIGHs at pins 12, 10 and 13 of IC M1. (Note: A constant HIGH should be present at pin 13. A LOW pulse, however, will end the SINGLE STEP operation.) Trace the LOW pulse at IC M1 pin 8 to a HIGH pulse at pin 23 of IC M on the CPU board.		the instructions on page 4-5. If problems are suspected with IC F or IC M, refer to page 4-20, step 6.
2	If SLOW (on the Display/Control board) will not function, follow steps A, B and C below:		
	A. Check for C18 pulses at pin 10 of IC P1 on the Display/Control board.	If present, proceed to Step B.	If absent, check the logic from pin 10 of IC P1 to jumper JD. (JD is located next to switch A1.) If pulses are not present at pins 2, 13 and 14 of IC X, refer to Section 4-3, steps 9 and 10 on page 4-22 to check ICs L and X.
	B. Holding the SLOW switch down should produce HIGHs at pin 9 of IC P1 and at pins 1 and 13 of IC D1 on the Display/Control board.	If present, proceed to Step C.	If pin 13 of IC D1 is LOW, check IC J pins 1, 2 and 13 as described in Table 4-5, Step 3, page 4-39. If pin 9 of IC P1 or pin 1 of IC D1 is LOW, check the logic of ICs C1 and N1. Check ICs C1 and N1 according to the instructions on page 4-5 if necessary.
	C. C18 pulses should occur at ICs D1 pin 2 and M1 pin 11 on the Display/Control	If proper operation is present, proceed to Step 3.	If LOW pulses are absent at pin 13 of IC M1, refer to step A on page 4-39. Any IC whose logic does not follow its truth table should be

Step	Instructions	If Correct	If Incorrect
	board. LOW going pulses should be present at IC M1 pin 13. (Note: A constant LOW level should never be present at M1 pin 13.) Pins 12 and 10 of IC M should be HIGH. Trace the LOW going pulses at IC M1 pin 8 to the HIGH going pulses on the READY line (pin 23 of IC M on the CPU board).		checked according to the instructions on page 4-5. HIGH pulses should be present at pin 3 of IC F on the CPU board. If ICs M or F appear defective, refer to Section 4-3, steps 5 and 6, page 4-20.
3	If SINGLE STEP and SLOW will not actuate a stopped condition, follow steps A and B below:		
	A. Pressing the SINGLE STEP/ SLOW switch should produce LOWs at ICs M1 pin 2 and P1 pin 1 and HIGHs at ICs M1 pin 1 and P1 pin 12 on the Display/Control board. Check for a LOW going pulse at pin 13 of IC M1. (Note: This pulse may be hard to detect. If so, hit the RUN switch to produce several of these pulses	If the proper signals are present, proceed to Step B.	Check any IC whose logic does not follow its truth table according to the instructions on page 4-5. Pin 1 of ICs C1 and N1 should be HIGH. If not, trace continuity to VR1 pin 2 and repair as necessary. If pin 13 of IC M1 is constantly LOW, refer to Step A, page 4-39.

Step	Instructions	If Correct	If Incorrect
	B. Check pin 5 of IC T1 on the Display/Control board for a HIGH $\overline{POC}$ signal. HIGH going pulses should be present at pins 3 and 4 of IC T1.	If present, proceed to Table 4-8.	If a HIGH $\overline{POC}$ signal is not present at pin 5, refer to Section 4-3, step 11, page 4-22. If HIGH going pulses are absent at pins 3 and 4, check for PSYNC and STSTB pulses at pins 2, 13, 11 and 10 of IC T1. If these pulses are missing, trace logic to the CPU board according to the instructions on page 4-37, step C. Check any suspected ICs according to the instructions on page 4-5.

Table 4-8. Protect/Unprotect Check

Note 1: Table 4-8 deals with problems on the Display/Control board only; memory board problems are not included in this table.

Note 2: In order to perform the PROTECT/UNPROTECT check, one memory board that has the PROTECT/UNPROTECT option must be installed in the chassis. (16K Static boards do not have this function. PROM memory boards, when addressed, always cause the PROTECT LED to light.)

Problem

Description: If pressing the PROTECT switch does not protect the memory board from depositing new data and if the UNPROTECT switch does not allow new data to be deposited, follow the steps below.

Step	Instructions	If Correct	If Incorrect
1	Pressing the PROTECT (or UNPROTECT) should produce a LOW at pin 13 of IC G1 on the Display/Control board as long as the switch is held. Pressing the UNPROTECT switch causes the same operation to occur at pin 12 of IC G1. The LOW at pin 13 of IC G1 causes a LOW at pin 10 of IC W1 (for PROTECT). The LOW at pin 12 of IC G1 causes a LOW at pin 14 of IC W1 (for UNPROTECT). Trace the LOW active $\overline{\text{PROTECT}}$ (or UNPROTECT) signal to bus pin 20 (or 70). (Note: The memory board must be addressed in order to be protected.)	If proper operation is present, proceed to Step 2.	Check ICs G1 and W1 according to the instructions on page 4-5. Check any IC (on the Interface board) whose logic does not follow its truth table according to the instructions on page 4-5.

Step	Instructions	If Correct	If Incorrect
2	A LOW on the PS line (bus #69) should cause the PROTECT LED to light.	If so, proceed to Table 4-9 on page 4-50.	If the PROTECT LED does not light, refer to Section 4-3, step 17 on page 4-24.

Table 4-9. Sense Switch Check

Problem

Description: If the data input from the SENSE switches does not match the settings of A8-A15, follow the steps below.

Step	Instructions	If Correct	If Incorrect
1	Pressing Single Step twice for the following program should produce LOW levels at pins 8 and 9 of IC D on the Interface board. (Note: JE should not be jumpered to JF on the Display/Control board for this check.) All address lines (AØ-A15) should be HIGH. Location / Bit Pattern 000 333 001 377 002 303 003 000 004 000 Note: If this program cannot be deposited, proceed to Table 11 on page 4-55 to correct the DEPOSIT problem.	If LOWs are present at pins 8 and 9 when the program is run, proceed to Step 2.	If LOW levels are not present at pins 8 and 9 of IC D, check the logic operation from IC M (AØ-A15) on the CPU board to IC D on the Interface board. Check any suspected ICs according to the instructions on page 4-5.
2	Pin 12 of IC J on the Interface board should be HIGH.	If so, proceed to Step 3.	If pin 12 is LOW, check IC D according to the instructions on page 4-5.
3	Pin 13 of IC J should be HIGH. If not, check for a HIGH SINP signal at bus pin 46.	If pin 13 of IC J is HIGH, proceed to Step 4.	If pin 13 of IC J is not HIGH, check IC C according to the instructions on page 4-5. If the SINP signal is absent at bus pin 46, trace logic to pin 6 of IC K on the CPU board. Check

Step	Instructions	If Correct	If Incorrect
			any suspected ICs according to the instructions on page 4-5. Check for HIGHs at pins 2, 11 and 13 of IC K. If absent, trace continuity to VR1 pin 2 on the CPU board, and repair as necessary. Press RUN and check for LOW $\overline{\text{STSTB}}$ pulses on pin 1 of IC K (see Table 4-10, Step 3 on page 4-53).
4	Pin 11 of IC J on the Interface board ($\overline{\text{SSWI}}$) should be LOW. Checking logic and continuity, trace this signal to a LOW on pin 10 of IC Z on the Display/ Control board.	If correct, proceed to Step 5.	Check the logic of ICs J and H on the Interface board. Check any suspected ICs according to the instructions on page 4-5.
5	For each address switch (A8-A15) that is lifted, the corresponding output pin of either IC W or IC U on the Display/Control board should be LOW.	If LOWs are present at the proper IC pins, proceed to Step 6.	If these IC pins are HIGH, check for shorts. Check ICs W and U according to the instructions on page 4-5.
6	Trace the LOW level output from IC W or IC U to a HIGH on the corresponding output pin of IC E or IC M on the Interface board.	If proper logic is present, proceed to Step 7.	Check any suspected ICs according to the instructions on page 4-5.
7	Check PDBIN (pin 2 of IC B on the Interface board and pin 4 of IC C on the CPU board) for HIGH levels.	If present, proceed to Step 8.	If absent, check IC V on the CPU board according to the instructions on page 4-5. Trace logic to a HIGH at pin 17 of IC M on the CPU board. Check any suspected ICs according to the instructions

Step	Instructions	If Correct	If Incorrect
			on page 4-5.
8	A LOW $\overline{\text{SSWI}}$ level should produce LOWs at pins 6 and 13 of IC B on the Interface board. Pin 8 of IC B should be HIGH, causing LOWs to appear at bus pin 57 (DIG1) and pin 6 of IC B. A LOW at pin 57 should produce a HIGH at pin 6 of IC C on the CPU board. Pins 4, 5, 9 and 10 of IC B should be HIGH.	If correct, proceed to Step 9.	If any of these signals are incorrect or absent, check continuity and check the ICs according to the instructions on page 4-5. If HIGHs are not present at IC B pins 4, 5, 9 and 10, trace continuity to VR1 pin 2 on the Interface board.
9	Refer to schematic 3-14. Lifting any of the A8-A15 address switches should cause the corresponding data line of ICs D, E and M on the CPU board to go HIGH.	If the proper data lines are HIGH, proceed to Table 4-10.	Check logic from the outputs of ICs E and M on the Interface board to ICs D and E on the CPU board. Check any suspected ICs according to the instructions on page 4-5.

Table 4-10. Status Check

Problem
Description: If status is incorrect when the computer is turned on and if pressing the RESET switch fails to achieve proper status, follow the steps below.

Step	Instructions	If Correct	If Incorrect
1	Check for HIGHs at pins 2, 13, 11 and 14 of IC K on the CPU board.	If present, proceed to Step 2.	If pins 2, 13, 11 or 14 are LOW, trace continuity to VR1 pin 2 on the CPU board. Repair as necessary.
2	$\overline{\text{PRESET}}$ should be HIGH on the bus.	If so, proceed to Step 3.	If not, check the logic for the RESET switch according to the instructions in Table 4, page 4-32.
3	Check for a LOW going $\overline{\text{STSTB}}$ pulse at pin 1 of IC K on the CPU board while the computer is running.	If present, proceed to Step 4.	If absent, check continuity from pin 7 of IC F to pin 1 of IC K. If continuity is absent, check IC F on the CPU board according to the instructions in Table 5, Step C, page 4-38.
4	Check for MEMR and M1 signals at IC K pins 4 and 8 on the CPU board. Check continuity from the outputs of ICs D and E to the inputs of IC K on the CPU board.	If present, proceed to Step 5.	If pins 3 and 7 of IC K are constantly LOW when the computer is running, look for shorts on the CPU board and repair as necessary.
5	If pins 4 and 8 of IC K are HIGH, the M1 and MEMR LEDs on the front panel should be lit.	If the correct LEDs are lit, proceed to Section 4-5 if problems exist with the EXAMINE/EXAMINE NEXT, DEPOSIT/DEPOSIT NEXT, ACCUMULATOR DISPLAY/ ACCUMULATOR LOAD or IN/ OUT switches.	If the correct LEDs are not lit, check for proper logic operation from IC K on the CPU board to the front panel LEDs. Check any suspected ICs according to the instructions on page 4-5. If the ICs are working properly, refer to Step 17 on page 4-24 to check the LED circuitry.

4-5. PROM RELATED SWITCH PROBLEMS

Section 4-5 contains procedures to solve problems relating to the EXAMINE/EXAMINE NEXT, DEPOSIT/DEPOSIT NEXT, ACCUMULATOR DISPLAY/ACCUMULATOR LOAD and IN/OUT switches. Problems involving the RESET, RUN/STOP, SINGLE STEP/SLOW, PROTECT/UNPROTECT, SENSE and STATUS switches should be checked before performing the tests in Section 4-5. Refer to Section 4-4 to solve problems of this kind.

The text in Section 4-5 is divided into 16 major steps. These are general procedures that should always be followed when testing the PROM related switches.

Table 4-11. PROM Related Switch Problems

Step	Instructions	If Correct	If Incorrect
1	When a PROM related switch is pressed and held, the upper four bits (RA7-RA4) of the beginning address (as shown in Table 3-2 in the Theory of Operation section) are produced on the PROM (IC G on the Display/Control board) address lines. The chart below shows how the PROM address lines (RA7-RA4) correspond to the switch. Address Bit RA7 RA6 RA5 RA4 Corresponding PROM Pin: 17 18 19 20 Switch EXAMINE: LOW HIGH HIGH HIGH EXAMINE NEXT: HIGH LOW HIGH HIGH DEPOSIT: HIGH HIGH LOW HIGH DEPOSIT NEXT: HIGH HIGH HIGH LOW ACCUMULATOR DISPLAY: LOW LOW HIGH HIGH ACCUMULATOR LOAD: HIGH LOW LOW HIGH IN: HIGH HIGH LOW LOW OUT: HIGH LOW HIGH LOW If no PROM related switches are pressed, RA7-RA4 (pins 17-20 of IC G) should be HIGH.	If RA7-RA4 go to the appropriate levels when the corresponding switch is pressed, proceed to Step 2.	If RA7-RA4 are LOW when none of the switches are pressed, check for LOW input signals at ICs V1 and Z1 on the Display/Control board. Trace continuity from RA4-RA7 through RP1 to VR1 pin 2 (Vcc), and repair as necessary. If a HIGH input is found, check the logic operation of ICs F1, U1, A1 and V1. Pin 1 of ICs H1, U1, Y1 and F1 should be HIGH. If not, trace to VR1 pin 2 on the Display/Control board. Pins 4, 5, 13 and 12 of ICs F1 and H1 should be HIGH when none of the switches are pressed. If HIGH signals are not present, trace continuity to VR1 pin 2 and repair as necessary. Press and hold down the suspected switch and trace logic to the switch from pins 17, 18, 19 and 20 of IC G on the Display/Control board. Check any suspected ICs according to the instructions on page 4-5.

Step	Instructions	If Correct	If Incorrect
2	Check for a HIGH clear pulse (less than .1 μsec. wide) at pin 2 of IC P on the Display/Control board each time a PROM related switch is pressed. (Note: In order to better detect this pulse, turn the scope's time base to the lowest frequency setting, or highest time/cm setting, and turn up the intensity. A logic probe may also be needed.)	If the pulse is present, proceed to Step 3.	If the pulse is absent, check for HIGHs at pins 2 and 4 of IC L and at pins 1, 2, 11 and 12 of IC X1 on the Display/Control board. If absent, trace continuity to VR1 pin 2 on the Display/Control board. Repair as necessary. Pressing any PROM related switch will cause at least one LOW on the input pins of IC X1, producing a HIGH at pin 3 of IC L1. The LOW going pulse at pin 6 ($\overline{\text{RC-CLR}}$) of IC L1 should cause a HIGH pulse at pin 2 of IC P. At the same time, pin 5 (AL-STB) of IC L1 should pulse HIGH. If this does not occur, check ICs L1 and Z according to the instructions on page 4-5.
3	Refer to schematic 3-16, sheet 1 of 3. Press the PROM related switch and check for proper operation (as shown in schematic 3-16) on the RAØ-RA3 address lines of IC G on the Display/Control board. For example, the DEPOSIT switch covers addresses 320-323. Address lines RA2 and RA3 (which correspond to pins 8 and 11, respectively, of IC P) are never used. Consequently, when the DEPOSIT switch is pressed,	If address lines RAØ-RA3 are operating properly, proceed to Step 4.	If proper operation is not present at address lines RAØ-RA3, check IC P according to the instructions in Table 4-5, Step F, on page 4-41.

Step	Instructions	If Correct	If Incorrect

pulses should not be present at pins 8 and 11 of IC P. When the switch is released, pulses may be present at all outputs of IC P. The following chart shows the correct pulse level for each switch.

Switch	Address Bit			
	RA3	RA2	RA1	RA0
EXAMINE	NP	P	P	P
EXAMINE NEXT	NP	NP	P	P
DEPOSIT	NP	NP	P	P
DEPOSIT NEXT	NP	P	P	P
ACCUMULATOR DISPLAY	P	P	P	P
ACCUMULATOR LOAD	P	P	P	P
IN	P	P	P	P
OUT	P	P	P	P

NP = No pulses

P = Pulses

(Note: This chart is valid only when the switch is pressed and held. When the switch is released, pulses may appear at all of the address lines.)

Step	Instructions	If Correct	If Incorrect
4	For each data line, check continuity (with an ohmmeter set at X1K or higher) from the output pins of ICs N and F on the Interface board to the appropriate pins of ICs D and E on the CPU board.	If continuity is present, proceed to Step 5.	If continuity is absent, check for opens or a bad connection in the CPU to Interface board cable. An open will cause the same bit to be deposited no matter what condition the A0-A7 switches are in. The EXAMINE switch will show that the address bit is HIGH along with the corresponding bit in addresses A8-A15. Resolder the cable if necessary and solder over opens.
5	If a pulse counter is available, check for the appropriate number of clock pulses at IC M1 pin 11 on the Display/Control board as listed below:	If correct, proceed to Step 6.	If the correct number of pulses is not present at IC M1 pin 11, check IC G on the Display/Control board. Also check CS, C8, $\overline{C13}$, C6 and M1 (refer to pages 4-23 step 13, 4-24 step 15, 4-22 step 10, 4-24 step 14 and 4-37 step C, respectively).

Switch	Number of Pulses
EXAMINE	3
EXAMINE NEXT	1
DEPOSIT	0
DEPOSIT NEXT	1
ACCUMULATOR DISPLAY	6
ACCUMULATOR LOAD	6
INPUT	6
OUTPUT	6

(Note: Each number corresponds to the number of S8 pulses set in Table 3-2.)

Step	Instructions	If Correct	If Incorrect
6	If the $\overline{CT3}$, $\overline{C6}$, C8 and CS signals have not been checked, refer to page 4-22 step 10, page 4-24 step 14, page 4-24 step 15, and page 4-23 step 13, respectively, to check these signals.	If these signals are functioning properly, proceed to Step 7.	Repair according to the instructions on the appropriate page.
7	The PROM functions usually cause each PROM data output to change levels at least once. Bit 7 of EXAMINE NEXT is the only exception to this rule. Press each PROM related switch while monitoring the output pins of IC G on the Display/Control board for pulses.	If constant levels are not present, proceed to Step 8.	If a constant LOW or HIGH signal is present on pins 4, 5, 6, 7, 8, 9, 10 or 11 of IC G on the Display/Control board when a switch is pressed, check continuity with an ohmmeter and look for shorts and bad socket connections. Repair as necessary.
8	Check for HIGH signals at pins 2, 14 and 11 of IC A on the Display/Control board. Check continuity from pins 1 and 12 of IC P to pin 1 of IC A and to pin 2 of IC Z on the Display/Control board.	If HIGH signals and continuity are present, proceed to Step 9.	If HIGH signals and/or continuity are absent, check continuity from the suspected pin to VR1 pin 2 on the Display/Control board and repair as necessary.
9	One second after the switch is pressed, the final address (as shown in Table 3-2) should appear on lines RA0-RA7 and remain there until the switch	If correct, proceed to Step 10.	If the final address is not 177, check IC G according to the instructions on page 4-24, step 16. Also look for shorts and repair as necessary.

Step	Instructions	If Correct	If Incorrect
	is released. 177 should also be present at IC G on the Display/ Control board.		
10	Refer to the following chart and check for S pulses at pins 4, 6, 8, 10, 15, 17, 19 or 21 of IC A on the Display/Control board.	If present, proceed to Step 11.	If the proper pulses are absent, or if the improper pulses are present at IC A, check IC A according to the instructions on page 4-5. Also look for shorts and repair as necessary.
	Switch — S Pulse		
	EXAMINE — S1, S2, S5, S7, S8		
	EXAMINE NEXT — S5, S7, S8		
	DEPOSIT — S1, S6, S7		
	DEPOSIT NEXT — S1, S6, S7, S8, S5		
	ACCUMULATOR DISPLAY — S3, S4, S5, S7, S8		
	ACCUMULATOR LOAD — S1, S3, S4, S5, S7 S8		
	IN — S2, S3, S4, S5, S7, S8		
	OUT — S2, S3, S4, S5, S7, S8		
11	The S pulses listed in Step 10 should produce the following results:		
	A. For each A0-A7 switch that is up, S1 should produce a HIGH pulse on the corresponding output pin of IC E	If present, proceed to Step B.	If these HIGH pulses are absent, trace continuity from pin 21 of IC A to the input pins of ICs Y and W on the Display/Control board. Also trace continuity from the output pins of ICs Y and W

Step	Instructions	If Correct	If Incorrect
	or IC M on the Interface board. To check for S1, press the DEPOSIT switch.		to the input pins of ICs E and M on the Interface board with the corresponding switch up. Repair as necessary. Check logic operation from the input pins of ICs Y and W on the Display/Control board to the output pins of ICs E and M on the Interface board. Check any suspected ICs according to the instructions on page 4-5.
B.	A HIGH S2 pulse should cause LOW pulses at the outputs of ICs W and U on the Display/Control board (if the corresponding switch is up).	If LOW pulses are present, proceed to Step C.	If LOW pulses are absent, check the logic of ICs A1, Z, W and V. Test the ICs according to the instructions on page 4-5, if necessary.
C.	HIGH S3 and S4 pulses should produce HIGHs at ICs B1 pin 13 and T pin 13 on the Display/Control board.	If HIGH signals are present at B1 pin 13 and T pin 13, proceed to Step D.	If HIGH pulses are absent, check continuity with an ohmmeter and repair as necessary.
D.	A HIGH S5 pulse should produce LOWs at IC R pins 1 and 15 and IC S pin 1 on the Display/Control board.	If LOW signals are present, proceed to Step E.	If LOW signals are absent, check continuity from pin 10 of IC A to pin 9 of IC A1 on the Display/Control board. If the logic on IC A1 is incorrect, check the IC according to the instructions on page 4-5.
E.	A HIGH S6 pulse should produce a HIGH MWRITE pulse at bus pin 68 and a HIGH DIG1 pulse at bus pin 57.	If HIGH pulses are present, proceed to Step F.	If a HIGH MWRITE pulse is absent at bus pin 68, check for a LOW $\overline{\text{DEP}}$ pulse at pin 8 of IC J. If absent, check pin 10 of IC J on the Display/

Step	Instructions	If Correct	If Incorrect
	If the MWRITE signal is absent, "1's" will appear in the data lights (for each AØ-A7 switch that is up) for as long as the DEPOSIT switch is held. When the DEPOSIT switch is released, the data lights will return to their original pattern. The DEPOSIT NEXT switch will act as EXAMINE NEXT, i.e. it will increment an address, but fail to deposit it in memory.		Control board when the switch is pressed. If absent, check continuity from pin 10 of IC J to pin 13 of IC A, pin 2 of IC Z, and pins 12 and 1 of IC P. Repair as necessary. Pins 2 and 14 of IC A should be HIGH. If not, trace continuity to Vcc. If the $\overline{DEP}$ pulse is still absent, check IC J according to the instructions on page 4-5. If IC J is working properly, and if continuity is present, check ICs A and H on the Interface board for proper logic operation. If a HIGH DIGI pulse does not occur at bus pin 57, trace logic from IC C pin 5 on the Display/Control board to a LOW pulse at pins 6 and 12 of IC B on the Interface board. Trace the HIGH pulse from IC B pin 8 to a HIGH at pin 6 of IC C on the CPU board. Pin 2 of IC B should pulse HIGH simultaneously with IC C pin 6. If not, check the logic from pin 2 of IC B to pin 17 of IC M on the CPU board. Check the ICs, if necessary, according to the instructions on page 4-5. If absent, check for a CS signal at pin 4 of IC J and for HIGH pulses from IC P pin 12 to pin 5 of IC J on the Display/Control board. If the signals are absent, trace continuity and repair as necessary. Trace logic to IC B pin 12 on the Interface board. Pins 4, 5, 9, 10, 13 and 2 of IC B
F.	A HIGH S7 pulse should produce LOWs at IC F pins 1 and 15 and IC N pin 15 on the Interface board, and a HIGH at pin 6 of IC C on the CPU board.	If present, proceed to Step G.	

Step	Instructions	If Correct	If Incorrect
			should be HIGH. If pins 4, 5, 9 or 10 are LOW, trace continuity to VR1 pin 2 on the Interface board. If pin 2 of IC B is LOW, trace logic and continuity to pin 17 of IC M. IC M pin 17 should be HIGH. If not, look for shorts and check IC V according to the instructions on page 4-5. If pin 13 of IC B is LOW, check IC J on the Interface board according to the instructions on page 4-5. Pins 12 and 13 of IC J should be LOW. If not, check ICs C and D on the Interface board according to the instructions on page 4-5. S7 should produce a LOW pulse at pin 12 of IC B, causing a HIGH pulse at pin 1 (of IC B). If a HIGH pulse is not present at pin 1, check IC B according to the instructions on page 4-5. Trace the HIGH pulse from IC B pin 1 to IC C pin 5 on the CPU board. (Pin 4 of IC C should be HIGH.) Absence of a LOW pulse at pin 6 of IC B will cause all "1's" to be deposited into memory (no matter how the AØ-A7 switches are set) when the DEPOSIT switch is pressed. Pressing the EXAMINE switch will cause HIGHs only at A3, A4 and A5 (no matter how the AØ-A15 switches are set), since the CPU receives an RST 7 (377) instruction and jumps to location 070.

Step	Instruction	If Correct	If Incorrect
	G. A HIGH S8 pulse should produce a HIGH READY pulse on pin 23 of IC M on the CPU board.	If present, proceed to Step 12.	If the READY pulse is absent at pin 23, check for a HIGH pulse (from IC P) at pin 1 of IC J on the Display/Control board and for a CS signal at pin 2 (of IC J). If the pulse is absent at pin 1, check continuity to pins 1 and 12 of IC P. Repair as necessary. If the CS signal is absent at pin 2, refer to Step 13 on page 4-23. Trace logic from pin 12 of IC J to a HIGH pulse on pin 11 of IC M1. Check any suspected ICs according to the instructions on page 4-5. Pins 12 and 10 of IC M1 should be HIGH. If not, trace continuity to Vcc. Pin 13 of IC M should be HIGH. If a constant LOW is present, check logic at ICs J1 and T1 and replace, if necessary. Trace logic from IC M1 pin 8 to IC M on the CPU board. Replace ICs and repair shorts or opens if necessary. If ICs M or F appear defective, refer to Section 4-3, Step 6 on page 4-20.
12	Check the DEPOSIT switch for proper operation; it should deposit each bit separately.	Proceed to Step 13.	If the switch cannot deposit the bits separately, try different bit combinations. A bit that cannot be deposited separately may be dependent on another bit; check for shorts with an ohmmeter set at X1K or higher. A LOW resistance reading between two data lines indicates a short. Repair as necessary.

Step	Instructions	If Correct	If Incorrect
13	Lower address switches A8-A15 in order to isolate any effect they may have on the circuitry. The switch symptoms should not change.	If there is no change in the symptoms, proceed to Step 14.	If the symptoms change when A8-A15 are lowered, check the logic operation of ICs W, U, Z, A1 and A. If necessary, check the ICs according to the instructions on page 4-5.
14	ICs B1 and T on the Display/Control board are not needed for the EXAMINE, EXAMINE NEXT, DEPOSIT and DEPOSIT NEXT functions. If problems occur with these functions, turn power off and remove ICs B1 and T from the board. Removal of B1 and T will isolate any effects these ICs may cause. However, the switch symptoms should not change.	If the symptoms do not change, make sure power is off and reinstall ICs B1 and T. Proceed to Step 15.	If the symptoms change, check pins 1 and 2 of both ICs for LOWs. If absent, trace continuity to the Ground pin of the 7805 voltage regulator on the Display/Control board. Pin 13 of both ICs should be LOW. If not, trace continuity to pin 17 (for IC B1) or 15 (for IC T) of IC A. Repair as necessary. Pin 13 of both ICs should never pulse HIGH for the EXAMINE/EXAMINE NEXT or DEPOSIT/DEPOSIT NEXT functions. Pin 14 of both ICs should be HIGH. If not, trace continuity to Vcc (VR1 pin 2).
15	Examine the IC outputs in order to test the Display/Control board's open collectors (ICs Y, W and U), the address switches and continuity to pull-up resistors R41-R48 by lifting up each address switch (A0-A15) separately.	Proceed to Step 16.	If any of the outputs fail to go HIGH when the corresponding address switch is lifted, check for a LOW input signal. If the input is not LOW, check for shorts and continuity to pin 21 of IC A. A LOW input signal indicates that a bad IC exists or that one of the components is holding the line LOW. Check Vcc and Ground to the IC. Pin 13 of both ICs B1 and T should be LOW. If not, trace continuity back to IC A and check IC

Step	Instructions	If Correct	If Incorrect
	A bad open collector can cause the switch data to be examined or deposited improperly. If an address switch is down, the corresponding open collector output is disconnected from Vcc and will float as a LOW. Lifting the address switch should raise the output of the open collector to approximately 4v. (Note: The common inputs of ICs Y, W and U should be LOW when the computer is stopped and no switches are pressed.)		A according to the instructions on page 4-5. Pins 1 and 15 of IC R and pin 1 of IC S (on the Display/Control board) should be HIGH. If not, trace logic to pin 10 of IC A. Test any suspected ICs according to the instructions on page 4-5. Check for shorts on both the Display/Control board and the Interface board along the FDIO-FDI7 lines.
16	A. If the ACCUMULATOR DISPLAY switch will not function, follow the steps below:		
	1) Check the ground strap from VR1 on the Display/Control board to the computer; it must be connected in order for the ACCUMULATOR DISPLAY switch to function properly.	Proceed to Step 2).	Repair as necessary.

Step	Instructions	If Correct	If Incorrect
2)	Make sure jumper JD to JC is present on the Interface board.	Proceed to Step 3).	Repair if necessary.
3)	Check for LOWs at pins 2 and 1 of ICs B1 and T on the Display/Control board. (A constant HIGH should be present at pin 14 of both ICs.)	Proceed to Step 4).	If pins 2 and 1 are HIGH, trace continuity to Ground (pin 3 of VR1) on the Display/Control board. If pin 14 is LOW, trace continuity to VR1, pin 2. Repair as necessary.
4)	As long as the ACCUMULATOR DISPLAY switch is held, pin 2 of IC G on the Interface board should be LOW. Pins 13 and 14 of IC G should be HIGH and pin 1 should be LOW.	Proceed to Step 5).	If pin 2 is HIGH, trace logic from IC G to IC Y1 on the Display/Control board. Check any suspected ICs according to the instructions on page 4-5. If pins 13 and 14 of IC G are LOW, trace continuity to VR1 pin 2 (on the Interface board) and repair as necessary.
5)	Pressing the ACCUMULATOR DISPLAY switch should produce LOW pulses at pins 8 and 9 of IC D on the Interface board. As a result, pin 10 of IC D should pulse HIGH. Pins 10 and 11 of IC K should also pulse HIGH.	Proceed to Step B.	Since pulses are usually too rapid to detect visually, run the following program to generate several pulses.

Location	Bit Pattern
000	333
001	377
002	303
003	000
004	000

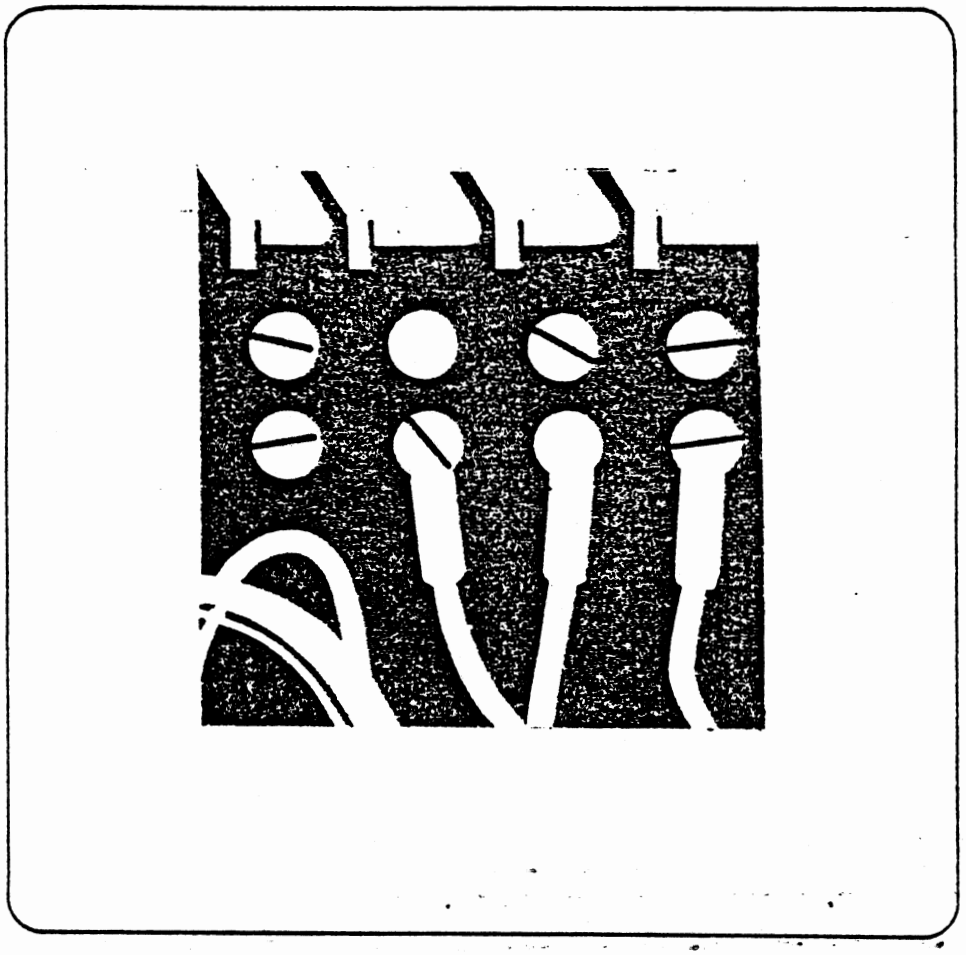
Step	Instructions	If Correct	If Incorrect
	If jumper JE to JF is present on the Interface board, a HIGH pulse should be present at pin 9 of IC K. The resulting LOW at pin 8 (of IC K) should produce a HIGH pulse at pin 11 of IC G.		(Note: Jumper JE to JF on the Display/Control board must be absent for the following check.) To check the levels of ICs D, J and G pin 4, stop the computer and examine to location 000. Lift the SINGLE STEP switch twice with the above program deposited into memory. If pin 10 of IC K is LOW, trace the SOUT logic to the CPU board. If pin 11 of IC K is LOW, trace the PWR signal to IC M on the CPU board. Check any suspected ICs according to the instructions on page 4-5.

B. If the ACCUMULATOR DEPOSIT switch will not function, check the inputs of ICs B1 and T as described in Step 14 on page 4-65.

C. If the IN switch will not function, check the SENSE switch operation as shown in Table 4-9, starting on page 4-50.

D. If the OUT switch will not function, check the sense switch operation as shown in Table 4-9, starting on page 4-50.

SECTION V



ASSEMBLY

SECTION V

ASSEMBLY

5-1. GENERAL

Section V contains instructions for the circuit and mechanical construction of the Altair 8800b computer. Included in this section are assembly hints, detailed component installation instructions, and printed circuit board and main frame assembly instructions.

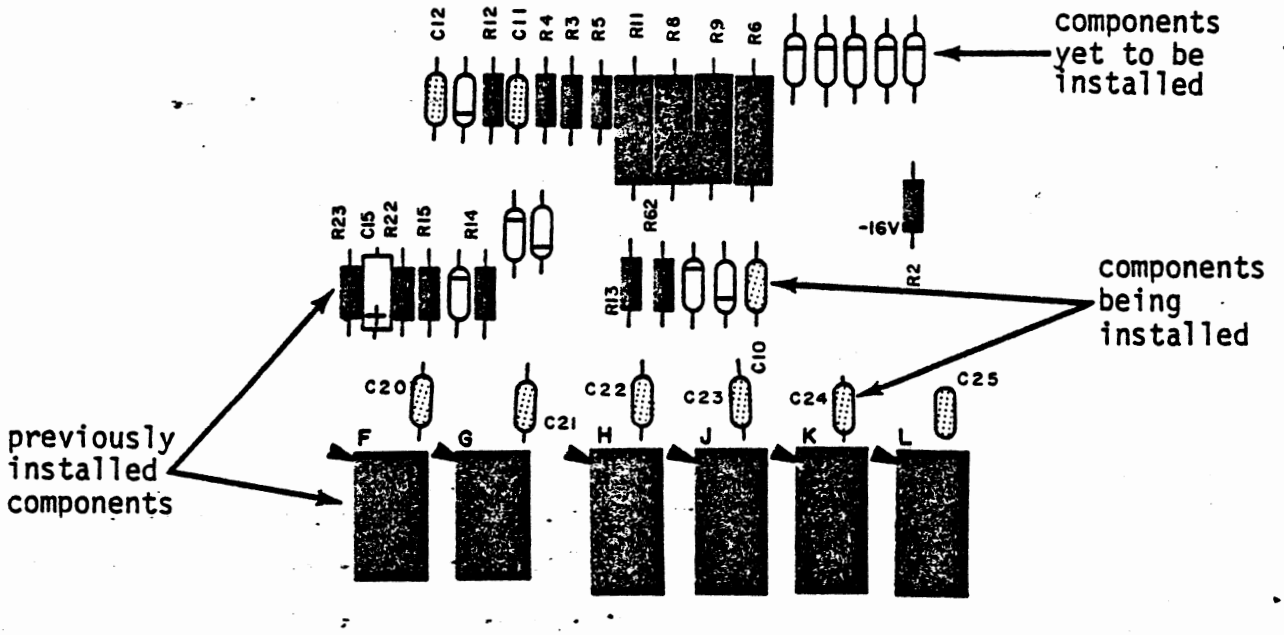
5-2. ASSEMBLY HINTS

Before beginning the construction of your unit, it is important that you read the "MITS Kits Assembly Hints" booklet included with your kit. Pay particular attention to the section on soldering, because most problems occur as the result of poor soldering. It is essential that you use the correct type of soldering iron. A 25-30 watt iron with a chisel tip (such as an Ungar 776 with a 7155 tip) is recommended in the assembly hints booklet.

> **NOTE**
>
> Some important warnings are also included in the hints booklet. Read them carefully before you begin work on your unit -- failure to heed these warnings could cause you to void your warranty.

Check the contents of your kit against Appendix B (Parts List) in this manual to make sure you have all the required components, hardware, and parts. The components are in plastic envelopes; do not open them until you need the components for an assembly step. You will need the tools called for in the "MITS Kits Assembly Hints" booklet.

As you construct your kit, follow the instructions in the order they are presented in the assembly manual. Always complete each section before going on to the next. Two organizational aids are provided throughout the manual to assist you: 1) Boxed off parts identification lists, with spaces provided to check off the components as they are installed; 2) reproductions of the silkscreens showing previously installed components, components being installed, and components yet to be installed (Figure 5-1).

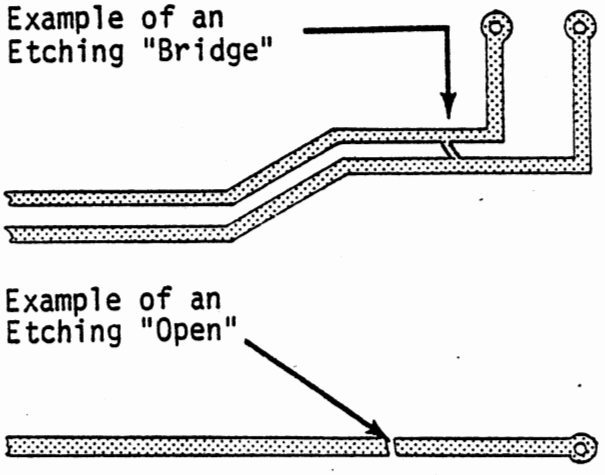


5-1. Typical Silkscreen

PRINTED CIRCUIT BOARD VISUAL INSPECTION

It is recommended that a visual inspection of the PC Board(s) in your kit be made before beginning the assembly procedures.

Look for etching "bridges" or etching "opens" in the printed circuit lands, as shown in the drawings below:



This could also appear as a "hairline" cut.

A thorough visual inspection will eliminate one possibility for errors, should the board not operate properly after it is assembled. Troubleshooting efforts may then be concentrated elsewhere.

5-3. COMPONENT INSTALLATION INSTRUCTIONS

Pages 5-6 through 5-12 describe the proper procedures for installing various types of components in your kit.

Read these instructions over very carefully and refer back to them whenever necessary. Failure to properly install components may cause permanent damage to the component or the rest of the unit; it will definitely void your warranty.

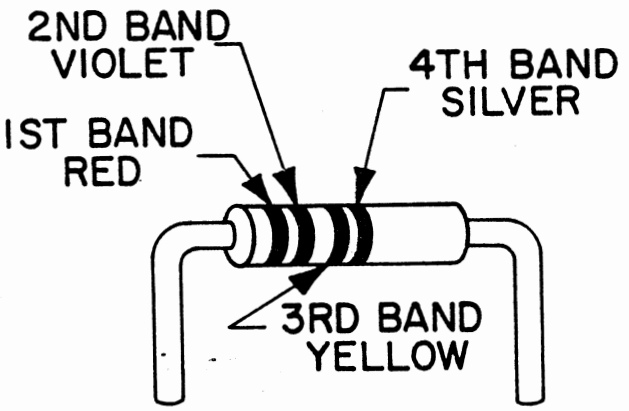
More specific instructions, or procedures of a less general nature, will be included within the assembly text itself.

Under no circumstances should you proceed with an assembly step without fully understanding the procedures involved. A little patience at this stage will save a great deal of time and potential "headaches" later.

5-4. Resistor Installation Instructions

Resistors have four (or possibly five) color-coded bands as represented in the chart below. The fourth band is gold or silver and indicates the tolerance. NOTE: In assembling a MITS kit, you need only be concerned with the three bands of color to the one side of the gold or silver (tolerance) band. These three bands denote the resistor's value in ohms. The first two bands correspond to the first two digits of the resistor's value and the third band represents a multiplier.

For example: a resistor with red, violet, yellow and silver bands has a value of 270,000 ohms and a tolerance of 10%. By looking at the chart below, you see that red is 2 and violet 7. By multiplying 27 by the yellow multiplier band (10,000), you find you have a 270,000 ohm (270K) resistor. The silver band denotes the 10% tolerance. Use this process to choose the correct resistor called for in the manual.



RESISTOR COLOR CODES		
COLOR	BANDS 1&2	3rd BAND (Multiplier)
Black	0	1
Brown	1	10^2
Red	2	10^3
Orange	3	10^4
Yellow	4	10^5
Green	5	10^6
Blue	6	10^7
Violet	7	10^8
Gray	8	10^9
White	9	

Use the following procedure to install the resistors onto the boards. Make sure the colored bands on each resistor match the colors called for in the list of Resistor Values and Color Codes given in the assembly instructions.

1. Using needle-nose pliers, bend the leads of the resistor at right angles to match their respective holes on the PC board.

2. Install the resistor into the correct holes on the silk-screened side of the PC board.

3. Holding the resistor in place with one hand, turn the board over and bend the two leads slightly outward.

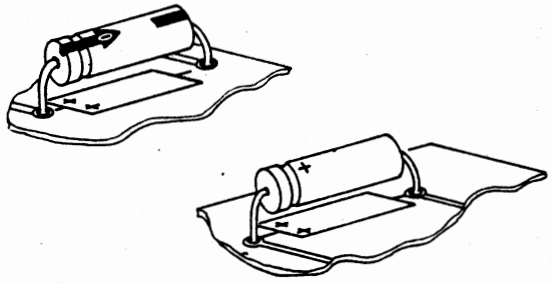
4. Solder the leads to the foil pattern on the back side of the board; then clip off any excess lead lengths.

5-5. Capacitor Installation Instructions

A. Electrolytic Capacitors

Polarity must be noted on electrolytic capacitors before they are installed.

The electrolytic capacitors contained in your kit may have one or possibly two of three types of polarity markings. To determine the correct orientation, look for the following.



ELECTROLYTIC CAPACITOR

One type will have plus (+) signs on the positive end; another will have a band or a groove around the positive side in addition to the plus signs. The third type will have an arrow on it; in the tip of the arrow there will be a negative (-) sign. The capacitor must be oriented so the arrow points to the negative side.

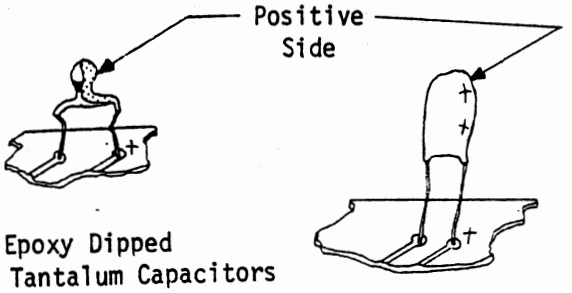
Install the electrolytic capacitors using the following procedure. Make sure you have the correct capacitor value before installing each one.

1. Bend the two leads of the capacitor at right angles to conform to their respective holes on the board. Insert the capacitor into the holes on the silk-screened side of the board, aligning the positive side with the "+" signs printed on the board.
2. Holding the capacitor in place, turn the board over and bend the two leads slightly outward. Solder the leads to the foil (bottom) side of the board and, clip off any excess lead lengths.

B. Epoxy Dipped Tantalum, Epoxy Dipped Ceramic, and Ceramic Disk Capacitors

Polarity must be noted on epoxy dipped tantalum capacitors before they are installed.

There are two types of epoxy dipped tantalum capacitors contained in you your kit. The first type is blue on the positive side. The second type is marked with "+" signs on the positive side. Both types of epoxy dipped tantalum capacitors are shown in the drawings below.



Epoxy Dipped
Tantalum Capacitors

The epoxy dipped ceramic capacitors and the ceramic disk capacitors are non-polarized.

These two types of capacitors are shown in the drawings below.

Epoxy Dipped
Ceramic Capacitor

Ceramic Disk
Capacitor

Install these 4 types of capacitors using the following procedure. Make sure you have the correct capacitor value before installing each one.

1. Bend the two capacitor leads to conform to their respective holes on the board.
2. Insert the capacitor into the correct holes from the silk-screened side of the board. Holding the capacitor in place, turn the board over and bend the two leads slightly outward.
3. Solder the two leads to the foil (bottom) side of the board and, clip off any excess lead lengths.

5-6. Diode Installation Instructions

NOTE: Diodes are marked with a band on one end indicating the cathode end. Each diode must be installed so that the end with the band is oriented towards the band printed on the PC board. Failure to orient the diodes correctly may result in permanent damage to your unit.

DIODE

Use the following procedure to install diodes onto the board. Refer to the list of Diode Part Numbers included for each board to make sure you install the correct diode each time.

1. Bend the leads of the diode at right angles to match their respective holes on the board.

2. Insert the diode into the correct holes on the silk screen, making sure the cathode end is properly oriented. Turn the board over and bend the leads slightly outward.

3. Solder the two leads to the foil pattern on the back side of the board; then clip off any excess lead lengths.

5-7. Transistor Installation Instructions

To install transistors, use the following instructions.

NOTE: Always check the part number of each transistor before you install it. (See listing of Transistor Part Numbers for each board.) Some transistors look identical but differ in electrical characteristics, according to part number. If you have received substitute part numbers for the transistors in your kit, check the Transistor Identification Chart which follows these instructions to be sure you make the correct substitutions.

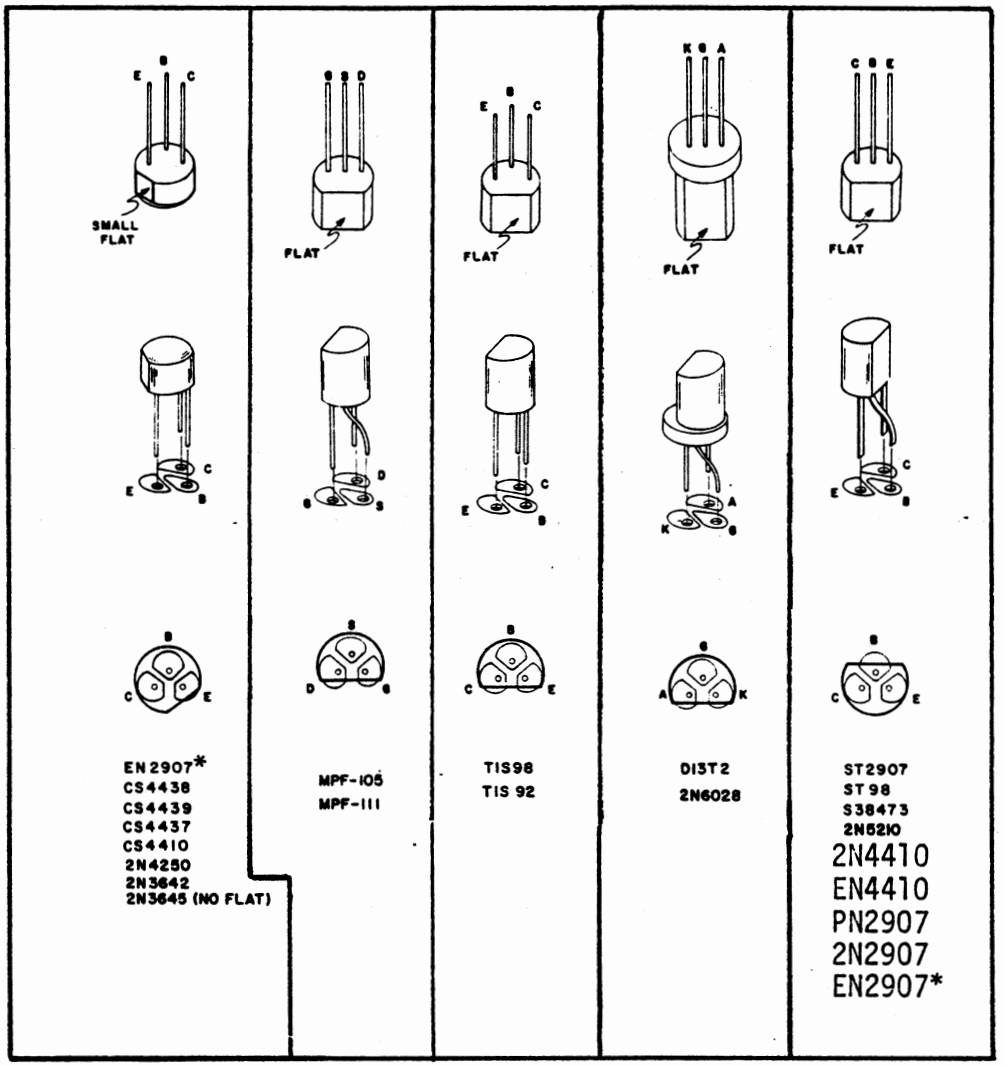
NOTE: Always make sure the transistor is oriented so that the emitter lead is installed in the hole on the PC board labeled with an "E". To determine which lead is the emitter lead, refer to the Transistor Identification Chart.

1. After the correct transistor has been selected and the leads have been properly oriented, insert the transistor into the holes on the silk-screened side of the board.

2. Holding the transistor in place, turn the board over and bend the three leads slightly outward.

3. Solder the leads to the foil pattern on the back side of the board; then clip off any excess lead lenghts.

TRANSISTOR IDENTIFICATION CHART



IN THE ILLUSTRATION ABOVE THE OUTLINE OF EACH TYPE OF TRANSISTOR IS SHOWN ABOVE THE PADS ON THE CIRCUIT BOARD WITH THE CORRECT DESIGNATION FOR EACH OF THE THREE LEADS. USE THIS INFORMATION TOGETHER WITH THE INFORMATION IN THE ASSEMBLY MANUAL FOR THE CORRECT ORIENTATION OF THE TRANSISTORS AS YOU INSTALL THEM.

THE FOLLOWING IS A LIST OF POSSIBLE SUBSTITUTIONS: IF ANY OTHERS ARE USED YOU WILL RISK DAMAGING YOUR UNIT:

2N4410 = EN4410 = CS4410 = CS4437, CS4438, TIS98, ST98, S38473 (NPN)

EN2907 = 2N2907 = PN2907 = ST2907, CS4439 (PNP)

WHEN MAKING SUBSTITUTIONS, REFER TO THE ILLUSTRATION TO DETERMINE THE CORRECT ORIENTATION FOR THE THREE LEADS.

*Configuration of the leads on EN2907 may vary.

5-8. IC Installation Instructions

All ICs must be oriented so that the notched end is toward the end with the arrowhead printed on the PC board. Pin 1 of the IC should correspond with the pad marked with the arrowhead. If the IC does not have a notch on one end, refer to the IC Identification Chart to identify Pin 1.

To prepare ICs for installation:
All ICs are damaged easily and should be handled carefully -- especially static-sensitive MOS ICs. Always try to hold the IC by the ends, touching the pins as little as possible. When you remove the IC from its holder, CAREFULLY straighten any bent pins using needle-nose pliers. All pins should be evenly spaced and should be aligned in a straight line, perpendicular to the body of the IC itself.

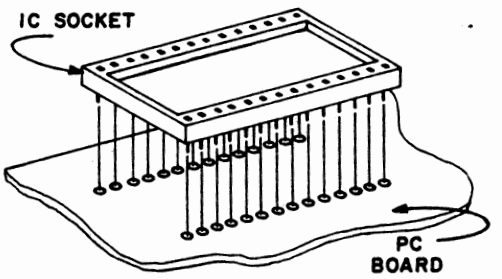
A. Installing ICs without sockets:

1. Orient the IC so that Pin 1 coincides with the arrowhead on the PC board.
2. Align the pins on one side of the IC so that just the tips are inserted into the proper holes on the board.
3. Lower the other side of the IC into place. If the pins don't go into their holes right away, rock the IC back, exerting a little inward pressure, and try again. Be patient. The tip of a small screwdriver may be used to help guide the pins into place. When the tips of all the pins have been started into their holes, push the IC into the board the rest of the way. Tape the IC to the board with a piece of masking tape.
4. Turn the board over and solder each pin to the foil pattern on the back side of the board. Be sure to solder each pin and be careful not to leave any solder bridges. Remove the masking tape.

> WARNING:
> Make sure none of the pins have been pushed underneath the IC during insertion.

B. Installing ICs with sockets:

1. Referring to the drawing below, set the IC socket into the designated holes on the board and secure it with a piece of masking tape.



2. Turn the board over and solder each pin to the foil pattern on the back side of the board. Be sure to solder each pin and be careful not to leave any solder bridges. Remove the masking tape.
3. Orient the IC over the socket so that Pin 1 coincides with the arrowhead on the PC board.
4. Align the pins on one side of the socket so that just the tips are inserted into the holes.
5. Lower the other side of the IC into place. If the pins don't go into their holes right away, rock the IC back, exerting a little inward pressure, and try again. Be patient. When the tips of all the pins have been started into their holes, push the IC into the socket the rest of the way.

MOS IC SPECIAL HANDLING PRECAUTIONS

There are several MOS integrated circuits contained in this kit. These IC's are very sensitive to static electricity and transient voltages. In order to prevent damaging these components, read over the following precautions and adhere to them as closely as possible. FAILURE TO DO SO MAY RESULT IN PERMANENT DAMAGE TO THE IC.

1) All equipment (soldering iron, tools, solder, etc.) should be at the same potential as the PC board, the assembler, the work surface and the IC itself along with its container. This can be accomplished by continuous physical contact with the work surface, the components, and everything else involved in the operation.

2) When handling the IC, develop the habit of first touching the conductive container in which it is stored before touching the IC itself.

3) If the IC has to be moved from one container to another, touch both containers before doing so.

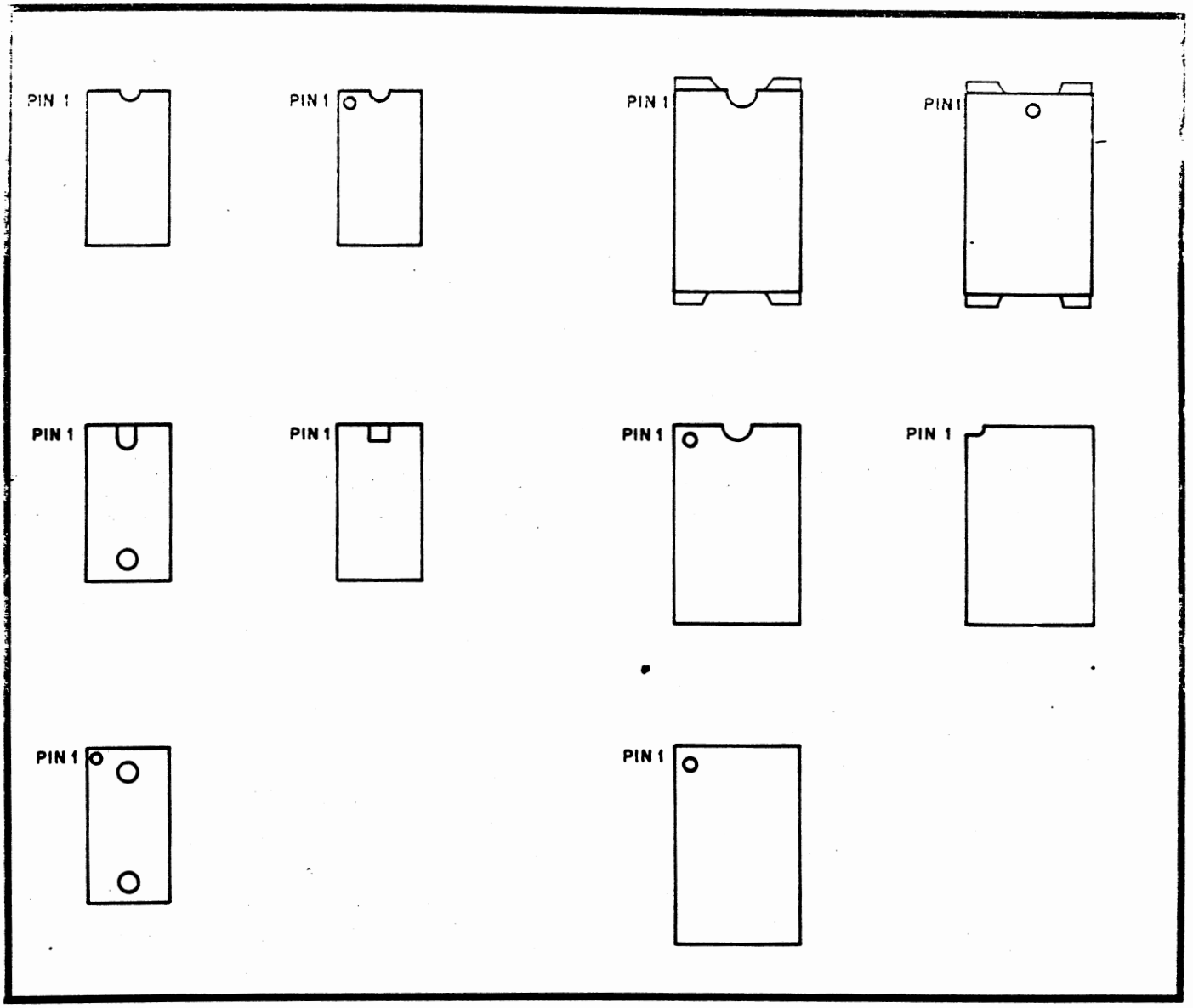
4) Do not wear clothing which will build up static charges. Preferably wear clothing made of cotton rather than wool or synthetic fibers.

5) Always touch the PC board before touching the IC to the board. Try to maintain this contact as much as possible while installing the IC.

6) Handle the IC by the edges. Avoid touching the pins themselves as much as possible.

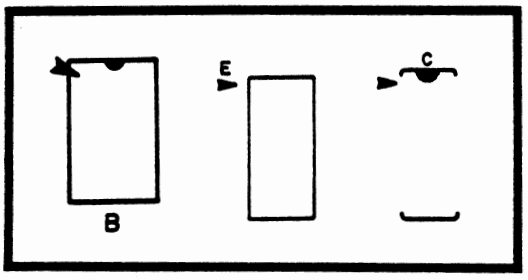
7) **Dry air moving over plastic can result in the development of a significant static charge. Avoid placing the IC near any such area or object.**

8) In general, never touch anything to the IC that you have not touched first while touching both it and the IC itself.



INTEGRATED CIRCUITS (IC's) CAN COME WITH ANY ONE OF, OR A COMBINATION OF, SEVERAL DIFFERENT MARKINGS. THESE MARKINGS ARE VERY IMPORTANT IN DETERMINING THE CORRECT ORIENTATION FOR THE IC's WHEN THEY ARE PLACED ON THE PRINTED CIRCUIT BOARDS. REFER TO THE ABOVE DRAWING TO LOCATE PIN 1 OF THE IC's, THEN USE THIS INFORMATION IN CONJUNCTION WITH THE INFORMATION BELOW TO PROPERLY ORIENT EACH IC FOR INSTALLATION.

WARNING: INCORRECTLY ORIENTED IC's MAY CAUSE PERMANENT DAMAGE!



THE DRAWING ON THE LEFT INDICATES VARIOUS METHODS USED TO SHOW THE POSITION OF IC's ON THE PRINTED CIRCUIT BOARDS. THESE ARE SILK-SCREENED DIRECTLY ON THE BOARD. THE ARROWHEAD INDICATES THE POSITION FOR PIN 1 WHEN THE IC IS INSTALLED.

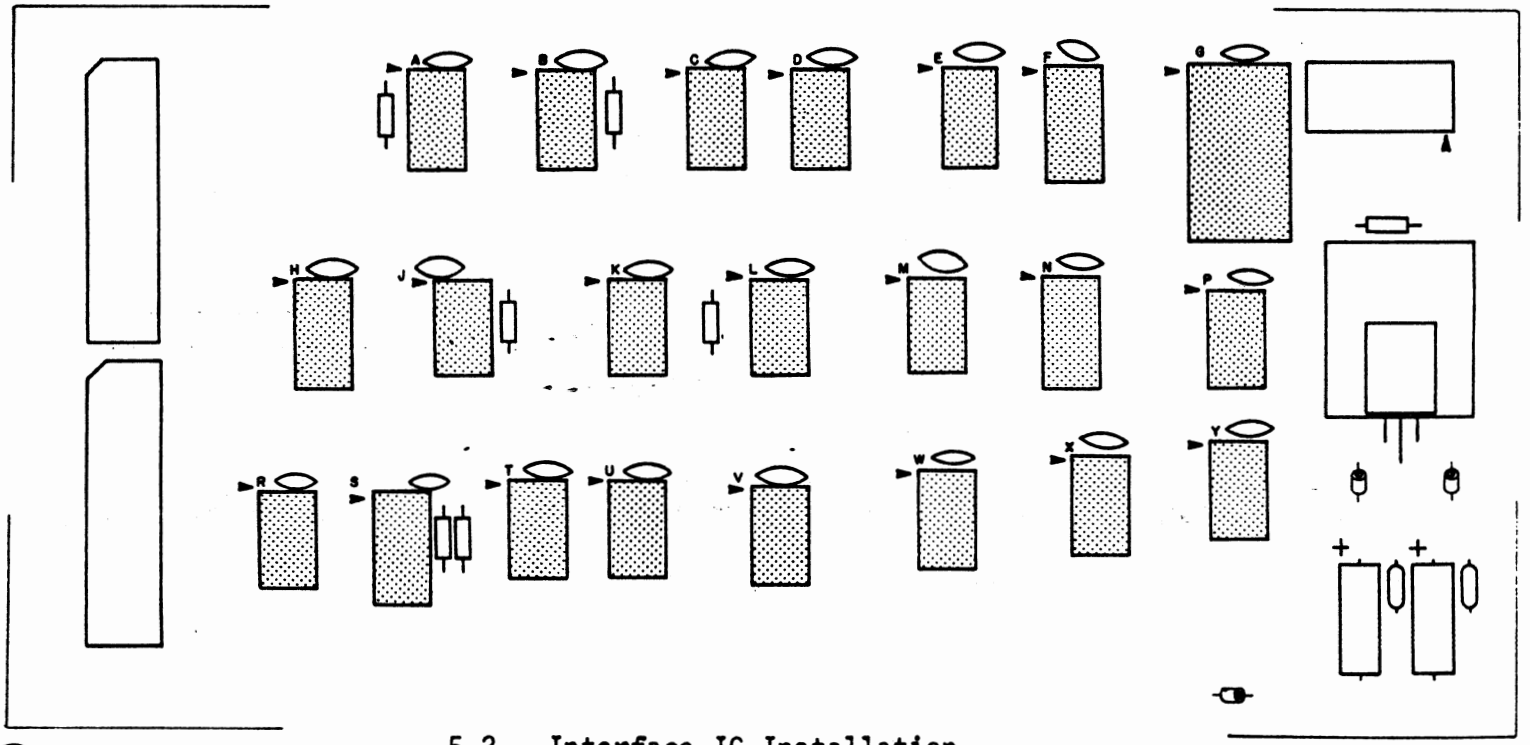
5-9. INTERFACE CARD ASSEMBLY

5-10. IC INSTALLATION (Figure 5-2)

Install the following 22 integrated circuits (Bag 1) on the Interface Card according to the IC Installation Instructions, Section A, given on page 5-10. IC G will be installed with a 24-pin socket according to the IC Installation Instructions, Section B, page 5-10.

The chart below lists the 22 ICs, their corresponding part numbers, and acceptable part substitutions.

IC Part Numbers	
( ) C,E,M,P,R,T U,V,W,X,Y	74LS04 or 74LS14
( ) A,B,L	74LS20 or 74LS13
(X) F,H,N,S	74367 or 8097 or 8T97
(X) J	7400 or 74LS00
(X) D	7402 or 74LS02
( ) K	7410 or 74LS10
(X) G (with socket)	8212



5-2. Interface IC Installation

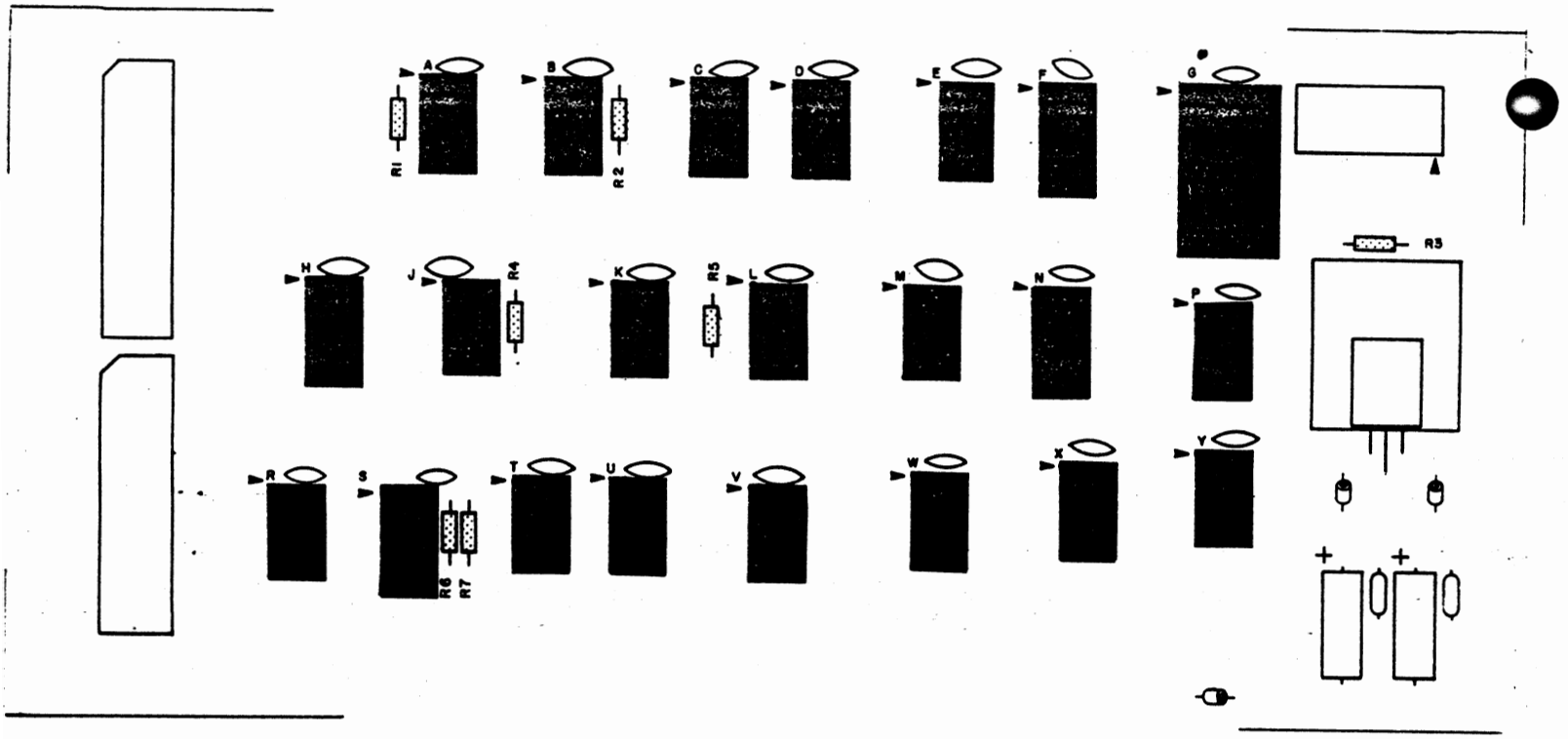
5-11. RESISTOR INSTALLATION (Figure 5-3)

Install the 7 resistors, R1 through R7 (Bag 5), on the Interface Card according to the Resistor Installation Instructions given on page 5-6.

Resistor Values	
(X) R1 through R7	2.2K ohm (red, red, red) 1/2W or 1/4W

NOTE

Save the excess resistor leads for use in Paragraph 5-15.



5-3. Interface Resistor Installation

5-12. SUPPRESSOR CAPACITOR INSTALLATION (Figure 5-4)

There are 22 suppressor capacitors (Bag 2) to be installed on the Interface Card. These capacitors are used for noise suppression. They are located next to the ICs on the silkscreen, but they have no individual component designations. Install the suppressor capacitors according to the Ceramic Disk Capacitor Installation Instructions given on page 5-7.

Suppressor Capacitor Values	
(✓) 22 suppressor capacitors	0.1uf, 12V or 0.1uf, 16V

NOTE

Save the clipped off capacitor leads for use as jumper wires in Paragraph 5-14.

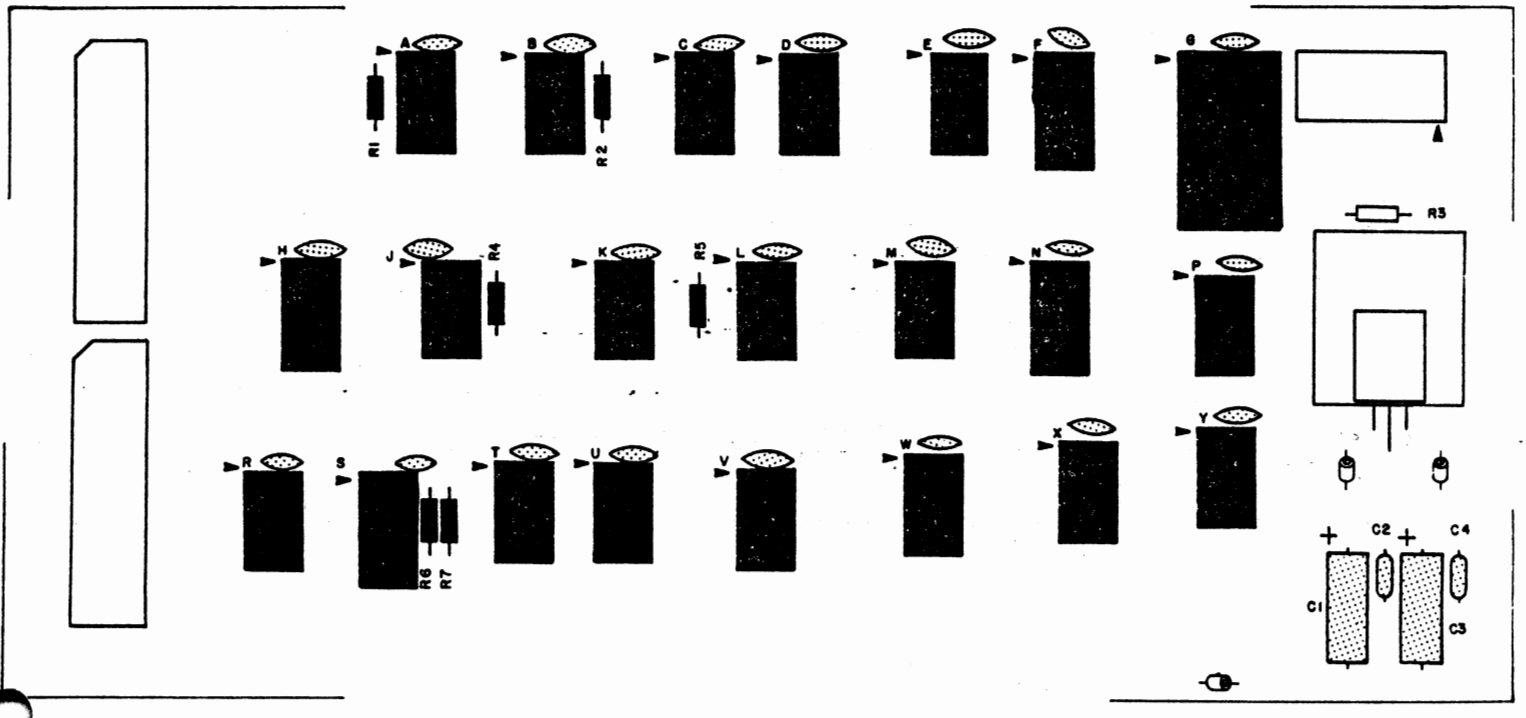
5-13. CAPACITOR INSTALLATION (Figure 5-4)

Install the two electrolytic capacitors, C1 and C3 (Bag 2), and the two ceramic disk capacitors, C2 and C4 (Bag 2), according to the instructions given on page 5-7.

The chart below lists the 4 capacitors and their values.

Capacitor Values		
(✓)	C1, C3*	20uf - 35uf, 12V - 20V, electrolytic
(✓)	C2, C4	0.1uf, 12V or 0.1uf, 16V, ceramic disk

*C1 and C3 may have any value within the range shown.



5-4. Interface Suppressor Capacitor and Capacitor Installation

5-14. JUMPER CONNECTIONS (Figure 5-5)

There are two jumper wires to be installed on the Interface Card. Use the capacitor leads saved from the Suppressor Capacitor Installation. Cut two leads, to 1-inch lengths, and jumper the following pads on the Interface Card.

Jumper Connections
(X) JC to JD
(X) JE to JF

NOTE
Do not jumper JA to JB here.

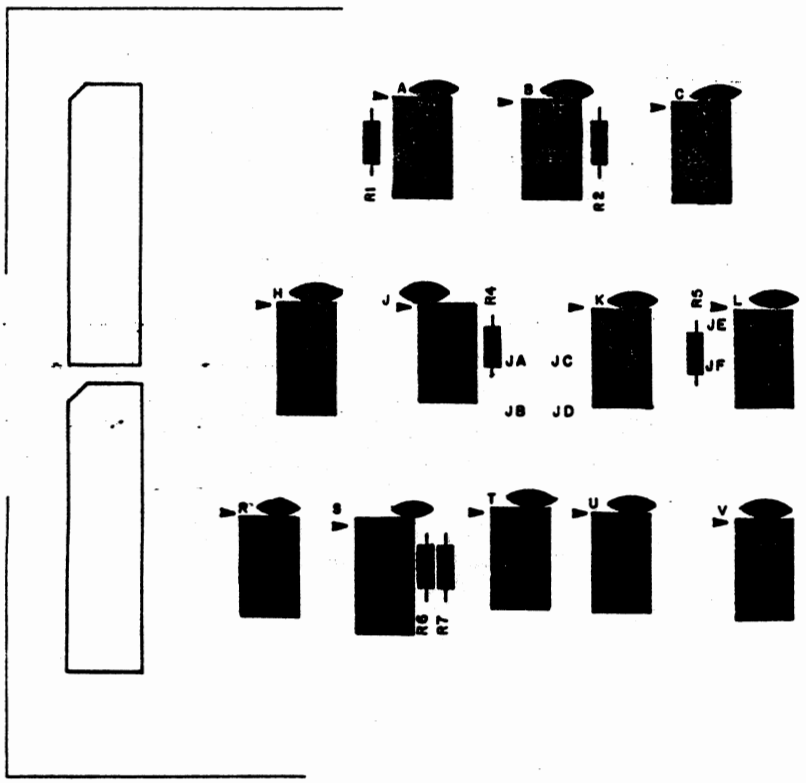
5-15. FERRITE BEAD INSTALLATION (Figure 5-6)

Install the three ferrite beads, L1 through L3 (Bag 3), according to the following instructions.

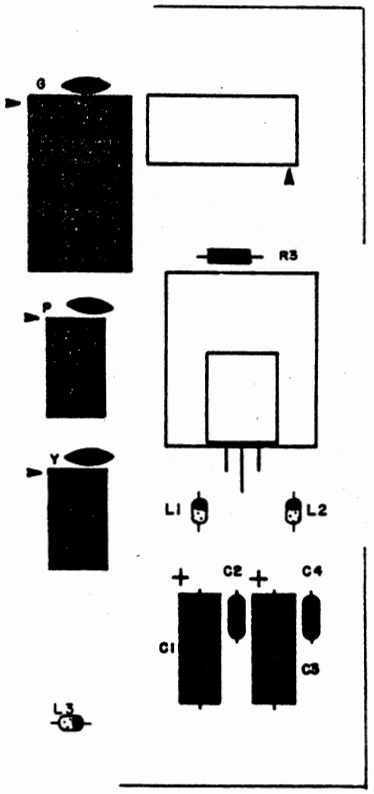
1. Using the resistor leads saved from Paragraph 5-11, cut three 1-inch lead lengths.

2. Insert a lead through the bead, and bend the ends so they conform to their designated holes on the Interface Card.

3. Insert the leads into the card, and solder to the foil (bottom) side of the card. Be sure not to leave any solder bridges and clip off any excess lead lengths.



5-5. Interface Jumper Connections



5-6. Interface Ferrite Bead Installation

5-16. VOLTAGE REGULATOR INSTALLATION (Figure 5-7)

Install the voltage regulator, VR1 (Bag 1), and heat sink on the Interface Card according to the following instructions.

1. Set the regulator in place on the silk-screened side of the Interface Card, aligning the leads with their designated holes.

2. Use needle-nose pliers to bend each of the three leads at a right angle to conform to its proper hole on the card.

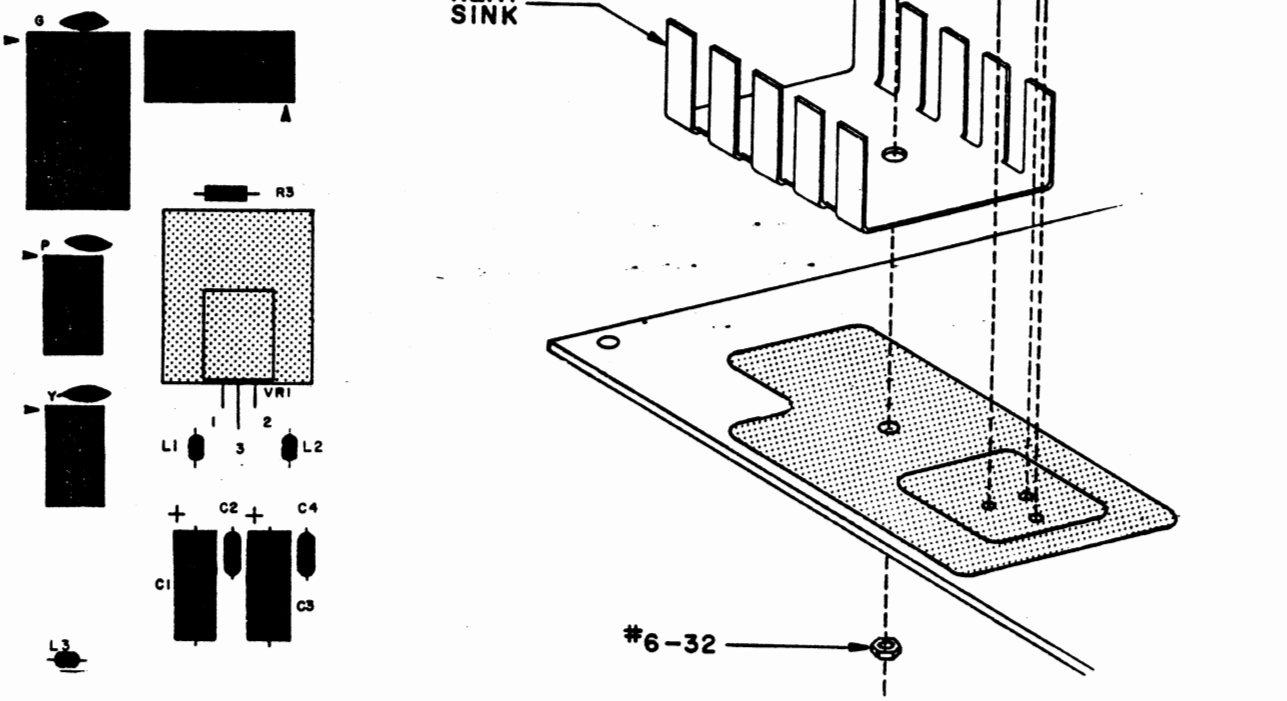
> NOTE
>
> Use heat sink grease when installing this component. Apply the grease to all metal surfaces which come in contact with each other.

3. Referring to Figure 5-7, set the regulator and heat sink in place on the silk-screened side of the card. Secure them in place with a #6-32 x 3/8 inch screw, a #6 lockwasher, and a #6-32 nut.

4. Solder the three leads to the foil (bottom) side of the card. Be sure not to leave any solder bridges.

5. Clip off any excess lead lengths.

Voltage Regulator Part Number	
(X) VR1	7805



5-7. Interface Voltage Regulator Installation

5-17. MALE CONNECTOR INSTALLATION (Figure 5-8)

Install one 10-pin Male Connector, P3 (Bag 3), on the Interface Card according to the following instructions.

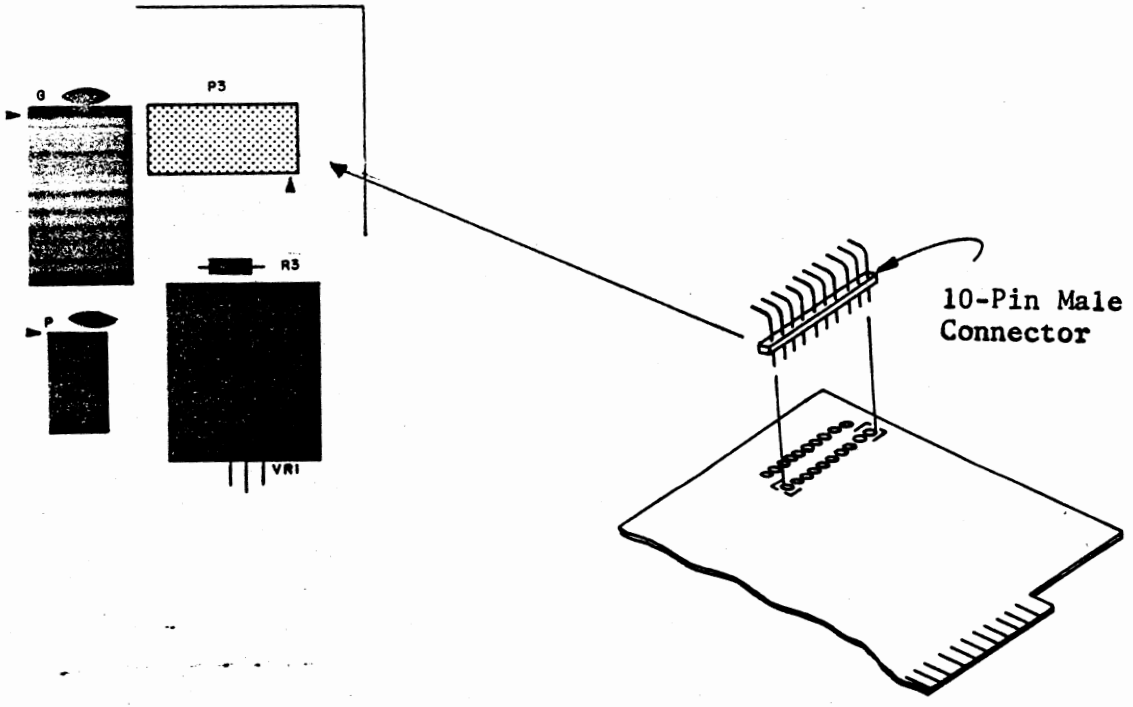
1. Orient the connector as shown in Figure 5-8, with the bent pins pointing towards the top of the card.

2. Insert the short pins into the 10 designated holes on the silkscreened side of the card.

3. Solder each pin to the foil (bottom) side of the card. Be sure not to leave any solder bridges.

4. Clip off any excess lead lengths.

5. The arrow on the silkscreen points to Pin #1. After installing the male connector, clip off pin #2 of the connector. This is done for keying purposes. Further keying instructions are given in Paragraph 5-76.



5-8. Interface Male Connector Installation

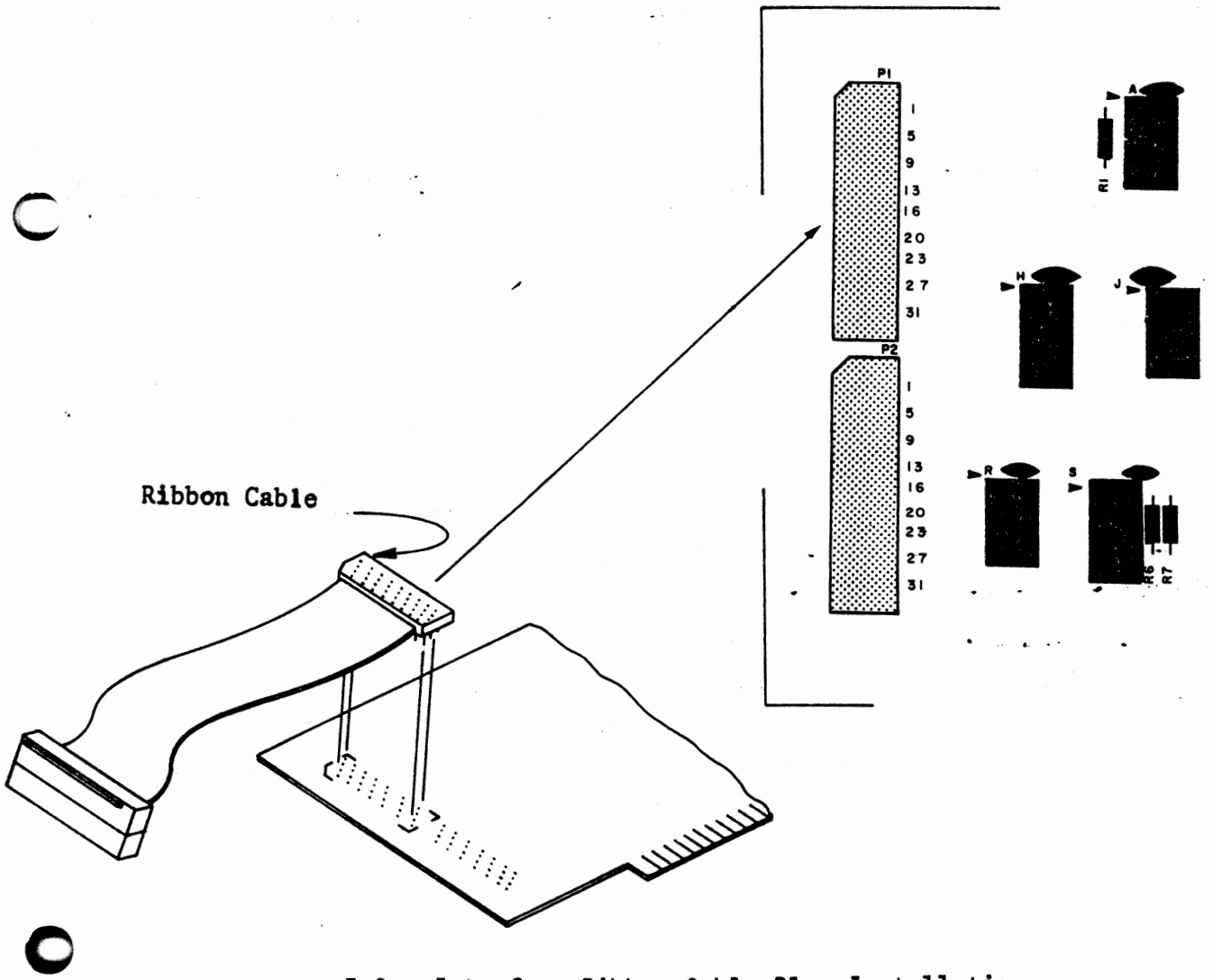
5-18. RIBBON CABLE PLUG INSTALLATION (FIGURE 5-9)

Install the two ribbon cable plugs, P1 and P2 (Bag 4), on the Interface Card according to the following instructions.

1. Orient the Ribbon Cable Plug as shown in Figure 5-9, so that the socket end of the plug hangs over the left side of the card.

2. Insert the pins into their proper holes and solder each pin to the foil (bottom) side of the card. Be sure not to leave any solder bridges.

> NOTE
>
> The socket end of the Ribbon Cable Plug will be connected later in Paragraph 5-75.



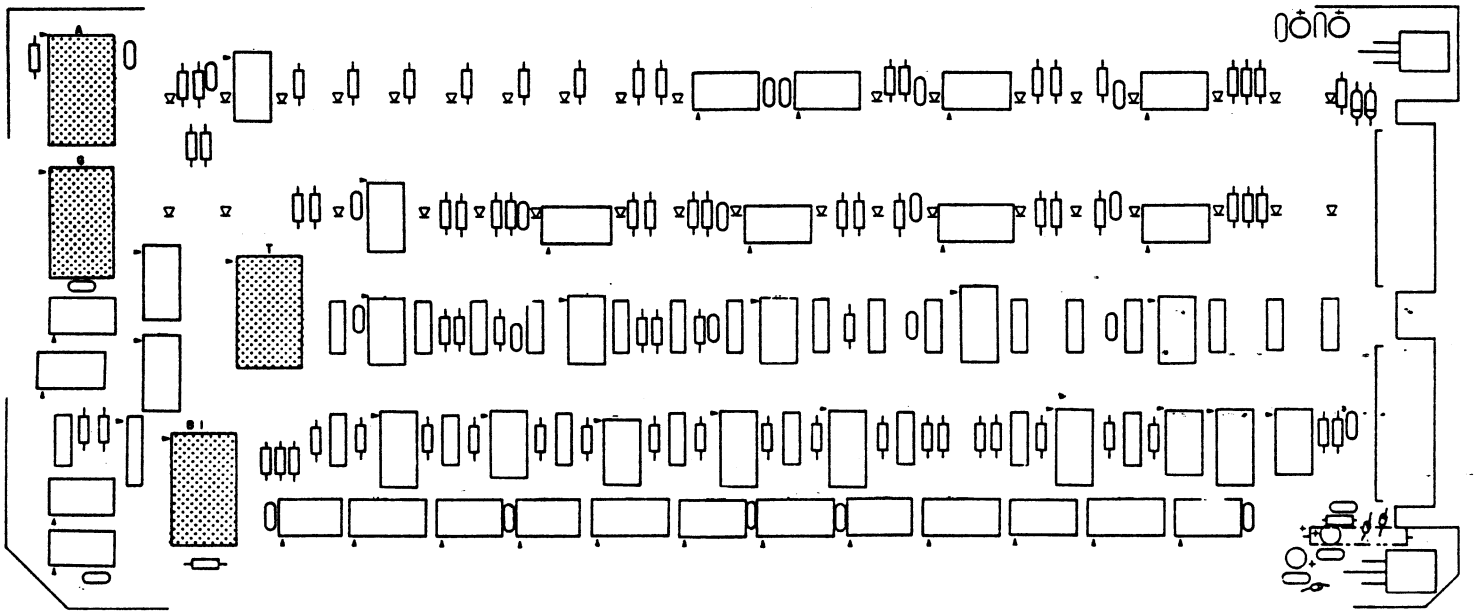
5-9. Interface Ribbon Cable Plug Installation

5-19. DISPLAY/CONTROL BOARD ASSEMBLY

5-20. IC SOCKET AND IC INSTALLATION (Figure 5-10)

There are 4 ICs, A, G, T, B1 (Bag10), to be installed with sockets on the Display/Control Board. Install these sockets and ICs according to the Integrated Circuit Installation Instructions, Section B, given on page 5-10.

Silkscreen Designation	IC Part Number	Socket Size
( ) A, T, B1	8212	24-pin
( ) G	1702A*	24-pin
*IC G is a programmed PROM IC labelled "B D/C".		

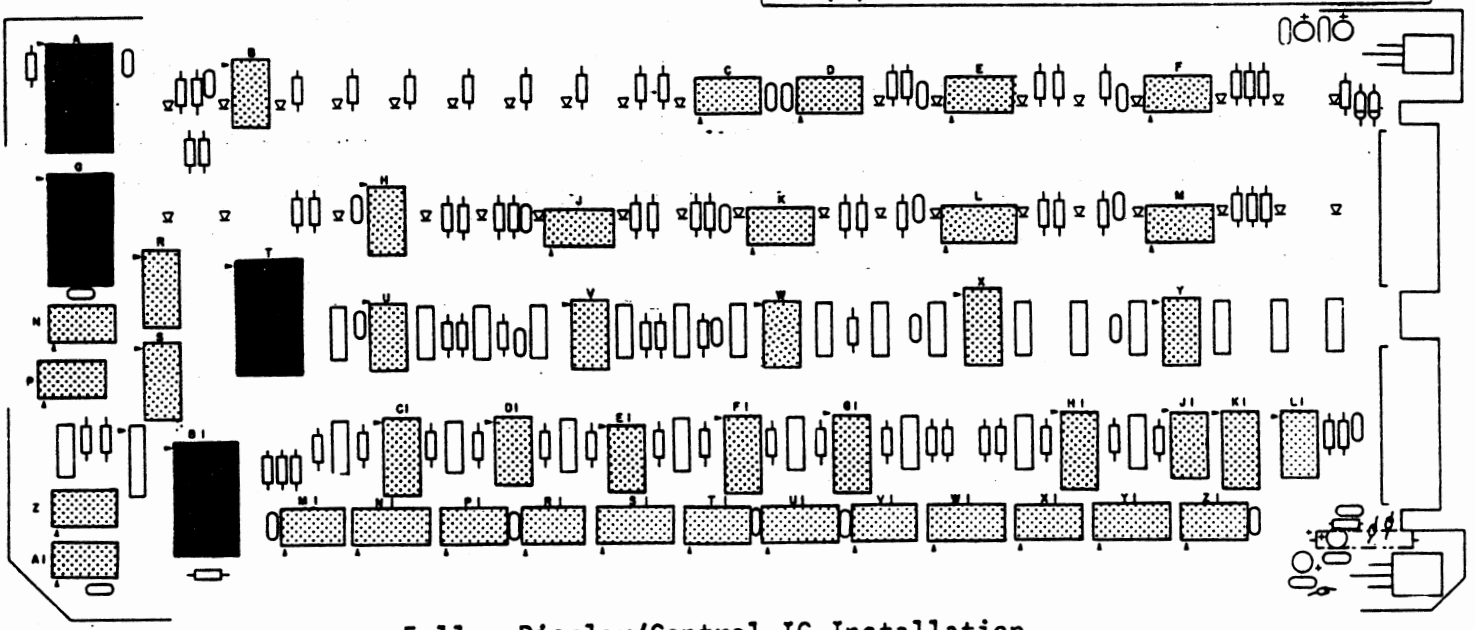


5-10. Display/Control IC Socket and IC Installation

5-21. IC INSTALLATION (Figure 5-11)

Install the following 42 integrated circuits (Bag 1) on the Display/ Control Board according to the Integrated Circuit Installation Instructions, Section A, given on page 5-10.

IC Part Numbers	
( ) B,D,E,F,H,K,M	7407
( ) U,W,Y,V1,Z1	7405 or 74LS05
( ) C1,N1,F1,U1, G1,W1,H1,Y1	74LS175
( ) L1,M1	74LS74
( ) K1	74367 or 8097 or 8T97
( ) R,S	8T98
( ) P	7493
( ) P1,Z	7400 or 74LS00
( ) C,J1,E1,R1	74LS04
( ) A1	74LS14
( ) J	74L10
( ) V,D1,T1	7410 or 74LS10
( ) X1,N	74LS30 or 74L30
( ) L,X	4040
( ) S1	4009 or 4049



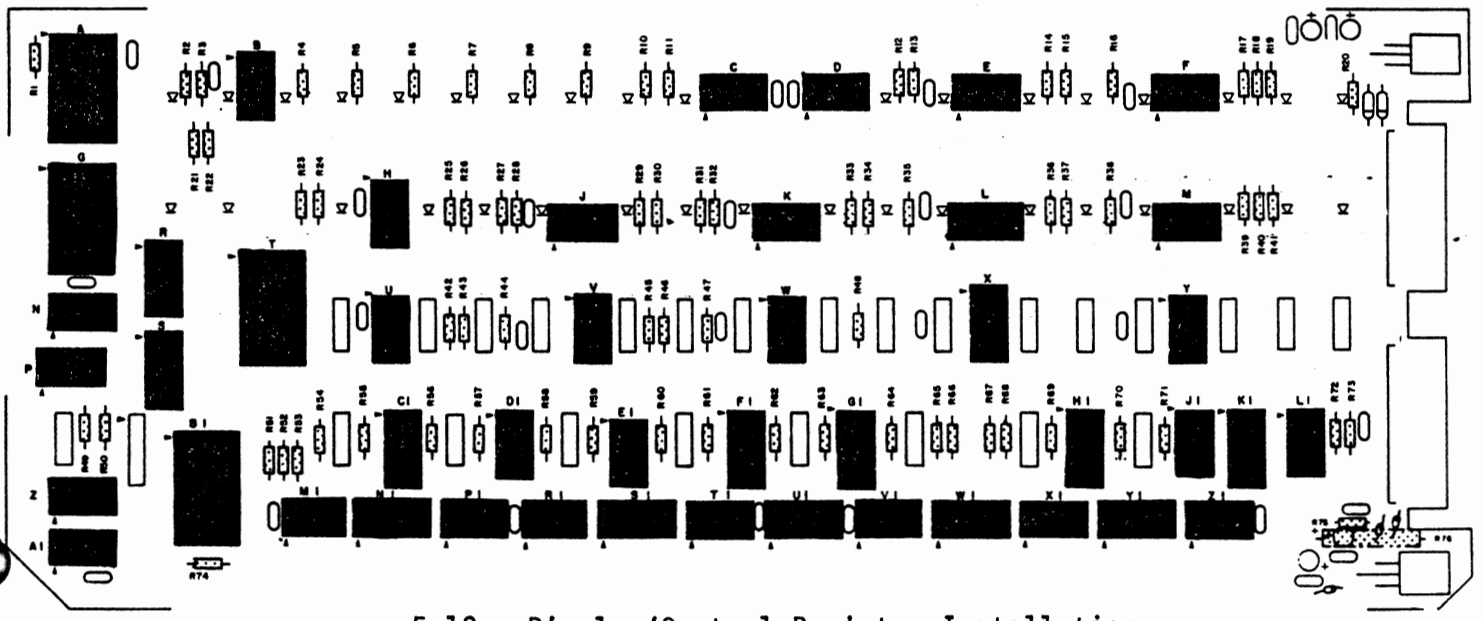
5-11. Display/Control IC Installation

5-22. RESISTOR INSTALLATION (Figure 5-12)

There are 76 resistors (Bags 2, 3, and 4) to be installed on the Display/Control Board. One of these resistors, R76, must be installed on the back of the board. Install the resistors according to the Resistor Installation Instructions given on page 5-6. Install R76 as shown by the dotted outline on the silkscreen below.

> **NOTE**
>
> Save any excess resistor leads for jumper connections in Paragraph 5-24 and for ferrite bead installation in Paragraph 5-28.

Resistor Values	
( ) R2-R19, R21, R22, R24-R26, R28-R30, R32-R41, R73	220 ohm (red, red, brown) 1/2W
( ) R50, R75	100 ohm (brown, black, brown) 1/2W
( ) R66	470 ohm (yellow, violet, brown) 1/2W
( ) R20	1K ohm (brown, black, red) 1/2W
( ) R1, R23, R27, R31, R42-R49, R51-R65, R67-R72, R74	2.2K ohm (red, red, red) 1/2W
( ) R76	5 ohm (wire wound resistor; has no color codes) 5W



5-12. Display/Control Resistor Installation

5-23. RESISTOR PACK INSTALLATION (Figures 5-13 and 5-14)

According to supply variations, your kit will contain either one resistor pack, RP1 (Bag 2), or 5 individual 4.7K-ohm resistors to be substituted for RP1.

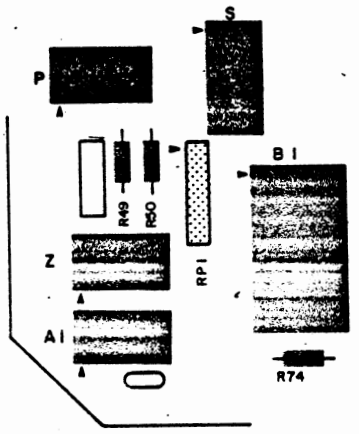
A. Resistor Pack (Figure 5-13). Use the following instructions to install the resistor pack as shown in Figure 5-13.

1. The resistor pack has a small dot printed at one end. This dot must correspond with the dot printed on the PC Board. Insert the resistor pack perpendicular to the silk-screened side of the board, aligning the small dots.

2. Solder each pin of the resistor pack to the foil (bottom) side of the board. Be careful not to leave any solder bridges.

3. Clip off any excess lead lengths.

Resistor Pack	Value
( ) RP1	4.7K ohms



5-13. Display/Control Resistor Pack Installation

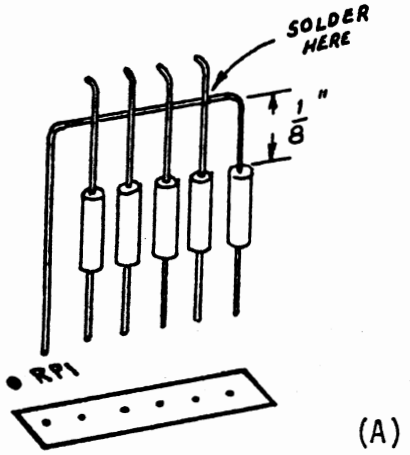
B. Substitute Resistors (Figure 5-14). If your kit is not supplied with a resistor pack, use the following instructions to install the 5 substitute resistors.

1. The resistor pack designation on the silkscreen has 5 holes. The left-most hole is marked on the silkscreen with a small dot. Vertically insert one resistor into the right-most hole on the board. Bend the top lead at a right angle as shown in Figure 5-14A until it is parallel with the board. Then bend the end of the lead at a right angle so that it may be inserted into the left-most hole marked with a small dot.

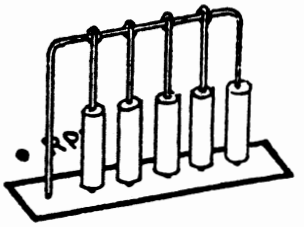
2. Solder the two inserted leads to the foil (bottom) side of the board.

3. Insert the remaining four resistors vertically into the designated holes on the silkscreen. Solder each of the top leads to the common horizontal lead as shown in Figure 5-14A. It may be helpful to bend the top leads against the horizontal lead for better contact before soldering.

4. Solder the inserted leads of the four resistors to the foil (bottom) side of the board. Clip off all excess leads from the top and bottom of the resistors. The properly completed resistor assembly is shown in Figure 5-14B.



(A)


(B)

5-14. Display/Control Substitute Resistor Assembly

5-24. JUMPER CONNECTIONS (Figure 5-15)

NOTE

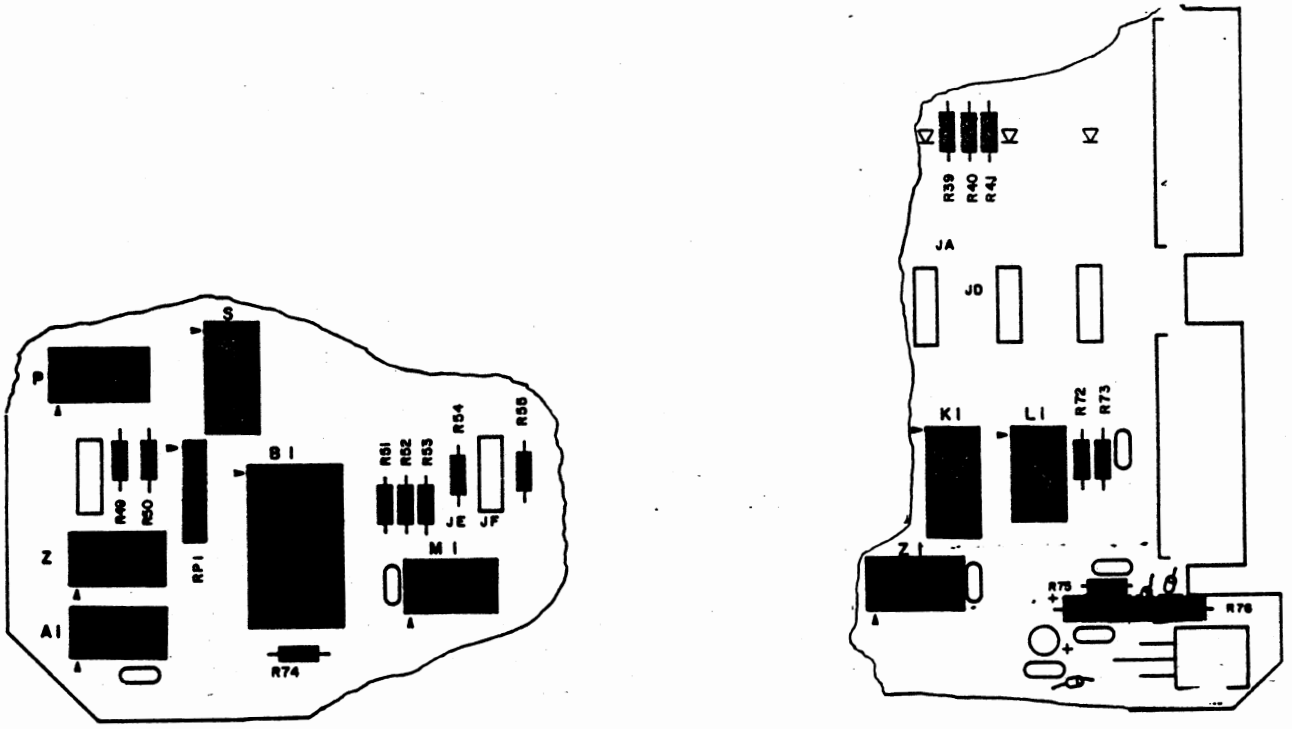
The following jumper connections are installed for standard 8800b operations. Refer to Paragraph 3-40 for jumper options.

There are two jumper wires to be installed on the Display/Control Board. Use the resistor leads saved from Paragraph 5-22 as jumper wires. Cut two leads to 1-inch lengths and jumper the following pads on the Display/Control Board.

Jumper Connections
( ) JE to JF
( ) JA to JD

NOTE

Do not jumper JH, JJ, or JG at this time.



5-15. Display/Control Jumper Connections

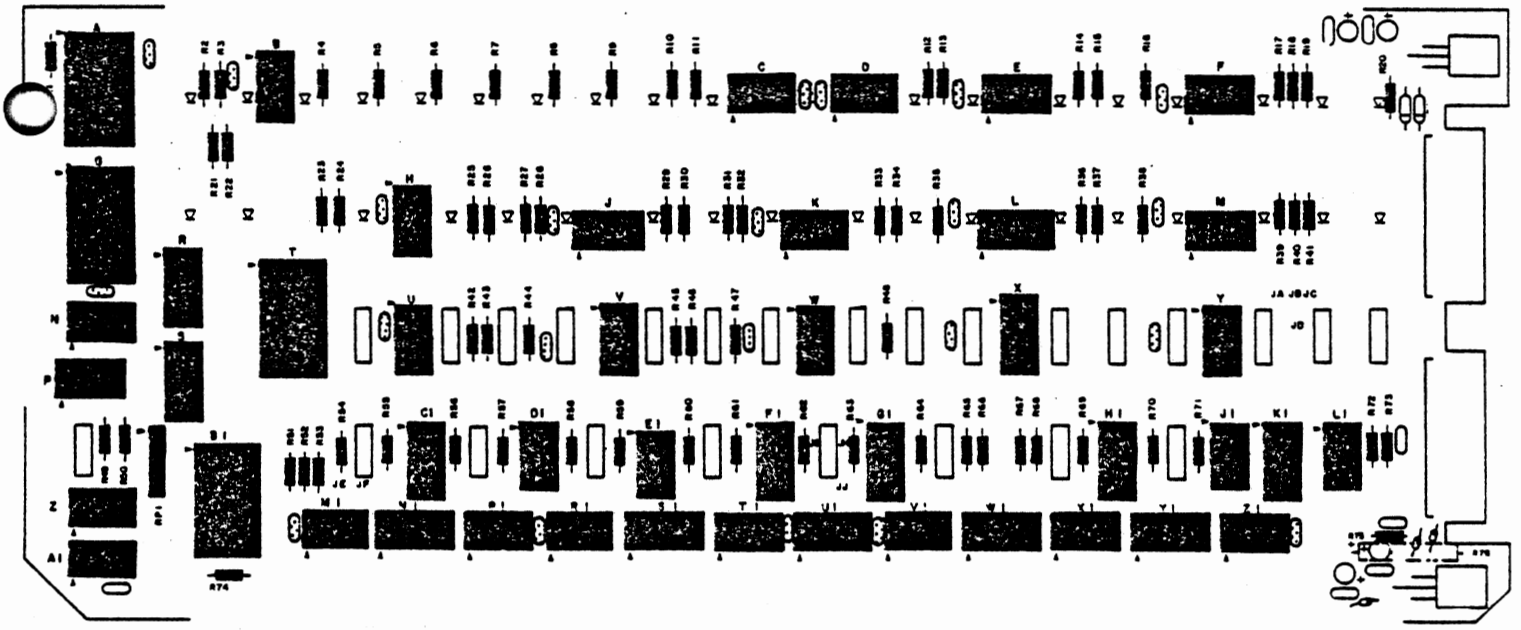
5-25. SUPPRESSOR CAPACITOR INSTALLATION (Figure 5-16)

There are 22 suppressor capacitors (Bag 6) to be installed on the Display/Control Board. These capacitors are used for noise suppression. They are located next to the ICs on the silkscreen, but they have no individual component designations.

Note that there is not enough space between P1 and R1; R1 and U1; and U1 and V1 for the suppressor capacitors to fit on the top of the board. These three capacitors will, therefore, be installed on the back of the board.

Install all 22 suppressor capacitors according to the Ceramic Disk Capacitor Installation Instructions given on page 5-7.

Suppressor Capacitors	Value
( ) 22 suppressor capacitors	.1uf, 12V

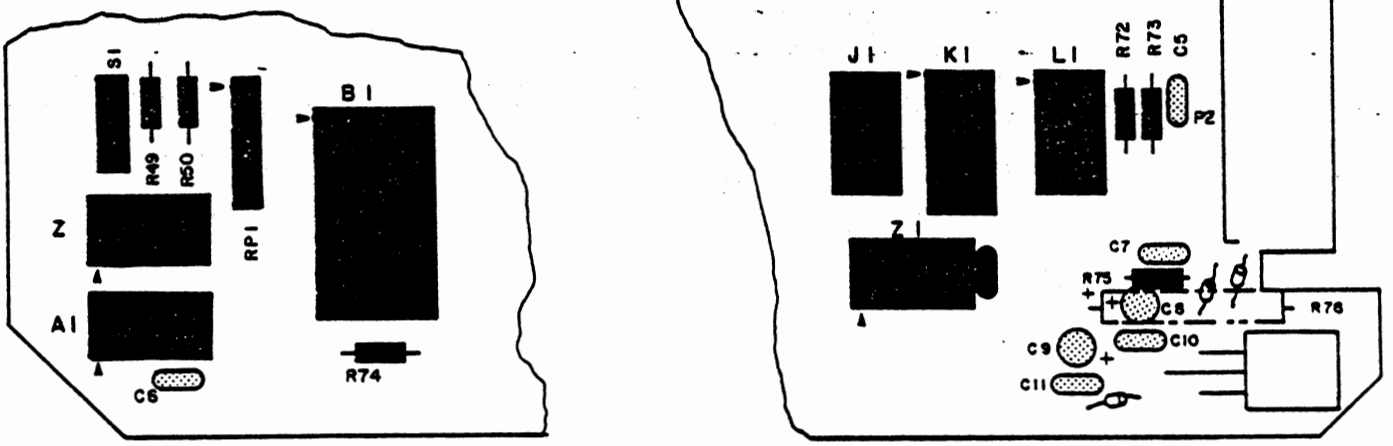


5-16. Display/Control Suppressor Capacitor Installation

5-26. CAPACITOR INSTALLATION (Figure 5-17)

There are two types of capacitors to be installed on the Display/Control Board. C2, C4, C8, and C9 (Bag 5) are dipped tantalum capacitors. They are marked with a plus sign on the positive side. Be sure to orient this plus sign with the plus sign on the silkscreen before installing each dipped tantalum capacitor. C1, C3, C5, C6, C7, C10, and C11 (Bag 5) are ceramic disk capacitors. They need no polarity orientation. Install the dipped tantalum capacitors and the ceramic disk capacitors according to the Epoxy Dipped Tantalum and Ceramic Disk Capacitor Installation Instructions given on page 5-7.

Capacitor Values	
( ) C2, C4	22uf, 35V, dipped tantalum
( ) C8, C9	47uf, 16V, dipped tantalum
( ) C1, C10, C11	.1uf, 12V or .1uf, 16V
( ) C3	.1uf, 50V (SK .1m)
( ) C5, C6, C7	.001uf



5-17. Display/Control Capacitor Installation

5-27. DIODE INSTALLATION (Figure 5-18)

Install the 2 diodes, D1 and D2 (Bag 2), on the Display/Control Board according to the Diode Installation Instructions given on page 5-8.

Diode	Part Number
( ) D1, D2	IN914

5-28. FERRITE BEAD INSTALLATION (Figure 5-18)

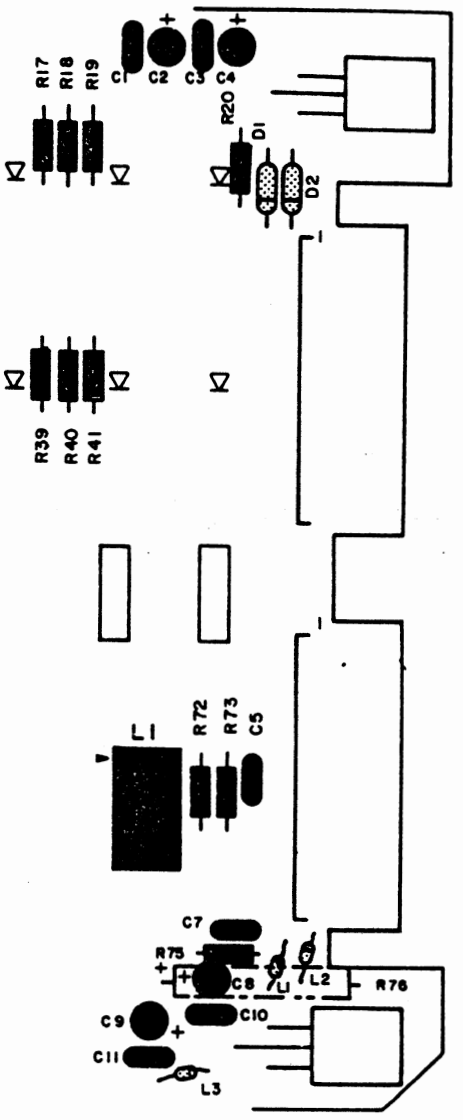
Install the three ferrite beads, L1 through L3 (Bag 2), on the Display/Control Board according to the following instructions.

1. Using the resistor leads saved from Paragraph 5-22, cut three 1-inch lead lengths.

2. Insert the lead through the bead and bend the ends of the lead to conform to the designated holes on the Display/Control Board.

3. Insert the lead into the proper holes from the silk-screened side of the board, and solder to the foil (bottom) side of the board. Be sure not to leave any solder bridges.

4. Clip off any excess lead lengths.



5-18. Display/Control Diode and Ferrite Bead Installation

5-29. VOLTAGE REGULATOR INSTALLATION (Figure 5-19)

Install the two voltage regulators, VR1 and VR2 (Bag 1), on the Display/Control Board according to the following instructions.

1. Set the regulator in place on the silk-screened side of the board, aligning the leads with their designated holes.

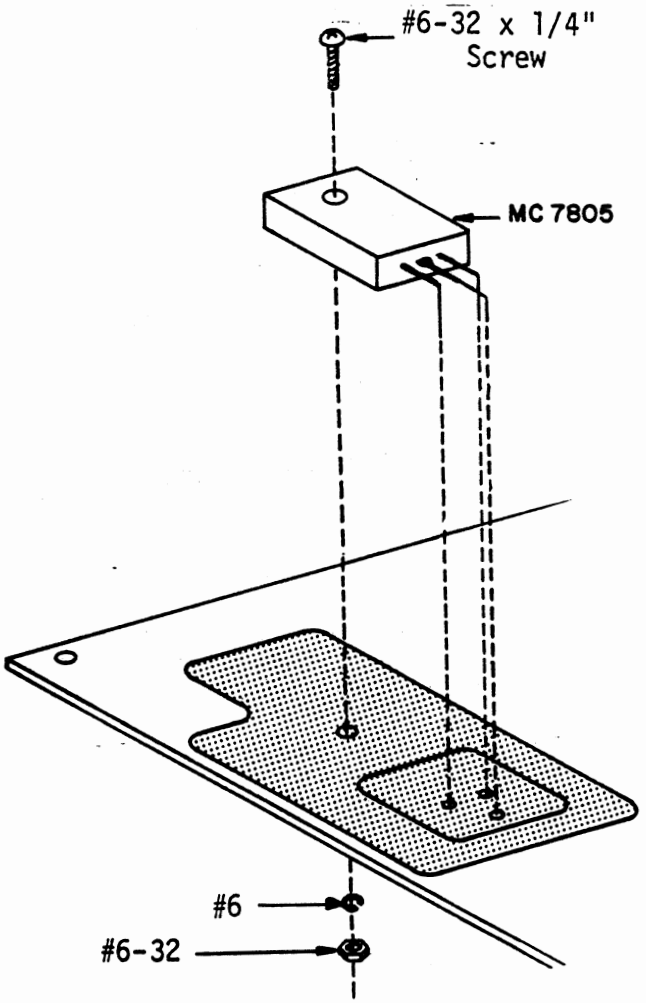
2. Use needle-nose pliers to bend each of the three leads at a right angle to conform to its proper hole on the board.

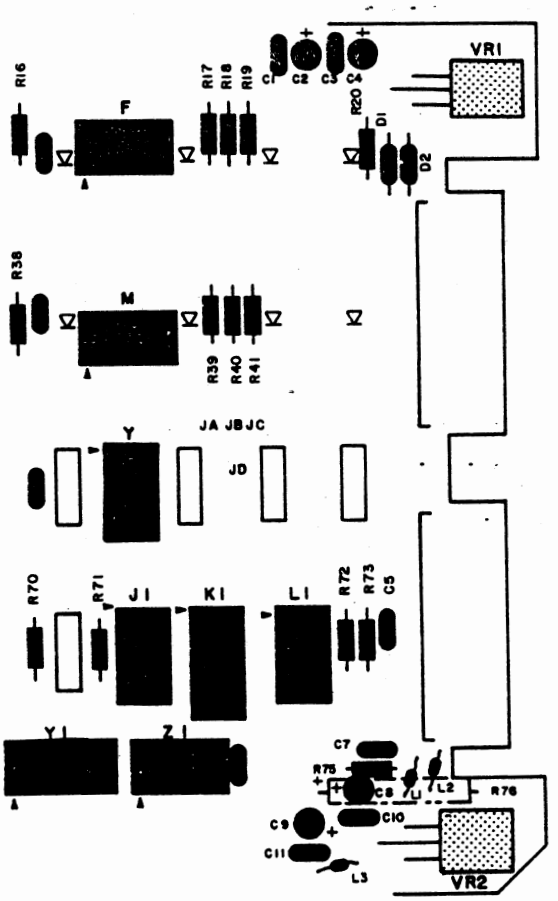
3. Referring to Figure 5-19, set the regulator in place on the silk-screened side of the board. Secure in place with a #6-32 x 1/4" screw, a #6 lockwasher, and a #6-32 nut.

4. Solder the three leads to the foil (bottom) side of the board. Be sure not to leave any solder bridges.

5. Clip off any excess lead lengths.

Voltage Regulator	Part Number
( ) VR1	79M08
( ) VR2	7805





5-19. Display/Control Voltage Regulator Installation

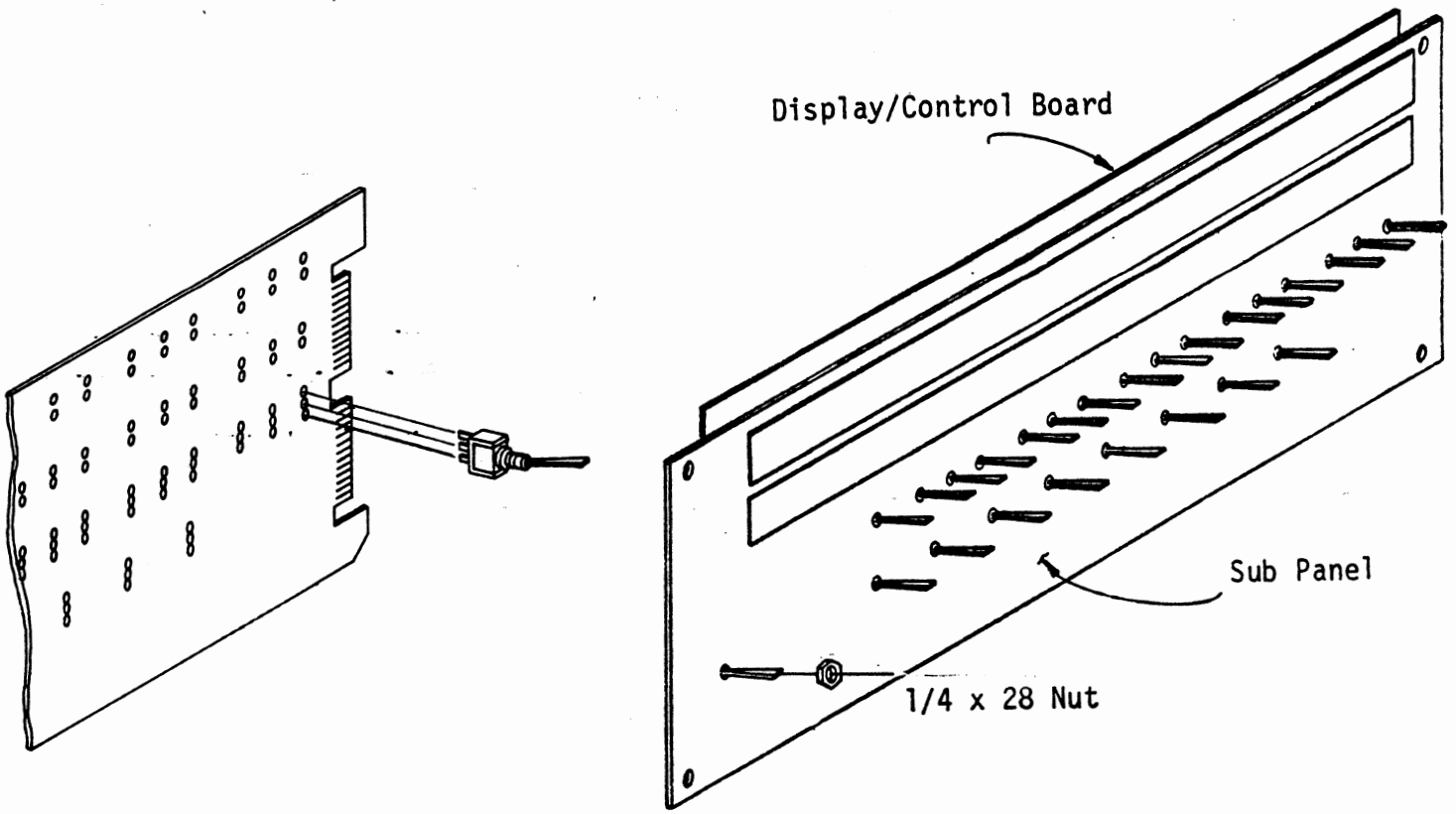
5-30. SWITCH INSTALLATION (Figure 5-20)

There are 25 switches (Bags 7 and 8) to be installed on the Display/ Control Board. S2 through S9 are momentary contact switches (i.e. they return to center position automatically when released). SA0 through SA15 and S1 are latching type switches (i.e. they remain in either the up or down position). To insure that all 25 switches are perfectly aligned, the Sub Panel will be temporarily installed at this time. Install the switches according to the following instructions.

> NOTE
>
> Set aside 25 of the nuts provided with the switches. The rest of the hardware associated with the switches will not be used.

1. With the notched side facing the bottom edge of the board, insert all 25 switches into the silk-screened side of the Display/ Control Board as shown in Figure 5-20A. Do not solder the switches at this time.

2. Place the Sub Panel over the Display/Control Board so that the switches come up through the proper switch holes on the Sub Panel. Secure the Sub Panel in place by placing one 1/4 x 28 nut over each switch (Figure 5-20A).



5-20(A). Display/Control Switch Installation

3. Solder all 3 pins of each switch to the foil (bottom) side of the Display/Control Board. Make sure the Display/Control Board is pressed tightly against each switch as it is soldered. If there is any "play" between the switches and the Display/Control Board, the alignment on the final display will not be straight.

4. After all of the switches have been installed, remove the nuts from the switches and set aside for use in Paragraph 5-31.

5. Remove the Sub Panel from the Display/Control Board.

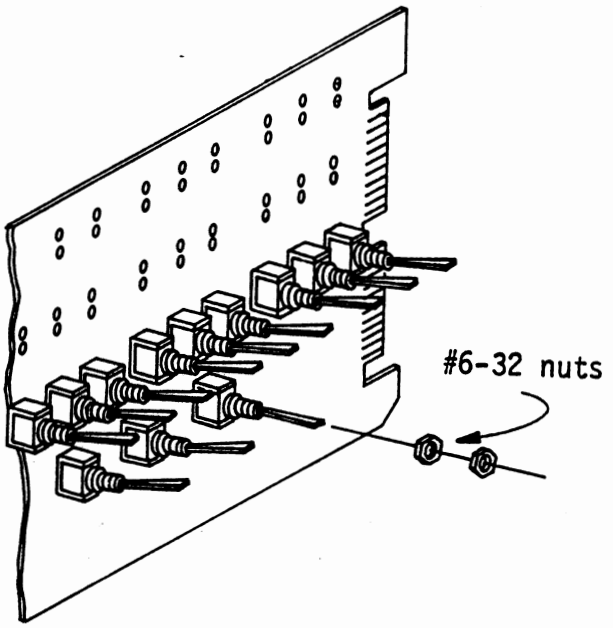
Switch	Type
( ) SA0 through SA15 and S1	latching type
( ) S2 through S9	momentary contact type

5-20(B). Display/Control Switch Installation

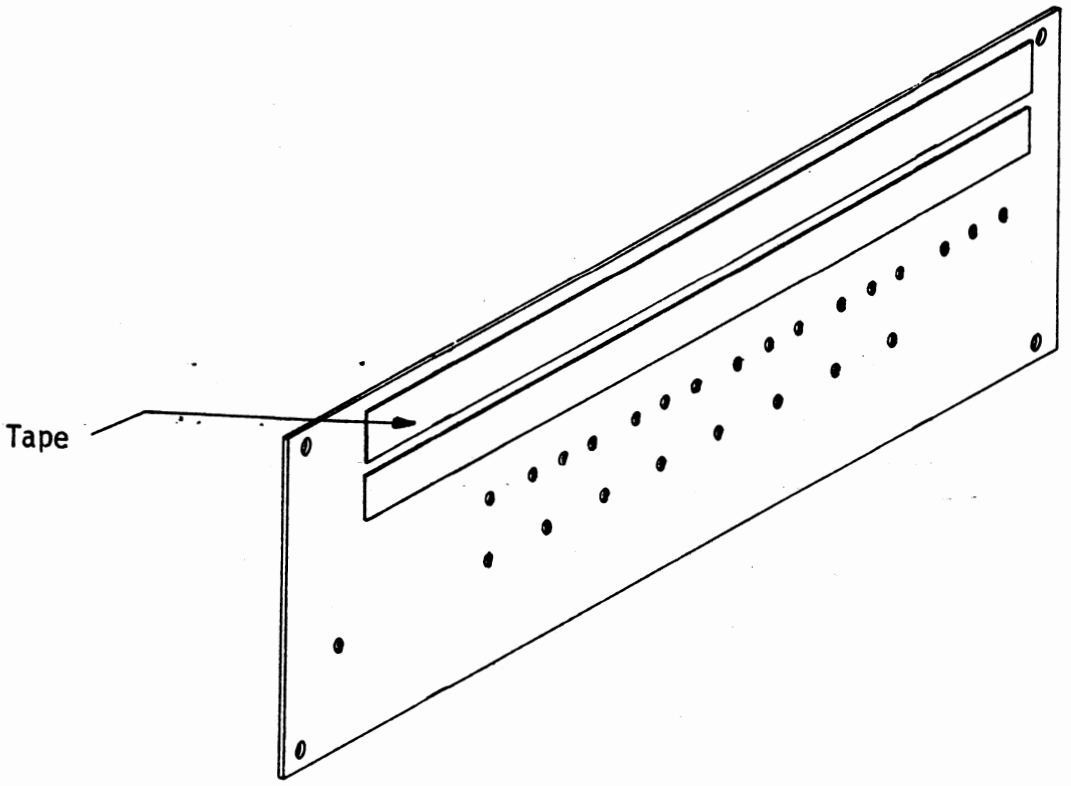
5-31. LED INSTALLATION AND SUB PANEL INSTALLATION (Figures 5-21 through 5-25)

There are 36 LEDs, RL-21 (Bag 9), to be installed on the Display/Control Board. The Sub Panel will also be installed at this time. Install the LEDs and the Sub Panel according to the following instructions.

1. Place two of the nuts saved from Paragraph 5-30 over each of the following switches: SA0, S9, S1, SA15, S5, as shown in Figure 5-21. Thread the nuts down as far as they will go. Place masking tape over the LED holes on the Sub Panel as shown in Figure 5-22.



5-21. Display/Control Switch Nut Placement

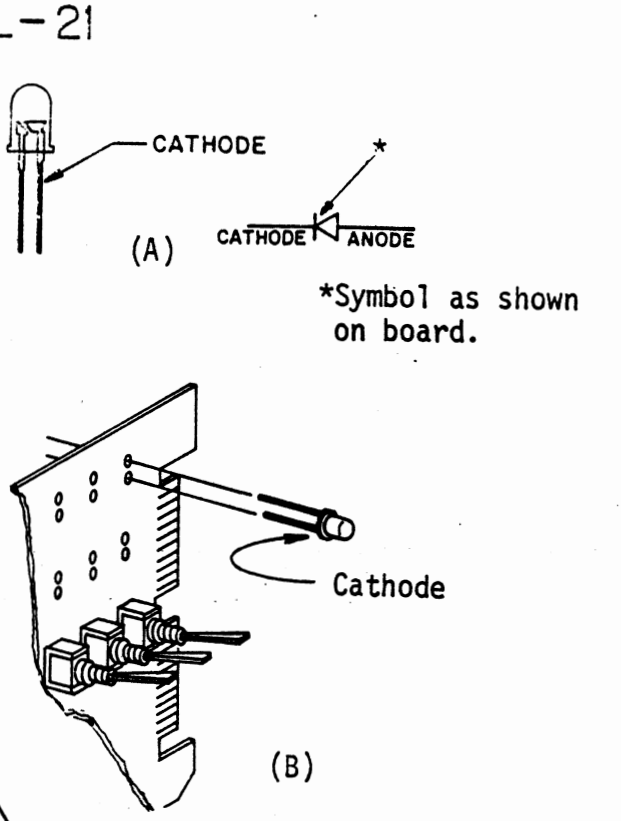


5-22. Covering LED Holes on Sub Panel

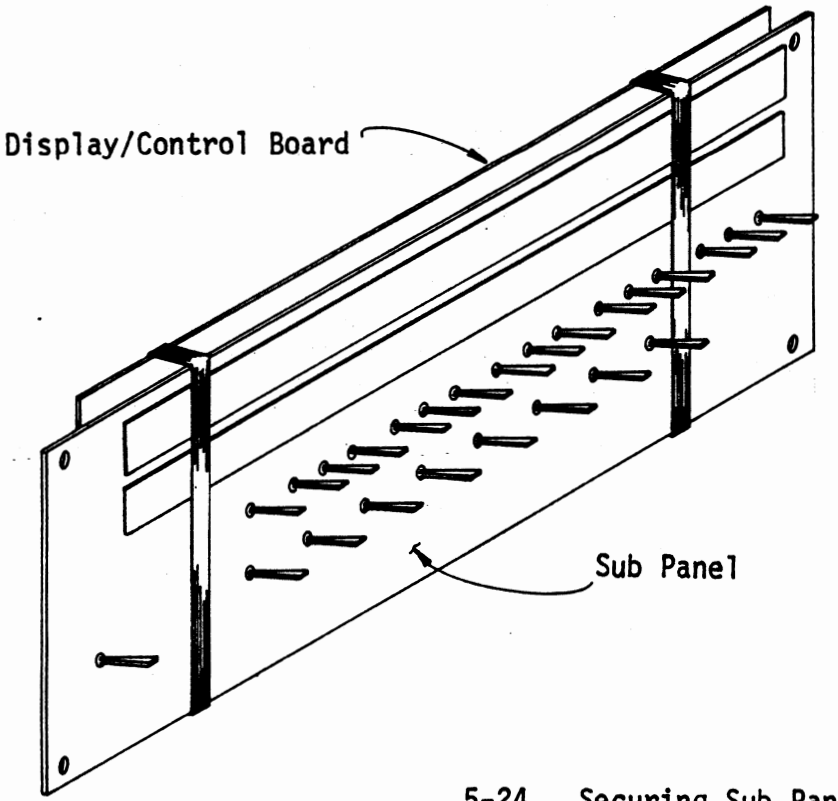
2. With the cathode lead correctly oriented (Figure 5-23A) insert all 36 LEDs into their respective holes from the silk-screened side of the board, as shown in Figure 5-23B.

NOTE
Do not solder the LED leads at this time.

3. **Place the Sub Panel over the Display/Control Panel and tape together as shown in Figure 5-24.**

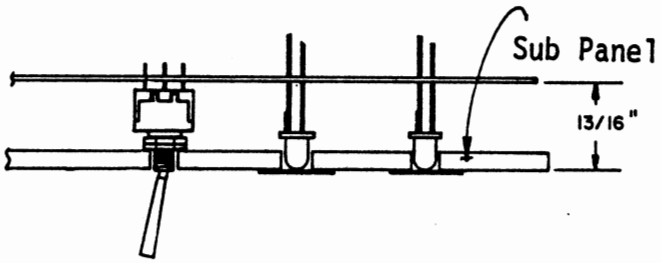


5-23. Display/Control LED Orientation and Installation



5-24. Securing Sub Panel Over Display/Control Board

4. Turn the Sub Panel to the bottom and adjust the LEDs until the top of each LED touches the tape as shown in Figure 5-25.



5-25. Display/Control LED Adjustment

5. Solder the LED leads to the foil (bottom) side of the Display/ Control Board. During this procedure it is advisable to prop the boards from underneath so that the switches are not resting on the work surface.

WARNING!

LEDs are heat-sensitive. Use a minimum amount of heat for a minimum length of time when soldering them.

Be sure not to leave any solder bridges, and clip off any excess lead lengths.

6. Remove all pieces of masking tape.

7. Remove the Sub Panel from the Display/Control Board.

8. Remove the nuts from SA0, S9, S1, SA15, and S5.

9. Place the Sub Panel over the Display/Control Board and secure by placing one nut on each switch on the Display/ Control Board.

5-32. CPU BOARD ASSEMBLY

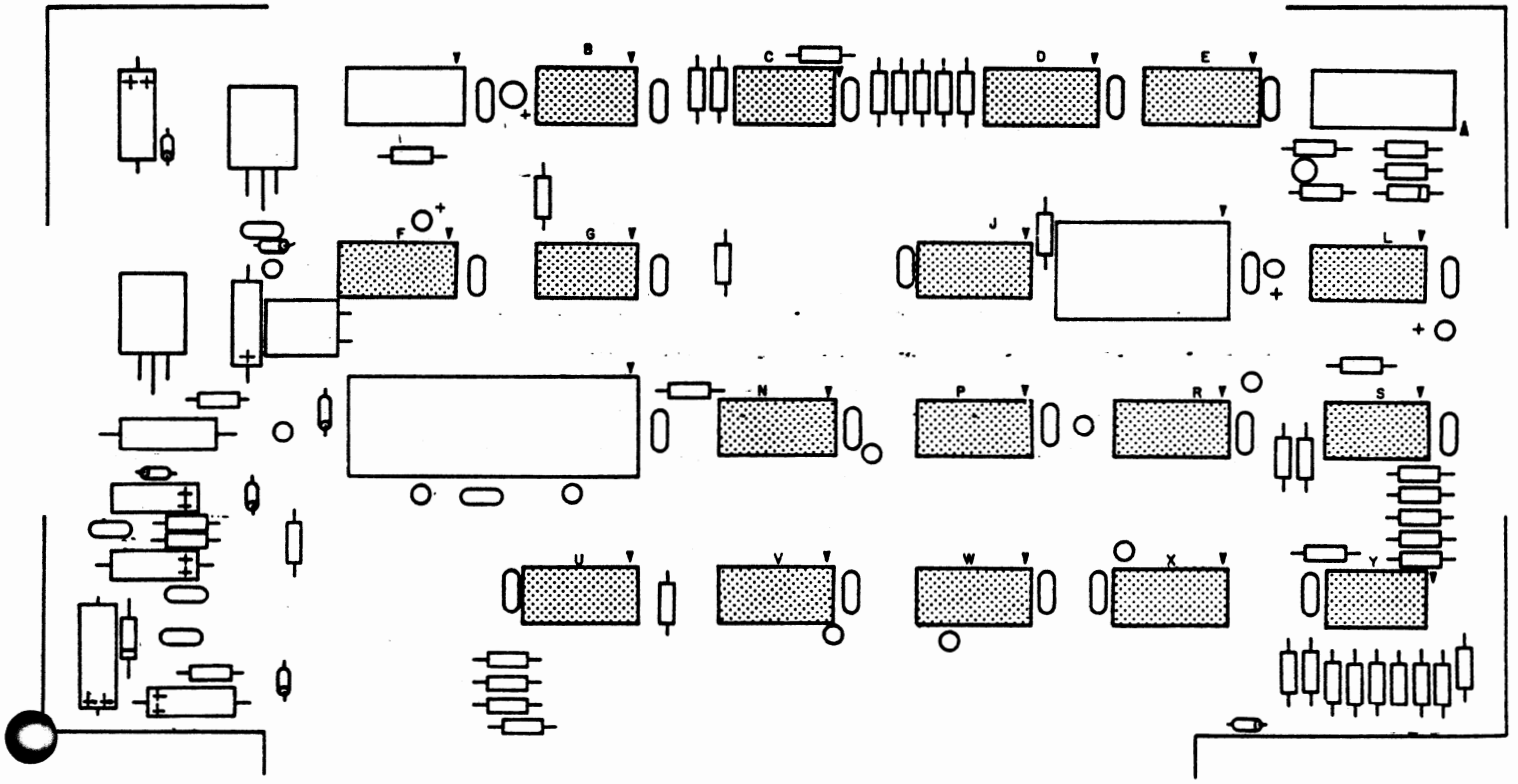
5-33. IC INSTALLATION (Figure 5-26)

Install the following 17 integrated circuits (Bag 2) on the CPU Board according to the Integrated Circuit Installation Instructions, Section A, given on page 5-10.

> NOTE
>
> Do not install ICs A, K, and M at this time. Installation instructions for these ICs are given in Paragraph 5-43.

The following chart lists each integrated circuit, its part number, and acceptable substitutions.

IC Part Numbers	
(X) D,E	8216
(X) F	8224
( ) N,P,R,U, V,W,X	74367
( ) S,Y	74LS14 or 74LS04
( ) C	74LS13 or 74LS20
( ) B,G	74LS04
( ) L,J	8T98 or 8098 or 74368



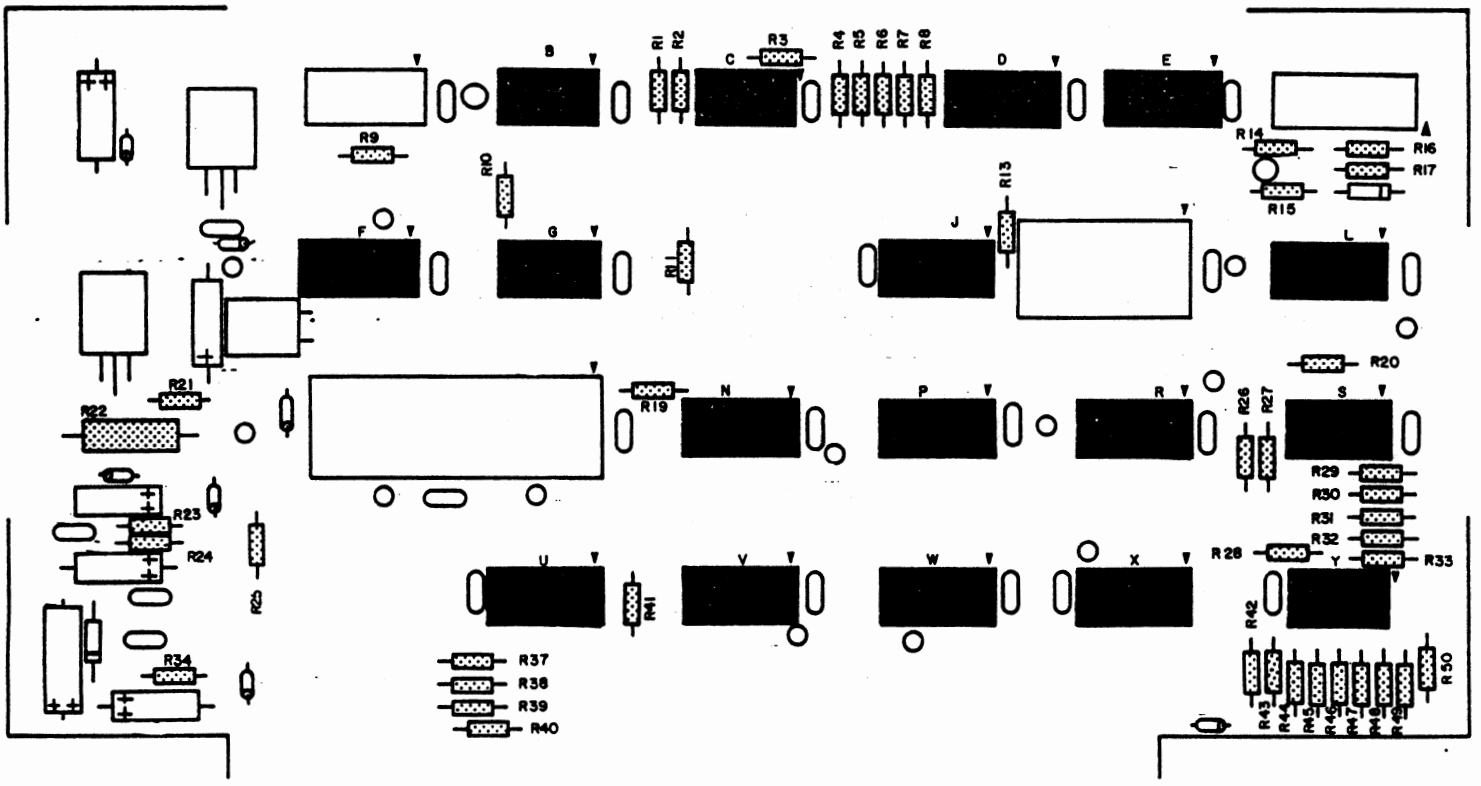
5-26. CPU IC Installation

5-34. RESISTOR INSTALLATION (Figure 5-27)

Install the following 46 resistors (Bags 3 and 4) on the CPU Board according to the Resistor Installation Instructions given on page 5-6.

> NOTE
>
> Save any excess resistor leads for ferrite bead installation in Paragraph 5-38.

Resistor Values	
(X) R3-R7, R11, R13, R14, R19, R20, R24, R25, R28-R33, R39-R43, R50	2.2K ohm (red, red, red) 1/2W or 1/4W
(X) R1, R2, R8, R26, R27, R37, R38, R44-R49	3.3K ohm (orange, orange, red) 1/2W or 1/4W
(X) R9	15K ohm (brown, green, orange) 1/2W or 1/4W
(X) R16	1K ohm (brown, black, red) 1/2W or 1/4W
(X) R34	620 ohm (blue, red, brown) 1/2W
(X) R10	330 ohm (orange, orange, brown) 1/2W or 1/4W
(X) R21, R23	470 ohm (yellow, violet, brown) 1/2W or 1/4W
(X) R17	10K ohm (brown, black, orange) 1/2W or 1/4W
(X) R22	10 ohm (brown, black, black) 2W
(X) R15	100 ohm (brown, black, brown) 1/2W or 1/4W

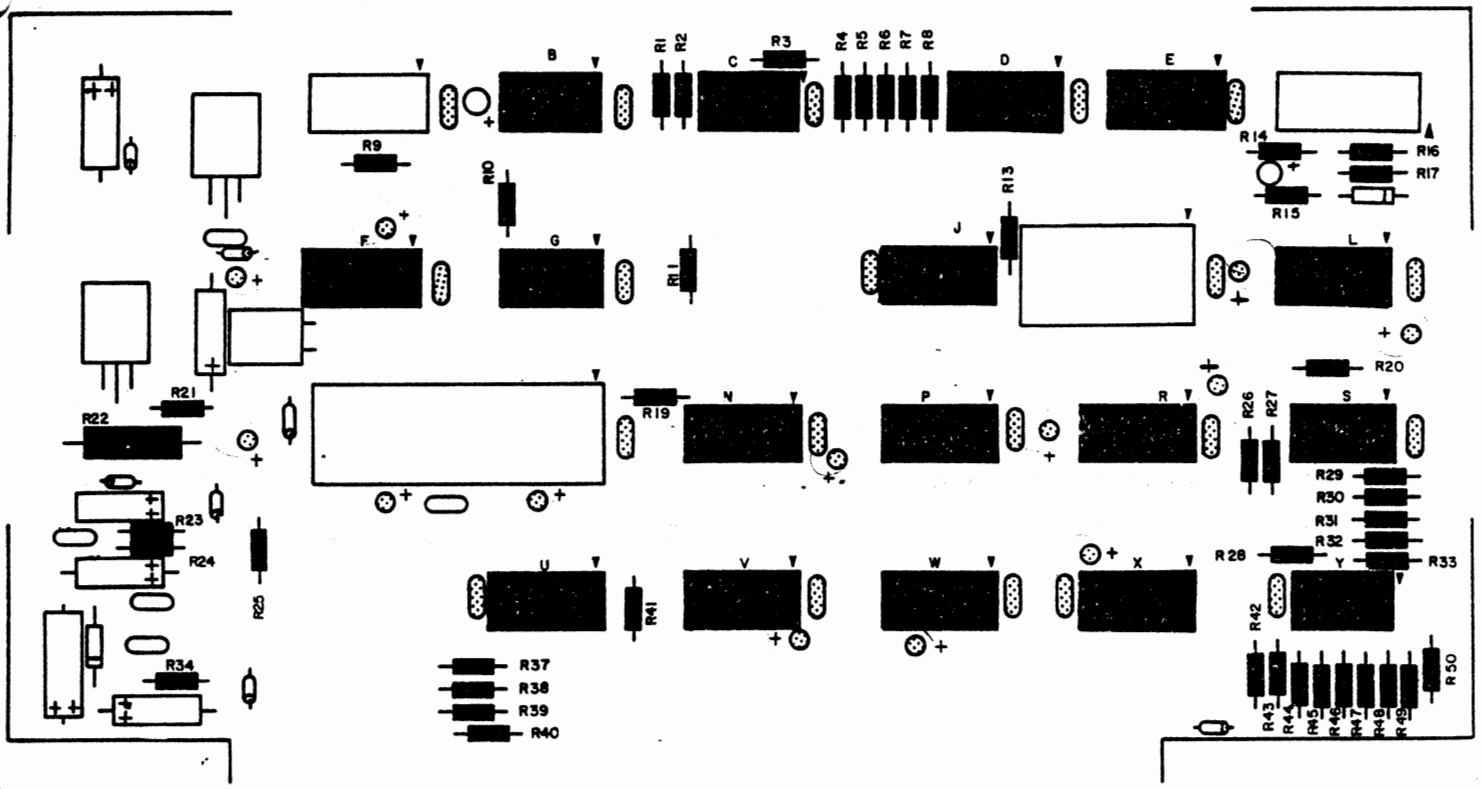


5-27. CPU Resistor Installation

5-35. SUPPRESSOR CAPACITOR INSTALLATION (Figure 5-28)

There are two types of suppressor capacitors to be installed on the CPU Board. The first type, the epoxy dipped tantalum capacitors (Bag 6), are blue on the positive side and are spherical in shape. Be sure to orient the blue side to the "+" sign on the silkscreen before installing each capacitor. The remaining suppressor capacitors are ceramic disk capacitors (Bag 5). They need no polarity orientation. Install both types of capacitors according to the Epoxy Dipped Tantalum and Ceramic Disk Capacitor Installation Instructions given on page 5-7.

Suppressor Capacitor Values	
(K) 13 dipped tantalum	luf, 35V
(Y) 20 ceramic disk	.luf, 12V



5-28. CPU Suppressor Capacitor Installation

5-36. CAPACITOR INSTALLATION (Figure 5-29)

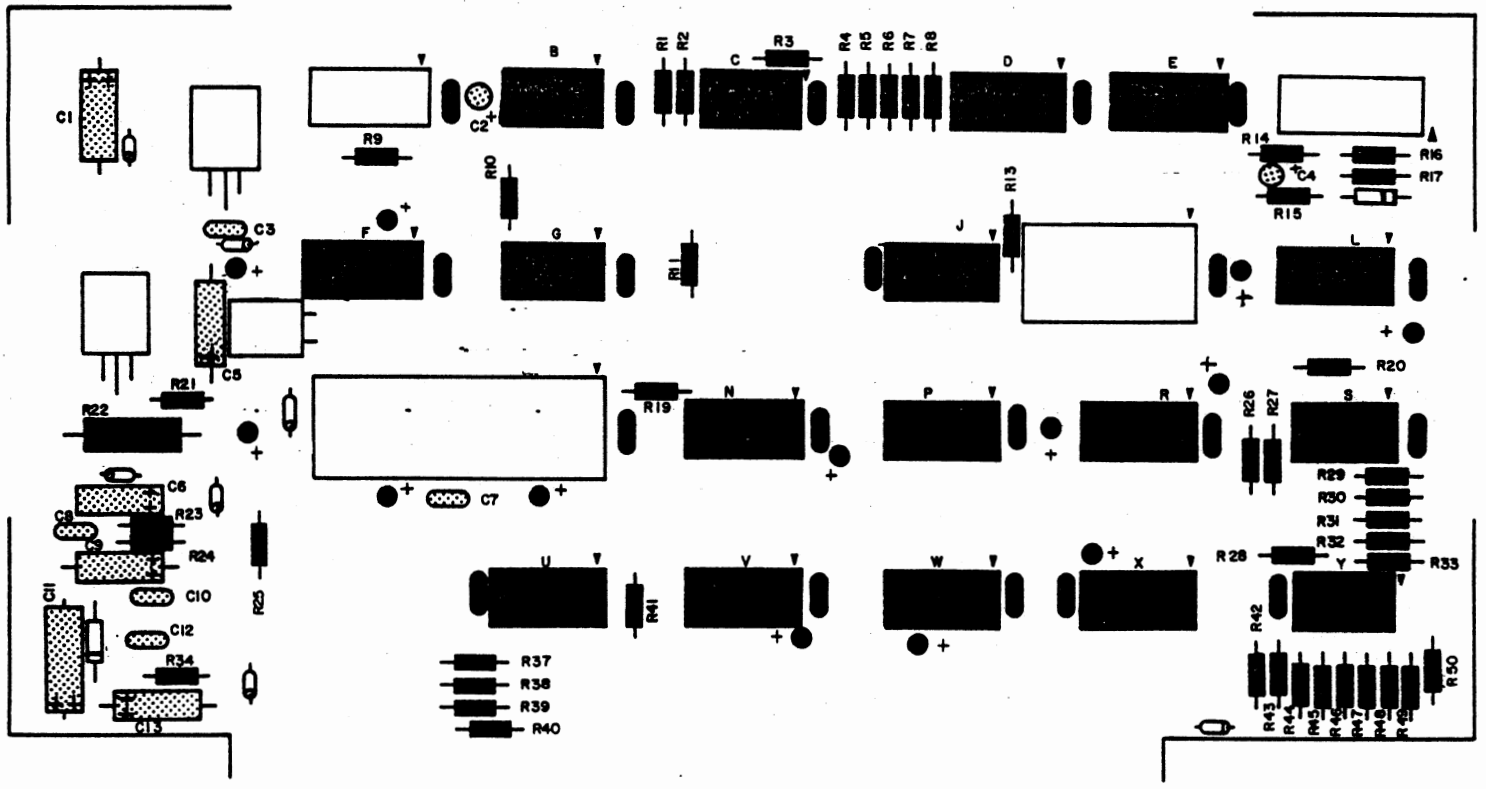
There are 2 dipped tantalum capacitors, 6 electrolytic capacitors, 2 ceramic disk capacitors, and 3 dipped ceramic capacitors (Bag 6) to be installed on the CPU Board. Install each capacitor according to the instructions given on page 5-7.

NOTE

When installing the dipped tantalum and the electrolytic capacitors, be sure the positive lead is installed in the "+" hole on the silkscreen.

Capacitor Values

(X) C1, C5, C6, C11	33uf, 16V, electrolytic
(X) C2	22uf, 16V, dipped tantalum
(X) C3, C7, C10	.1uf, 50V, dipped ceramic
(X) C4	10uf, 16V, dipped tantalum
(X) C8, C12	.1uf, 12V - 16V, ceramic disk
(X) C9, C13	10uf, 25V, electrolytic

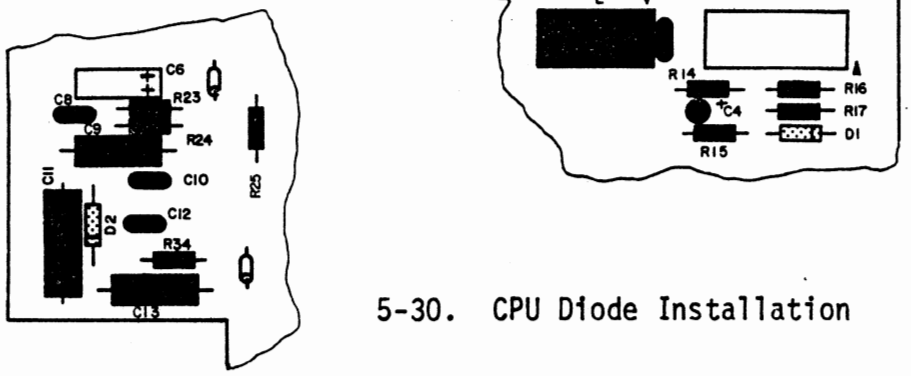


5-29. CPU Capacitor Installation

5-37. DIODE INSTALLATION (Figure 5-30)

Install the two diodes, D1 and D2 (Bag 4), on the CPU Board according to the Diode Installation Instructions given on page 5-8.

Diode Part Numbers	
(✓) D1	1N4730
(✓) D2	1N4733



5-30. CPU Diode Installation

5-38. FERRITE BEAD INSTALLATION (Figure 5-31)

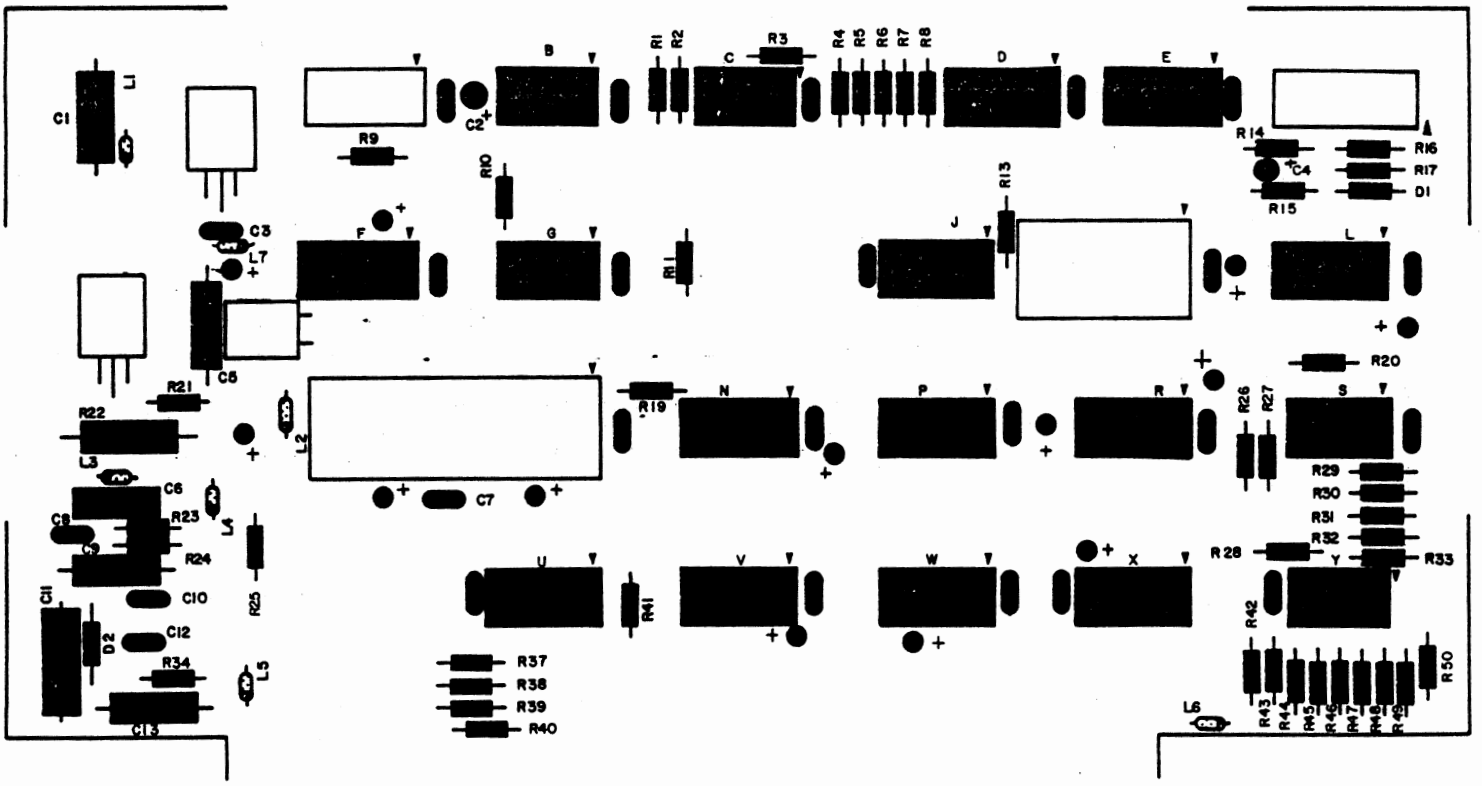
Install the 7 ferrite beads, L1 through L7 (Bag 7), on the CPU Board according to the following instructions.

1. Using the resistor leads saved from Paragraph 5-34, cut five 1-inch lead lengths.

2. Insert the lead through the bead, and bend the ends so they conform to the designated holes on the CPU Board.

3. Insert the leads into the board, and solder to the foil (bottom) side of the board. Be careful not to leave any solder bridges.

4. Clip off any excess lead lengths.



5-31. CPU Ferrite Bead Installation

5-39. VOLTAGE REGULATOR INSTALLATION (Figure 5-32)

Install the two voltage regulators, VR1 and VR2 (Bag 2), and heat sinks on the CPU Board according to the following instructions.

1. Set the regulator in place on the silk-screened side of the board, aligning the leads with their designated holes.

2. Use needle-nose pliers to bend each of the three leads at a right angle to conform to its proper hole on the board.

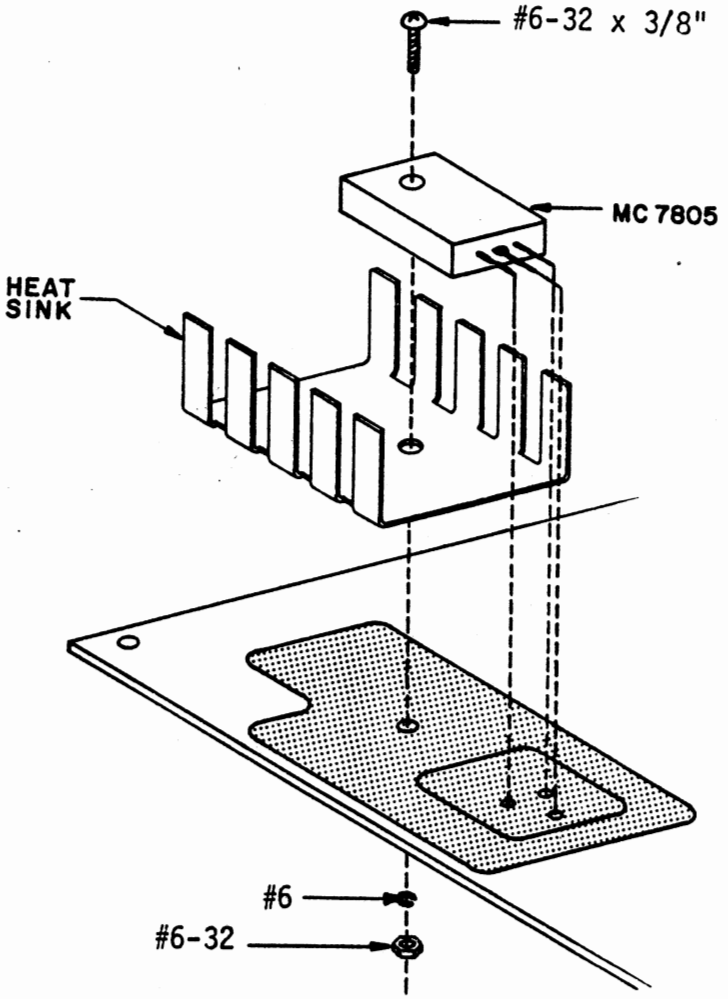
> NOTE
>
> Use heat sink grease when installing this component. Apply the grease to all metal surfaces which come in contact with each other.

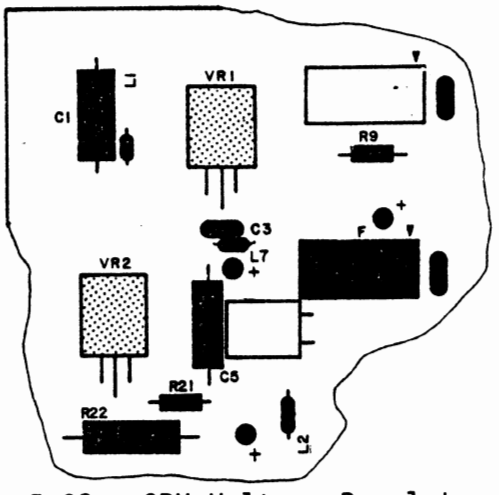
3. Referring to Figure 5-32, set the regulator and heat sink in place on the silk-screened side of the board. Secure them in place with a #6-32 x 3/8" screw, a #6-32 nut, and a #6 lockwasher.

4. Solder the three leads to the foil (bottom) side of the board. Be sure not to leave any solder bridges.

5. Clip off any excess lead lengths.

Voltage Regulator Part Numbers		
(X)	VR1	7805
(X)	VR2	7812





5-32. CPU Voltage Regulator Installation

5-40. TRANSISTOR INSTALLATION (Figure 5-33)

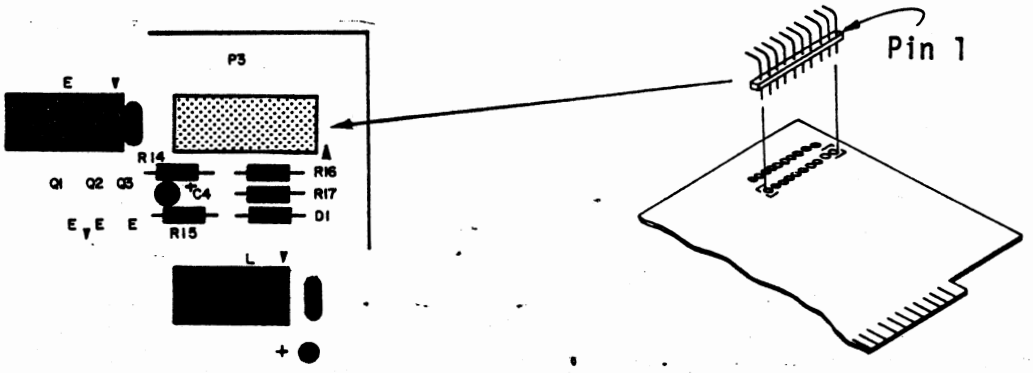
Install the three transistors, Q1 through Q3 (Bag 4), on the CPU Board according to the Transistor Installation Instructions given on page 5-8.

Transistor Part Numbers	
(X) Q1, Q2, Q3	2N4410 or CS4410

5-41. MALE CONNECTOR INSTALLATION (Figure 5-33)

Install one 10-pin Male Connector, P1 (Bag 7), on the CPU Board according to the following instructions.

1. Orient the connector as shown in Figure 5-33, with the bent pins pointing toward the top of the board.
2. Insert the short pins into the 10 designated holes on the silk-screened side of the board.
3. Solder each pin to the foil (bottom) side of the board. Be sure not to leave any solder bridges and clip off any excess lead lengths.
4. The arrow on the silkscreen points to Pin #1. After installing the male connector, clip off pin #2 of the connector. This is done for keying purposes. Further keying instructions are given on page 5-75.



5-33. CPU Transistor and Male Connector Installation

INSERT PAGE

ALTAIR 8800b

CPU Board Assembly Procedure

Erratum, Page 5-44, MALE CONNECTOR INSTALLATION

Kit builder may find that the 10-pin Male Connector may already be installed on the CPU Board. If it has been installed, ignore the installation instructions.

MITS, Inc.
August, 1976

5-42. CRYSTAL INSTALLATION (Figure 5-34)

Install one 18.00000 MHz crystal, XTAL (Bag 7), on the CPU Board according to the following instructions.

1. Referring to Figure 5-34, set the crystal in place on the silk-screened side of the CPU board, aligning the two leads with their respective holes.

2. Using needle-nose pliers, bend each lead at a right angle to conform to its respective hole on the board. Insert the leads so that the crystal is resting flat on the board on the square labelled "XTAL".

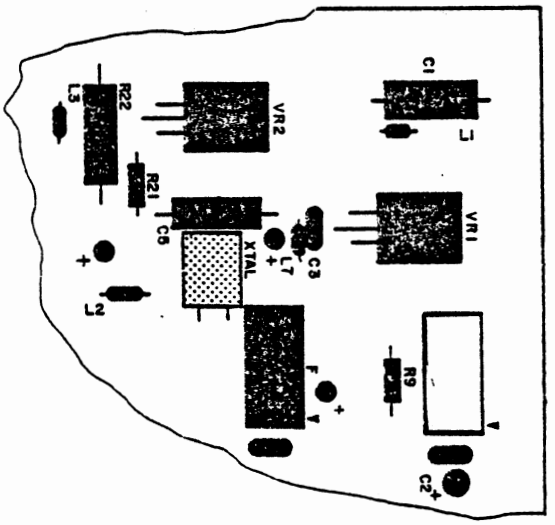
3. Solder the two leads to the foil (bottom) side of the board. Be sure not to leave any solder bridges.

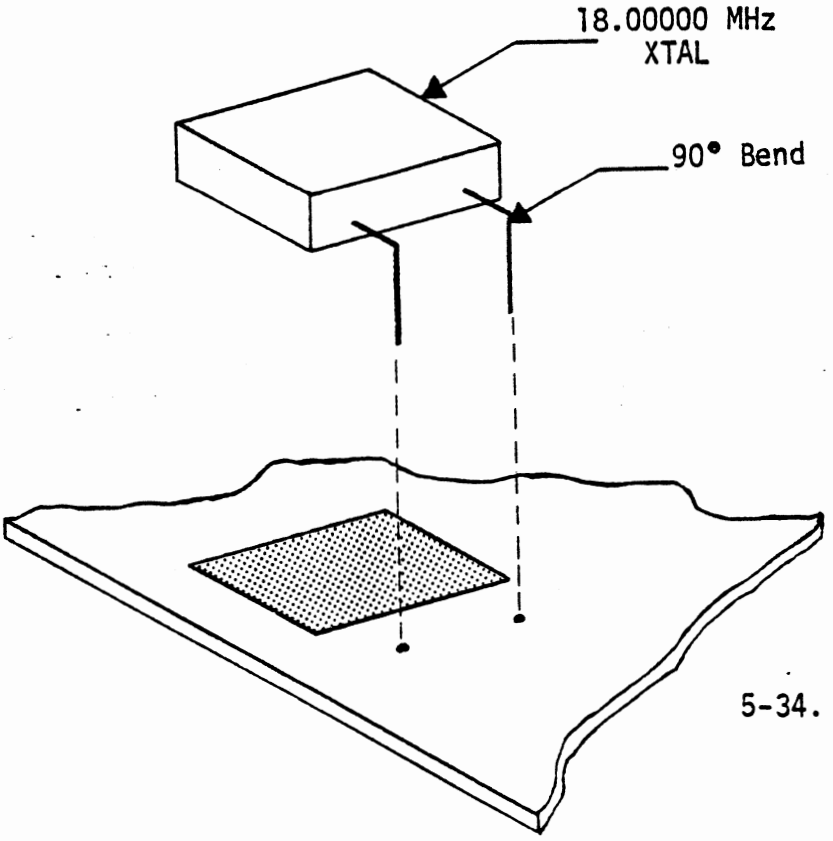
4. Clip off any excess lead lengths.

CAUTION

Make sure the crystal case does not come in contact with any of the tracks on the CPU Board.

Crystal	Part Number
(X) XTAL	18.00000MHz





5-34. CPU Crystal Installation

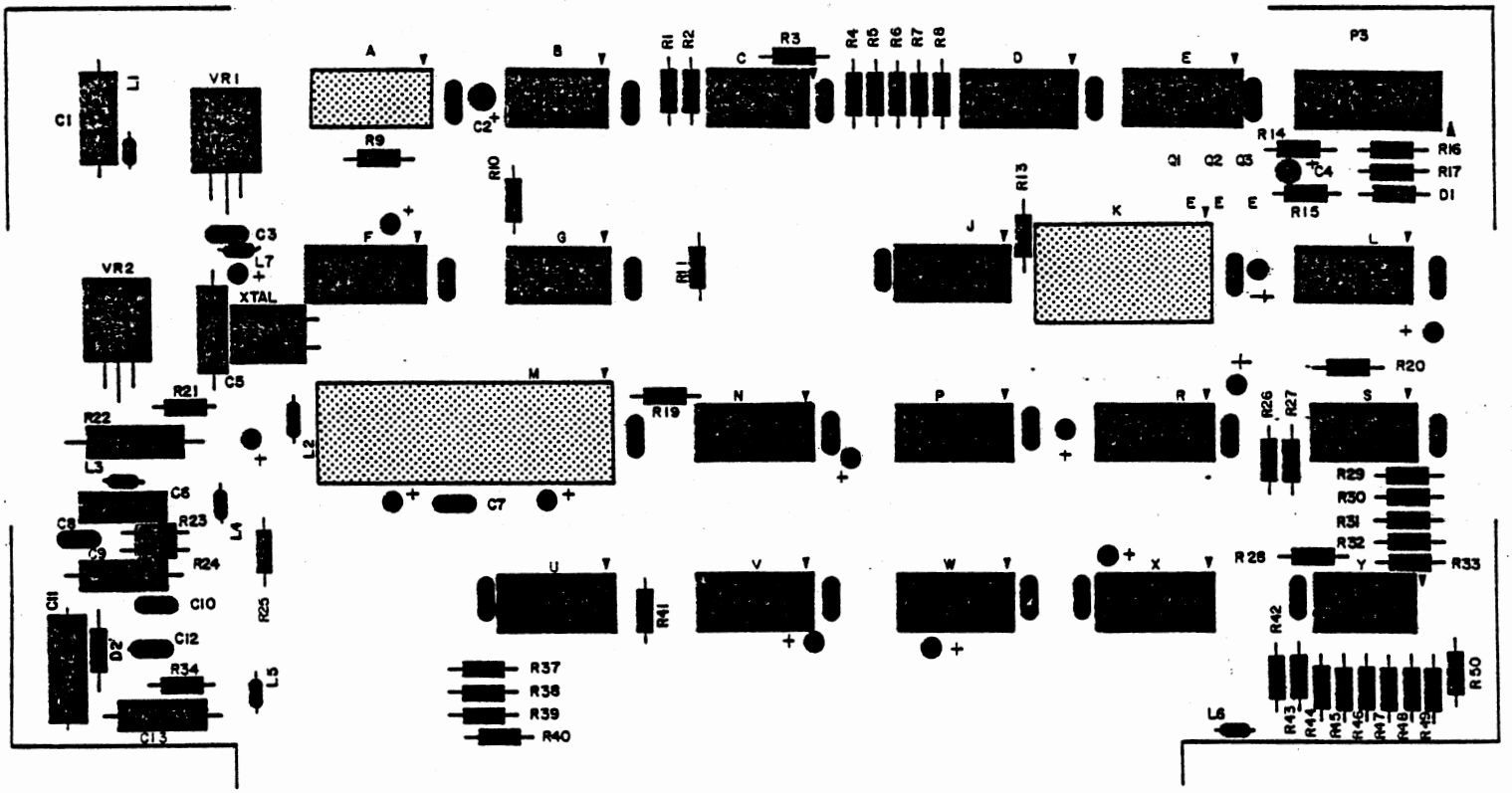
5-43. IC SOCKET AND IC INSTALLATION (Figure 5-35)

ICs A, K, and M (Bag 1) will be installed at this time. ICs K and M should be installed, with sockets, according to the IC Installation Instructions, Section B, on page 5-10. IC A should be installed (without a socket) according to the IC Installation Instructions, Section A, on page 5-10.

Silkscreen Designation	IC Part Number	Socket Size
(X) K	8212	24-pin
(X) M	8080	40-pin
(X) A	4009	------

WARNING!

ICs A and M are MOS static-sensitive ICs. See the "MOS IC Special Handling Precautions" on page 5-11 before installing these ICs.



5-35. CPU IC Socket and IC Installation

5-44. POWER SUPPLY BOARD ASSEMBLY

5-45. CAPACITOR INSTALLATION (Figure 5-36)

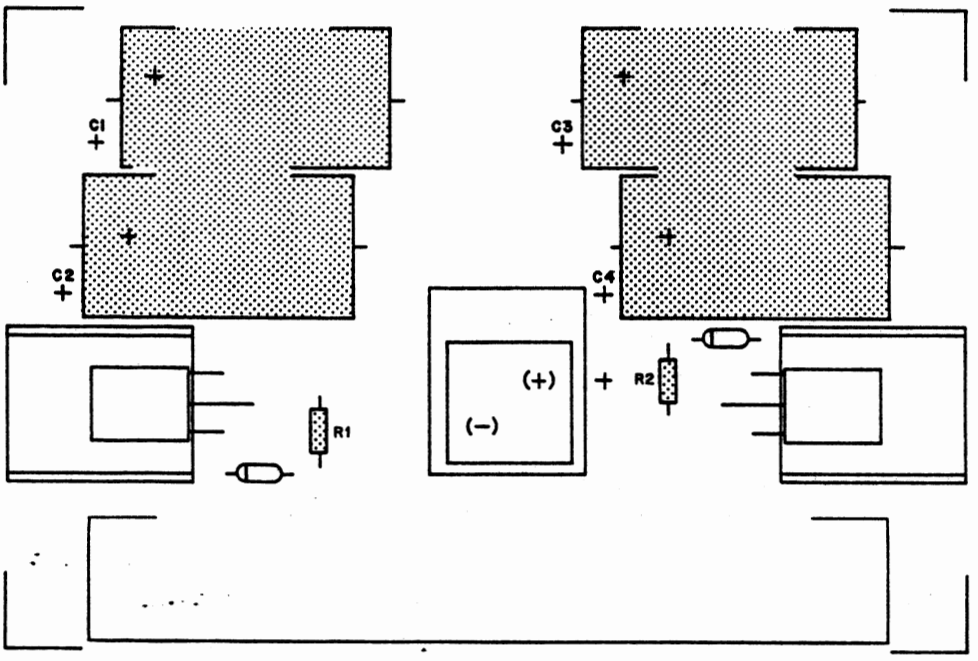
Install the 4 electrolytic capacitors, C1 through C4 (Bag 3), on the Power Supply Board according to the Capacitor Installation Instructions given on page 5-7.

Capacitor Values	
(X) C1 through C4	2200uf, 25V, electrolytic

5-46. RESISTOR INSTALLATION (Figure 5-36)

Install the 2 resistors, R1 and R2 (Bag 1), on the Power Supply Board according to the Resistor Installation Instructions given on page 5-6.

Resistor Values	
(X) R1 and R2	180 ohm (brown, gray, brown) 1/2W

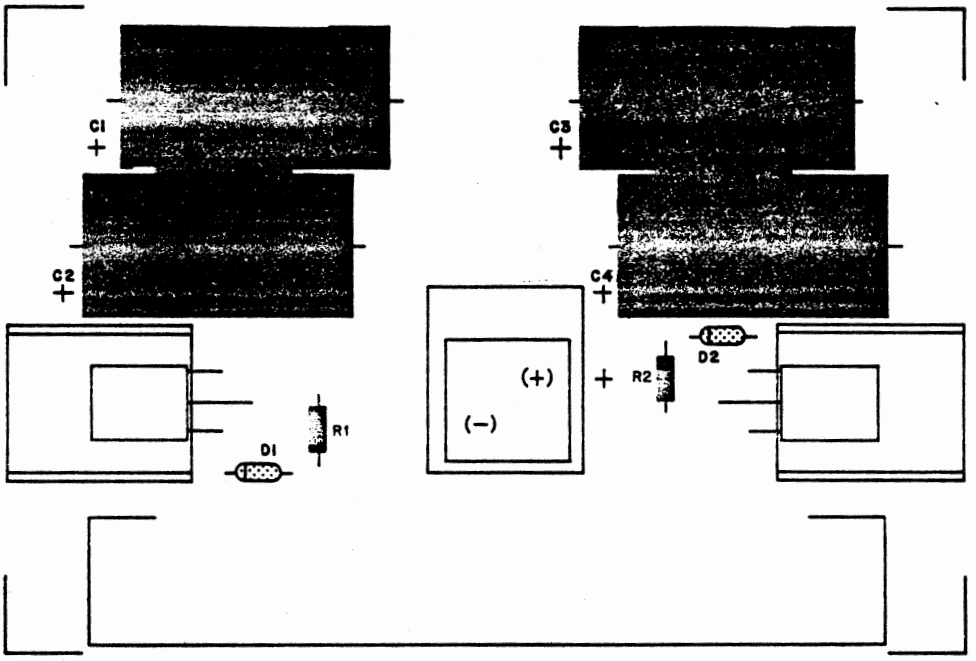


5-36. Power Supply Capacitor and Resistor Installation

5-47. DIODE INSTALLATION (Figure 5-37)

Install the 2 diodes, D1 and D2 (Bag 1), on the Power Supply Board according to the Diode Installation Instructions given on page 5-8.

Diode Part Numbers	
(✓) D1 and D2	IN4746



5-37. Power Supply Diode Installation

5-48. TRANSISTOR INSTALLATION (Figure 5-38)

Install the two transistors, Q1 and Q2 (Bag 1), mica insulators, and heat sinks on the Power Supply Board according to the following instructions.

1. Set the transistor in place on the silk-screened side of the board, aligning the leads with their designated holes.

2. Use needle-nose pliers to bend each of the three leads at a right angle to conform to its proper hole on the board.

> NOTE
>
> Use heat sink grease when installing this component. Apply the grease to all surfaces which come in contact with each other.

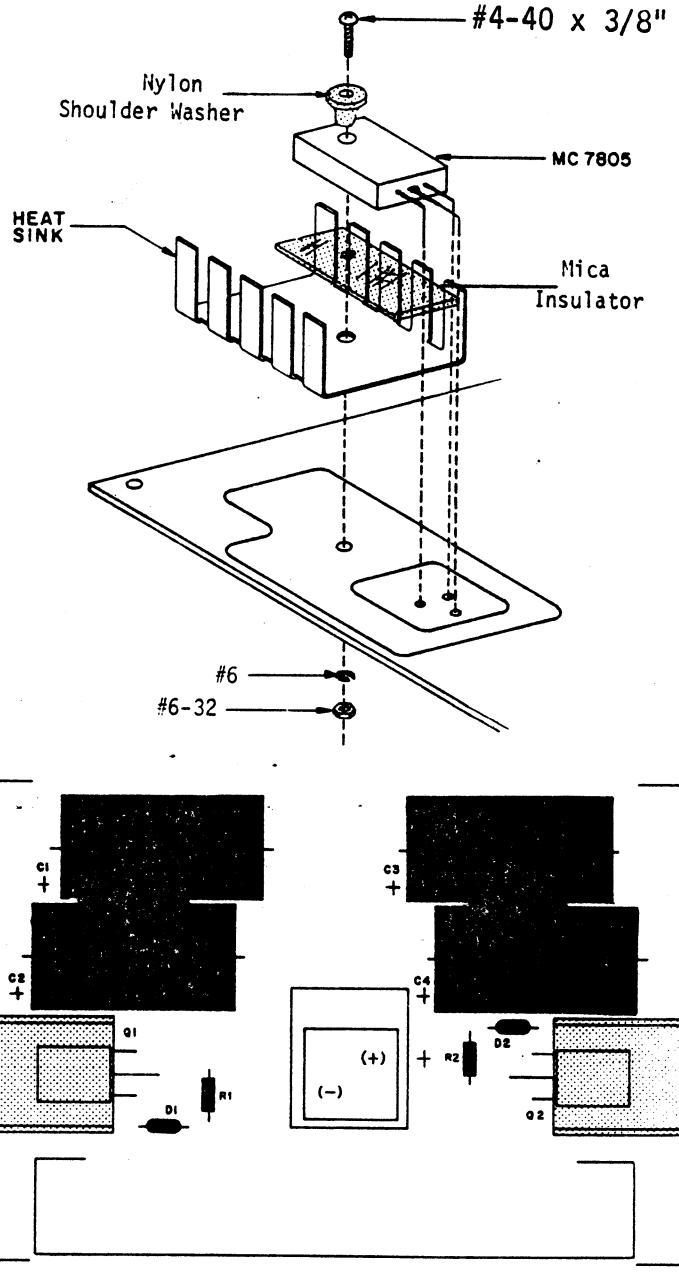
> NOTE
>
> According to supply variations, your kit may contain either two #6-32 x 3/8" nylon screws (Bag 5), or two #4-40 x 3/8" metal screws (Bag 5) to be used when installing transistors Q1 and Q2. If your kit contains metal screws, two fiber shoulder washers (Bag 5) must be used along with the screws. To install the fiber shoulder washers, refer to Figure 5-38.

3. Referring to Figure 5-38, set the transistor, mica insulator, and heat sink in place on the silk-screened side of the board. Secure them in place with a #6-32 x 3/8" screw, a #6 lockwasher, and a #6-32 nut (Bag).

4. Solder the three leads to the foil (bottom) side of the board. Be sure not to leave any solder bridges.

5. Clip off any excess lead lengths.

Transistor Part Numbers	
(✓) Q1	TIP145 or TIP146
(✓) Q2	TIP140 or TIP141



5-38. Power Supply Transistor Installation

5-49. BRIDGE RECTIFIER INSTALLATION (Figure 5-39)

Install one bridge rectifier, BR1 (Bag 1), on the Power Supply Board according to the following instructions.

> WARNING!
>
> It is essential that the bridge rectifier be oriented correctly, so that the "+" lead corresponds with the "+" hole on the Power Supply Board.

> NOTE
>
> Use heat sink grease when installing this component. Apply the grease to the bridge rectifier and the heat sink where they come in contact with each other.

1. Orient the bridge rectifier and the heat sink as shown in Figure 5-39. Note that the mounting hole in the heat sink is not centered, but is closer to one end. Make sure you orient the "+" lead of the rectifier under the wider end of the heat sink, as shown.

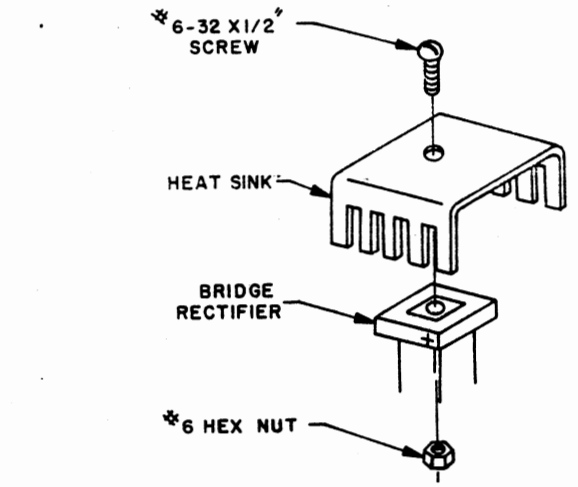
2. Attach the heat sink to the bridge rectifier, using a #6-32 x 1/2" screw and a #6 hex nut (Bag 5).

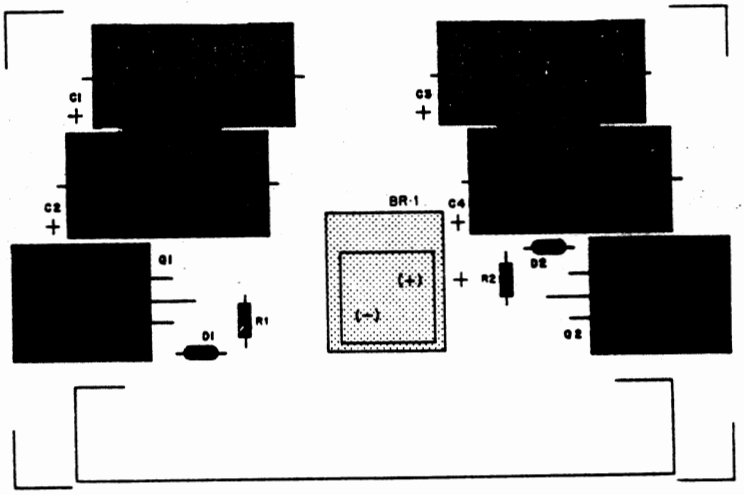
3. Orient the heat sink and rectifier assembly correctly over the board, as shown in Figure 5-39. When you have the proper alignment, the wider end of the heat sink will be pointing toward the right side of the Power Supply Board, and the "+" lead will be going into the "+" hole.

4. Insert the four leads from the bridge rectifier through the proper holes on the Power Supply Board until the legs of the heat sink rest on the board.

5. Holding the heat sink in place, turn the board over and bend the four leads slightly outward. Solder the leads to the foil (bottom) side of the board and clip off any excess lead lengths.

Bridge Rectifier	Part Number
(X) BR1	KBPC802





5-39. Power Supply Bridge Rectifier Installation

5-50. TERMINAL BLOCK INSTALLATION (Figures 5-40 through 5-42)

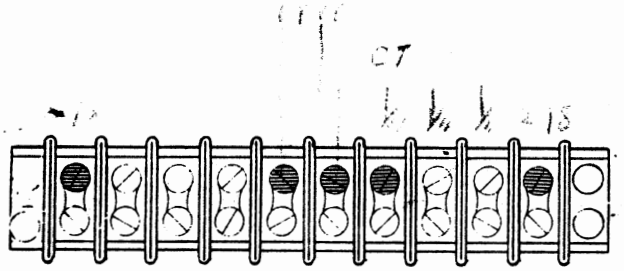
Install the terminal block, TB1 (Bag 2), on the Power Supply Board according to the following instructions.

1. Remove the five #6-32 x 1/4" screws shown in Figure 5-40 from the terminal block.

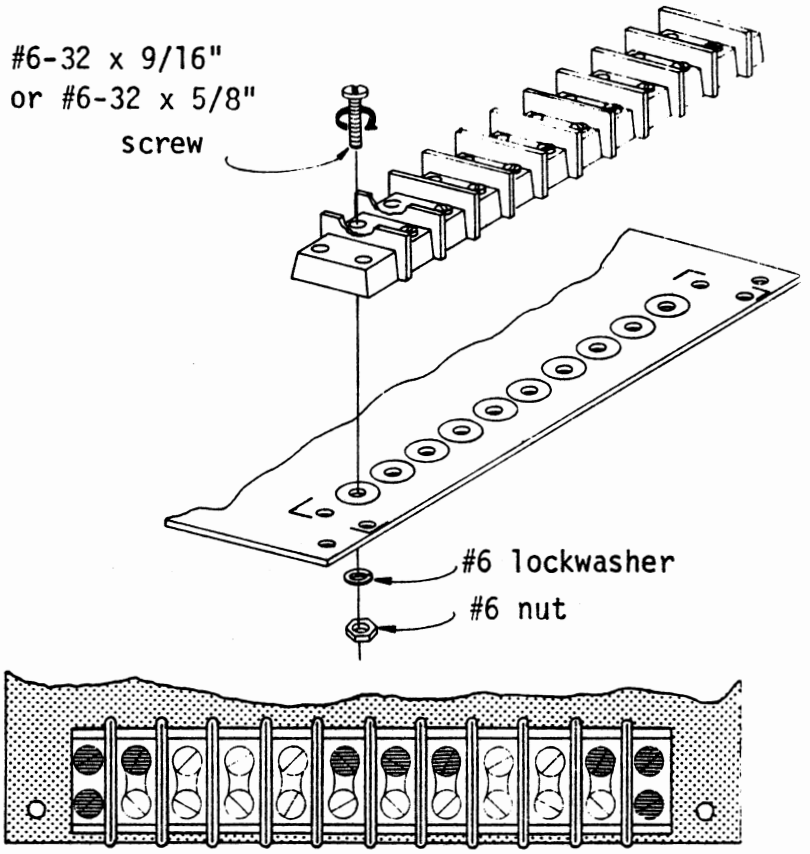
2. Set the terminal block in place on the silk-screened side of the Power Supply Board.

3. Secure the terminal block onto the board by inserting nine #6-32 x 9/16" or #6-32 x 5/8" screws, nine #6 lockwashers, and nine #6 nuts (Bag 5) into the proper holes as shown in Figure 5-41.

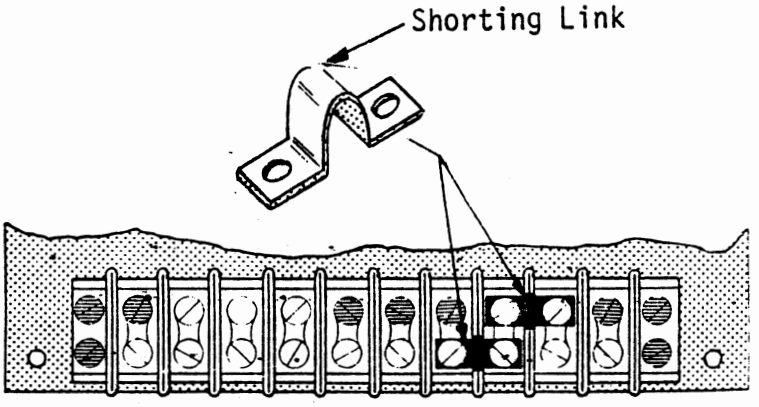
4. Insert 1 shorting link (Bag 2) over the lower portion of terminals 7 and 8, and 1 shorting link over the upper portion of terminals 8 and 9. Secure in place with four #6-32 x 1/4" screws (Figure 5-42).



5-40. Power Supply Terminal Block Screw Removal



5-41. Power Supply Terminal Block Screw Insertion



5-42. Power Supply Terminal Block Shorting Link Insertion

5-51. MOUNTING POWER SUPPLY BOARD ONTO CROSS MEMBER (Figure 5-43)

There are five holes on the Power Supply Board to be used in mounting the board to the Cross Member at the back of the main frame. Five 3/4" threaded spacers (Bag 5) and ten #6-32 x 3/8" screws (Bag 5) will be used in this procedure. Refer to Figure 5-43 and the following instructions for mounting the board to the Cross Member.

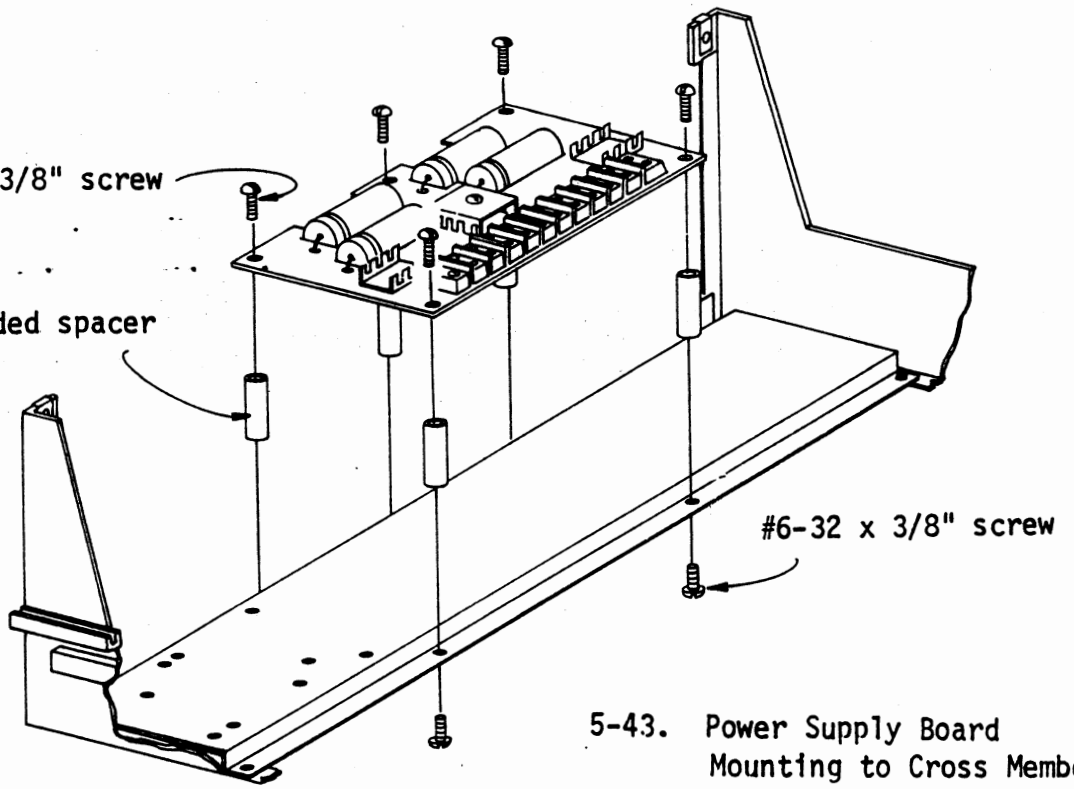
1. Insert one screw into each mounting hole on the board from the silk-screened side.

2. Put a spacer on each screw and tighten it down.

3. Rest the board on the Cross Member so that the spacers are aligned with the mounting holes.

4. Fasten the board into place by inserting another screw into each spacer from underneath the Cross Member.

> NOTE
>
> Before mounting the Power Supply Board, make a ground connection between terminal #9 on the terminal block and the lower, right-hand mounting screw on the cross member. Use a 3-inch piece of wire braid with solder lugs at each end. (Instructions for preparing the wire braid are detailed in Paragraph 5-72.



5-43. Power Supply Board Mounting to Cross Member

5-52. CAPACITOR AND CAPACITOR CLAMP INSTALLATION (Figures 5-44 and 5-45)

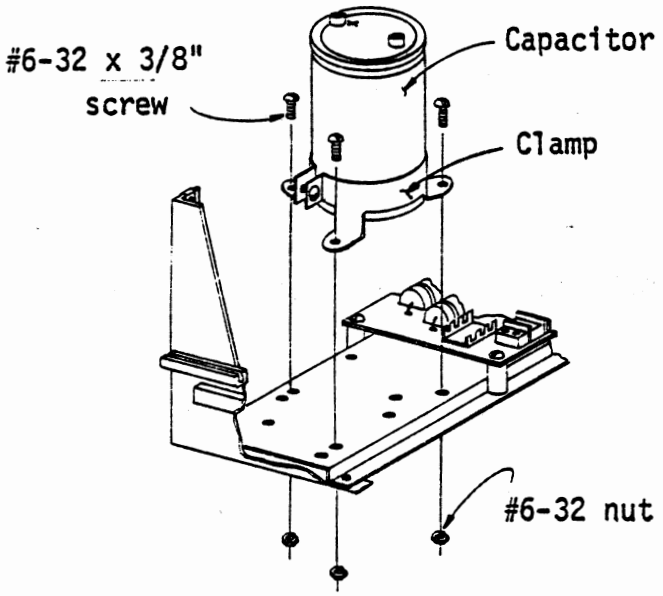
According to supply variations, your kit may contain either one capacitor (varying from 80,000uf - 100,000uf, 15V - 25V) or two capacitors (varying from 40,000uf - 50,000uf, 15V - 25V) to be mounted on the Cross Member. Figure 5-44 shows the proper placement for one capacitor. Figures 5-45A and 5-45B show the proper placement for two capacitors. The capacitor(s) are mounted in clamps using a #6-32 x 3/8" screw and a #6-32 nut (Bag 5).

Install the capacitor(s) according to the following instructions.

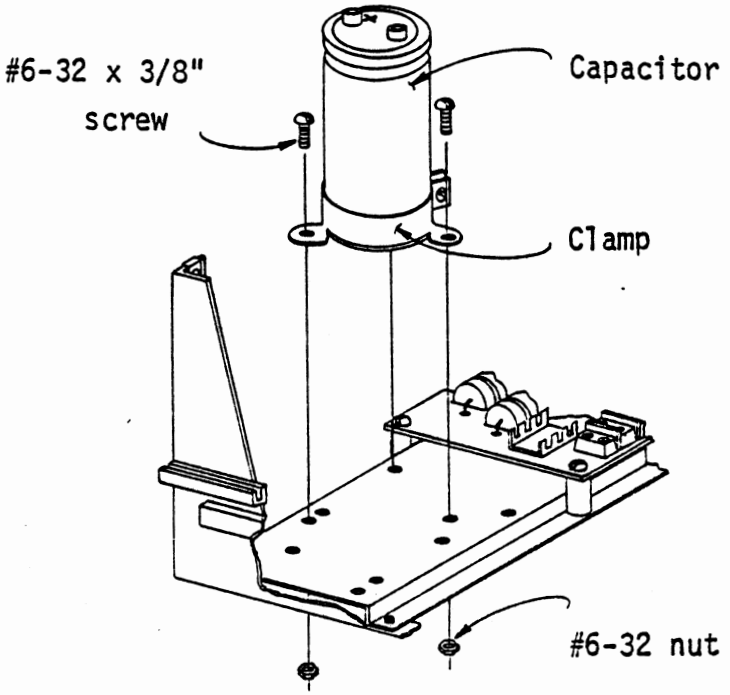
1. Secure the capacitor in the clamp with a #6-32 x 3/8" screw and orient the capacitor as shown in figure.

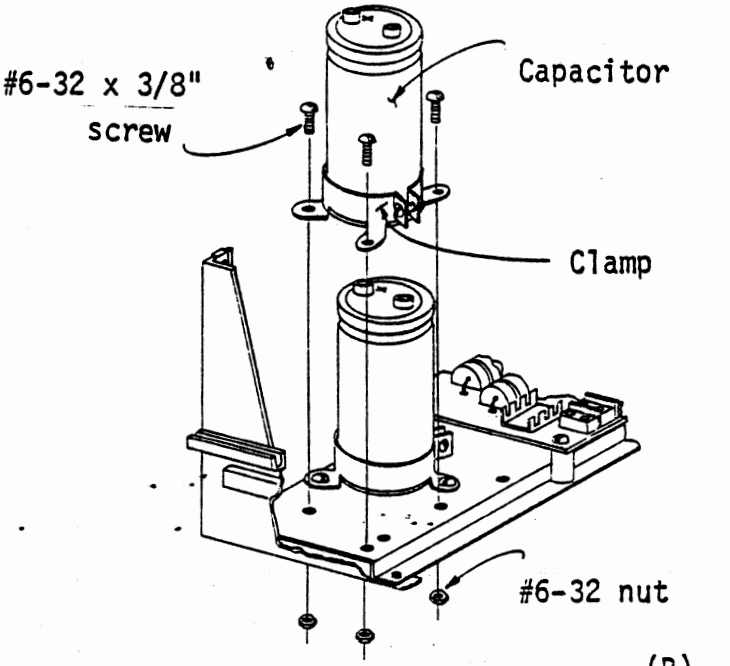
2. Place the clamp and capacitor on the Cross Member, aligning the mounting holes.

3. Secure the clamp to the Cross Member using three #6-32 x 3/8" screws and three #6-32 nuts.



5-44. Power Supply Capacitor and Clamp Installation (For One Capacitor)





5-45. Power Supply Capacitor and Clamp Installation (For Two Capacitors)

5-53. BACK PANEL ASSEMBLY (Figure 5-46)

The instructions for the assembly of the Altair 8800b back panel are divided into the following sections:

Procedural Instructions
Capacitor Wiring
Bridge Rectifier Installation
I/O Connectors
Fan Mounting
Fuse and Fuse Holder
AC Power Cord
Transformer
Back Panel Mounting

Before beginning the back panel assembly, remove the back panel from the mainframe and remove the mainframe from the case bottom. Set aside the mounting screws, as they will be replaced later in the assembly procedure.

To aid with the assembly of your unit, a view of a correctly assembled back panel is shown below in Figure 5-46.

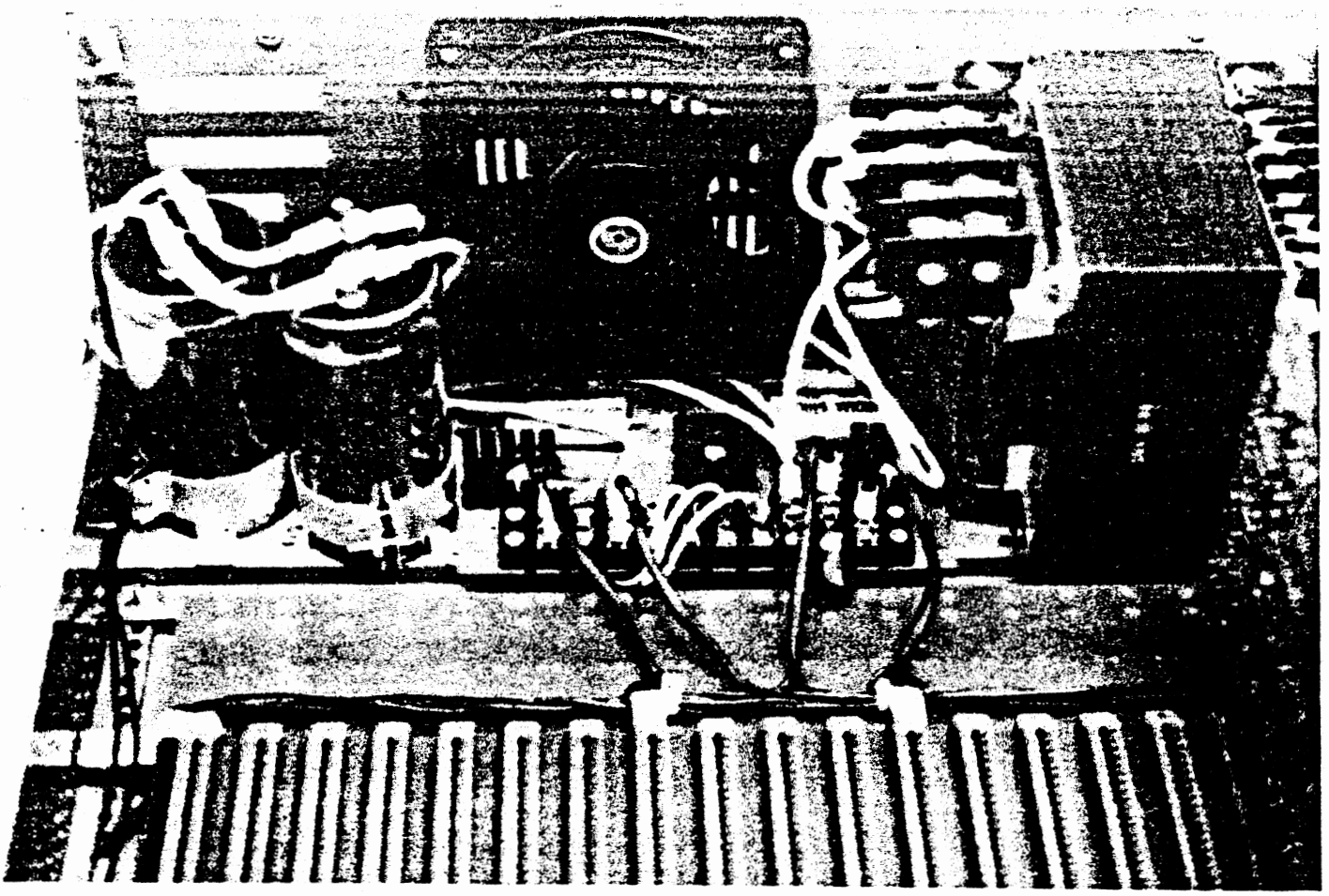


Figure 5-46. Completed Back Panel Assembly

5-54. PROCEDURAL INSTRUCTIONS (Figures 5-47 through 5-49)

Some of the terms and procedures that are repeatedly called out in the Back Panel Assembly Instructions will be explained in detail in Paragraphs 5-55 through 5-58. (The experienced kit builder who is already familiar with these procedures may wish to skip to Paragraph 5-59.)

5-55. Terminal Ends. There are five different sizes of terminal ends used in the wiring of the back panel. The sizes are shown in Figure 5-47. Refer to this figure whenever a terminal end size is called out in the assembly instructions.

5-56. Wire Preparation. Before any wire is used in an assembly step, it should be prepared as follows:

1. Cut the desired length of wire.
2. Strip 1/8" to 1/4" of insulation off the ends.
3. Tin the exposed portion of the wire by applying a thin coat of solder.

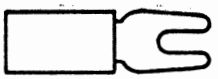
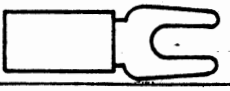
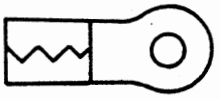
SIZE	BAG #	TERMINAL END	WIRE GAUGE	SCREW SIZE
A	2		12-10	slip on
B	2		22-18	#6 screw
C	2		12-10	#6 screw
D	2		12-10	#10 screw
E	2		12-10	#10 screw

Figure 5-47. Terminal End Sizes

5-57. Attaching Terminal Ends to Wires. Most of the wire connections in the Back Panel Assembly Instructions call for attaching a terminal end to a wire and mounting it to the proper terminal. This procedure is detailed below:

For terminal end sizes A through D:

1. Insert the exposed portion of a wire that you have prepared into the correct size terminal end as shown in Figure 5-48.

2. Heat the wire and terminal end with a soldering iron. Apply solder to the heated wire, allowing the solder to flow until there is a solid solder connection.

> NOTE
>
> If the insulator on the terminal end loosens during soldering, be sure to push it all the way back in place when soldering is completed.

> NOTE
>
> Be sure to hold A size terminal ends vertically (with the wire down) while soldering to prevent solder flowing onto the slip-on tabs.

For terminal end size E:

Size E terminal ends do not have insulators, and therefore must be insulated with heat shrink tubing. The procedure for attaching E size terminals ends varies slightly, as follows:

1. Set the E size terminal end on the work surface and heat it with a soldering iron until it is hot enough to allow solder to flow.

2. Insert the exposed portion of a wire you have prepared into the terminal end and apply solder until there is a solid connection.

3. After the wire has been soldered in place and the joint has cooled, cut a 1-inch piece of heat shrink tubing and place it over the terminal end. Use a heat gun, if available, or a match to shrink the tubing.

> CAUTION
>
> Terminal ends become extremely hot during soldering. Allow five minutes cooling time after soldering before touching the terminal ends.

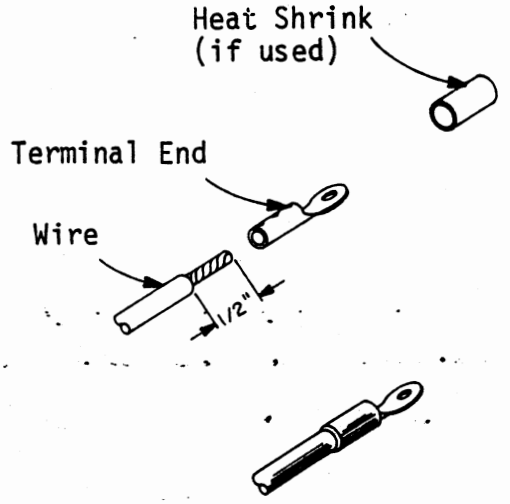


Figure 5-48. Terminal End Attachment

5-58. Connector Pins and Connector Sockets. Some of the wire connections in the back panel assembly instructions call for connector pins and connector sockets housed in a plastic plug. The general procedure for preparing these plug(s) is detailed below:

1. Insert the exposed portion of a wire that you have prepared into a connector pin or connector socket as shown in Figure 5-49A.

2. Crimp the lower portion of the pin or socket around the wire insulation. Solder the center portion of the pin or socket to the exposed portion of the wire.

3. Insert the pins and sockets into their respective housings as shown in Figure 5-49B.

4. Commoning tabs may be put into the pin housing over pins that must be shorted together. Push the commoning tabs all the way to the base of the pin housing, using the tip of a small screwdriver.

CAUTION
Make sure the commoning tabs do not come in contact with each other.

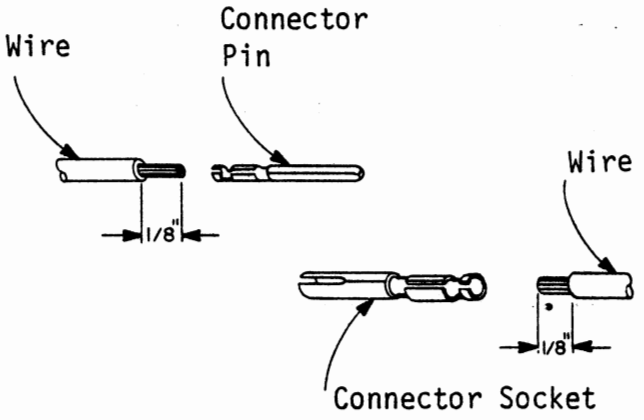


Figure 5-49A. Connector Pin and Connector Socket Wire Insertion

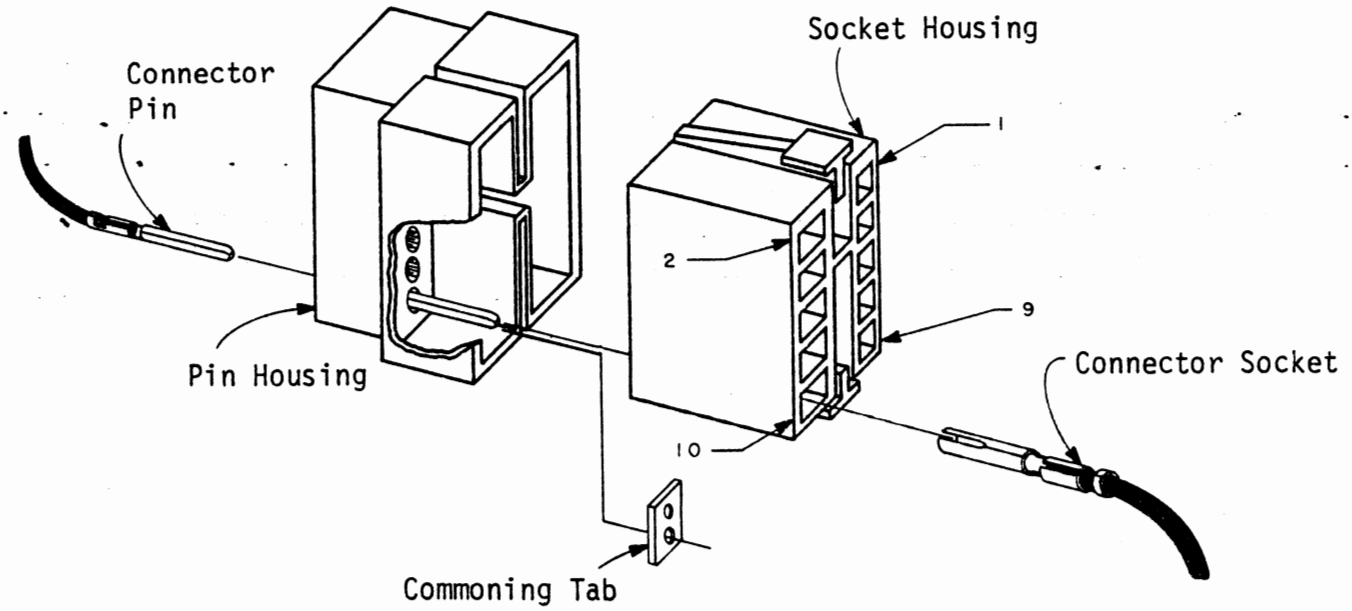


Figure 5-49B. Pin and Socket Housing Assembly

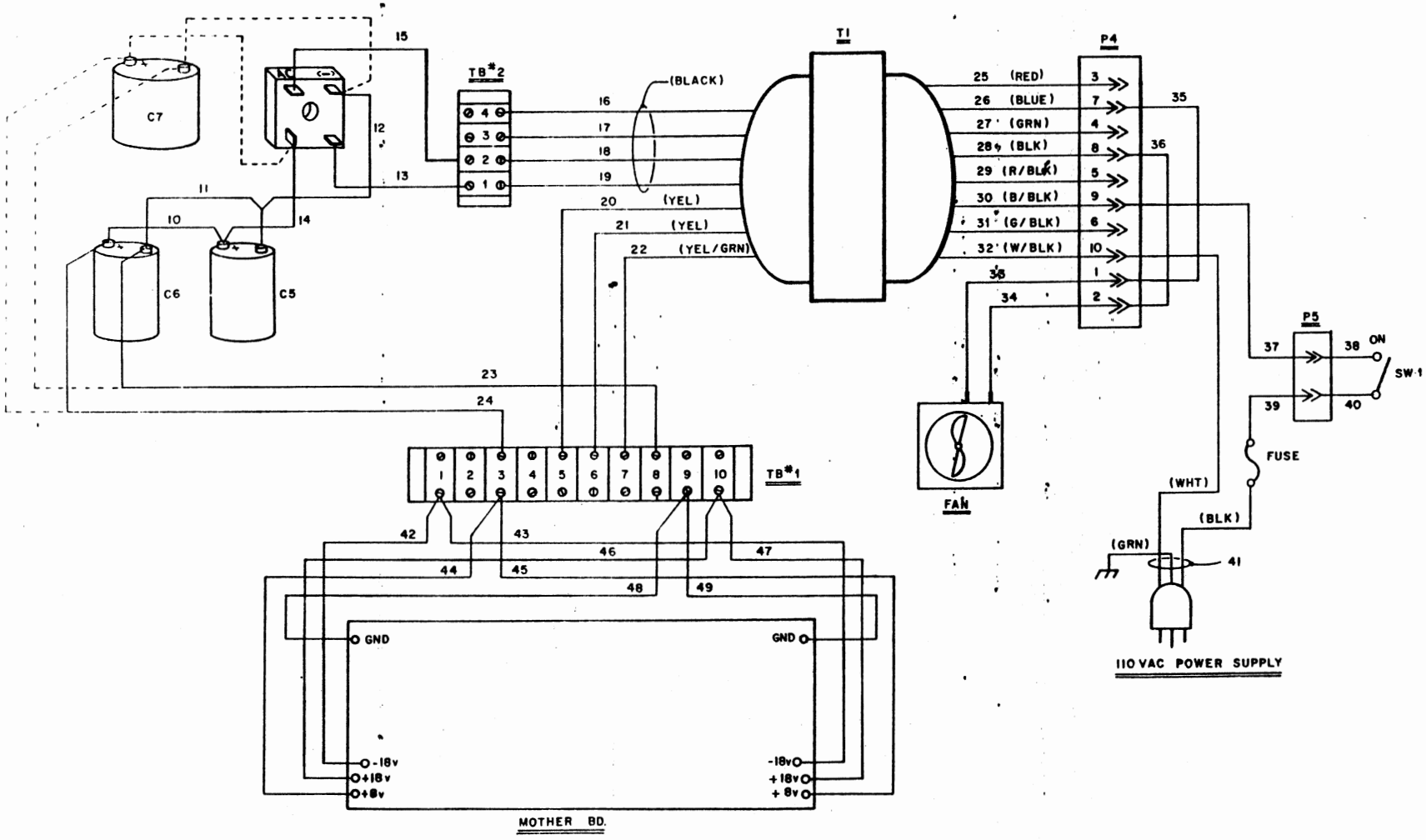


Figure 5-50. Wiring Diagram

5-59. CAPACITOR WIRING (Figure 5-50)

Before beginning assembly of the back panel, wire the capacitor or capacitors that are mounted on the Cross Member as follows:

Wiring For One Capacitor:

1. Cut two 9-inch lengths of 10-12 gauge wire. Attach C size terminal ends to one end of each wire. Attach D size terminal ends to the other end of each wire.

2. Connect the 9-inch wires to the capacitor by mounting the D size terminal ends to the "+" and ground terminals with the #10 screws provided.

3. Connect the wire from the "+" side of the capacitor to terminal #3 on the power supply board terminal block (TB1). (See wiring diagram, Figure 5-50.)

4. Connect the wire from the ground (-) side of the capacitor to terminal #8 of the terminal block (TB1). (See wiring diagram, Figure 5-50.)

Wiring For Two Capacitors:

1. Jumper the two "+" terminals to each other and the two ground terminals to each other with two 2-inch lengths of 10-12 gauge wire and four D size terminal ends.

2. Cut two 9-inch lengths of 10-12 gauge wire. Attach C size terminal ends to one end of each wire. Attach D size terminal ends to the other end of each wire.

3. Connect the 9-inch wires to C5 (capacitor closest to the Power Supply Board) by mounting the D size terminal ends to the "+" and ground terminals with the #10 screws.

4. Connect the wire from the "+" side of C5 to terminal #3 on the terminal block (TB1). (See wiring diagram, Figure 5-50.)

5. Connect the wire from the ground side of C5 to terminal #8 of the terminal block (TB1). (See wiring diagram, Figure 5-50.)

5-60. BRIDGE RECTIFIER INSTALLATION (Figure 5-51)

Use the following instructions to wire the bridge rectifier (Bag 1) and mount it to the back panel as shown in Figure 5-51. The bridge rectifier is part number KBH25005.

1. Mount the bridge rectifier to the back panel using a #6-32 x 3/4 inch screw, #6-32 nut, flat washer and lockwasher. Make sure the terminal labelled "-" is at the upper right corner.

2. Cut two 4-inch lengths of 12-10 gauge wire and two 19-inch lengths of 12-10 gauge wire.

3. Attach an A size terminal end to one end of each wire. Attach a D size terminal end to the other end of each wire.

4. Slip the A size terminal ends onto the bridge rectifier terminals as shown in Figure 5-51. Attach the two 4-inch wires to the "AC" terminals and use masking tape to label them 13 and 15. Attach the two 19-inch wires to the "+" and "-" terminals and label them 14 and 12 respectively.

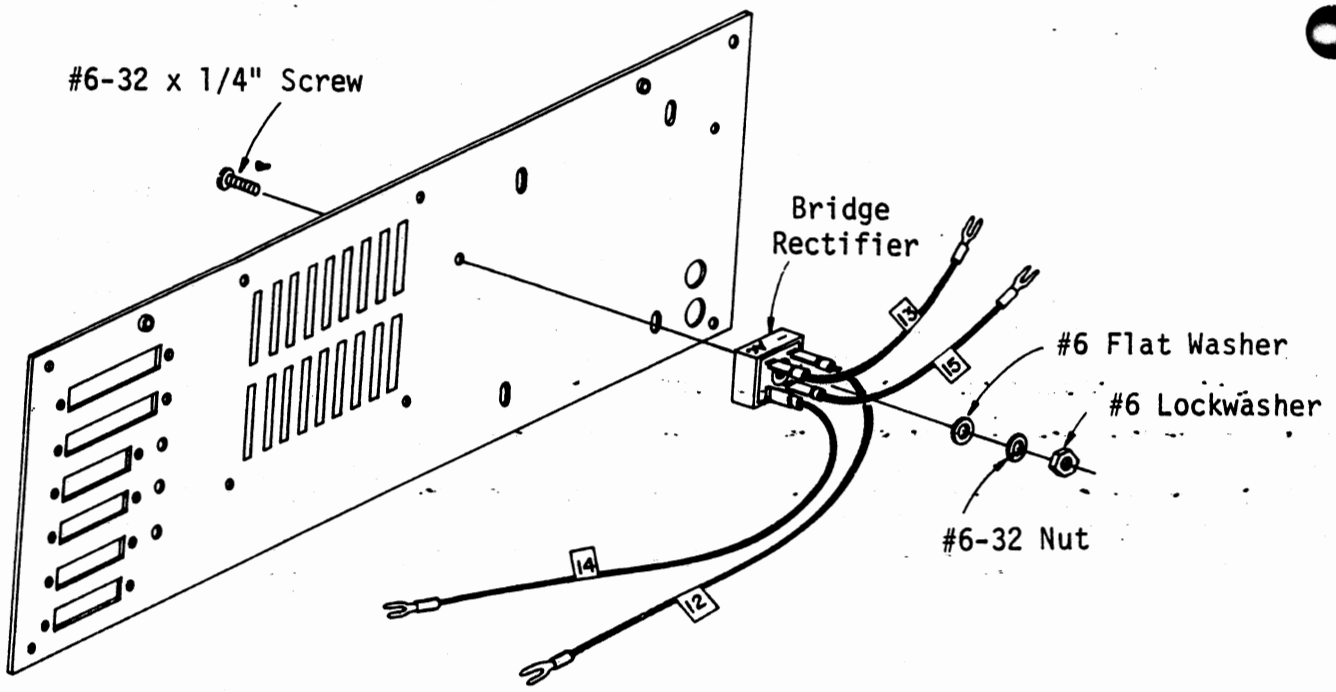


Figure 5-51. Bridge Rectifier Installation

5-61. FAN MOUNTING (Figure 5-52)

1. Before mounting the fan to the back panel, install the female plug onto the terminals as shown in Figure 5-52. If your kit does not supply a plug, solder two 20-inch lengths of 22-18 gauge wire to the terminals.

2. Attach connector sockets (Paragraph 5-58) to the two wire ends. (The wire ends on the plug have been stripped and pretinned.) Label the wires 33 and 34.

3. Mount the fan to the back panel with the airflow flowing inward. Use four #6-32 x 5/8 inch screws and four #6 "snap-on nuts" to mount the fan.

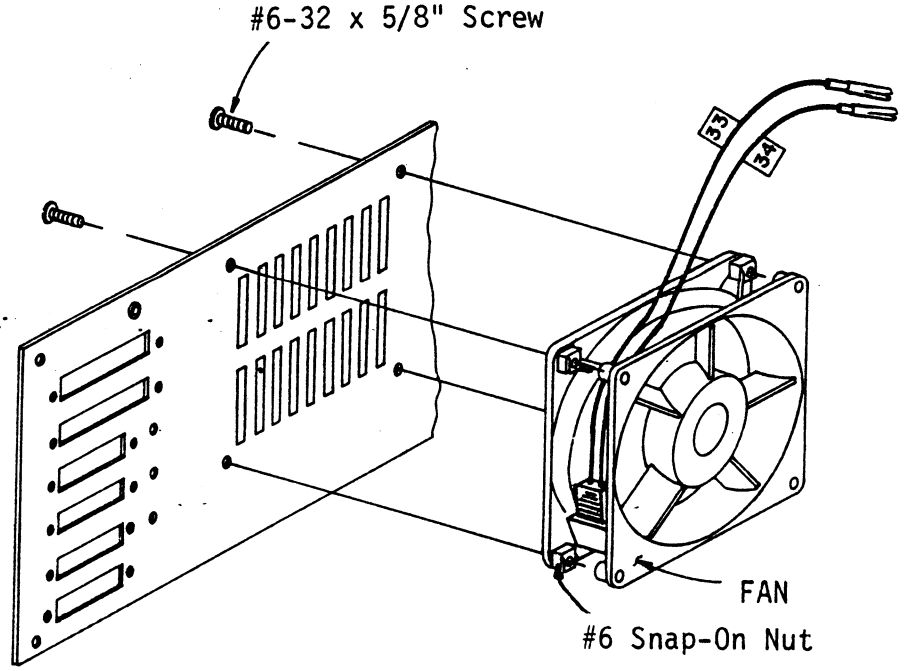


Figure 5-52. Fan Mounting

5-62. FUSE AND FUSE HOLDER (Figure 5-53)

1. Secure the fuse holder (Bag 2) into the hole provided on the back panel using a fiber washer and mounting nut as shown in Figure 5-53.

2. Attach a 40-inch length of 22-18 gauge wire to the side terminal on the fuse. Mount a connector pin to the end of the 40-inch wire and label the wire #39 (see Paragraph 5-58).

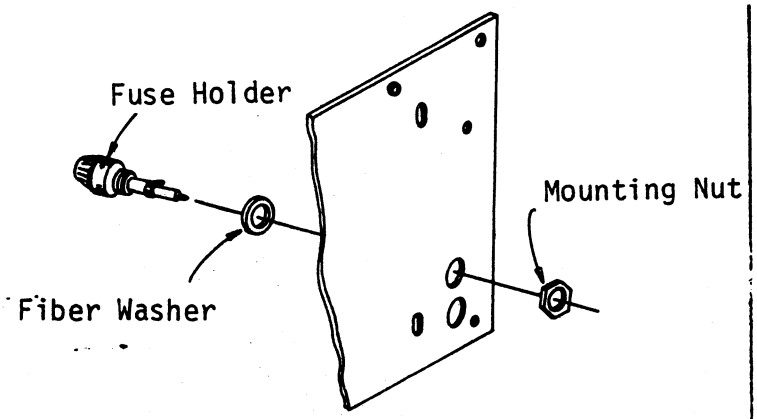


Figure 5-53. Fuse Holder Installation

5-63. AC POWER CORD (Figure 5-54)

1. Strip about 7 inches of casing off the end of the power cord to expose the three wires inside.

2. Put the strain relief (Bag 2) on the cord and position it as shown in Figure 5-54.

3. Snap the strain relief in place on the back panel.

4. Cut the black power cord wire to a length of 2 inches and solder it to the end of the fuse holder. Cut the green power cord wire to a length of 5 inches and attach a solder lug to the end. Attach a connector socket (Bag 4) (see Paragraph 5-58) to the end of the 7-inch white wire.

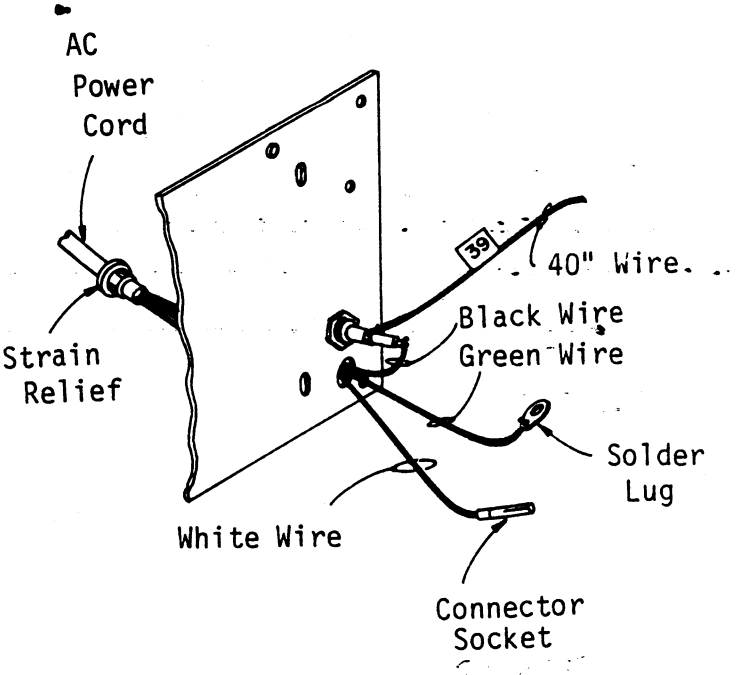


Figure 5-54. AC Power Cord Installation

5-64. TRANSFORMER (Figures 5-55 through 5-59)

The instructions for wiring and mounting the transformer will be divided into three parts: Secondary Wiring, Primary Wiring, and Transformer Mounting. Review Paragraphs 5-55 through 5-58 for the procedures involved.

5-65. Secondary Wiring.

1. Orient the transformer with the secondary side (four black wires) facing you. Remove the two top bolts and nuts and use them to mount two "L" brackets (Bag 2) as shown in Figure 5-55.

2. Attach an E size terminal end with heat shrink tubing (see Paragraph 5-58) to each of the four black transformer wires and label the wires 16-17-18-19, beginning with the top wire (Figure 5-56).

3. Attach a C size terminal end to each of the three remaining secondary wires (Figure 5-56). Label the two yellow wires 20 and 21, and label the yellow/green wire 22.

4. Bend each of the E size terminal ends at a right angle as shown in Figure 5-56. Mount the four black wires to one side of the 4-terminal block (TB2), using the screws provided.

5. Mount the terminal block to the "L" brackets on the transformer using four #6-32 x 3/4 inch screws, four #6-32 nuts and four #6 lockwashers (Figure 5-57).

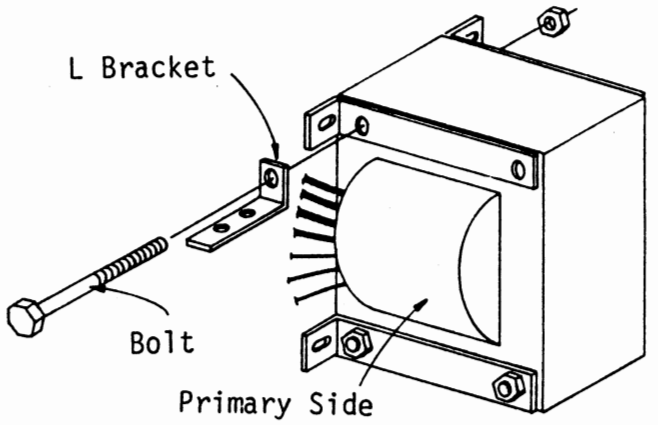


Figure 5-55. "L" Bracket Mounting

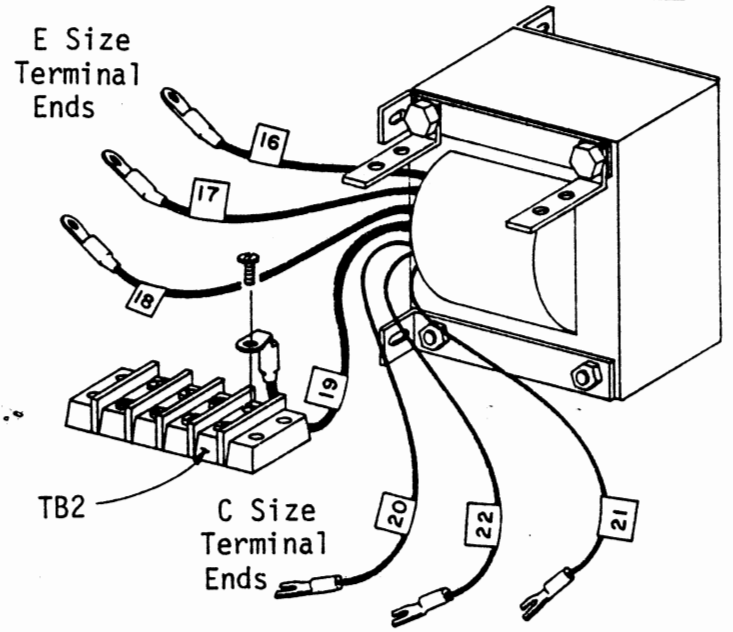


Figure 5-56. Terminal End Attachment

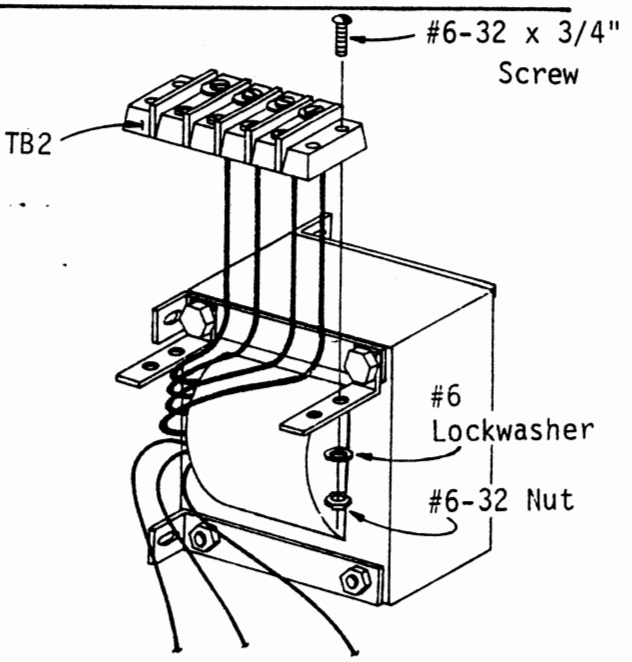


Figure 5-57. Terminal Block Mounting

5-66. Primary Wiring. The wires on the primary side of the transformer will be connected to the 110 volt source with a 10-pin plug (see Paragraph 5-58) according to the following instructions.

A. Pin Housing.

1. Attach a connector to each of the primary transformer wires.

2. When all eight wires on the primary side of the transformer have pins attached, insert the pin housing (P4) as shown in Figure 5-58. Insert the pins in the following order (see wiring diagram, Figure 5-50):

Wiring Diagram Designation	Transformer Wire Color (Primary Side)	P4 Pin Housing Slot Number
25	Red	3
26	Blue	7
27	Green	4
28	Black	8
29	Red/Black	5
30	Blue/Black	9
31	Green/Black	6
32	White/Black	10

Place a two-circuit commoning tab over the following pairs of pins:

3 and 5 — 4 and 6

7 and 9 — 8 and 10

Make sure the tabs do not come in contact with each other.

3. The two wires from the fan (33 and 34) are to be inserted into slots 1 and 2 of the P4 pin housing.

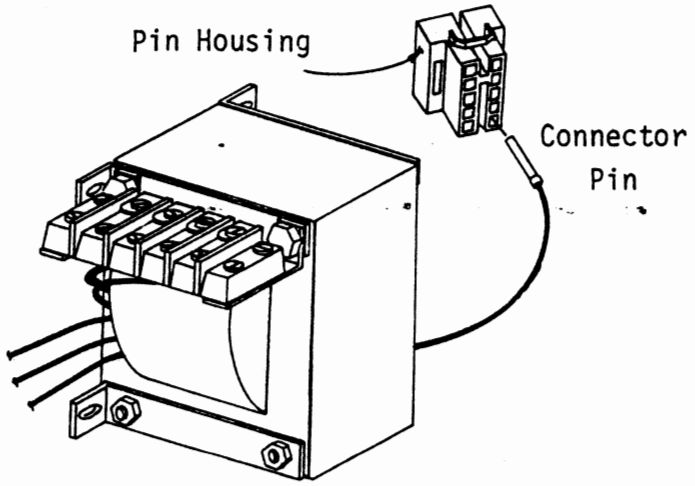


Figure 5-58. Pin Housing Insertion

B. Socket Housing.

1. Cut a 40-inch length of 22-18 gauge wire and attach a connector socket to each end. Label this wire 37.

2. Insert one connector socket of wire 37 into slot 9 of the 10-pin socket housing. Insert the socket on the 7-inch white AC power cord wire into slot 10 of the 10-pin socket housing.

3. Connect the socket housing to the pin housing, as shown in Figure 5-49.

5-67. Mount Transformer to Back Panel.

1. Mount the transformer to the back panel as shown in Figure 5-59 using four #10-32 x 1/2 inch screws, 4 nuts, 4 flat washers and four #10 lockwashers. (The transformer positioning may have to be adjusted later when the back panel is mounted to the mainframe, to insure the transformer is resting on the cross member.)

2. Attach wires 13 and 15 from the bridge rectifier to terminals 1 and 2 of the terminal block (TB2). (See Wiring Diagram, Figure 5-50.)

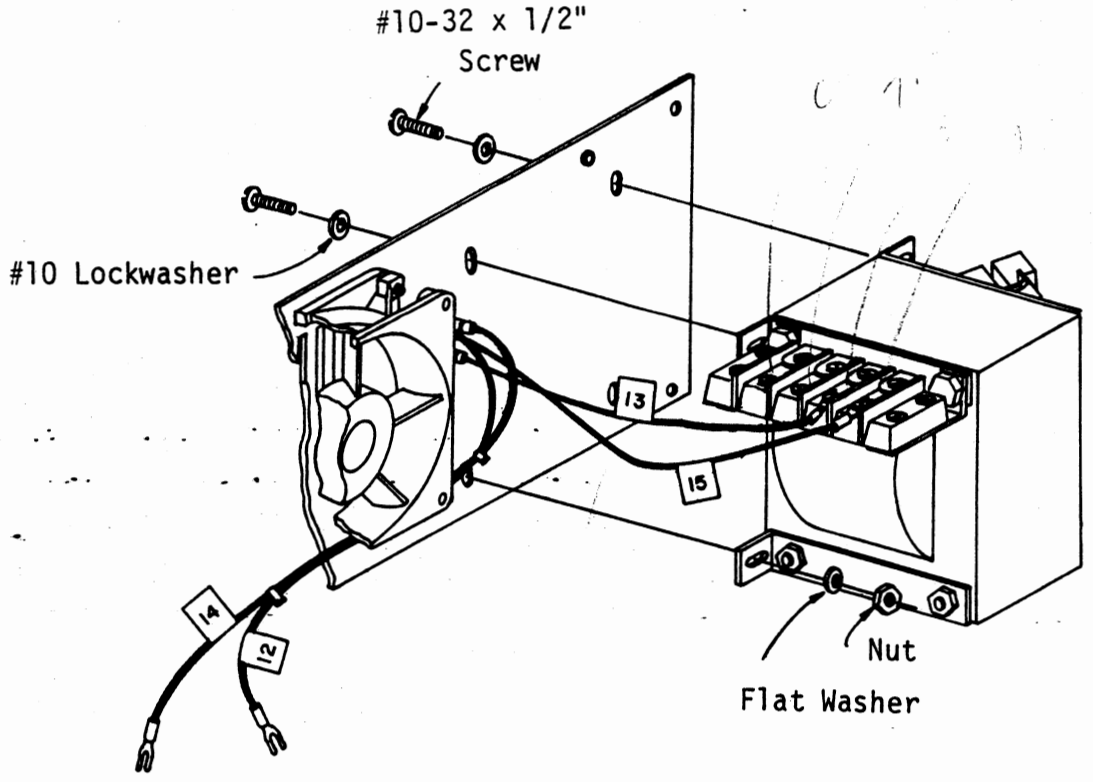


Figure 5-59. Transformer Mounting

5-68. MOUNT BACK PANEL TO MAINFRAME (Figure 5-60)

1. Mount the back panel to the mainframe as shown in Figure 5-60 using the original back panel mounting screws. (Tighten these screws down until they are just firm.)

2. Make sure the two 19-inch bridge rectifier wires, the 40-inch fuse wire (#39), and the 40-inch connector plug wire (#37) go under the fan as the back panel is mounted. Connect wire 14 from the bridge rectifier to the "+" side of the capacitor(s). Connect wire 12 from the bridge rectifier to the ground side of the capacitor(s). Make continuity checks (see wiring diagram, Figure 5-50).

> **NOTE**
>
> Make sure the wires from the fan go underneath the fan and the transformer as the back panel is mounted. Make sure the transformer rests solidly on the cross member when the back panel is in place.

3. Secure the solder lug on the green AC ground wire to one of the holes on the side of the mainframe using a #6-32 x 1/4" screw, a #6-32 nut, and a #6 lockwasher.

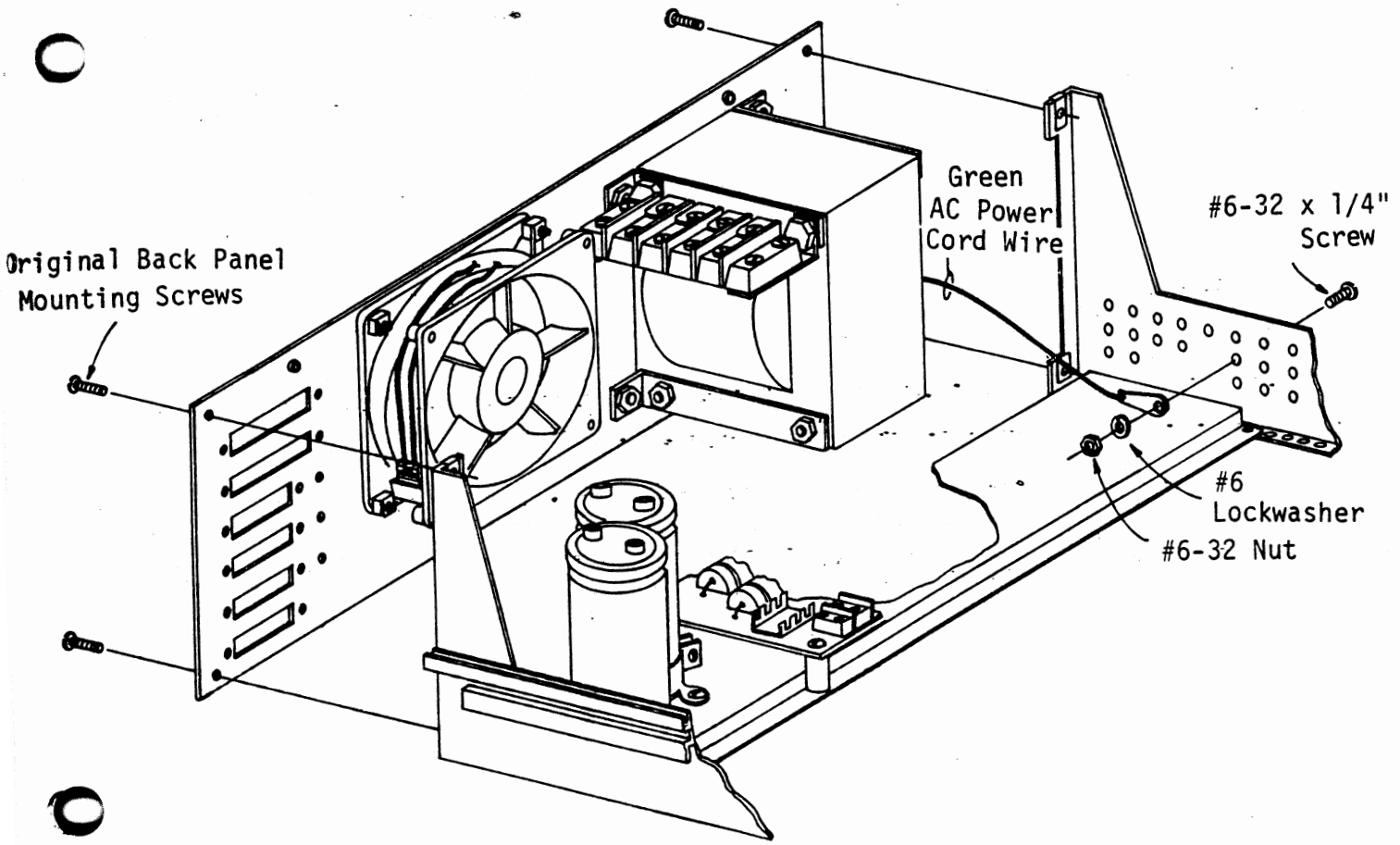


Figure 5-60. Back Panel Mounting

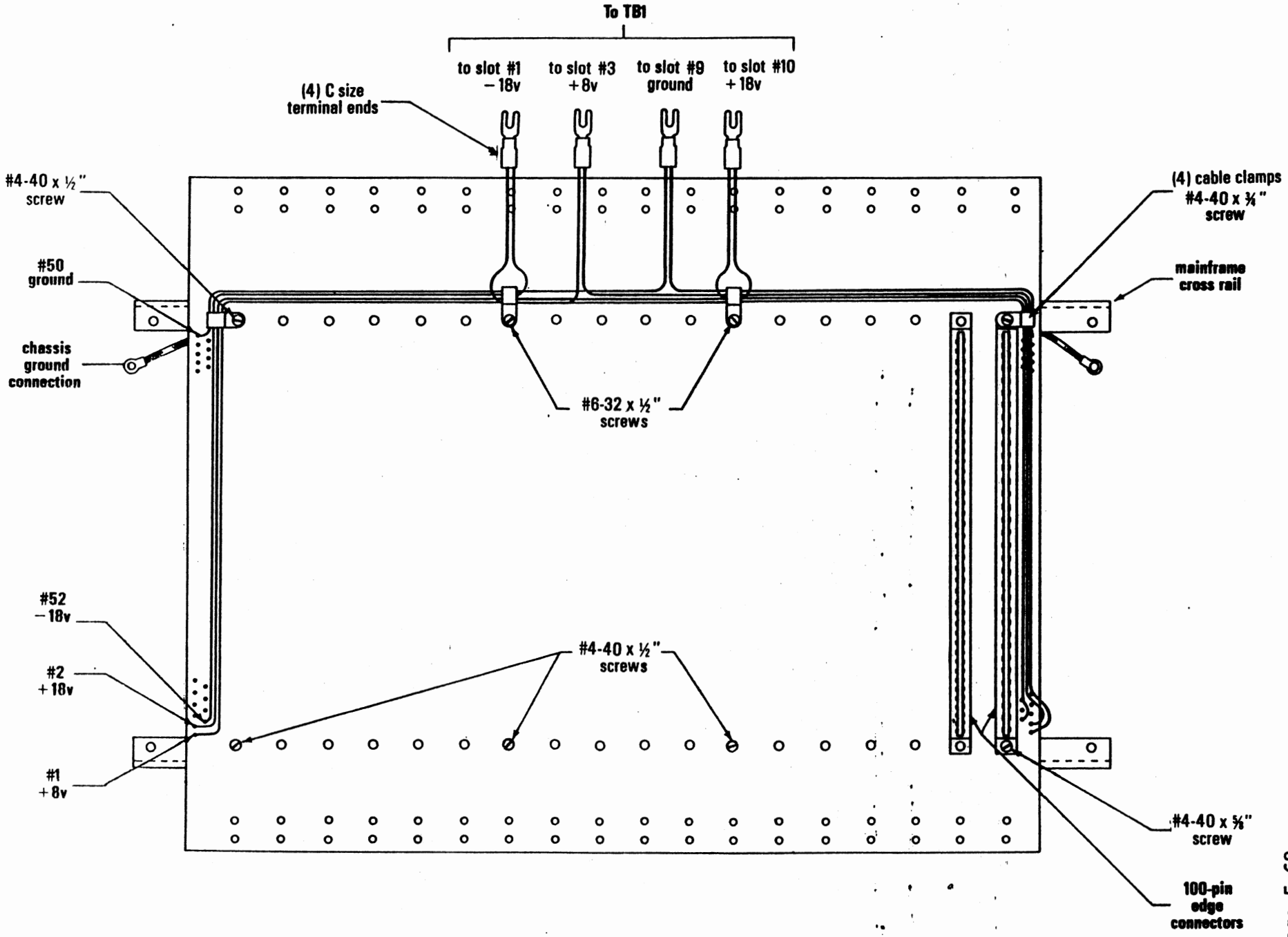


Figure 5-61. Motherboard Wire Connections

5-69. 18-SLOT MOTHERBOARD ASSEMBLY

5-70. BUS WIRE CONNECTIONS (Figure 5-61)

Refer to Figure 5-61. Note that the two outside rows of holes on either side of the motherboard each have four wire connections. These are the +8v, -18v, +18v and ground lines to the power supply from the bus. The wire connections are made by inserting the end of the wire from the top side of the motherboard and soldering it to the foil (bottom) side. On the foil side of the motherboard, hole #1 and hole #50 are marked on each side. Complete the wire connections according to the following instructions:

1. Cut six 20-inch lengths and two 14-inch lengths of 22-18 gauge wire.

On both sides of the motherboard:

2. Install one 20-inch wire into hole #1 (+8v).

3. Install one 20-inch wire into hole #2 (+18v).

4. Install one 20-inch wire into hole #52 (-18v).

5. Install one 14-inch wire into hole #50 (ground).

5-71. HARDWARE INSTALLATION (Figures 5-61 and 5-62)

At this time, the edge connectors, cable clamps, mainframe cross rails, and card guides will all be assembled onto the motherboard according to Figures 5-61 and 5-62 and the following instructions.

1. Position the two 100-pin edge connectors on the motherboard as shown in Figure 5-61. Carefully insert the connector pins into their respective holes. If necessary, guide some of the pins with the tip of a small screwdriver. Be sure that the connector is tight against the board and that all 100 pins have been inserted. Solder each connector pin to the foil pattern on the bottom of the board.

2. Visually inspect the connection to make sure there are no solder bridges.

3. Remove the two cross rails from the mainframe. Mount the cross rails to the bottom of the motherboard using eight screws, positioned as shown in Figure 5-61. Attach cable clamps to the four back mounting screws and run the bus wires through the cable clamps before tightening the screws down.

4. Match up the four pairs of bus wires at the back of the motherboard as shown in Figure 5-61. Attach a size C terminal end to each pair. Make sure the correct wires have been paired off:

   -18v with -18v
   +8v with +8v
   ground with ground
   +18v with +18v

5. Mount the card guides on both sides of the connectors, as shown in Figure 5-62.

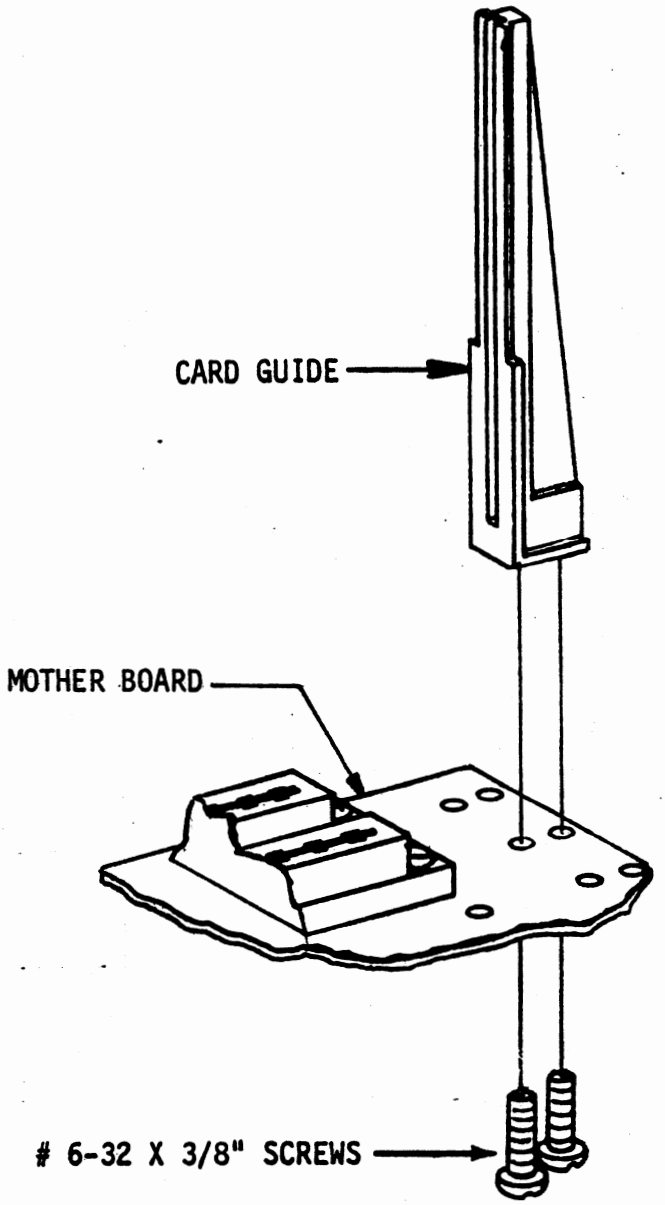


Figure 5-62. Card Guide Mounting

5-72. CHASSIS GROUND CONNECTION (Figure 5-63)

To insure a good ground connection between the motherboard and the chassis, two ground wires will be run from the ground land on the foil (bottom) side of the motherboard to the side rails of the mainframe. Refer to Figure 5-63 and make the ground connections according to the following instructions.

1. Cut two 6-inch pieces of wire braid.
2. Attach a solder lug to one end of each piece. To do this: twist the end of the wire braid; insert it into the small hole on the lug; solder the braid to the lug until the small hole is completely filled with solder.

On both sides of the motherboard:

3. Place the braid on the ground land along side the cross rail so that the lug and about three inches of braid hang over the side, as shown in Figure 5-63. Solder the remaining three inches to the ground land. It may be helpful to first "tack" the braid in place with small amounts of solder and then, using the flat of the soldering iron to heat the braid, make a solid solder connection over the entire three inches. Make sure there are no solder bridges to the adjacent lands on the board. The lugs will be attached to the side rails of the mainframe after the motherboard has been installed (Paragraph 5-73).

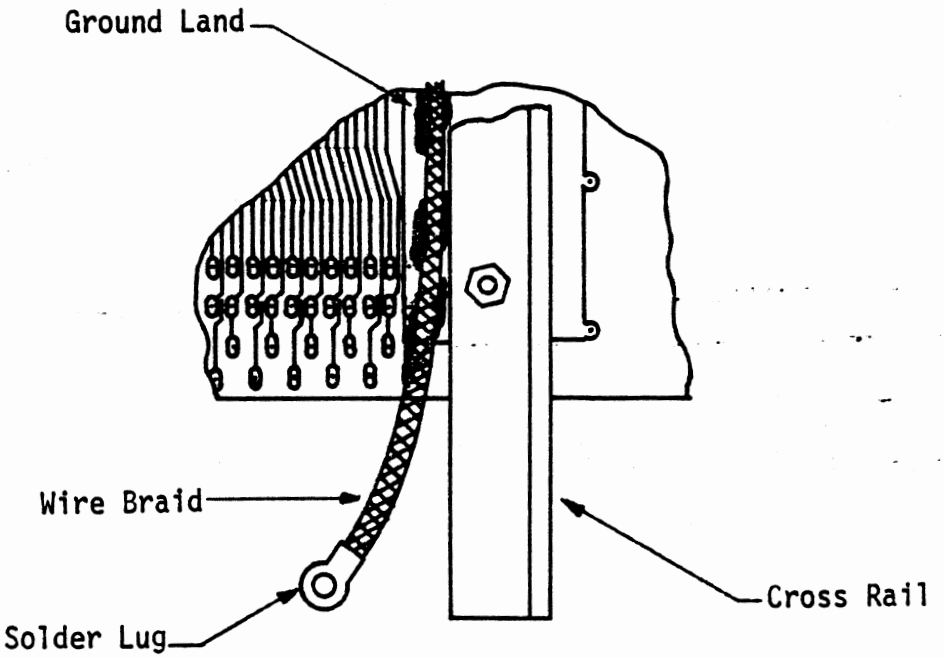


Figure 5-63. Chassis Ground Connection

5-73. INSTALL MOTHERBOARD ON MAINFRAME

1. Attach four #6-32 x 3/8" threaded spacers to the end holes in the crossrails, using #6-32 x 1/4" screws. Place the motherboard/crossrail assembly in the chassis so that the spacers at the front of the assembly align with the 8th hole (from the front) of the chassis side members. Secure the assembly to the chassis with four #6-32 x 1/4" screws.

2. Connect the four terminal ends on the bus wires to the terminal block (TB1) on the Power Supply Board as follows (see wiring diagram, Figure 5-50):

Voltage	Bus Connection	TB1 Connection
-18v	holes #52	slot #1
+8v	holes #1	slot #3
ground	holes #50	slot #9
+18v	holes #2	slot #10

Check for continuity between each bus connection and its respective terminal block connection.

3. To assure a good ground connection, rub the alodine coating off the chassis side member with steel wool. On each side of the board, connect the chassis ground wire from the motherboard to one of the holes on the chassis side member. Secure with a #6-32 x 3/8" screw and a #6-32 nut.

5-74. ON/OFF SWITCH WIRING (Figure 5-64)

The on/off switch (S1) on the Display/Control Board will connect to wires 37 and 39 from the power supply by means of a 2-pin plug, P5. (See wiring diagram, Figure 5-50.) Prepare the 2-pin plug (Bag 4) according to the following instructions. (Refer to Paragraph 5-58 for procedural instructions on preparing the connector sockets and pins.)

1. Cut two 2-inch pieces of 22-18 gauge wire.

2. Solder one wire (wire #40) to the center pin of S1 on the foil (bottom) side of the Display/ Control Board. Solder the other wire (wire #38) to the bottom pin of S1.

3. Attach a connector pin to the free end of both wires. Insert the connector pins into the 2-pin pin housing, as shown in Figure 5-64.

4. Insert the connector sockets of wires 37 and 39 from the power supply into the 2-pin socket housing.

> CAUTION
>
> These sockets (37 and 39) will be directly connected to the 110v source: Make sure the sockets are completely enclosed inside the socket housing. It is advisable to use tape or heat shrink to insulate the wires where they enter the socket housing.

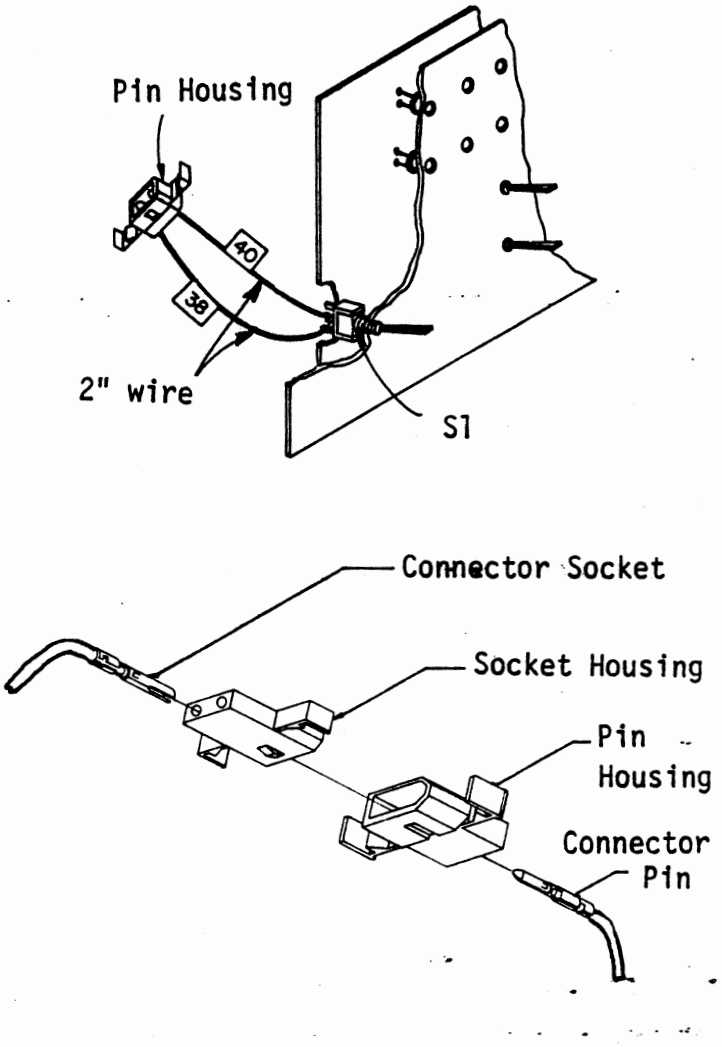


Figure 5-64. On/Off Switch Wiring

5-75. MOUNT PC BOARDS IN MAINFRAME

1. Slide the Sub Panel (with the Display/Control Board attached) onto the front of the mainframe so that the front uprights are in between the Display/Control Board and the Sub Panel.

2. Secure the Sub Panel in place from the front of the mainframe using the four #6-32 flathead screws that came with the chassis.

3. Perform a voltage check before installing the Interface Board and CPU Board. Connect the pin and socket housings of P5, put the fuse into the fuse holder, plug in the power cord, and turn S1 on. Monitor the voltages on the motherboard. If the voltages are not correct, refer to Section IV, Troubleshooting. (Disconnect power before proceeding with the next steps.)

4. Install the Interface Board onto the motherboard in the first (right-most) 100-pin connector. The ribbon connectors, P1 and P2 should be next to the Display/Control Board. Connect P1 and P2 from the Interface Board to P1 and P2 on the Display/Control Board.

5. Install the CPU Board into the next 100-pin connector. Prepare two female connectors (see Paragraph 5-76) and mount them so that P3 on the Interface Board is connected to P3 on the CPU Board.

5-76. Instructions for Female Connectors, P3 (Figure 5-65)

1. Using the wire in Bag 4 of the Interface Board, cut the wire into eight 2-inch lengths.

2. Strip 1/8 inch of insulation from the ends of each wire and tin the exposed ends by applying a thin coat of solder.

3. Install a connector pin (Bag 3 of D/C Interface Board) onto both ends of each wire by crimping the wire into place as shown in Figure 5-65 A and B. Then solder the exposed portion of the wire to the pin.

4. Insert the 8 pins into connector slots 3 through 10 on both connectors, as shown in Figure 5-65(C).

5. Insert the key (Bag 3 of D/C Interface Board) into connector slot #2. This key is inserted to insure that the female connectors are installed correctly.

NOTE
Slot #1 will not be wired.

6. Aligning slot #1 with pin #1, install the female connector onto the male connector (P3) on the Interface Board and on the CPU Board.

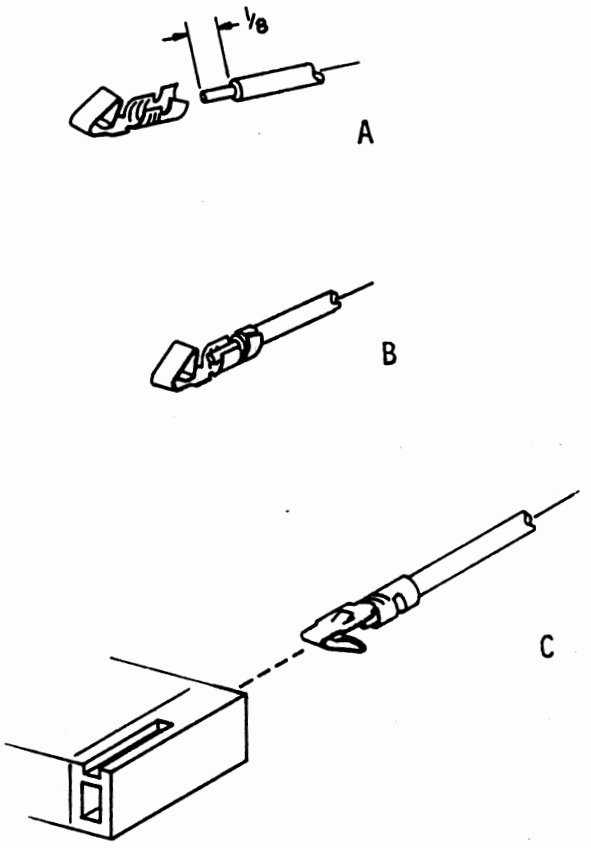


Figure 5-65. Female Connector Wiring for P3

5-77. CASE

1. Snap the dress panel in place in front of the case bottom.

2. Lower the mainframe into the case bottom at a front-to-back angle, so the switches on the Display/Control Board fit through the holes on the dress panel.

3. Secure the mainframe in place on both sides by replacing the two original #6-32 x 3/8" mounting screws.

4. Put the case top on the case bottom.

appendix A

parts list

8800b Interface Board

Bag	Quantity	Component	MITS Stock Number
1	11	74LS04 Integrated Circuit	101042
	3	74LS20 Integrated Circuit	101134
	4	74367 Integrated Circuit	101040
	1	7400 Integrated Circuit	101020
	1	7402 Integrated Circuit	101021
	1	7410 Integrated Circuit	101024
	1	8212 Integrated Circuit	101071
	1	7805 Voltage Regulator	101074
	1	24-pin Socket	102105
2	24	.1 uf 12v Capacitor	100348
	2	33 uf 16v Capacitor	100326
3	2	Molex Key	101791
	3	Ferrite Bead	101876
	1	Heat Sink	101870
	1	Small 10-pin Right Angle Connector	101798
	2	Molex Plug	101720
	20	Molex Terminal	101723
	5	6-32 x 3/8" Screw	100925
	2	4-40 x 5/8" Screw	100904
	1	6-32 Nut	100933
	2	4-40 Nut	100932
	1	#6 Lockwasher	100942
	1	#4 Lockwasher	100941

8800b Interface Board - Continued

Bag	Quantity	Component	MITS Stock Number
4	1	100-pin Edge Connector	101864
	2	Card Guides	101714
	2	Ribbon Cable Assembly 34 Conductor	103038
	4	14" Green or Blue Wire	103051 or 103052
5	7	2.2K 1/2w 5% Resistor	101945
MISC.	1	PC Board	100201

8800b Display Control Board

Bag	Quantity	Component	MITS Stock Number
1	7	7407 Integrated Circuit	101142
	5	7405 Integrated Circuit	101052
	8	74LS175 Integrated Circuit	101140
	2	74LS74 Integrated Circuit	101088
	1	74367 Integrated Circuit	101040
	2	8T98 Integrated Circuit	101045
	1	7493 Integrated Circuit	101030
	2	7400 Integrated Circuit	101020
	4	74LS04 Integrated Circuit	101042
	1	74LS14 Integrated Circuit	101123
	3	7410 Integrated Circuit	101024
	1	74L10 Integrated Circuit	101081
	2	74LS30 Integrated Circuit	101135
	2	4040 Integrated Circuit	101130
	1	4009 Integrated Circuit	101104
	1	7805 Voltage Regulator	101074
	1	79M08 Voltage Regulator	101111
2	2	100 Ohm 1/2w 5% Resistor	101924
	1	470 Ohm 1/2w 5% Resistor	101927
	1	1K 1/2w 5% Resistor	101928
	1	4.7K Resistor Pack	101999
	1	5 Ohm 5w 5% Resistor	102074
	2	6-32 x 1/4" Screw	100917
	2	IN914 Diode	100705

8800b Display Control Board - Continued

Bag	Quantity	Component	MITS Stock Number
	2	6-32 Nut	100933
	2	#6 Lockwasher	100942
	3	Ferrite Beads	101876
3	37	220 Ohm 1/2w 5% Resistor	101925
4	34	2.2K Ohm 1/2w 5% Resistor	101945
5	3	.001uf 1kv Capacitor	100328
	1	.1uf 50v Capacitor	100380
	2	47uf 16v Capacitor	100392
	2	22uf 35v Capacitor	100393
6	25	.1uf 12v Capacitor	100348
7	17	SPDT (ST1-1F2C) Switch	101879
8	8	MOM (ST1-3F2C) Switch	101880
9	36	RL-21 LED	100702
10	1	1702A Programmed PROM	
	3	8212 Integrated Circuit	101071
	4	24-pin Socket	102105
MISC.	1	PC Board	100200

8800b CPU Board

Bag	Quantity	Component	MITS Stock Number
1	1	8080 Integrated Circuit	101070
	1	8212 Integrated Circuit	101071
	1	4009 Integrated Circuit	101143
	1	24-pin Socket	102105
	1	40-pin Socket	102106
2	2	8216 Integrated Circuit	101141
	1	8224 Integrated Circuit	101125
	7	74367 Integrated Circuit	101040
	2	74368 Integrated Circuit	101045
	2	74LS14 Integrated Circuit	101123
	1	74LS13 Integrated Circuit	101124
	2	74LS04 Integrated Circuit	101042
	1	7805 Voltage Regulator	101074
	1	7812 Voltage Regulator	101085
3	24	2.2K 1/2w 5% Resistor	101945
4	13	3.3K 1/2w 5% Resistor	102085
	1	15K 1/2w 5% Resistor	102083
	1	1K 1/2w 5% Resistor	101928
	1	620 Ohm 1/2w 5% Resistor	102095
	1	330 Ohm 1/2w 5% Resistor	101926
	2	470 Ohm 1/4w 5% Resistor	101902
	1	10K 1/2w 5% Resistor	101932
	1	100 Ohm 1/2w 5% Resistor	101949
	1	10 Ohm 2w Resistor	101960

8800b CPU Board - Continued

Bag	Quantity	Component	MITS Stock Number
	1	IN4733 5v Diode	100721
	1	IN4730 3.9v Diode	100734
	3	CS4410 or 2N4410 Transistor	102806
5	22	.1uf 12v Capacitor	100348
6	3	.1uf 50v Capacitor	100380
	13	1uf 35v Capacitor	100308
	4	33uf 16v Capacitor	100326
	2	10uf 25v Capacitor	100352
	1	10uf 16v Capacitor	100394
	1	22uf 16v Capacitor	100395
7	1	Small 10-pin Right Angle Connector	101798
	1	100-pin Edge Connector	101864
	2	Card Guides	101714
	7	Ferrite Beads	101876
	1	18 MHz Crystal	101877
	2	Heat Sink (Large)	101870
	6	6-32 x 3/8" Screw	100925
	2	6-32 Nut	100933
	2	#6 Lockwasher	100942
	2	4-40 x 5/8" Screw	100904
	2	4-40 Nut	100932
	2	#4 Lockwasher	100941
MISC.	1	PC Board	100198

8800b Power Supply Board

Bag	Quantity	Component	MITS Stock Number
1	1	Bridge Rectifier 25 AMP, 50v (KBH25005)	100735
	1	Bridge Rectifier TJ 118-0 (KBPC802)	100733
	1	Transistor TIP 140, TIP 141 (with mica insulator and washer)	102819
	1	Transistor TIP 145, TIP 146 (with mica insulator and washer)	102820
	2	IN4746 18v Zener Diode	100726
	2	180 Ohm 1/2w Resistor	101998
	3	Heat Sink (large)	101870
2	1	Terminal Block 150 Series, 4 Term.	101627
	1	Terminal Block 141 Series, 10 Term.	101868
	2	Jumper for 141 Series	101651
	1	Fuse - 3 amp SLO-BLOW	101772
	1	Fuse Holder	101813
	2	T.B. Brackets	101652
	1	Strain Relief	101719
	4	Rubber Feet	101751
	4	Ring Terminal #10-#12 wire, #10 bolt	101642
	6	Spade Terminal #10-#12 wire, #10 bolt	101643
	6	Spade Terminal #10-#12 wire, #6 bolt	101644
	4	Quik Disconnect #10-#12 wire, 1/4" tab	101645
	4	Spade Terminal #18-#22 wire, #6 bolt	101646
3	4	2200uf, 25v Capacitor	100375
4	1	Plug MATE-N-LOK 10 Circuit	101635
	1	Receptacle MATE-N-LOK 10 Circuit	101636
	12	Pin MATE-N-LOK	101639
	12	Socket MATE-N-LOK	101640

Mag	Quantity	Component	MITS Stock Number
	4	Commoning Tab	101641
	1	Plug MATE-N-LOK 2 Circuit	101637
	1	Receptacle MATE-N-LOK 2 Circuit	101638
5	1	6-32 x 1/2" Screw	100918
	19	6-32 x 3/8" Screw	100925
	5	6-32 x 5/8" Screw	100916
	9	6-32 x 9/16" Screw	100956
	4	6-32 x 3/4" Screw	100935
	1	8-32 x 1" Screw	100927
	4	10-32 x 1/2" Screw	100958
	13	6-32 x 1/4" Screw	100917
	19	6-32 Nut	100933
	4	#6 Snap-On Nut (with fan)	------
	1	8-32 Nut	100929
	4	10-32 Nut	100962
	2	6-32 x 3/8" Screw (Nylon)	100959
	2	6-32 Nut (Nylon)	100960
	17	#6 Lockwasher	100942
	1	#8 Lockwasher	100945
	4	#10 Lockwasher	100963
	5	3/4" 6-32 Spacer (Threaded)	101626
	4	#6 Flat washer	100943
	1	#8 Flat washer	100939
	4	#10 Flat washer	100961
	4	3/8" 6-32 Threaded Spacer	101863

Bag	Quantity	Component	MITS Stock Number
MISC.	1	95000uf 15v DC with Clamp	100391
	1	PC Board	100202
	1	6Ft. 3-wire Power Cord	101742
	1	Fan	101869
	20'	#18 Stranded Wire	103090
	8'	#12 Stranded Wire	103092
	2'	Grn. Braid	101801
	4	3/16" Cable Clamps	103023
	20	Tie Wrap	103037
	6"	Heat Shrink	103073
Separate Box	1	Transformer	102616

8800b Case and Misc.

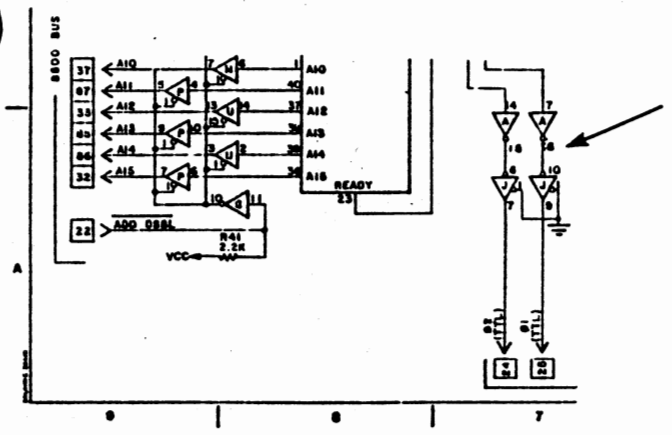
Quantity	Component	MITS Stock Number
1	Case	100505
1	Back Panel	100545
1	Dress Panel	100541
1	Main Board	100193
2	Card Rail	101603
1	Manual (Altair 8800b Documentation)	101537
1	Micro Processor Dictionary and Guide	101539
1	Intel 8080 Manual	101585

17. Page 3-63, Figure 3-14, CPU Schematic.

An output pin at IC A is labelled incorrectly as pin 7.

CHANGE TO:

From the 8080 the Ø1 signal enters NAND gate A at pin 7 and passes from pin 6 of IC A to IC J at pin 10.



10. Page 5-60, Bridge Rectifier Installation, Steps 2 and 4:

2. Cut two 4-inch lengths of 12-10 gauge wire . . .

CHANGE TO:

2. Cut two 5-inch lengths of 12-10 gauge wire . . .

- - - - -

4. Slip the A size terminal ends onto the bridge rectifier terminals as shown in Figure 5-51. Attach the two 4-inch wires . . .

CHANGE TO:

4. Slip the A size terminal ends onto the bridge rectifier terminals as shown in Figure 5-51. Attach the two 5-inch wires . . .

11. Page 5-63, Secondary Wiring, Steps 1, 2 and 4:

1. Orient the transformer with the secondary side (four black wires) . . .

CHANGE TO:

1. Orient the transformer with the secondary side (four large wires) . . .

- - - - -

2. Attach an E size terminal end with heat shrink tubing (see Paragraph 5-58) to each of the four black transformer wires and label the wires 16-17-18-19, beginning with the top wire (Figure 5-56).

CHANGE TO:

2. Attach an E size terminal end with heat shrink tubing (see Paragraph 5-58) to each of the four large transformer wires and label the wires 16-17-18-19 as shown in Figure 5-56.

- - - - -

4. Bend each of the E size terminal ends at a right angle as shown in Figure 5-56. Mount the four black wires . . .

CHANGE TO:

4. Bend each of the E size terminal ends at a right angle as shown in Figure 5-56. Mount the four large wires . . .

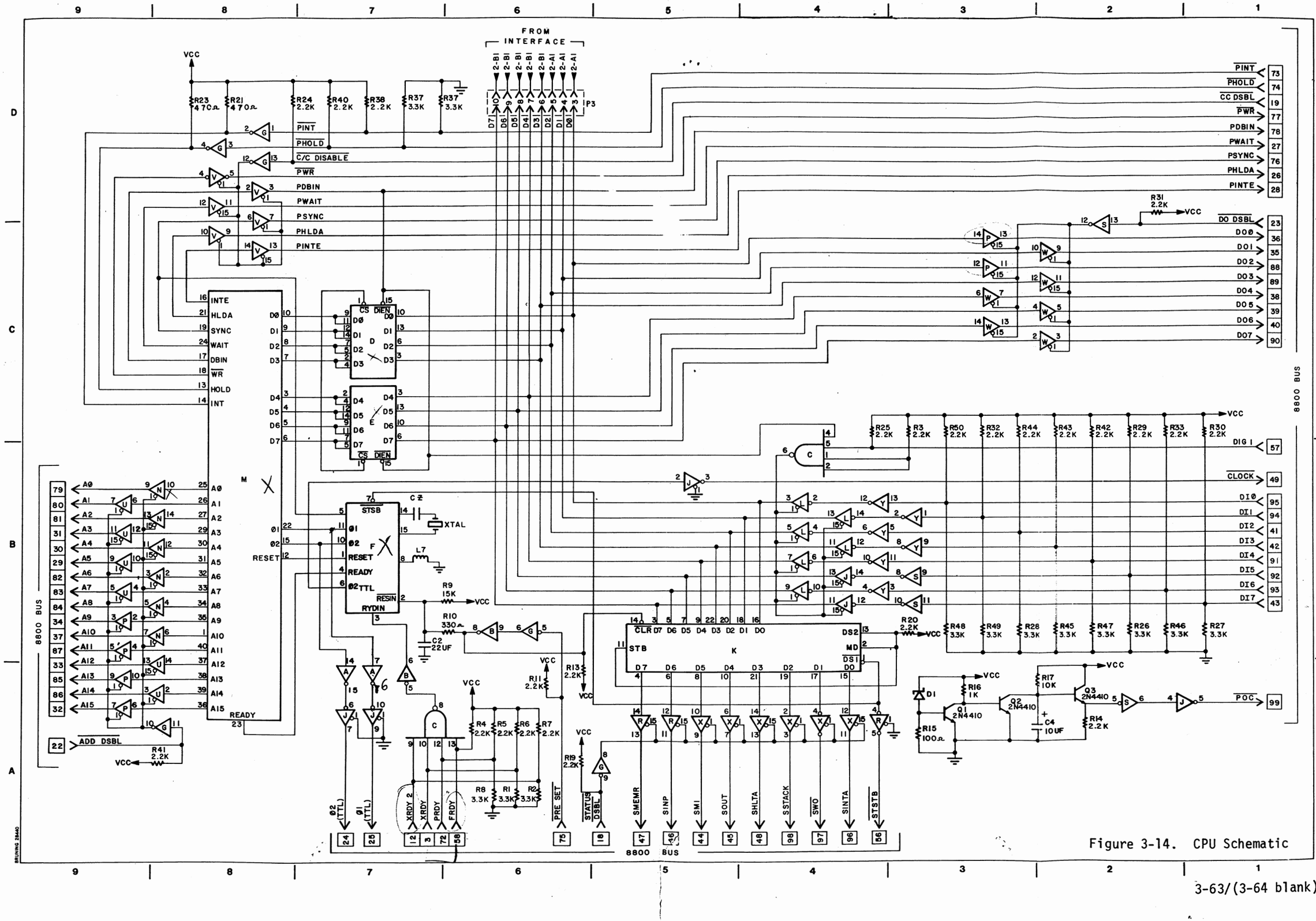


Figure 3-14. CPU Schematic

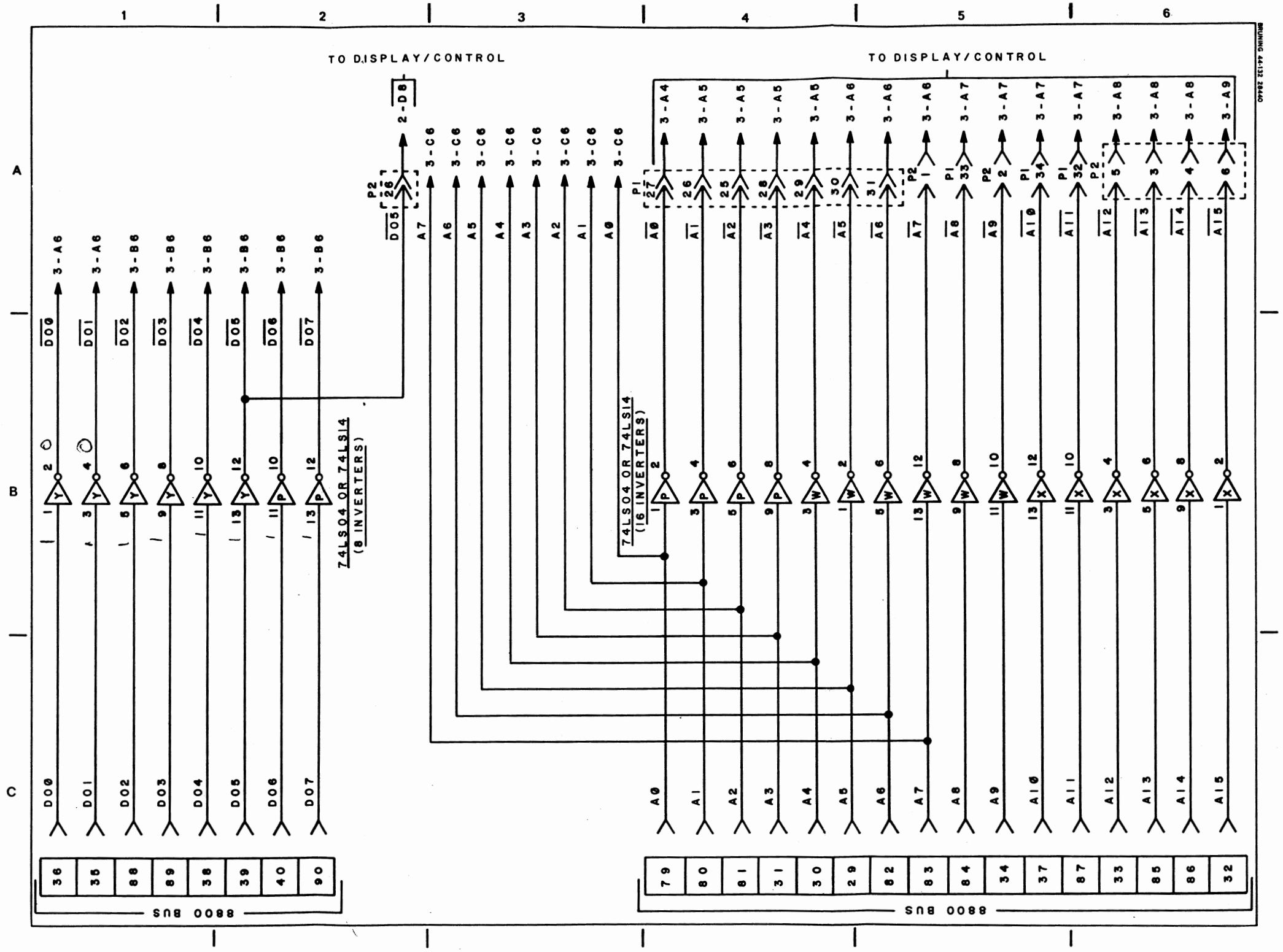


Figure 3-15. Interface Schematic (sheet 1 of 3)

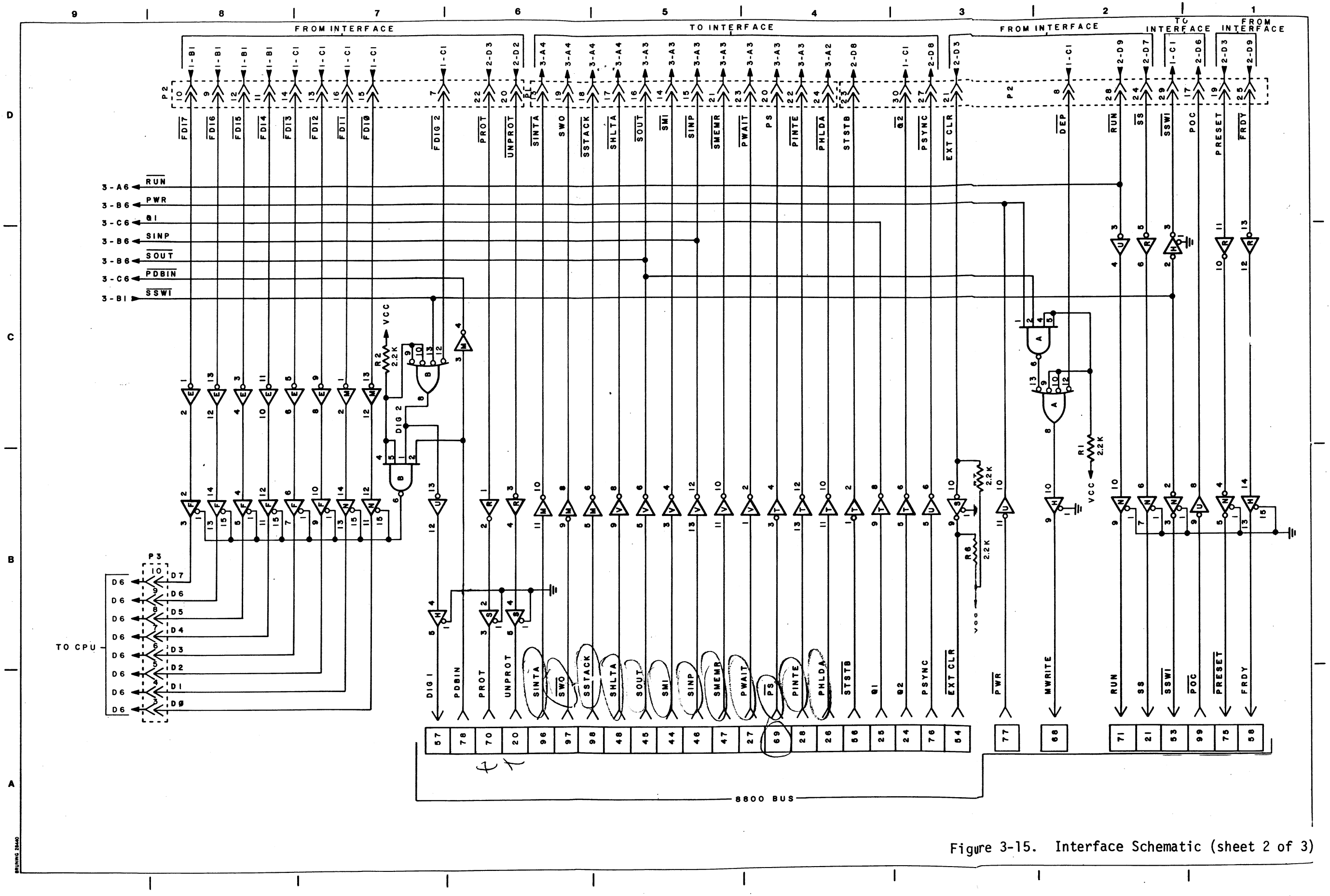


Figure 3-15. Interface Schematic (sheet 2 of 3)

POWER CONNECTIONS				
QTY	TYPE	VCC	GND	OTHER
1	7400 OR 74LS00	14	7	
1	7402 OR 74LS02	14	7	
1	7404 OR 74LS04	14	7	
1	7410 OR 74LS10	14	7	
1	74LS13	14	7	
1	74LS14	14	7	
1	7420	14	7	
1	8212	24	12	

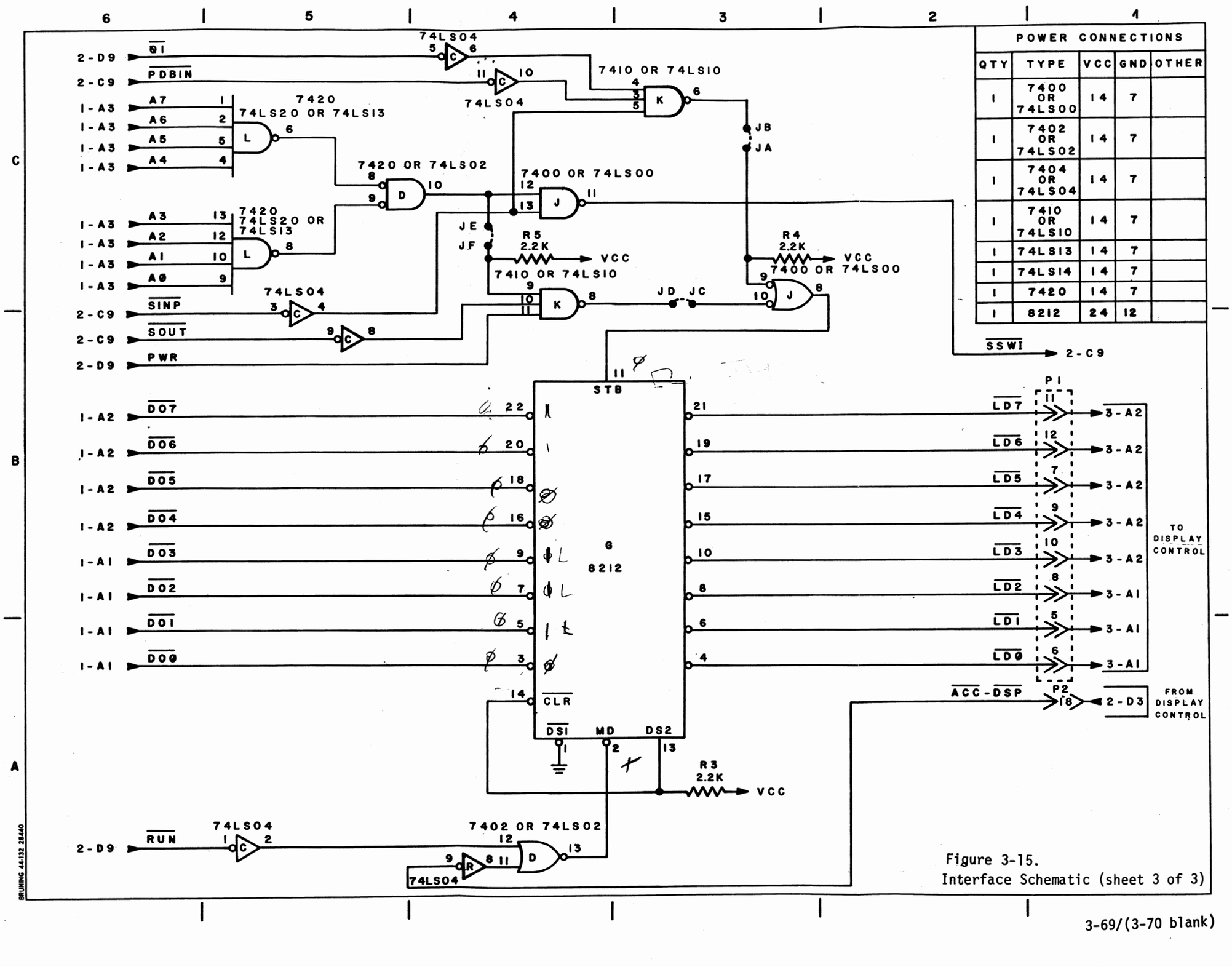


Figure 3-15.
Interface Schematic (sheet 3 of 3)

POWER CONNECTIONS				
IC	TYPE	VCC	GND	OTHER
Z	7400 OR 74LS00	14	7	
J,V	7410 OR 74LS10	14	7	
E1	74LS04	14	7	
U,W,Y	7405	14	7	
P	7493	5	10	4,6,7,13=NC
R	8T98	16	8	
B1,P	8212	24	12	
G	1702A	12,13,15,22,23	—	24,16=-9V
N	74L30 OR 74LS30	14	7	
L, X	4040	16	8	
SI	4009 OR 4049	1,16	8	13=NC

Figure 3-16.
Display/Control Schematic (sheet 1 of 3)

POWER CONNECTIONS				
QTY	TYPE	VCC	GND	OTHER
1	7400	14	7	
1	7404	14	7	
2	7405	14	7	
2	7410	14	7	
1	7430	14	7	
2	74LS74	14	7	
8	74LS175	16	8	
1	8T97	16	8	

Figure 3-16. Display/Control Schematic (sheet 2 of 3)

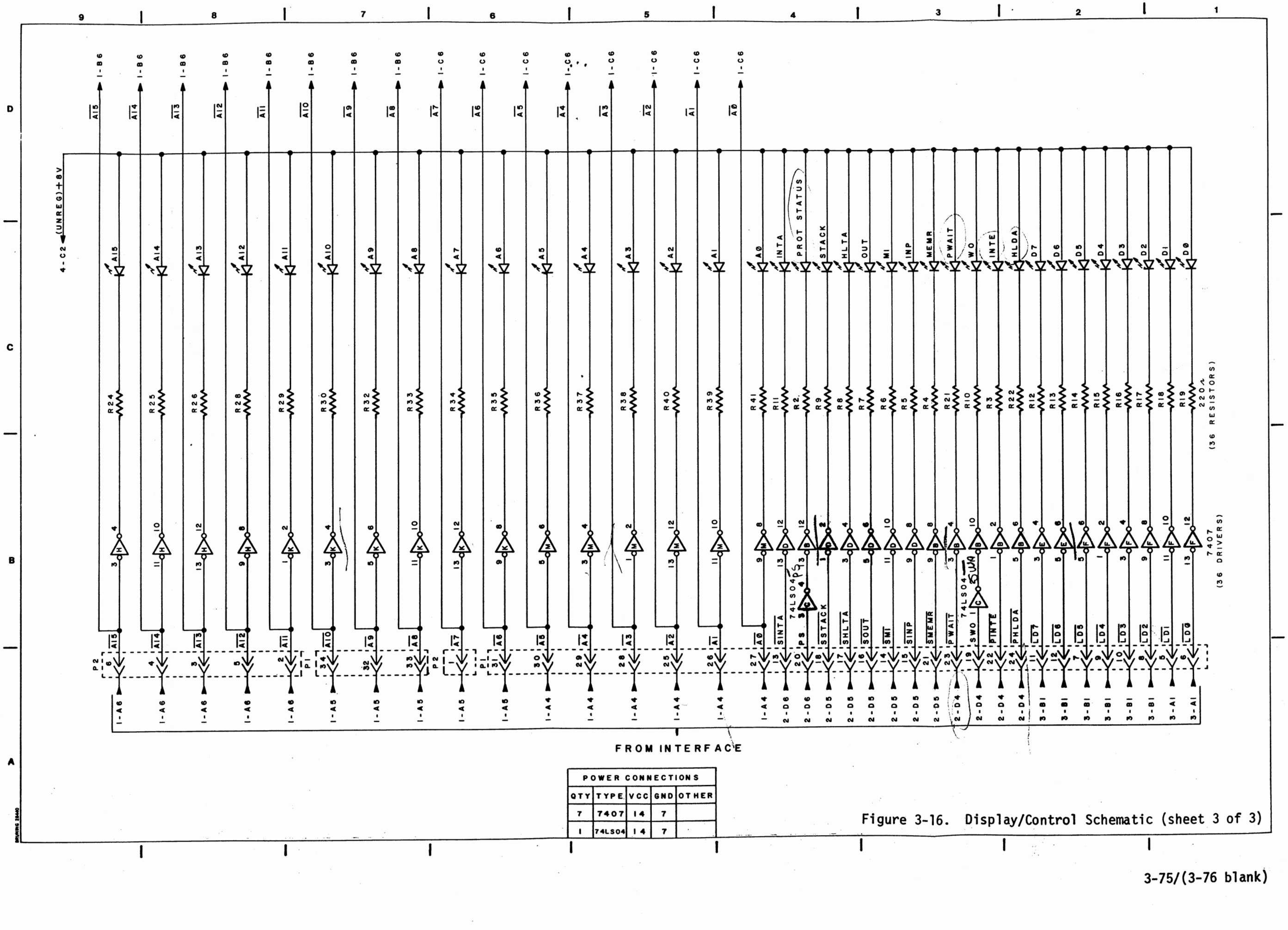


Figure 3-16. Display/Control Schematic (sheet 3 of 3)

880-101
COMPUTER CPU & BUFFERS

8080
I C A

+5V
+12V
-5V
GND
RESET
INT
HOLD
INTE
READY
WAIT
HLDA
DBIN
SYNC
WR
Φ1
Φ2
RUN
SS
SSW DSB
SINTA
SWO
SSTACK
SHLTA
SOUT
SM1
SINP
SMEMR
STATUS DSBL
CLOC (2 MHz)
PSYNC
PDBIN
C/C DSBL
PWAIT
PWR
PHLDA
PINTE
PRDY
XRDY
PHOLD
PINT
PRESET
ADDR DSBL
DO DSBL
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15
D0 D1 D2 D3 D4 D5 D6 D7
DI0 DI1 DI2 DI3 DI4 DI5 DI6 DI7
DO0 DO1 DO2 DO3 DO4 DO5 DO6 DO7
POC
TO DISPLAY/CONTROL BD
8212
CLOCK ICP 7404 (4 GATES)
ICQ 74123
ICA 8080
ICB 1/2 7474
ICC 1/2 7474
ICD 8212
ICE 8T98
ICF 8T98
ICG 8T98
ICH 8T98
ICI 8T98
ICJ 8T98
ICK 8T98
ICL 8T98
ICM 8T98
ICN 8T98
ICO 8T98
ICP 8T98
ICQ 74123
ICR 8T98
R1 R2 R3 R4 R5 R6 R7 R8 R9 R10 R11 R12 R13 R14 R15 R16 R17 R18 R19 R20 R21 R22 R23 R24 R25 R26 R27 R28 R29 R30 R32 R33 R34 R35 R36 R44
47K
1K
20K
470
.1MF
C1
Q1 CS9410
+12V
GND
NC
Q-4
Q-12
Q-13
(2MHz) P-10
SS 6
RUN 5
HLDA 3
DBIN 2
HOLD 13
INT 14
RESET 12
SYNC 18
DBIN 17
WAIT 24
WR 18
HLDA 21
INTE 10
READY 23
Φ1 22
Φ2 15
A0 25
A1 26
A2 27
A3 29
A4 30
A5 31
A6 32
A7 33
A8 34
A9 35
A10 1
A11 40
A12 37
A13 38
A14 39
A15 36
D0 10
D1 9
D2 8
D3 7
D4 3
D5 4
D6 5
D7 6
DI0 14
DI1 12
DI2 41
DI3 42
DI4 91
DI5 92
DI6 93
DI7 43
DO0 36
DO1 35
DO2 88
DO3 89
DO4 38
DO5 39
DO6 40
DO7 90
POC 99
A0 79
A1 80
A2 81
A3 31
A4 30
A5 29
A6 82
A7 83
A8 84
A9 34
A10 37
A11 87
A12 33
A13 85
A14 86
A15 32
SINTA 96
SWO 97
SSTACK 98
SHLTA 48
SOUT 45
SM1 44
SINP 46
SMEMR 47
STATUS DSBL 18
CLOC (2 MHz) 49
PSYNC 76
PDBIN 78
C/C DSBL 19
PWAIT 27
PWR 17
PHLDA 26
PINTE 72
PRDY
XRDY
3
PHOLD 74
PINT 73
PRESET 75
Φ1 25
Φ2 24
ADDR DSBL 22
DO DSBL 23
SS 21
RUN 71