1981 Microcomputer Components Data Book

ADDENDUM AND

Document Change Notice

Zilog

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This Document Change Notice provides changes for the publication specified above as well as for the stand-alone product specifications on each product. These changes will remain in effect unless specifically amended by another DCN or superceded by a publication revision. Please file this DCN at the back of specified documents to provide a record of changes.

Note: The first page cited refers to the 1981 Data Book. The second page, cited in parentheses, refers to the individual product specification printed stand-alone in cases where the change is applicable to both.

Page iii

Delete the final paragraph.

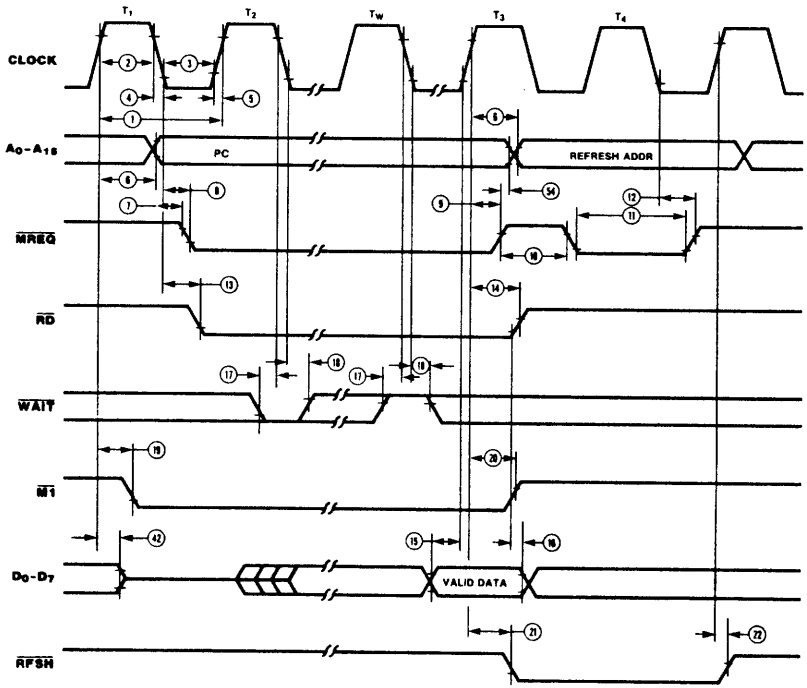
Page 3

Delete Z80 CPU from right margin.

Z8400 Z80® CPU
Product Specification

Page 18
(Page 14)

In Figure 5, delete #45 and insert #54 in its place.



NOTE: T_W-Wait cycle added when necessary for slow ancilliary devices.

Figure 5. Instruction Opcode Fetch

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In Figure 6, "Memory Read or Write Cycle," extend parameter 45 as illustrated in the corrected version of the art that follows.

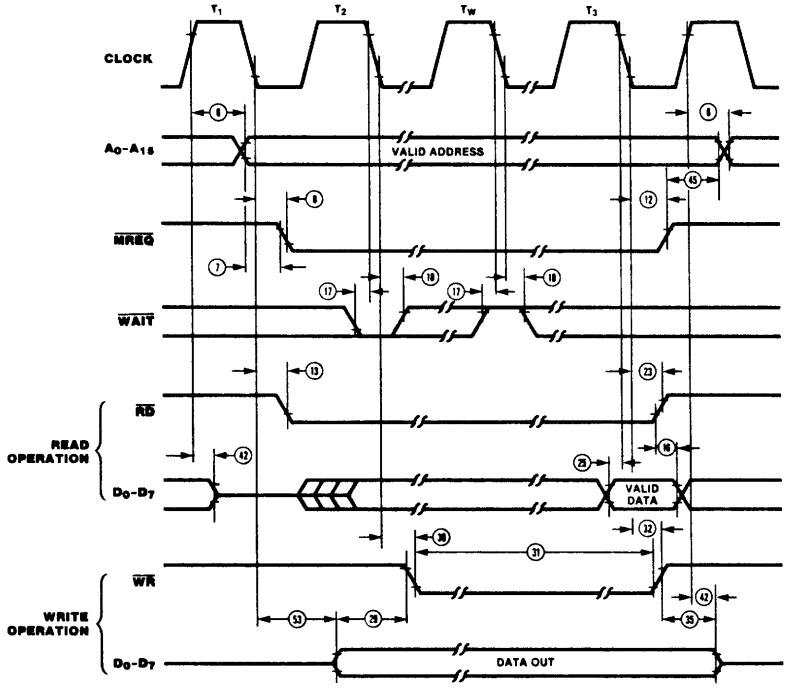

Figure 6. Memory Read or Write Cycles

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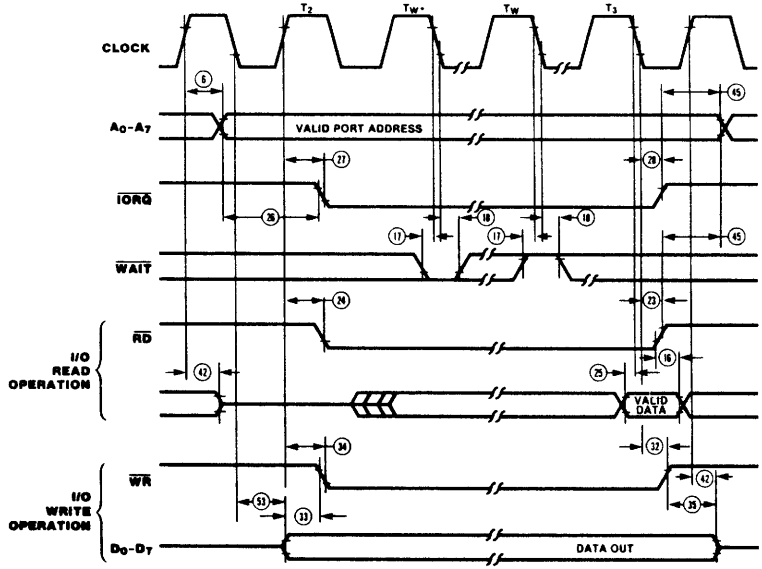
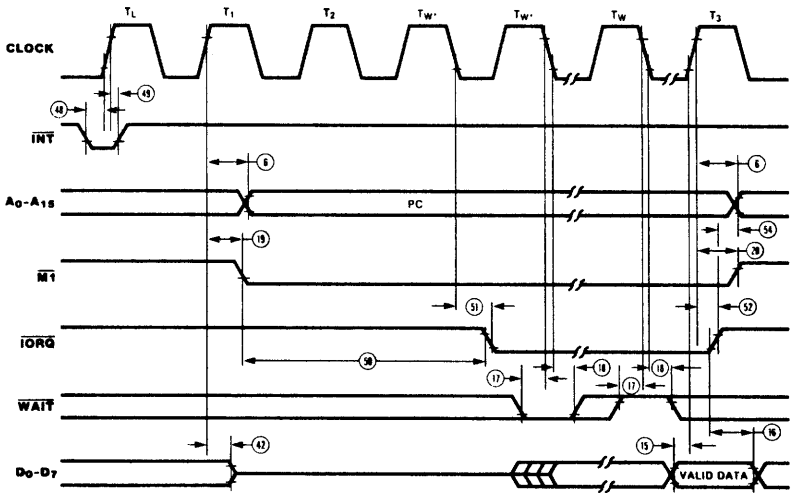
In Figure 7, "Input or Output Cycles," the diagram is incorrect for the ADDRESS BUS, the INPUT/OUTPUT REQUEST, and WAIT lines. A corrected version of the art follows.



NOTE: T_{W}* = One Wait cycle automatically inserted by CPU.

Figure 7. Input or Output Cycles

In Figure 8, "Interrupt Request/Acknowledge Cycle," the diagram is incorrect for the ADDRESS BUS, MACHINE CYCLE ONE and INPUT/OUTPUT REQUEST lines. A corrected version of the art follows.



NOTE: 1) T_L = Last state of previous instruction. 2) Two Wait cycles automatically inserted by CPU(*).

Figure 8. Interrupt Request/Acknowledge Cycle

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Make the following changes in **AC CHARACTERISTICS:**

1) In parameter 45 change "Address Stable after" to "to Address Hold Time."
2) Add the following line of characteristics:

Number	Symbol	Parameter	Z80 CPU min.	Z80A CPU min.	Z80B CPU min.
54	TdCTr(A)	$\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$ to Address Hold Time	0	0	0

3) Add the footnote:

** All timings assume equal loading on pins with 100 pF.

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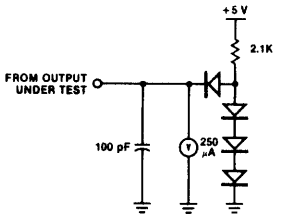
(Page 21)

In **Standard Test Conditions** the art is incorrect. A corrected version follows.



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In Figure 13, "Read Register Bit Functions," add the following note to Read Register 2*:

*(Channel B only)

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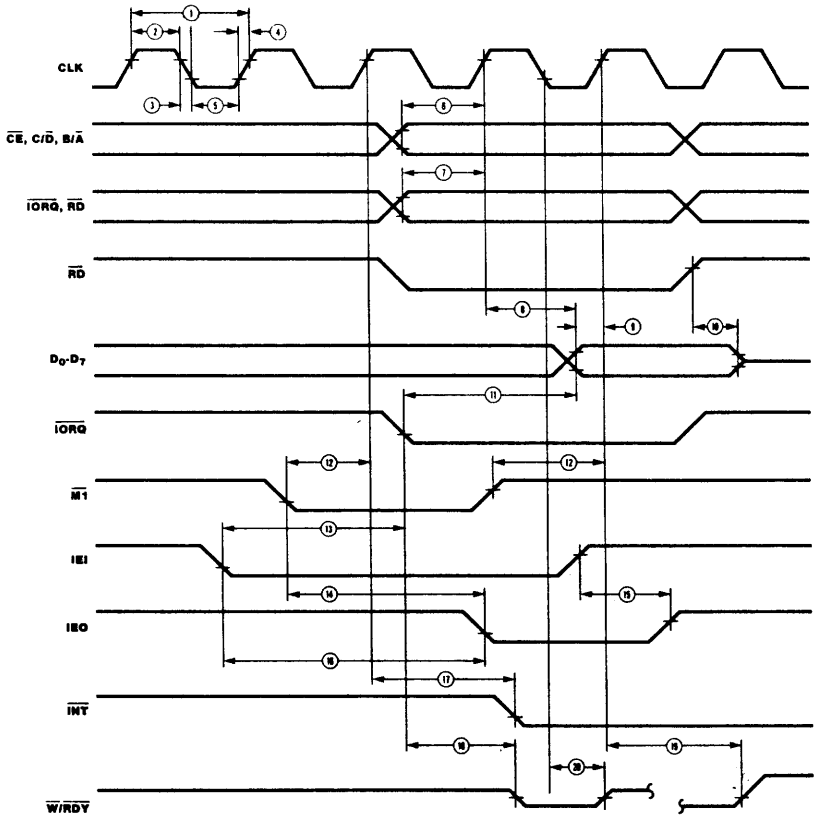
(Page 14)

To the diagram of AC Electrical Characteristics add W/RDY, WAIT/READY, as a label to the last signal line. A corrected version of the art for that line follows.



The parameter of number 18 should read:

$\overline{IORQ}$ ↓ or $\overline{CE}$ ↓ to $\overline{W}/\overline{RDY}$ ↓ Delay (Wait Mode).

The parameter of number 19 should read:

Clock ↑ to $\overline{W}/\overline{RDY}$ ↑ Delay (Ready Mode).

Z8470 Z80 DART
Product Specification

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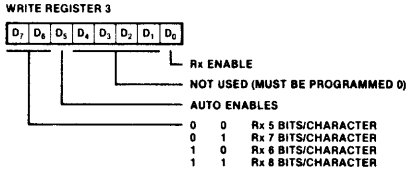
In the **Z80 Dart Read and Write Registers,** Write Register 3, the label for bits D_4-D_3-D_2-D_1 should read:

Not Used (Must Be Programmed 0)



Z8001/2 Z8000™ CPU
Product Specification

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(Page 1)

The final **Feature** should read:

4, 6, and 10 MHz clock rate.

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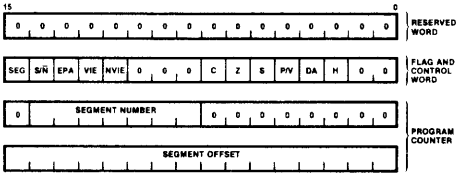
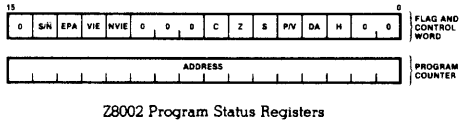
(Page 3)

In **Program Status Information,** Figure 5, "Z8000 CPU Special Registers" the Flag and Control Word art is incorrectly labeled in bit 13. It should read EPA. A corrected version of the art follows.



Z8001 Program Status Registers



Z8002 Program Status Registers

Figure 5. Z8000 CPU Special Registers

In **Interrupt and Trap Structure,** the first sentence of the second paragraph should read:

The CPU supports three types of interrupts (non-maskable, vectored and non-vectored) and four traps (system call, Extended Processing Architecture instruction, privileged instructions and segmentation trap).

In **Interrupt and Trap Structure** the first sentence of the third paragraph should read:

The remaining traps occur when instructions limited to the system mode are used in the normal mode, or as a result of the System Call instruction, or for an EPA instruction.

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Change Z8010 MMU in right margin to Z8001/2 CPU.

In **Reset** delete "ST_0-ST_3 and" from the third entry.

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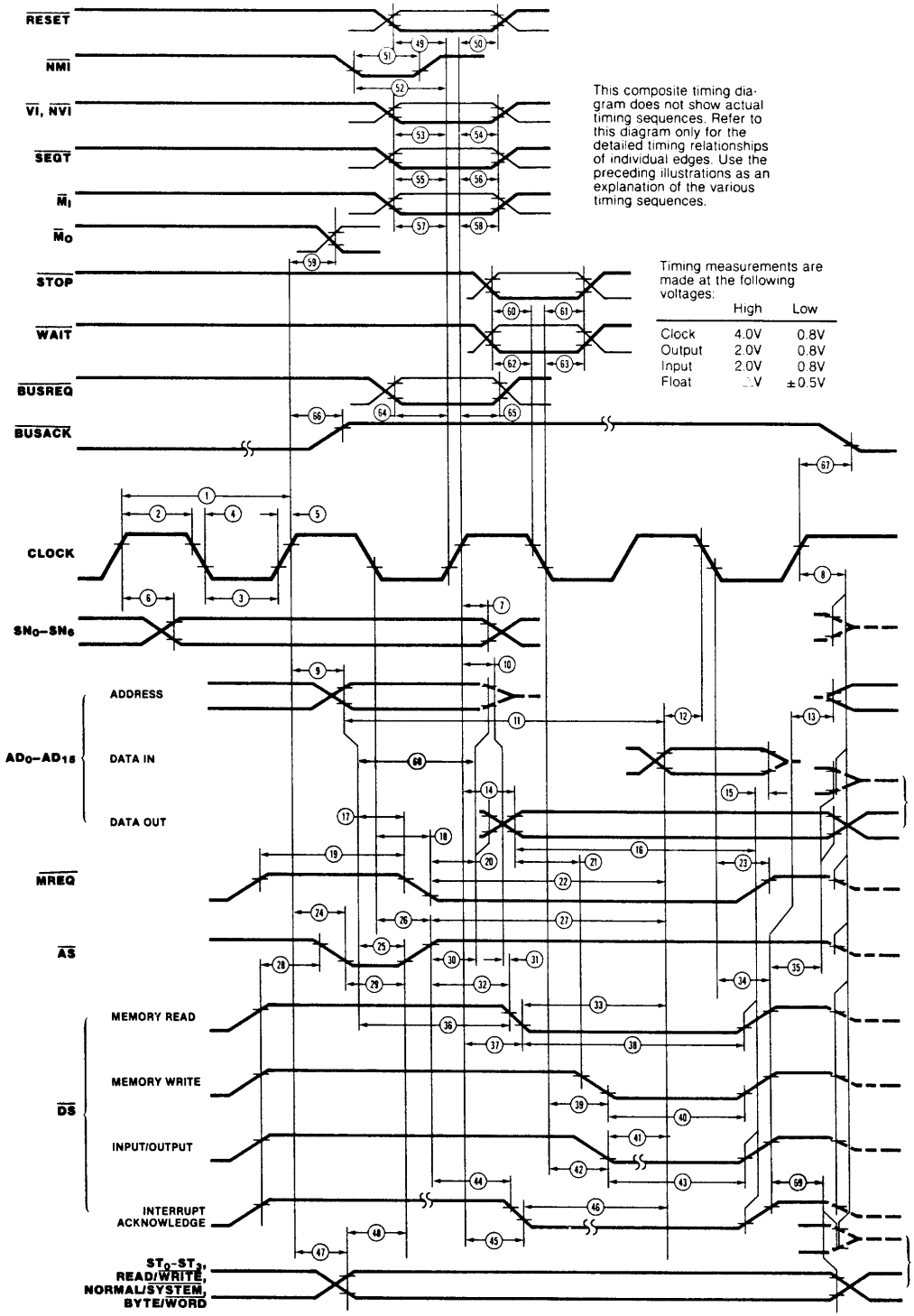
(Page 24)

To the **Composite AC Timing Diagram** add the parameters 68 and 69 as illustrated in the following corrected art.



A revised version of the **AC Timing Table** follows.

(Page 129)			Z8001/Z8002 4MHz		Z8001A/Z8002A 6MHz		Z8001B/Z8002B 10MHz	
No.	**Symbol**	**Parameter**	**Min(ns)**	**Max(ns)**	**Min(ns)**	**Max(ns)**	**Min(ns)**	**Max(ns)**
1	TcC	Clock Cycle Time	250	2000	165	2000	100	2000
2	TwCh	Clock Width (High)	105	2000	70	2000	40	
3	TwCl	Clock Width (Low)	105	2000	70	2000	40	
4	TfC	Clock Fall Time		20		10		10
5	TrC	Clock Rise Time		20		15		10
6	TdC(SNv)	Clock ↑ to Segment Number Valid (50 pF load)		130		110		70
7	TdC(SNn)	Clock ↑ to Segment Number Not Valid	20		10		5	
8	TdC(Bz)	Clock ↑ to Bus Float		65		55		40
9	TdC(A)	Clock ↑ to Address Valid		100		75		50
10	TdC(Az)	Clock ↑ to Address Float		65		55		40
11	TdA(DR)	Address Valid to Read Data Required Valid		475*		305*		180*
12	TsDR(C)	Read Data to Clock ↓ Setup Time	30		20		10	
13	TdDS(A)	$\overline{DS}$ ↑ to Address Active	80*		45*		20*	
14	TdC(DW)	Clock ↑ to Write Data Valid		100		75		50
15	ThDR(DS)	Read Data to $\overline{DS}$ ↑ Hold Time	0		0		0	
16	TdDW(DS)	Write Data Valid to $\overline{DS}$ ↑ Delay	295*		195*		110*	
17	TdA(MR)	Address Valid to $\overline{MREQ}$ ↓ Delay	55*		35*		20*	
18	TdC(MR)	Clock ↓ to $\overline{MREQ}$ ↓ Delay		80		70		40
19	TwMRh	$\overline{MREQ}$ Width (High)	210*		135*		80*	
20	TdMR(A)	$\overline{MREQ}$ ↓ to Address Not Active	70*		35*		20*	
21	TdDW(DSW)	Write Data Valid to $\overline{DS}$ ↓ (Write) Delay	55*		35*		15*	
22	TdMR(DR)	$\overline{MREQ}$ ↓ to Read Data Required Valid	375*		230*		140*	
23	TdC(MR)	Clock ↓ $\overline{MREQ}$ ↑ Delay		80		60		45
24	TdC(ASf)	Clock ↑ to $\overline{AS}$ ↓ Delay		80		60		40
25	TdA(AS)	Address Valid to $\overline{AS}$ ↑ Delay	55*		35*		20*	
26	TdC(ASr)	Clock ↓ to $\overline{AS}$ ↑ Delay		90		80		40
27	TdAS(DR)	$\overline{AS}$ ↑ to Read Data Required Valid	360*		220*		140*	
28	TdDS(AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay	70*		35*		15*	
29	TwAS	$\overline{AS}$ Width (Low)	85*		55*		30*	
30	TdAS(A)	$\overline{AS}$ ↑ to Address Not Active Delay	70*		45*		20*	
31	TdAz(DSR)	Address Float to $\overline{DS}$ (Read) ↓ Delay	0		0		0	
32	TdAS(DSR)	$\overline{AS}$ ↑ to $\overline{DS}$ (Read) ↓ Delay	80*		55*		30*	
33	TdDSR(DR)	$\overline{DS}$ (Read) ↓ to Read Data Required Valid	205*		130*		70*	
34	TdC(DSr)	Clock ↓ to $\overline{DS}$ ↑ Delay		70		65		45
35	TdDS(DW)	$\overline{DS}$ ↑ to Write Data Not Valid	75*		45*		25*	
36	TdA(DSR)	Address Valid to $\overline{DS}$ (Read) ↓ Delay	180*		110*		65*	
37	TdC(DSR)	Clock ↑ to $\overline{DS}$ (Read) ↓ Delay		120		85		60
38	TwDSR	$\overline{DS}$ (Read) Width (Low)	275*		185*		110*	
39	TdC(DSW)	Clock ↓ to $\overline{DS}$ (Write) ↓ Delay		95		80		60
40	TwDSW	$\overline{DS}$ (Write) Width (Low)	185*		110*		75*	
41	TdDSI(DR)	$\overline{DS}$ (I/O) ↓ to Read Data Required Valid	330*		210*		120*	
42	TdC(DSf)	Clock ↓ to $\overline{DS}$ (I/O) ↓ Delay		120		90		60
43	TwDS	$\overline{DS}$ (I/O) Width (Low)	410*		255*		160*	
44	TdAS(DSA)	$\overline{AS}$ ↑ to $\overline{DS}$ (Acknowledge) ↓ Delay	1065*		690*		410*	
45	TdC(DSA)	Clock ↑ to $\overline{DS}$ (Acknowledge) ↓ Delay		120		85		65
46	TdDSA(DR)	$\overline{DS}$ (Acknowledge) ↓ to Read Data Required Delay	455*		295*		165*	
47	TdC(S)	Clock ↑ to Status Valid Delay		110		85		60
48	TdS(AS)	Status Valid to $\overline{AS}$ ↑ Delay	50*		30*		10*	
49	TsR(C)	$\overline{RESET}$ to Clock ↑ Setup Time	180		70		50	
50	ThR(C)	$\overline{RESET}$ to Clock ↑ Hold Time	0		0		0	
51	TwNMI	$\overline{NMI}$ Width (Low)	100		70		50	
52	TsNMI(C)	$\overline{NMI}$ to Clock ↑ Setup Time	140		70		50	
53	TsVI(C)	$\overline{VI}$, $\overline{NVI}$ to Clock ↑ Setup Time	110		50		40	
54	ThVI(C)	$\overline{VI}$, $\overline{NVI}$ to Clock ↑ Hold Time	20		20		10	
55	TsSGT(C)	$\overline{SEGT}$ to Clock ↑ Setup Time	70		55		40	
56	ThSGT(C)	$\overline{SEGT}$ to Clock ↑ Hold Time	0		0		0	
57	TsMI(C)	$\overline{MI}$ to Clock ↑ Setup Time	180		110		80	
58	ThMI(C)	$\overline{MI}$ to Clock ↑ Hold Time	0		0		0	
59	TdC(MO)	Clock ↑ to MO Delay		120		85		70
60	TsSTP(C)	$\overline{STOP}$ to Clock ↓ Setup Time	140		80		50	

*Clock-cycle-time-dependent characteristics. See table on following page.

No.	Symbol	Parameter	Z8001/Z8002 4MHz Min(ns)	Z8001/Z8002 4MHz Max(ns)	Z8001A/Z8002A 6MHz Min(ns)	Z8001A/Z8002A 6MHz Max(ns)	Z8001B/Z8002B 10MHz Min(ns)	Z8001B/Z8002B 10MHz Max(ns)
61	ThSTP(C)	$\overline{STOP}$ to Clock ↓ Hold Time	0		0		0	
62	TsW(C)	$\overline{WAIT}$ to Clock ↓ Setup Time	50		30		20	
63	ThW(C)	$\overline{WAIT}$ to Clock ↓ Hold Time	10		10		5	
64	TsBRQ(C)	$\overline{BUSREQ}$ to Clock ↑ Setup Time	90		80		60	
65	ThBRQ(C)	$\overline{BUSREQ}$ to Clock ↑ Hold Time	10		10		5	
66	TdC(BAKr)	Clock ↑ to $\overline{BUSACK}$ ↑ Delay		100		75		60
67	TdC(BAKf)	Clock ↑ to $\overline{BUSACK}$ ↓ Delay		100		75		60
68	TwA	Address Valid Width	150*		95*		50*	
69	TdDS(S)	$\overline{DS}$ ↑ to STATUS Not Valid	80*		55*		30*	

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A revised version of the **Clock-Cycle-Time-Dependent Characteristics** follows.

Clock-Cycle-Time-Dependent Characteristics (Page 130)

Number	Symbol	Z8001/Z8002 Equation	Z8001A/Z8002A Equation	Z8001B/Z8002B Equation
11	TdA(DR)	2TcC + TwCh - 130 ns	2TcC + TwCh - 95 ns	2TcC + TwCh - 60 ns
13	TdDS(A)	TwCl - 25 ns	TWCl - 25 ns	TwCl - 20 ns
16	TdDW(DS)	TcC + TwCh - 60 ns	TcC + TwCh - 40 ns	TcC + TwCh - 30 ns
17	TdA(MR)	TwCh - 50 ns	TwCh - 35 ns	TwCh - 20 ns
19	TwMRh	TcC - 40 ns	TcC - 30 ns	TcC - 20 ns
20	TdMR(A)	TwCl - 35 ns	TwCl - 35 ns	TwCl - 20 ns
21	TdDW(DSW)	TwCh - 50 ns	TwCh - 35 ns	TwCh - 25 ns
22	TdMR(DR)	2TcC - 130 ns	2TcC - 100 ns	2TcC - 60 ns
25	TdA(AS)	TwCh - 50 ns	TwCh - 35 ns	TwCh - 20 ns
27	TdAS(DR)	2TcC - 140 ns	2TcC - 110 ns	2TcC - 60 ns
28	TdDS(AS)	TwCl - 35 ns	TwCl - 35 ns	TwCl - 25 ns
29	TwAS	TwCh - 20 ns	TwCh - 15 ns	TwCh - 10 ns
30	TdAS(A)	TwCl - 35 ns	TwCl - 25 ns	TwCl - 20 ns
32	TdAS(DSR)	TwCl - 25 ns	TwCl - 15 ns	TwCl - 10 ns
33	TdDSR(DR)	TcC + TwCh - 150 ns	TcC + TwCh - 105 ns	TcC + TwCh - 70 ns
35	TdDS(DW)	TwCl - 30 ns	TwCl - 25 ns	TwCl - 15 ns
36	TdA(DSR)	TcC - 70 ns	TcC - 55 ns	TcC - 35 ns
38	TwDSR	TcC + TwCh - 80 ns	TcC + TwCh - 50 ns	TcC + TwCh - 30 ns
40	TwDSW	TcC - 65 ns	TcC - 55 ns	TcC - 25 ns
41	TdDSI(DR)	2TcC - 170 ns	2TcC - 120 ns	2TcC - 80 ns
43	TwDS	2TcC - 90 ns	2TcC - 75 ns	2TcC - 40 ns
44	TdAS(DSA)	4TcC + TwCl - 40 ns	4TcC + TwCl - 40 ns	4TcC + TwCl - 30 ns
46	TdDSA(DR)	2TcC + TwCh - 150 ns	2TcC + TwCh - 105 ns	2TcC + TwCh - 75 ns
48	TdS(AS)	TwCh - 55 ns	TwCh - 40 ns	TwCh - 30 ns
68	TwA	TcC - 90 ns	TcC - 70 ns	TcC - 50 ns
69	TdDS(S)	TwCl - 25 ns	TwCl - 15 ns	TwCl - 10 ns

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In **Test Conditions,** the first sentence of the note following the diagram should read:

> All ac parameters assume a total load capacitance (including parasitic capacitances) of 100 pF max, except for parameter 6 (50 pF max).

In **Ordering Information** the Description of all Z8001 and Z8001A Product Numbers should read:

> CPU (segmented, 48-pin).

In the Notes to **Ordering Information** change CM = -55°C to +125°C to read:

> MB = -55°C to +125°C.

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(Page 1)

In Figure 2, "Pin Assignments," $\overline{DS}$ and $\overline{AS}$ were reversed. A corrected version of the art follows.

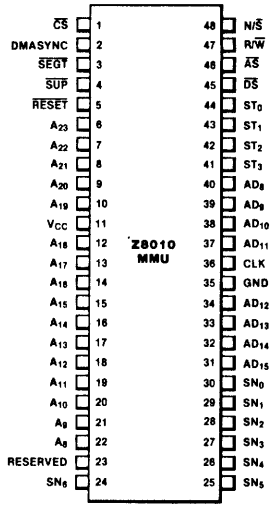

Figure 2. Pin Assignments

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(Page 6)

In **Segment Trap and Acknowledge** the first sentence of the third paragraph should read:

> Following the acknowledge cycle the CPU automatically pushes the Program Status (PC and FCW) onto the system stack and loads another Program Status from the Program Status Area.

The third sentence of the third paragraph should read:

> If the store creates a write warning condition, a Segment Trap Request is generated and is serviced at the end of the program status swap.

The fifth sentence of the third paragraph should read:

> If a violation rather than a write warning occurs during the program status swap, the FATL flag is set rather than the SWW flag.

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(Page 7)

In **DMA Operation** the third paragraph, the first three sentences should read as follows:

> At the start of a DMA cycle, DMASYNC must go Low for at least two clock cycles, indicating to the MMU the beginning of a DMA cycle. A Low DMASYNC inhibits the MMU from using an indeterminate segment number on lines SN_0-SN_6. When the DMA logical memory address is valid, the DMASYNC line must be High before a rising edge of Clock and the MMU then performs its address translation and access protection functions.

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(Page 12)

The DMASYC Pin Description should read as follows:

> DMA/Segment Number Synchronization Strobe (input, active High). A Low on this line indicates that the segment number lines are 3-state; a High indicates that the segment number is valid. It must always be High during CPU cycles. If a DMA device does not use the MMU for address translation, the BUSACK signal from the CPU may be used as an input to DMASYNC.

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(Page 13)

Add the following note to the **DC Characteristics:**

> NOTE: The on-chip back-bias voltage generator takes approximately 20 us to pump the back-bias voltage to -2.5V after the power has been turned on. The performance of the Z8010 Z-MMU is not guaranteed during this period.

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(Page 14)

Add the following note to AC Characteristics:

> ** Timing measurements are made at the following voltages:

	High	Low
Clock	4.0V	0.8V
Output	2.0V	0.8V
Input	2.0V	0.8V
Float	Δ V	$\pm$0.5V

Z8030 Z8000 Z-SCC
Product Specification

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In **Interrupts** add the following to the end of the fifth paragraph:

> Two or three $\overline{AS}$ rising edges are required from the time an interrupt condition occurs until $\overline{INT}$ is activated.

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(Page 10)

Add the following to the end of the first paragraph of **Programming:**

> In the shift right mode the channel select A/$\overline{B}$ is taken from AD_0 and the state of AD_5 is ignored. In the shift left mode A/$\overline{B}$ is taken from AD_5 and the state of AD_0 is ignored. AD_7 and AD_6 are always ignored as address bits and the register address itself occupies AD_4-AD_1.

Pages 164-68
(Pages 16-20)

The timing tables on these pages have been revised and expanded to include 6 MHz timing. Corrected versions of these tables follow.

Z-SCC Read and Write Timing (Page 164)

No.	Symbol	Parameter	4 MHz Min(ns)	4 MHz Max(ns)	6 MHz Min(ns)	6 MHz Max(ns)	Notes*
1	TwAS	$\overline{AS}$ Low Width	70		50		
2	TdDS(AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay	50		25		
3	TsCS0(AS)	$\overline{CS_0}$ to $\overline{AS}$ ↑ Setup Time	0		0		1
4	ThCS0(AS)	$\overline{CS_0}$ to $\overline{AS}$ ↑ Hold Time	60		40		1
5	TsCS1(DS)	CS_1 to $\overline{DS}$ ↓ Setup Time	100		80		1
6	ThCS1(DS)	CS_1 to $\overline{DS}$ ↓ Hold Time	55		40		1
7	TsIA(AS)	$\overline{INTACK}$ to $\overline{AS}$ ↑ Setup Time	0		0		
8	ThIA(AS)	$\overline{INTACK}$ to $\overline{AS}$ ↑ Hold Time	250		250		
9	TsRWR(DS)	R/$\overline{W}$(Read) to $\overline{DS}$ ↓ Setup Time	100		80		
10	ThRW(DS)	R/$\overline{W}$ to $\overline{DS}$ ↑ Hold Time	55		40		
11	TsRWW(DS)	R/$\overline{W}$(Write) to $\overline{DS}$ ↓ Setup Time	0		0		
12	TdAS(DS)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ Delay	60		40		
13	TwDSl	$\overline{DS}$ Low Width	390		250		
14	TrC	Valid Access Recovery Time	6TcPC +200		6TcPC +130		2
15	TsA(AS)	Address to $\overline{AS}$ ↑ Setup Time	30		10		1
16	ThA(AS)	Address to $\overline{AS}$ ↑ Hold Time	50		30		1
17	TsDW(DS)	Write Data to $\overline{DS}$ ↓ Setup Time	30		20		
18	ThDW(DS)	Write Data to $\overline{DS}$ ↑ Hold Time	30		20		
19	TdDS(DA)	$\overline{DS}$ ↓ to Data Active Delay	0		0		
20	TdDSr(DR)	$\overline{DS}$ ↑ to Read Data Not Valid Delay	0		0		
21	TdDSf(DR)	$\overline{DS}$ ↓ to Read Data Valid Delay		250		180	
22	TdAS(DR)	$\overline{AS}$ ↑ to Read Data Valid Delay		520		335	

NOTES:

1. Parameter does not apply to Interrupt Acknowledge transactions.
2. Parameter applies only between transactions involving the Z-SCC.

Z-SCC Cycle Timing (Page 165)

No.	Symbol	Parameter	4 MHz Min(ns)	4 MHz Max(ns)	6 MHz Min(ns)	6 MHz Max(ns)	Notes*
23	TdDS(DRz)	$\overline{DS}$ ↑ to Read Data Float Delay		70		45	3
24	TdA(DR)	Address Required Valid to Read Data Valid Delay		570		420	
25	TdDS(W)	$\overline{DS}$ ↓ to Wait Valid Delay		240		200	4
26	TdDSf(REQ)	$\overline{DS}$ ↓ to $\overline{W/REQ}$ Not Valid Delay		240		200	
27	TdDSr(REQ)	$\overline{DS}$ ↓ to $\overline{DTR/REQ}$ Not Valid Delay		5TcPC +300		5TcPC +250	
28	TdAS(INT)	$\overline{AS}$ ↑ to $\overline{INT}$ Valid Delay		500		500	4
29	TdAS(DSA)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ (Acknowledge) Delay					5
30	TwDSA	$\overline{DS}$ (Acknowledge) Low Width	390		250		
31	TdDSA(DR)	$\overline{DS}$ ↓ (Acknowledge) to Read Data Valid Delay		250		180	
32	TsIEI(DSA)	IEI to $\overline{DS}$ ↓ (Acknowledge) Setup Time	120		100		
33	ThIEI(DSA)	IEI to $\overline{DS}$ ↑ (Acknowledge) Hold Time	0		0		
34	TdIEI(IEO)	IEI to IEO Delay		120		100	
35	TdAS(IEO)	$\overline{AS}$ ↑ to IEO Delay		250		250	6
36	TdDSA(INT)	$\overline{DS}$ ↓ (Acknowledge) to $\overline{INT}$ Inactive Delay		500		500	4
37	TdDS(ASQ)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay for No Reset	30		15		
38	TdASQ(DS)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ Delay for No Reset	30		30		
39	TwRES	$\overline{AS}$ and $\overline{DS}$ Coincident Low for Reset	250		250		7
40	TwPCl	PCLK Low Width	105	2000	70	1000	
41	TwPCh	PCLK High Width	105	2000	70	1000	
42	TcPC	PCLK Cycle Time	250	4000	165	2000	
43	TrPC	PCLK Rise Time		20		15	
44	TfPC	PCLK Fall Time		20		10	

NOTES:

3. Float delay is defined as the time required for a ±0.5 V change in the output with a maximum dc load and minimum ac load.
4. Open-drain output, measured with open-drain test load.
5. Parameter is system dependent. For any Z-SCC in the daisy chain, TdAS(DSA) must be greater than the sum of TdAS(IEO) for the highest priority device in the daisy chain, TsIEI(DSA) for the Z-SCC, and TdIEIf(IEO) for each device separating them in the daisy chain.
6. Parameter applies only to a Z-SCC pulling $\overline{INT}$ Low at the beginning of the Interrupt Acknowledge transaction.
7. Internal circuitry allows for the reset provided by the Z8 to be recognized as a reset by the Z-SCC.

*Timings are preliminary and subject to change. All timing references assume 2.0 V for a logic "1" and 0.8 V for a logic "0".

Z-SCC General Timing (Page 166)

No.	Symbol	Parameter	4 MHz Min(ns)	4 MHz Max(ns)	6 MHz Min(ns)	6 MHz Max(ns)	Notes*
1	TdPC(REQ)	PCLK ↓ to W/REQ Valid		250		250	
2	TdPC(W)	PCLK ↓ to Wait Inactive Delay		350		350	
3	TsRXC(PC)	RxC ↑ to PCLK ↑ Setup Time	50		50		1,4
4	TsRXD(RXCr)	RxD to RxC ↑ Setup Time (X1 Mode)	0		0		1
5	ThRXD(RXCr)	RxD to RxC ↑ Hold Time (X1 Mode)	150		150		1
6	TsRXD(RXCf)	RxD to RxC ↓ Setup Time (X1 Mode)	0		0		1,5
7	ThRXD(RXCf)	RxD to RxC ↓ Hold Time (X1 Mode)	150		150		1,5
8	TsSY(RXC)	SYNC to RxC ↑ Setup Time	-200		-200		1
9	ThSY(RXC)	SYNC to RxC ↑ Hold Time	3TcPC		3TcPC		
			+200		+200		1
10	TsTXC(PC)	TxC ↓ to PCLK ↑ Setup Time	0		0		2,4
11	TdTXCf(TXD)	TxC ↓ to TxD Delay (X1 Mode)		300		300	2
12	TdTXCr(TXD)	TxC ↑ to TxD Delay (X1 Mode)		300		300	2,5
13	TdTXD(TRX)	TxD to TRxC Delay (Send Clock Echo)					
14	TwRTXh	RTxC High Width	180		180		
15	TwRTXl	RTxC Low Width	180		180		
16	TcRTX	RTxC Cycle Time	400		400		
17	TcRTXX	Crystal Oscillator Period	250	1000	250	1000	3
18	TwTRXh	TRxC High Width	180		180		
19	TwTRXl	TRxC Low Width	180		180		
20	TcTRX	TRxC Cycle Time	400		400		
21	TwEXT	DCD or CTS Pulse Width	200		200		
22	TwSY	SYNC Pulse Width	200				

NOTES:

1. RxC is RTxC or TRxC, whichever is supplying the receive clock.
2. TxC is TRxC or RTxC, whichever is supplying the transmit clock.
3. Both RTxC and SYNC have 30 pF capacitors to the ground connected to them.
4. Parameter applies only if the data rate is one-fourth the PCLK rate. In all other cases, no phase relationship between RxC and and PCLK or TxC and PCLK is required.
5. Parameter applies only to FM encoding/decoding.

*Timings are preliminary and subject to change.

Z-SCC System Timing (Page 168)

No.	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	Units	Notes*
1	TdRXC(REQ)	RxC ↑ to W/REQ Valid Delay	8	12	8	12	TcPC	2
2	TdRXC(W)	RxC ↑ to Wait Inactive Delay	8	12	8	12	TcPC	1,2
3	TdRXC(SY)	RxC ↑ to SYNC Valid Delay	4	7	4	7	TcPC	2
4	TdRXC(INT)	RxC ↑ INT Valid Delay	8	12	8	12	TcPC	1,2
			+2	+3	+2	+3	AS	
5	TdTXC(REQ)	TxC ↓ to W/REQ Valid Delay	5	8	5	8	TcPC	3
6	TdTXC(W)	TxC ↓ to Wait Inactive Delay	5	8	5	8	TcPC	1,3
7	TdTXC(DRQ)	TxC ↓ to DTR/REQ Valid Delay	4	7	4	7	TcPC	3
8	TdTXC(INT)	TxC ↓ to INT Valid Delay	4	6	4	6	TcPC	1,3
			+2	+3	+2	+3	AS	
9	TdSY(INT)	SYNC Transition to INT Valid Delay	2	3	2	3	AS	1
10	TdEXT(INT)	DCD or CTS Transition to INT Valid Delay	2	3	2	3	AS	1

NOTES:

1. Open-drain output, measured with open-drain test load.
2. RxC is RTxC or TRxC, whichever is supplying the receive clock.
3. TxC is TRxC or RTxC, whichever is supplying the transmit clock.

*Timings are preliminary and subject to change.

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(Page 2)

In **Pin Description,** the **PCLK** entry, delete the last sentence:

Maximum input frequency is 4MHz.

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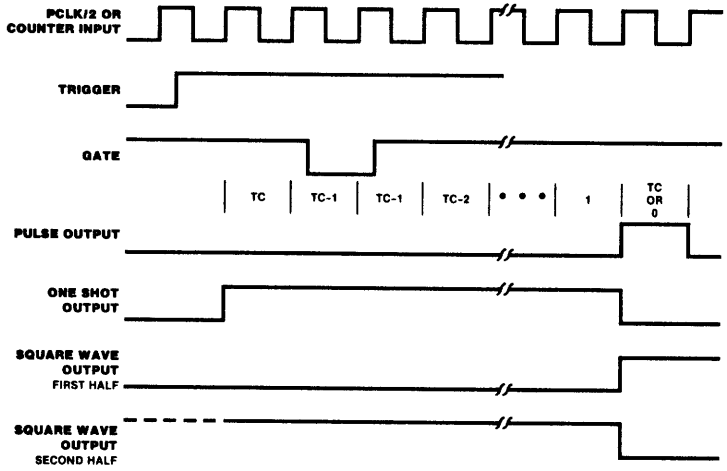
(Page 9)

In Figure 10, "Counter/Timer Waveforms," the time constant line is incorrect between TC-2 and 1. A corrected version of the art follows.



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(Page 12)

In Figure 11, "Master Control Registers," the mnemonics were omitted for bits D_1 and D_5. They should read, respectively:

Right Justified Addresses (RJA)
No Vector (NV)

Master Interrupt Control Register
Address: 000000
(Read/Write)

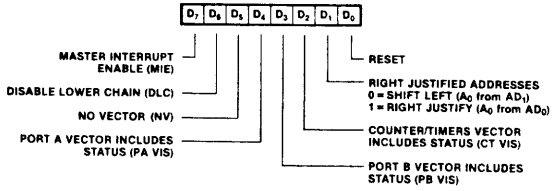

Figure 11. Master Control Registers

In Figure 12, "Port Specification Registers," the Port Mode Specification Registers Addresses should read:

100000 Port A
101000 Port B

The Port Handshake Specification Registers Addresses should read:

100001 Port A
101001 Port B

The Port Command and Status Registers Addresses should read:

001000 Port A
001001 Port B

In Port Mode Specification Registers "PTS2" should read "PTS0." Corrected versions of the art follow.

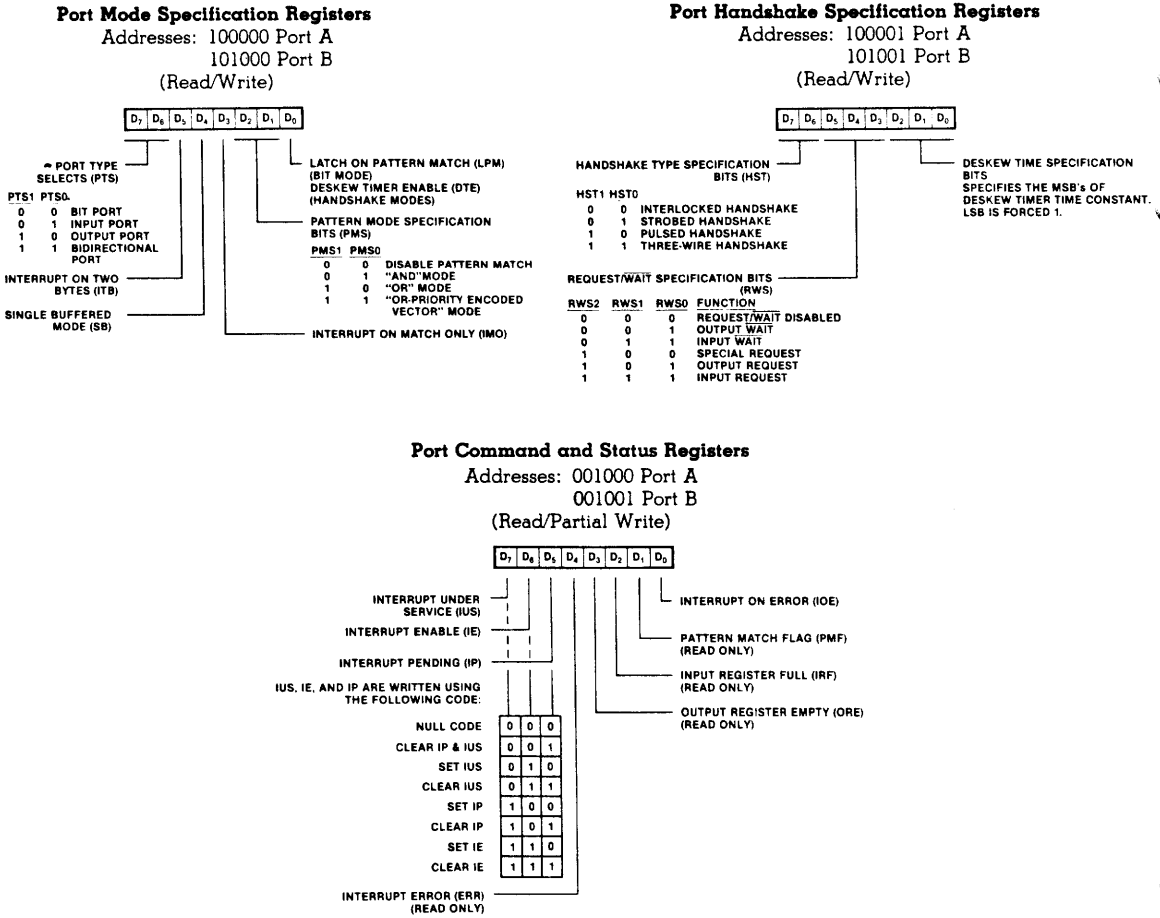

Figure 12. Port Specification Registers

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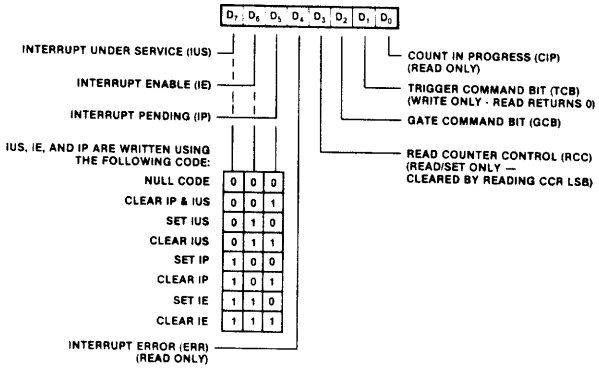
(Page 14)

In Figure 16, "Counter/Timer Registers," the Counter/Timer Mode Specification Registers, DSC1 should read DCS1.

Counter/Timer Command and Status Registers
Addresses: 001010 Counter/Timer 1
001011 Counter/Timer 2
001100 Counter/Timer 3
(Read/Partial Write)



Counter/Timer Mode Specification Registers
Addresses: 011100 Counter/Timer 1
011101 Counter/Timer 2
011110 Counter/Timer 3
(Read/Write)

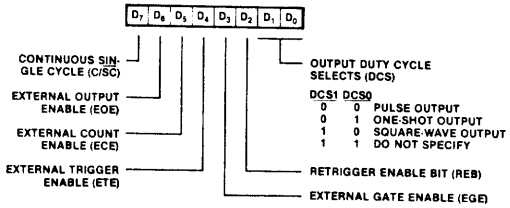


Figure 16. Counter/Timer Registers

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(Page 15)

In the Register Address Summary add the following note to the Address columns:

*When RJA = 0, A_0 from AD_1; when RJA = 1, A_0 from AD_0.

Delete (AD_7-AD_0) below Address in all cases. Delete XX at the end of the Address in all cases.

In **Most Often Accessed Registers** change Counter/Timer Control to Counter/Timer Command and Status in all cases. A corrected version of the art follows.

Register Address Summary

Main Control Registers

Address	Register Name
000000	Master Interrupt Control
000001	Master Configuration Control
000010	Port A's Interrupt Vector
000011	Port B's Interrupt Vector
000100	Counter/Timer's Interrupt Vector
000101	Port C's Data Path Polarity
000110	Port C's Data Direction
000111	Port C's Special I/O Control

Most Often Accessed Registers

Address	Register Name
001000	Port A's Command and Status
001001	Port B's Command and Status
001010	Counter/Timer 1's Command and Status
001011	Counter/Timer 2's Command and Status
001100	Counter/Timer 3's Command and Status
001101	Port A's Data
001110	Port B's Data
001111	Port C's Data

Counter/Timer Related Registers

Address	Register Name
010000	Counter/Timer 1's Current Count-MSBs
010001	Counter/Timer 1's Current Count-LSBs
010010	Counter/Timer 2's Current Count-MSBs
010011	Counter/Timer 2's Current Count-LSBs
010100	Counter/Timer 3's Current Count-MSBs
010101	Counter/Timer 3's Current Count-LSBs
010110	Counter/Timer 1's Time Constant-MSBs
010111	Counter/Timer 1's Time Constant-LSBs
011000	Counter/Timer 2's Time Constant-MSBs
011001	Counter/Timer 2's Time Constant-LSBs
011010	Counter/Timer 3's Time Constant-MSBs
011011	Counter/Timer 3's Time Constant-LSBs
011100	Counter/Timer 1's Mode Specification
011101	Counter/Timer 2's Mode Specification
011110	Counter/Timer 3's Mode Specification
011111	Current Vector

Port A Specification Registers

Address	Register Name
100000	Port A's Mode Specification
100001	Port A's Handshake Specification
100010	Port A's Data Path Polarity
100011	Port A's Data Direction
100100	Port A's Special I/O Control
100101	Port A's Pattern Polarity
100110	Port A's Pattern Transition
100111	Port A's Pattern Mask

Port B Specification Registers

Address	Register Name
101000	Port B's Mode Specification
101001	Port B's Handshake Specification
101010	Port B's Data Path Polarity
101011	Port B's Data Direction
101100	Port B's Special I/O Control
101101	Port B's Pattern Polarity
101110	Port B's Pattern Transition
101111	Port B's Pattern Mask

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In **DC Characteristics** the Maximum rating for Symbol I_{CC} should read 200.

Pages 188-194
(Pages 18-23)

The timing tables for these pages have been revised and expanded to include the 6MHz timing. Corrected versions of the tables follow.

Z-CIO CPU Interface Timing (Page 188)

No.	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	Units	Notes*
1	TwAS	$\overline{AS}$ Low Width	70	2000	50	2000	ns	
2	TsA(AS)	Address to $\overline{AS}$ ↑ Setup Time	30		10		ns	1
3	ThA(AS)	Address to $\overline{AS}$ ↑ Hold Time	50		30		ns	1
4	TsA(DS)	Address to $\overline{DS}$ ↓ Setup Time	130		100		ns	1
5	TsCSO(AS)	$\overline{CS_0}$ to $\overline{AS}$ ↑ Setup Time	0		0		ns	1
6	ThCSO(AS)	$\overline{CS_0}$ to $\overline{AS}$ ↑ Hold Time	60		40		ns	1
7	TdAS(DS)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ Delay	60		40		ns	1
8	TsCS1(DS)	CS_1 to $\overline{DS}$ ↓ Setup Time	100		80		ns	
9	TsRWR(DS)	R/$\overline{W}$ (Read) to $\overline{DS}$ ↓ Setup Time	100		80		ns	
10	TsRWW(DS)	R/$\overline{W}$ (Write) to $\overline{DS}$ ↓ Setup Time	0		0			
11	TwDS	$\overline{DS}$ Low Width	390		250		ns	
12	TsDW(DSf)	Write Data to $\overline{DS}$ ↓ Setup Time	30		20		ns	
13	TdDS(DRV)	$\overline{DS}$ (Read) ↓ to Address Data Bus Driven	0		0			
14	TdDSf(DR)	$\overline{DS}$ ↓ to Read Data Valid Delay		250		180	ns	
15	ThDW(DS)	Write Data to $\overline{DS}$ ↑ Hold Time	30		20		ns	
16	TdDSr(DR)	$\overline{DS}$ ↑ to Read Data Not Valid Delay	0		0			
17	TdDS(DRz)	$\overline{DS}$ ↑ to Read Data Float Delay		70		45	ns	2
18	ThRW(DS)	R/$\overline{W}$ to $\overline{DS}$ ↑ Hold Time	55		40		ns	
19	ThCS1(DS)	CS_1 to $\overline{DS}$ ↑ Hold Time	55		40		ns	
20	TdDS(AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay	50		25		ns	
21	Trc	Valid Access Recovery Time	1000		650		ns	3
		Z-CIO Interrupt Timing						
22	TdPM(INT)	Pattern Match to $\overline{INT}$ Delay (Bit Port)		1		1	$\overline{AS}$ cycle +ns	
23	TdACK(INT)	$\overline{ACKIN}$ to $\overline{INT}$ Delay (Port with Handshake)		4		4	$\overline{AS}$ cycle +ns	4
24	TdCI(INT)	Counter Input to $\overline{INT}$ Delay (Counter Mode)		1		1	$\overline{AS}$ cycle +ns	
25	TdPC(INT)	PCLK to $\overline{INT}$ Delay (Timer Mode)		1		1	$\overline{AS}$ cycle +ns	
26	TdAS(INT)	$\overline{AS}$ to $\overline{INT}$ Delay					ns	
		Z-CIO Interrupt Acknowledge Timing						
27	TsIA(AS)	$\overline{INTACK}$ to $\overline{AS}$ ↑ Setup Time	0		0		ns	
28	ThIA(AS)	$\overline{INTACK}$ to $\overline{AS}$ ↑ Hold Time	250		250		ns	
29	TsAS(DSA)	$\overline{AS}$ ↑ to $\overline{DS}$ (Acknowledge) ↓ Setup Time	350		250		ns	5
30	TdDSA(DR)	$\overline{DS}$ (Acknowledge) ↓ to Read Data Valid Delay		250		180	ns	
31	TwDSA	$\overline{DS}$ (Acknowledge) Low Width	390		250		ns	
32	TdAS(IEO)	$\overline{AS}$ ↑ to IEO ↓ Delay ($\overline{INTACK}$ Cycle)		350		250	ns	5
33	TdIEI(IEO)	IEI to IEO Delay		150		100	ns	5
34	TsIEI(DSA)	IEI to $\overline{DS}$ (Acknowledge) ↓ Setup Time	100		70		ns	5
35	ThIEI(DSA)	IEI to $\overline{DS}$ (Acknowledge) ↑ Hold Time	100		70		ns	
36	TdDSA(INT)	$\overline{DS}$ (Acknowledge) ↓ to $\overline{INT}$ ↑ Delay		600		600	ns	

NOTES:

1. Parameter does not apply to Interrupt Acknowledge transactions.
2. Float delay is measured to the time when the output has changed 0.5 V from steady state with minimum ac load and maximum dc load.
3. This is the delay from $\overline{DS}$ ↑ of one CIO access to $\overline{DS}$ ↓ of another CIO access.
4. The delay is from $\overline{DAV}$ ↓ for 3-Wire Input Handshake. The delay is from DAC ↑ for 3-Wire Output Handshake. One additional $\overline{AS}$ cycle is required for ports in the Single Buffered mode.
5. The parameters for the devices in any particular daisy chain must meet the following constraint: the delay from $\overline{AS}$ ↑ to $\overline{DS}$ ↓ must be greater than the sum of TdAS(IEO) for the highest priority peripheral, TsIEI(DSA) for lowest priority peripheral, and TdIEI(IEO) for each peripheral separating them in the chain.

*Timings are preliminary and subject to change. All timing references assume 2.0 V for a logic "1" and 0.8 V for a logic "0".

Z-CIO Handshake Timing (Page 190)

No.	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	Units	Notes*
1	TsDI(ACK)	Data Input to $\overline{ACKIN}$ ↓ Setup Time	0		0		ns	
2	ThDI(ACK)	Data Input to $\overline{ACKIN}$ ↓ Hold Time--Strobed Handshake					ns	
3	TdACKf(RFD)	$\overline{ACKIN}$ ↓ to RFD ↓ Delay	0		0		ns	
4	TwACKl	$\overline{ACKIN}$ Low Width--Strobed Handshake					ns	
5	TwACKh	$\overline{ACKIN}$ High Width--Strobed Handshake					ns	
6	TdRFDr(ACK)	RFD ↑ to $\overline{ACKIN}$ ↓ Delay	0		0		ns	
7	TsDO(DAV)	Data Out to $\overline{DAV}$ ↓ Setup Time	25		20		ns	1
8	TdDAVf(ACK)	$\overline{DAV}$ ↓ to $\overline{ACKIN}$ ↓ Delay	0		0		ns	
9	ThDO(ACK)	Data Out to $\overline{ACKIN}$ ↓ Hold Time	1		1		$\overline{AS}$ cycle	
10	TdACK(DAV)	$\overline{ACKIN}$ ↓ to $\overline{DAV}$ ↑ Delay	1		1		$\overline{AS}$ cycle	
11	ThDI(RFD)	Data Input to RFD ↓ Hold Time--Interlocked Handshake	0		0		ns	
12	TdRFDf(ACK)	RFD ↓ to $\overline{ACKIN}$ ↑ Delay--Interlocked Handshake	0		0		ns	
13	TdACKr(RFD)	$\overline{ACKIN}$ ↑ ($\overline{DAV}$ ↑) to RFD ↑ Delay--Interlocked and 3-Wire Handshake	0		0		ns	
14	TdDAVr(ACK)	$\overline{DAV}$↑to $\overline{ACKIN}$ ↑ (RFD ↑)--Interlocked and 3-Wire Handshake	0		0		ns	
15	TdACK(DAV)	$\overline{ACKIN}$ ↑ (RFD ↑) to $\overline{DAV}$ ↓ Delay Interlocked and 3-Wire Handshake	0		0		ns	
16	TdDAVIf(DAC)	$\overline{DAV}$ ↓ to DAC ↑ Delay--Input 3-Wire Handshake	0		0		ns	
17	ThDI(DAC)	Data Input to DAC ↑ Hold Time--3-Wire Handshake	0		0		ns	
18	TdDACOr(DAV)	DAC ↑ to $\overline{DAV}$ ↑ Delay--Input 3-Wire Handshake	0		0		ns	
19	TdDAVIr(DAC)	$\overline{DAV}$ ↑ to DAC ↓ Delay--Input 3-Wire Handshake	0		0		ns	
20	TdDAVOf(DAC)	$\overline{DAV}$ ↓ to DAC ↑ Delay--Output 3-Wire Handshake	0		0		ns	
21	ThDO(DAC)	Data Output to DAC ↑ Hold Time--3-Wire Handshake	1		1		$\overline{AS}$ cycle	
22	TdDACIr(DAV)	DAC↑to $\overline{DAV}$ ↑ Delay--Output 3-Wire Handshake	1		1		$\overline{AS}$ cycle	
23	TdDAVOr(DAC)	$\overline{DAV}$ ↑ to DAC ↓ Delay--Output 3-Wire Handshake	0		0		ns	

NOTES:
1. This time can be extended through the use of the deskew timers.

All timing references assume 2.0 V for a logic "1" and 0.8 V for a logic "0".

*Timings are preliminary and subject to change.

Z-CIO Counter/Timer Timing (Page 192)

No.	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	Units	Notes*
1	TcPC	PCLK Cycle Time	250	4000	165	4000	ns	1
2	TwPCh	PCLK High Width	105	2000	70	2000	ns	
3	TwPCl	PCLK Low Width	105	2000	70	2000	ns	
4	TfPC	PCLK Fall Time		20		10	ns	
5	TrPC	PCLK Rise Time		20		15	ns	
6	TcCI	Counter Input Cycle Time	500		330		ns	
7	TCIh	Counter Input High Width	230		150		ns	
8	TwCIl	Counter Input Low Width	230		150		ns	
9	TfCI	Counter Input Fall Time		20		15	ns	
10	TrCI	Counter Input Rise Time		20		15	ns	
11	TsTI(PC)	Trigger Input to PCLK ↓ Setup Time (Timer Mode)					ns	2
12	TsTI(CI)	Trigger Input to Counter Input ↓ Setup Time (Counter Mode)					ns	2
13	TwTI	Trigger Input Pulse Width (High or Low)					ns	
14	TsGI(PC)	Gate Input to PCLK ↓ Setup Time (Timer Mode)					ns	2
15	TsGI(CI)	Gate Input to Counter Input ↓ Setup Time (Counter Mode)					ns	2

No.	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	Units	Notes*
16	ThGI(PC)	Gate Input to PCLK ↓ Hold Time (Timer Mode)					ns	2
17	ThGI(CI)	Gate Input to Counter Input ↓ Hold Time (Counter Mode)					ns	2
18	TdPC(CO)	PCLK to Counter Output Delay (Timer Mode)					ns	
19	TdCI(CO)	Counter Input to Counter Output Delay (Counter Mode)					ns	

NOTES:

1. PCLK is only used with the counter/timers (in Timer mode), the deskew timers, and the REQUEST/$\overline{\text{WAIT}}$ logic. If these functions are not used, the PCLK input can be held Low.
2. These parameters must be met to guarantee trigger or gate are valid for the next counter/timer cycle.

*Timings are preliminary and subject to change. All timing references assume 2.0 V for a logic "1" and 0.8 V for a logic "0".

Z-CIO REQUEST/WAIT Timing (Page 193)

No.	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	Units	Notes*
1	TdDS(REQ)	$\overline{\text{DS}}$ ↓ to REQ ↓ Delay					ns	
2	TdDS(WAIT)	$\overline{\text{DS}}$ ↓ to $\overline{\text{WAIT}}$ ↓ Delay					ns	
3	TdPC(REQ)	PCLK ↓ to REQ ↑ Delay					ns	
4	TdPC(WAIT)	PCLK ↓ to $\overline{\text{Wait}}$ ↑ Delay					ns	
5	TdACK(REQ)	$\overline{\text{ACKIN}}$ ↓ to REQ ↑ Delay					$\overline{\text{AS}}$ cycles +PCLK cycles +ns	1
6	TdACK(WAIT)	$\overline{\text{ACKIN}}$ ↓ to $\overline{\text{Wait}}$ ↑ Delay					PCLK cycles +ns	

NOTES:

1. The Delay is from $\overline{\text{DAV}}$ ↓ for the 3-Wire Input Handshake. The delay is from DAC ↓ for the 3-Wire Output Handshake.

*Timings are preliminary and subject to change. All timing references assume 2.0 V for a logic "1" and 0.8 V for a logic "0".

Z-CIO Reset Timing

No.	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	Units	Notes*
1	TdDSQ(AS)	Delay from $\overline{\text{DS}}$ ↑ to $\overline{\text{AS}}$ ↓ for No Reset	40		15		ns	
2	TdASQ(DS)	Delay from $\overline{\text{AS}}$ ↑ to $\overline{\text{DS}}$ ↓ for No Reset	50		30		ns	
3	TwRES	Minimum Width of $\overline{\text{AS}}$ and $\overline{\text{DS}}$ both Low for Reset	250		170		ns	1

NOTES:

1. Internal circuitry allows for the reset provided by the Z8 ($\overline{\text{DS}}$ held Low while $\overline{\text{AS}}$ pulses) to be sufficient.

*Timings are preliminary and subject to change. All timing references assume 2.0 V for a logic "1" and 0.8 V for a logic "0".

Z-CIO Miscellaneous Port Timing (Page 194)

No.	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	Units	Notes*
1	TrI	Any Input Rise Time		100		100	ns	
2	TfI	Any Input Fall Time		100		100	ns	
3	Tw1's	1's Catcher High Width	250		170		ns	1
4	TwPM	Pattern Match Input Valid (Bit Port)	750		500		ns	
5	TsPMD	Data Latched on Pattern Match Setup Time (Bit Port)	0		0		ns	
6	ThPMD	Data Latched on Pattern Match Hold Time (Bit Port)	1000		650		ns	

NOTES:

1. If the input is programmed inverting, a Low-going pulse of the same width will be detected.

*Timings are preliminary and subject to change.

All timing references assume 2.0 V for a logic "1" and 0.8 V for a logic "0".

Page 196
(Page 1)

Delete the following from the chapter heading:

Z8038 Z-BUS™ Version FIO
Z8538 Universal Version FIO

Page 202
(Page 8)

In **Interrupt Operation** add the following paragraph at the end of the text:

In Z-BUS mode IPs are set by an $\overline{AS}$ following the event.

Page 212
(Page 18)

In Figure 28, "Byte Count Register," add the following note to Byte Counter Register:

(Read only)

In Figure 30, "Pattern Match Register," the Address should read:

1101

Page 213
(Page 19)

Add the following to **DC Characteristics** between symbols I_{OL} and I_{CC}:

Symbol	Parameter	Min	Max	Unit	Condition
I_{LM}	Mode pins input leakage	±100	+10	µA	$0 < V_{IN} < V_{CC}$

In **DC Characteristics** change the Max reading of I_{CC} from 250 to 200.

Pages 214-24
(Pages 20-30)

The timing tables for these pages have been revised and expanded to include the 6 MHz timing. Corrected versions of the tables follow.

Z-FIO Z-BUS CPU Interface Timing (Page 214)

No.	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	Units	Notes*
1	TwAS	$\overline{AS}$ Low Width	70		50		ns	
2	TsA(AS)	Address to $\overline{AS}$ ↑ Setup Time	30		10		ns	1
3	ThA(AS)	Address to $\overline{AS}$ ↑ Hold Time	50		30		ns	1
4	TsCSO(AS)	$\overline{CS}$ to $\overline{AS}$ ↑ Setup Time	0		0		ns	1
5	ThCSO(AS)	$\overline{CS}$ to $\overline{AS}$ ↑ Hold Time	60		40		ns	1
6	TdAS(DS)	$\overline{AS}$ ↑ to $\overline{DS}$ ↑ Delay	60		40		ns	1
7	TsA(DS)	Address to $\overline{DS}$ ↓ (with $\overline{AS}$ ↑ to $\overline{DS}$ ↓ = 60 ns)	120		100		ns	
8	TsRWR(DS)	R/$\overline{W}$ (Read) to $\overline{DS}$ ↓ Setup Time	100		80		ns	
9	TsRWW(DS)	R/$\overline{W}$ (Write) to $\overline{DS}$ ↓ Setup Time	0		0		ns	
10	TwDS	$\overline{DS}$ Low Width	390		250		ns	
11	TsDW(DSf)	Write Data to $\overline{DS}$ ↓ Setup Time	30		20		ns	
12	TdDS(DRV)	$\overline{DS}$ (Read) ↓ to Address Data Bus Driven	0		0		ns	
13	TdDSf(DR)	$\overline{DS}$ ↓ to Read Data Valid Delay		250		180	ns	
14	ThDW(DS)	Write Data to $\overline{DS}$ ↑ Hold Time	30		20		ns	
15	TdDSr(DR)	$\overline{DS}$ ↑ to Read Data Not Valid Delay	0		0		ns	
16	TdDS(DRz)	$\overline{DS}$ ↑ to Read Data Float Delay		70		45	ns	2
17	ThRW(DS)	R/$\overline{W}$ to $\overline{DS}$ ↑ Hold Time	55		40		ns	
18	TdDS(AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay	50		25		ns	
19	Trc	Valid Access Recovery Time	1000		650		ns	3

NOTES:
1. Parameter does not apply to Interrupt Acknowledge transactions.
2. Float delay is measured to the time when the output has changed 0.5 V from steady state with minimum as load and maximum dc load.
3. This is the delay from $\overline{DS}$ of one CIO access to $\overline{DS}$ of another FIO access (either read or or write).

*All timing references assume 2.0 V for a logic "1" and 0.8 V for a logic "0".

Z-FIO Z-BUS CPU Interrupt Acknowledge Timing (Page 215)

No.	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	Units	Notes
20	TsIA(AS)	$\overline{INTACK}$ to $\overline{AS}$ ↑ Setup Time	0			0	ns	
21	ThIA(AS)	$\overline{INTACK}$ to $\overline{AS}$ ↑ Hold Time	250		250		ns	
22	TdDSA(DR)	$\overline{DS}$ (Acknowledge) ↓ to Read Data Valid Delay		250		180	ns	
23	TwDSA	$\overline{DS}$ (Acknowledge) Low Width	390		250		ns	
24	TdAS(IEO)	$\overline{AS}$ ↑ to IEO ↓ Delay ($\overline{INTACK}$ Cycle)		350		250	ns	4
25	TdIEI(IEO)	IEI to IEO Delay		150		100	ns	4
26	TsIEI(DSA)	IEI to $\overline{DS}$ (Acknowledge) ↓ Setup Time	100		70		ns	
27	ThIEI(DSA)	IEI to $\overline{DS}$ (Acknowledge) ↑ Hold Time	50		30		ns	4
28	TdDS(INT)	$\overline{DS}$ ($\overline{INTACK}$ Cycle) to $\overline{INT}$ Delay		900		800	ns	
29	TdDCST	Interrupt Daisy Chain Settle Time					ns	4

NOTES:

4. The parameters for the devices in any particular daisy chain must meet the following constraint: The delay from $\overline{AS}$ to $\overline{DS}$ must be greater than the sum of TdAS(IEO) for the highest priority peripheral, TsIEI(DSA) for the lowest priority peripheral, and TdIEI(IEO) for each peripheral, separating them in the chain.

Z-FIO Z-BUS Interrupt Timing (Page 216)

No.	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	Units	Notes
30	TdMW(INT)	Message Write to $\overline{INT}$ Delay		1		1	$\overline{AS}$ Cycles +ns	5
31	TdDC(INT)	Data Direction Change to $\overline{INT}$ Delay		1		1	$\overline{AS}$ Cycles +ns	6
32	TdPMW(INT)	Pattern Match to $\overline{INT}$ Delay (Write Case)		1		1	$\overline{AS}$ Cycles +ns	
33	TdPMR(INT)	Pattern Match (Read Case) to $\overline{INT}$ Delay		1		1	$\overline{AS}$ Cycles +ns	
34	TdSC(INT)	Status Compare to $\overline{INT}$ Delay		1		1	$\overline{AS}$ Cycles +ns	6
35	TdER(INT)	Error to $\overline{INT}$ Delay		1		1	$\overline{AS}$ Cycles +ns	
36	TdEM(INT)	Empty to $\overline{INT}$ Delay		1		1	$\overline{AS}$ Cycles +ns	6
37	TdFL(INT)	Full to $\overline{INT}$ Delay		1		1	$\overline{AS}$ Cycles +ns	6
38	TdAS(INT)	$\overline{AS}$ to $\overline{INT}$ Delay					$\overline{AS}$ Cycles +ns	

NOTES:

5. Write is from the other side of FIO.
6. Write can be from either side, depending on programming of FIO.

Z-FIO Request/Wait Timing (Page 217)

No.	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	Units	Notes
1	TdDS(WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↓ Delay		190		160	ns	
2	TdDS1(WAIT)	$\overline{DS1}$ ↑ to $\overline{WAIT}$ ↑ Delay		1000		1000	ns	
3	TdACK(WAIT)	$\overline{ACKIN}$ ↓ to $\overline{WAIT}$ ↑ Delay		1000		1000	ns	1
4	TdDS(REQ)	$\overline{DS}$ ↓ to $\overline{REQ}$ ↑ Delay		350		300	ns	
5	TdDMA(REQ)	$\overline{DMASTB}$ ↓ to $\overline{REQ}$ ↑ Delay		350		300	ns	
6	TdDS1(REQ)	$\overline{DS1}$ ↑ to $\overline{REQ}$ ↓ Delay		1000		1000	ns	
7	TdACK(REQ)	$\overline{ACKIN}$ ↓ to $\overline{REQ}$ ↓ Delay		1000		1000	ns	
8	TdSU(DMA)	Data Setup Time to $\overline{DMASTB}$	200		150		ns	
9	TdH(DMA)	Data Hold Time to $\overline{DMASTB}$	30		20		ns	
10	TdDMA(DR)	$\overline{DMASTB}$ ↓ to Valid Data		150		100	ns	
11	TdDMA(DRH)	$\overline{DMASTB}$ ↑ to Data Not Valid	0		0		ns	
12	TdDMA(DR2)	$\overline{DMASTB}$ ↑ to DATA Bus Float		70		45	ns	

NOTES:
1. The delay is from $\overline{DAV}$ for 3-Wire Input Handshake. The delay is from DAC for 3-Wire Handshake.

Z-FIO Z-BUS Reset Timing

No.	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	Units	Notes
1	TdDSQ(AS)	Delay from $\overline{DS}$ ↑ to $\overline{AS}$ ↓ for No Reset	40		20		ns	
2	TdASQ(DS)	Delay for $\overline{AS}$ ↑ to $\overline{DS}$ ↓ for No Reset	50		30		ns	
3	Tw(AS + DS)	Minimum Width of $\overline{AS}$ and $\overline{DS}$ Both Low for Reset	500		350		ns	1

NOTES:
1. Internal circuitry allows for the reset provided by the Z8 ($\overline{DS}$ held Low while $\overline{AS}$ pulses) to be sufficient.

Z-FIO Non Z-BUS CPU Interface Timing (Page 218)

No.	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	Units	Notes
1	TsA(RD)	Address Setup to $\overline{RD}$ ↓	80		80		ns	1
2	TsA(WR)	Address Setup to $\overline{WR}$ ↓	80		80		ns	
3	ThA(RD)	Address Hold Time to $\overline{RD}$ ↑	0		0		ns	1
4	ThA(WR)	Address Hold Time to $\overline{WR}$ ↑	0		0		ns	
5	TsCEI(RD)	$\overline{CE}$ Low Setup Time to $\overline{RD}$	0		0		ns	1
6	TsCEI(WR)	$\overline{CE}$ Low Setup Time to $\overline{WR}$	0		0		ns	
7	ThCEI(RD)	$\overline{CE}$ Low Hold Time to $\overline{RD}$	0		0		ns	1
8	ThCEI(WR)	$\overline{CE}$ Low Hold Time to $\overline{WR}$	0		0		ns	
9	TsCEh(RD)	$\overline{CE}$ High Setup Time to $\overline{RD}$	100		70		ns	1
10	TsCEh(WR)	$\overline{CE}$ High Setup Time to $\overline{WR}$	100		70		ns	
11	TwRDl	$\overline{RD}$ Low Width	390		250		ns	
12	TdRD(DRA)	$\overline{RD}$ ↓ to Read Data Active Delay	0		0		ns	
13	TdRDf(DR)	$\overline{RD}$ ↓ to Valid Data Delay		250		180	ns	
14	TdRDr(DR)	$\overline{RD}$ ↑ to Read Data Not Valid Delay	0		0		ns	
15	TdRD(DRz)	$\overline{RD}$ ↑ to Data Bus Float		70		45	ns	2
16	TwWRl	$\overline{WR}$ Low Width	390		250		ns	
17	TsDW(WR)	Data Setup Time to $\overline{WR}$	0		0		ns	
18	ThDW(WR)	Data Hold Time to $\overline{WR}$	30		20		ns	
19	Trc	Valid Access Recovery Time	1000		650		ns	3

NOTES:
1. Parameter does not apply to Interrupt Acknowledge transactions.
2. Float delay is measured to the time the output has changed 0.5 V from steady state with minimum ac load and maximum dc load.
3. This is the delay from $\overline{RD}$ ↑ to $\overline{WR}$ ↑ of one FIO access to $\overline{RD}$ ↓ or $\overline{WR}$ ↓ of another FIO access.

Z-FIO Non Z-BUS Interrupt Acknowledge Timing (Page 219)

No.	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	Units	Notes
20	TdIEI(IEO)	IEI to IEO Delay		150		100	ns	4
21	TdI(IEO)	$\overline{INTACK}$ ↓ to IEO ↓ Delay		350		250	ns	4
22	TsIEI(RDA)	IEI Setup Time to $\overline{RD}$ (Acknowledge)	100		70		ns	4
23	TdRD(DR)	$\overline{RD}$ ↓ to Vector Valid Delay		250		180	ns	
24	TwRD1(IA)	Read Low Width (Interrupt Acknowledge)	390		250		ns	
25	ThIA(RD)	$\overline{INTACK}$ ↑ to $\overline{RD}$ ↑ Hold Time	30		20		ns	
26	ThIEI(RD)	IEI Hold Time to $\overline{RD}$ ↑	20		10		ns	
27	TdRD(INT)	$\overline{RD}$ ↑ to $\overline{INT}$ ↑ Delay		900		800	ns	
28	TdDCST	Interrupt Daisy Chain Settle Time		350		250	ns	4

NOTES:

4. The parameter for the devices in any particular daisy chain must meet the following constraint: The delay from $\overline{INTACK}$ ↓ to $\overline{RD}$ ↓ must be greater than the sum of TdINA(IEO) for the highest priority peripheral, TsIEI(RD) for the lowest priority peripheral, and TdIEI(IEO) for each peripheral separating them in the chain.

Z-FIO Non-Z-BUS Interrupt Timing (Page 220)

No.	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	Units	Notes
29	TdMW(INT)	Message Write to $\overline{INT}$ Delay					ns	5,6
30	TdDC(INT)	Data Direction Change to $\overline{INT}$ Delay					ns	5,7
31	TdPMW(INT)	Pattern Match (Write Case) to $\overline{INT}$ Delay					ns	5
32	TdPMR(INT)	Pattern Match (Read Case) to $\overline{INT}$ Delay					ns	5
33	TdSC(INT)	Status Compare to $\overline{INT}$ Delay					ns	5,7
34	TdER(INT)	Error to $\overline{INT}$ Delay					ns	5,7
35	TdEM(INT)	Empty to $\overline{INT}$ Delay					ns	5,7
36	TdFL(INT)	Full to $\overline{INT}$ Delay					ns	5,7
37	TdSO(INT)	State 0 to $\overline{INT}$ Delay					ns	

NOTES:

5. Delay number is valid for State 0 only.
6. Write is from other side of FIO.
7. Write can be from either side, depending on programming of FIO.

Z-FIO Non-Z-BUS Request/Wait Timing (Page 221)

No.	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	Units	Notes
1	TdRD(WT)	$\overline{CE}$ ↓ to $\overline{WAIT}$ Active		200		170	ns	
2	TdRD1(WT)	$\overline{RD1}$ ↑ or $\overline{WR1}$ ↑ to $\overline{WAIT}$ Inactive		1000		1000	ns	
3	TdACK(WT)	$\overline{ACKIN}$ ↓ to $\overline{WAIT}$ Inactive		1000		1000	ns	1
4	TdRD(REQ)	$\overline{RD}$ ↓ or $\overline{WR}$ ↓ to REQ Inactive		350		300	ns	
5	TdRD1(REQ)	$\overline{RD1}$ ↑ or $\overline{WR1}$ ↑ to REQ Active		1000		1000	ns	
6	TdACK(REQ)	$\overline{ACKIN}$ ↓ to REQ Active		1000		1000	ns	
7	TdDAC(RD)	$\overline{DACK}$ ↓ to $\overline{RD}$ ↓ or $\overline{WR}$ ↓	100		80		ns	
8	TSU(WR)	Data Setup Time to $\overline{WR}$	200				ns	
9	Th(WR)	Data Hold Time to $\overline{WR}$	30			20	ns	
10	TdDMA	$\overline{RD}$ ↓ to Valid Data		150		100	ns	2
11	TdDMA(DRH)	$\overline{RD}$ ↑ to Data Not Valid	0		0		ns	2
12	TdDMA(DRZ)	$\overline{RD}$ ↑ to Data Bus Float		70		45	ns	2

NOTES:

1. The delay is from $\overline{DAV}$ ↓ for 3-Wire Input Handshake. The delay is from DAC ↑ for 3-Wire Input Handshake.
2. Only when $\overline{DACK}$ is active.

Z-FIO Non-Z-BUS Reset Timing (Page 222)

No.	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	Units
1	TdWR(RD)	Delay from $\overline{WR}$ ↑ to $\overline{RD}$ ↓	100		70		ns
2	TdRD(WR)	Delay from $\overline{RD}$ ↑ to $\overline{WR}$ ↓	100		70		ns
3	TwRD + WR	Width of $\overline{RD}$ and $\overline{WR}$, both Low for Reset	500		350		ns

Z-FIO Port 2 Side Operation

1	TwCLR	Width of Clear to Reset FIFO	700		700		ns
2	TdOE(DO)	$\overline{OE}$ ↓ to Data Bus Driven	0		0		ns
3	TdOE(DRZ)	$\overline{OE}$ ↑ to Data Bus Float					ns

Z-FIO 2-Wire Handshake Timing (Page 223)

No.	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	Units
1	TsDI(ACK)	Data Input to $\overline{ACKIN}$ ↓ to Setup Time	50		50		ns
2	TdACKf(RFD)	$\overline{ACKIN}$ ↓ to RFD ↓ Delay	0	500	0	500	ns
3	TdRFDr(ACK)	RFD ↑ to $\overline{ACKIN}$ ↓ Delay	0		0		ns
4	TsDO(DAV)	Data Out to $\overline{DAV}$ ↓ Setup Time	25		25		ns
5	TdDAVf(ACK)	$\overline{DAV}$ ↓ to $\overline{ACKIN}$ ↓ Delay	0		0		ns
6	ThDO(ACK)	Data Out to $\overline{ACKIN}$ Hold Time	50		50		ns
7	TdACK(DAV)	$\overline{ACKIN}$ ↓ to $\overline{DAV}$ ↑ Delay	0	500	0	500	ns
8	ThDI(RFD)	Data Input to RFD ↓ Hold Time	0		0		ns
9	TdRFDf(ACK)	RFD ↓ to $\overline{ACKIN}$ ↑ Delay	0		0		ns
10	TdACKr(RFD)	$\overline{ACKIN}$ ↑ ($\overline{DAV}$ ↑) to RFD ↑ Delay-- Interlocked and 3-Wire Handshake	0	400	0	400	ns
11	TdDAVr(ACK)	$\overline{DAV}$ ↑ to $\overline{ACKIN}$ ↑ (RFD ↑)	0		0		ns
12	TdACKr(DAV)	$\overline{ACKIN}$ ↑ to $\overline{DAV}$ ↓	0	800	0	800	ns

Z-FIO 3-Wire Handshake Timing (Page 224)

No.	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	Units
1	TsDI(DAV)	Data Input to $\overline{DAV}$ ↓ Setup Time	50		50		ns
2	TdDAVIf(RFD)	$\overline{DAV}$ ↓ to RFD ↓ Delay	0	500	0	500	ns
3	TdDAVf(DAC)	$\overline{DAV}$ ↓ to DAC ↑ Delay	0	500	0	500	ns
4	ThDI(DAC)	Data In to DAC ↑ Hold Time	0		0		ns
5	TdDACIr(DAV)	DAC ↑ to $\overline{DAV}$ ↑ Delay	0		0		ns
6	TdDAVIr(DAC)	$\overline{DAV}$ ↑ to DAC ↓ Delay	0	500	0	500	ns
7	TdDAVIr(RFD)	$\overline{DAV}$ ↑ to RFD ↑ Delay	0	500	0	500	ns
8	TdRFDI(DAV)	RFD ↑ to $\overline{DAV}$ ↓ Delay	0		0		ns
9	TsDO(DAC)	Data Out to $\overline{DAV}$↓					ns
10	TdDAVOf(RFD)	$\overline{DAV}$ ↓ to RFD ↓ Delay	0		0		ns
11	TdDAVOf(DAC)	$\overline{DAV}$ ↓ to DAC ↑ Delay	0		0		ns
12	ThDO(DAC)	Data Out to DAC ↑ Hold Time					ns
13	TdDACOr(DAV)	DAC ↑ to $\overline{DAV}$ ↑ Delay		400		400	ns
14	TdDAVOr(DAC)	$\overline{DAV}$ ↑ to DAC ↓ Delay	0		0		ns
15	TdDAVOr(RFD)	$\overline{DAV}$ ↑ to RFD ↑ Delay	0		0		ns
16	TdRFDO(DAV)	RFD ↑ to $\overline{DAV}$ ↓ Delay	0	800	0	800	ns

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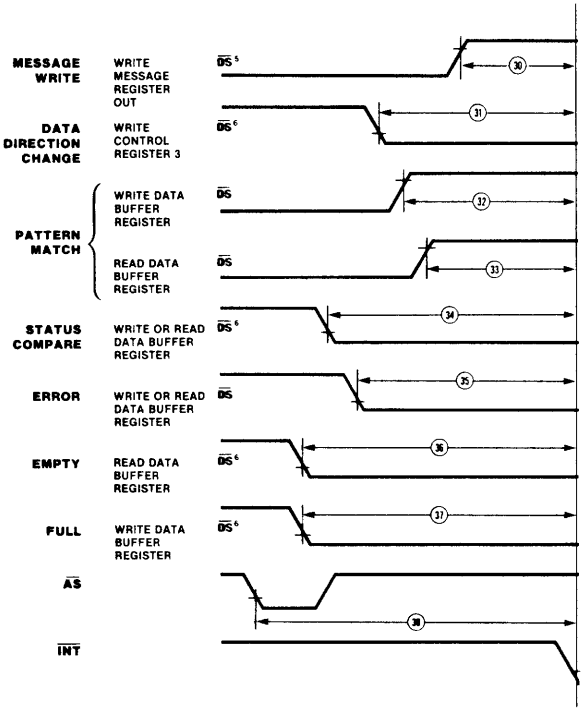
(Page 22)

The timing diagram is incorrect for parameters 30, 31, 36, and 37 for the **Z-BUS Interrupt Timing** diagram. A corrected version of the art follows.

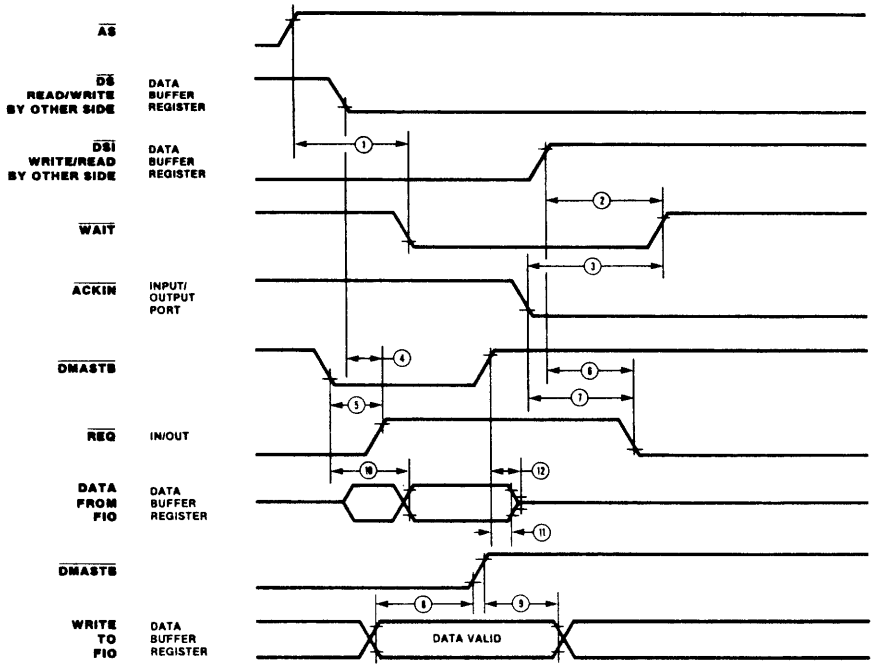


Page 217
(Page 23)

In **Z-BUS Request/Wait Timing** change the parameter in number 1 from $\overline{DS}$ to $\overline{AS}$.

The **Z-BUS Request/Wait Timing** diagram is incorrect for parameter 1. A corrected version of the art follows.

Z-BUS Request/Wait Timing



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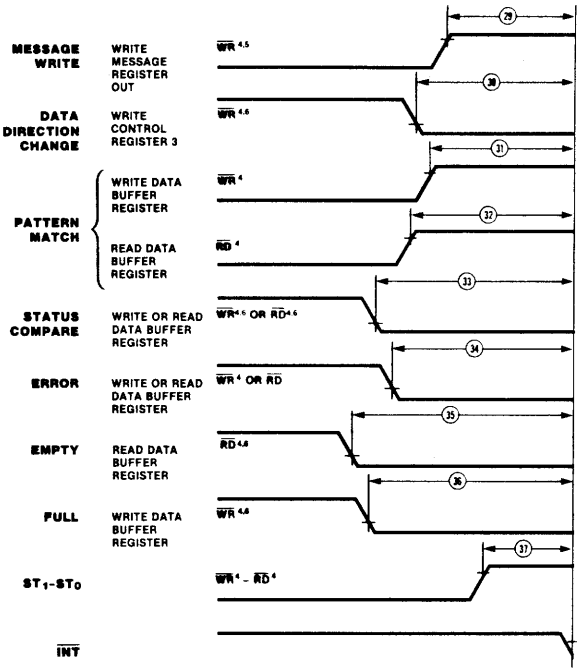
(Page 26)

The timing diagram for **Non-Z-BUS Interrupt Timing** is incorrect for parameters 29, 30, 35, and 36. A corrected version of the art follows.



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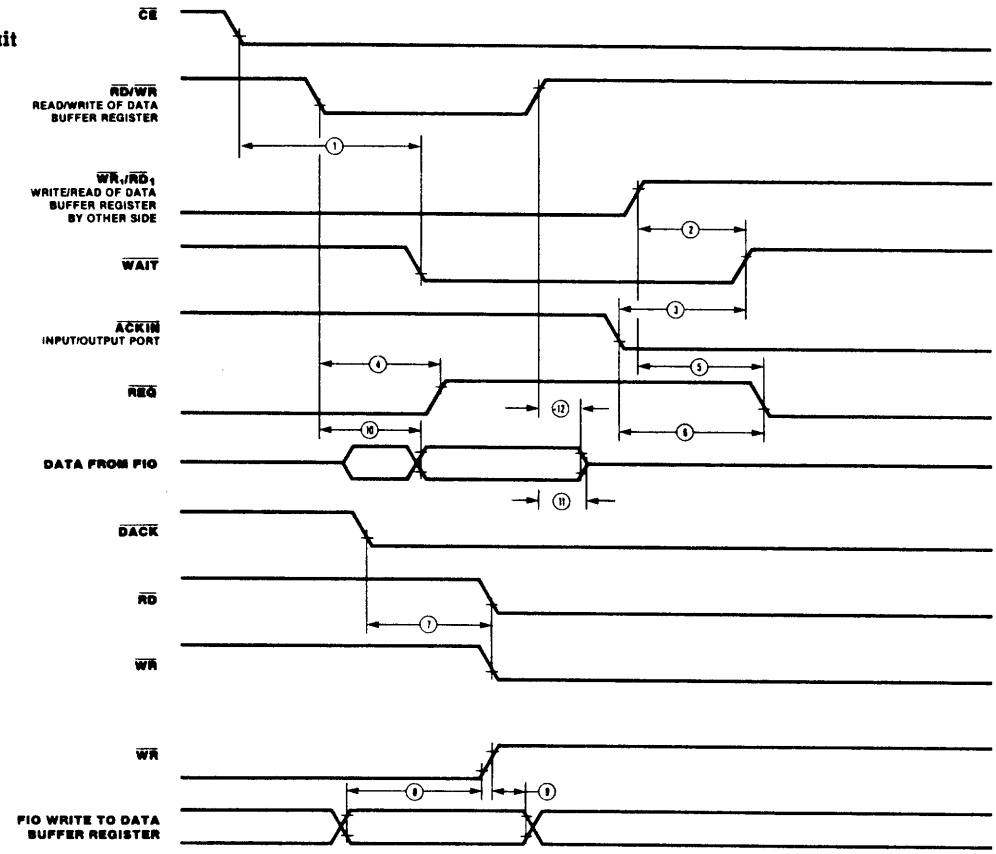
(Page 27)

In **Non-Z-BUS Request/Wait Timing,** number 1 parameter should read:

$\overline{CE}$ ↓ to $\overline{WAIT}$ Active.

The timing diagram is incorrect for parameter 1. A corrected version of the art follows.

Non-Z-BUS Request/Wait Timing



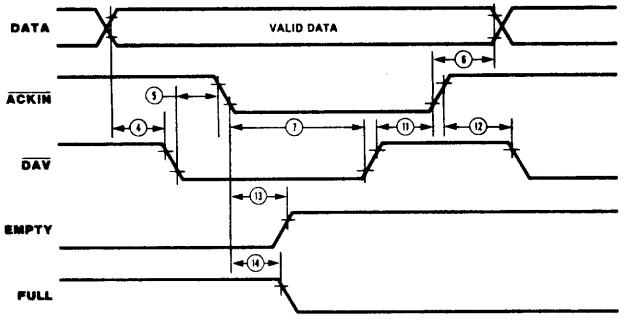
*Whichever signal is later

Page 223
(Page 29)

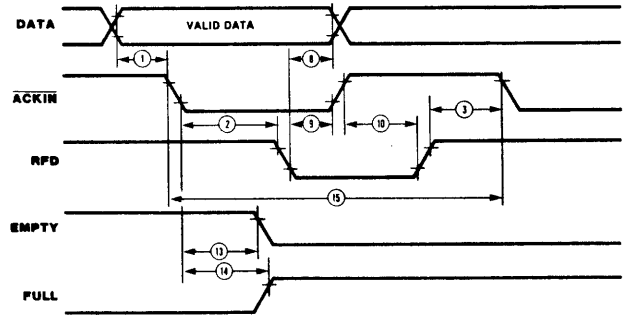
Add the following to the **PIO 2-Wire Handshake Timing** table:

Number	Symbol	Parameter	Min
13	TdACK(Empty)	ACKIN to Empty	
14	TdACK(Full)	ACKIN to Full	
15	ACKIN Clock Rate		1.0

Both timing diagrams are incorrect. Corrected versions of the art follow.



2-Wire Handshake (Port 2 Side Only) Output



2-Wire Handshake (Port 2 Side Only) Input

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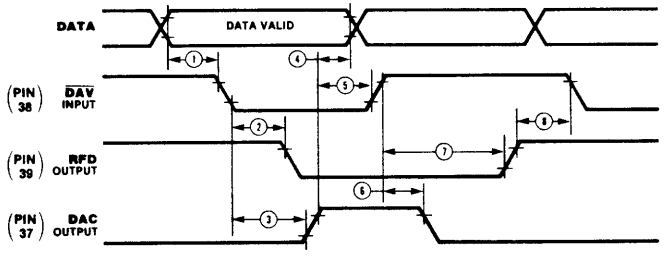
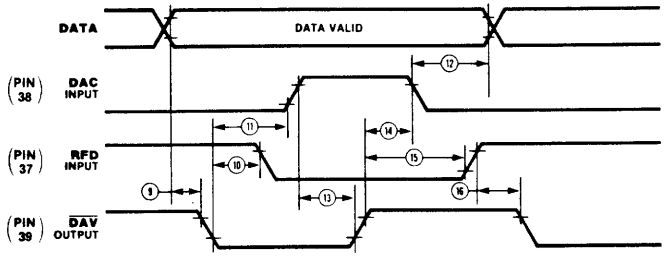
(Page 30)

To the timing diagrams for 3-Wire Handshake add the pin numbers as illustrated in the following corrected versions of the art.



3-Wire Handshake Input



3-Wire Handshake Output

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Delete from Ordering Information all Product Numbers, Package/Temp, Speed and Description Information. Delete from Product Numbers Z8038 and Z8038A the information in parentheses:

(Z-BUS compatible 40-pin).

Z8090 Z8000 Z-UPC
Product Specification

Odd Numbered
Pages 235-251

Should be labeled **Z-UPC** in the right-hand margin.

Page 237
(Page 5)

In the second column, paragraph 2, sentence 2, IRQ_6 should read IRQ_0.

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(Page 6)

In Block Access the first paragraph, sentences one and two should read:

> The master CPU may transmit or receive blocks of data via address xxx10101 (xx10101x shifted). When the master CPU accesses this address, the Z-UPC register pointed to by the Data Indirection register is decremented, for example, when the master CPU issues a read or write to address xxx10101 while the Data Indirection register contains the value 33H.

In Table 3, "Master CPU/Z-UPC Register Map," change Decimal line @5** to read:

Decimal	Hex	Identifier	No-Shift Address	Shift Address
@5**	@5H**		xxx10101	xx10101x

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(Page 10)

In the **Opcode Map,** Upper Nibble F, Lower Nibbles 0 and 1, should read 8,5 Execution and Pipeline Cycles rather than 6,7.

Page 244
(Page 12)

In Figure 12, "Port Mode Registers," R247 P3M, Port 3 Mode Register, for bit D_2, 1 P_{35} should read:

1 $P_{35} = \overline{INT}$.

R247 P3M
Port 3 Mode Register
Z-UPC register address (Hex): F7

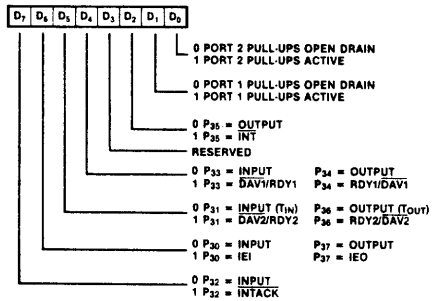

Figure 12. Port Mode Registers

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In Figure 16, "Master CPU-Z-UPC Data Transfer Registers," R0 DTC, the labels for D_2 and D_1 have been reversed. A corrected version of the art follows.

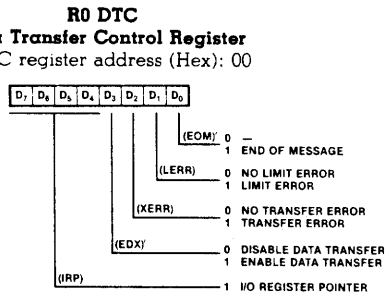

Figure 16. Master CPU-Z-UPC Data Transfer Registers

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(Page 14)

For **Control Register** $F7_H$ Comment $P3_5$ = INT should read $P3_5 = \overline{INT}$.

Page 247
(Page 15)

To **DC Characteristics** add the following note:

* For Protopak versions I_{CC} = 180 µA plus the current for the memory IC used.

Pages 248-250
(Page 16-18)

The timing tables for these pages have been revised and expanded to include the 6 MHz timing. Corrected versions of the tables follow.

Z-UPC Master CPU Interface Timing (Page 248)

No.	Symbol	Parameter	4 MHz Min(ns)	4 MHz Max(ns)	6 MHz Min(ns)	6 MHz Max(ns)	Notes*
1	TrC	Clock Rise Time		20		15	
2	TwCh	Clock High Width	105	1855	70	1855	
3	TfC	Clock Fall Time		20		10	
4	TwCl	Clock Low Width	105	1855	70	1855	
5	TpC	Clock Period	250	2000	165	2000	
6	TsCS(AS)	$\overline{CS}$ to $\overline{AS}$ ↑ Setup Time	0		0		1
7	ThCS(AS)	CS to AS ↑ Hold Time	60		40		1
8	TsA(AS)	Address to $\overline{AS}$ ↑ Setup Time	30		10		1
9	ThA(AS)	Address to $\overline{AS}$ ↑ Hold Time	50		30		1
10	TwAS	$\overline{AS}$ Low Width	70		50		
11	TdDS(DR)	$\overline{DS}$ ↑ to Read Data Not Valid	0		0		
12	TdDS(DRz)	$\overline{DS}$ ↑ to Read Data Float Delay		70		45	2
13	TdAS(DS)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ Delay	60	2095	40	2095	
14	TdDS(AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay	50		35		
15	ThDW(DS)	Write Data to $\overline{DS}$ ↑ Hold Time	30		20		1
16	TdDS(DR)	$\overline{DS}$ ↓ to Read Data Valid Delay					3
17	TdAz(DS)	Address Float to $\overline{DS}$ Delay	0		0		
18	TwDS	$\overline{DS}$ Low Width	390		250		
19	TsRWR(DS)	R/$\overline{W}$ (Read) to $\overline{DS}$ ↓ Setup Time	100		80		
20	TsRWW(DS)	R/$\overline{W}$ (Write) to $\overline{DS}$ ↓ Setup Time	0		0		
21	TsDW(DSf)	Write Data to $\overline{DS}$ ↓ Setup Time	30		20		
22	TdAS(W)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↓ Valid Delay		195		160	
23	ThRW(DS)	R/$\overline{W}$ to $\overline{DS}$ ↑ Hold Time	60		40		
24	TsDR(W)	Read Data Valid to $\overline{WAIT}$ ↑	0		0		

Z-UPC Interrupt Acknowledge Timing

24	TsIA(AS)	$\overline{INTACK}$ to $\overline{AS}$ ↑ Setup Time	0		0	
26	ThIA(AS)	$\overline{INTACK}$ to $\overline{AS}$ ↑ Hold Time	250		250	
27	TdAS(DSA)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ (Acknowledge) Delay	940		200	
28	TdDSA(DR)	$\overline{DS}$ ↓ (Acknowledge) to Read Data Valid Delay		360		180
29	TwDSA	$\overline{DS}$ ↓ (Acknowledge) Low Width	475		250	
30	TdAS(IEO)	$\overline{AS}$ ↑ to IEO Delay		290		250
31	TdIEIf(IEO)	IEI to IEO Delay		120		100
32	TsIEI(DSA)	IEI to $\overline{DS}$ ↓ (Acknowledge) Setup Time	150		120	
33	TdDS(INT)	$\overline{DS}$ ↓ to $\overline{INT}$ Delay		500		500
34	ThIEI(DS)	IEI to $\overline{DS}$ ↑ Hold Time	100		100	

NOTES:
1. Parameter does not apply to Interrupt Acknowledge transactions.
2. The maximum value for TdAS(DS) does not apply to Interrupt Acknowledge transactions.
3. This parameter is dependent on the state of UPC at the time of master CPU access.
4. The timing characteristics given reference 2.0 V as High and 0.8 V as Low.
5. All output ac parameters use test load 1.

*Timings are preliminary and subject to change.

Z-UPC Handshake Timing (Page 250)

No.	Symbol	Parameter	4 MHz Min(ns)	4 MHz Max(ns)	6 MHz Min(ns)	6 MHz Max(ns)	Notes*
1	TsDI(DA)	Data In Setup Time	0		0		
2	ThDA(DI)	Data In Hold Time	230		230		
3	TwDA	Data Available Width	175		175		1,2
4	TdDAL(RY)	Data Available Low To Ready Delay Time	20 0	175	20 0	175	1,2 2,3
5	TdDAH(RY)	Data Available High to Ready Delay Time	0	150	0	150	1,2 2,3
6	TdDO(DA)	Data Out to Data Available Delay Time	50		50		2
7	TdRY(DA)	Ready to Data Available Delay Time	0	205	0	205	2

Z-UPC Reset Timing

1	TdRDQ(WR)	Delay from DS ↑ to AS ↑ for No Reset	40		35		
2	TdWRQ(RD)	Delay from AS ↑ to DS ↓ for No Reset	50		35		
3	TwRES	Minimum Width of AS and DS both Low for Reset	250		250		4

Z-UPC RAM Version Program Memory Timing

1	TwMAS	Memory Address Strobe Width	60		55		5
2	TdA(MAS)	Address Valid to Memory Address Strobe ↑ Delay	30		30		5
3	TdMR/W(MAS)	Memory Read/Write to Memory Address Strobe ↑ Delay	30		30		5
4	TdMDS(A)	Memory Data Strobe ↑ to Address Change Delay	60		60		
5	TDMDS(MR/W)	Memory Data Strobe ↑ to Memory Read/Write Not Valid Delay	80		75		
6	Tw(MDS)	Memory Data Strobe Width (Write Case)	160		110		6
7	TdDO(MDS)	Data Out Valid to Memory Data Strobe ↓ Delay	30		30		5
8	TdMDS(DO)	Memory Data Strobe ↑ to Data Out Change Delay	30		30		5
9	Tw(MDS)	Memory Data Strobe Width (Read Case)	230		230		6
10	TdMDS(DI)	Memory Data Strobe ↓ to Data In Valid Delay		160		130	7
11	TdMAS(DI)	Memory Address Strobe ↑ to Data In Valid Delay		180		220	7
12	ThMDS(DI)	Memory Data Strobe ↑ to Data In Hold Time	0		0		
13	TwSY	Instruction Sync Out Width	160		100		
14	TdSY(MDS)	Instruction Sync Out to Memory Data Strobe Delay	200		160		
15	TwI	Interrupt Request via Port 3 Input Width	100		100		

NOTES:
1. Input Handshake.
2. Test Load 1.
3. Output Handshake.
4. Internal reset signal is 1/2 to 2 clock delays from external reset condition.
5. Delay times are specified for an input clock frequency of 4MHz. When operating at a lower frequency, the increase in input clock period must be added to the specified delay time.
6. Data strobe width is specified for an input clock frequency of 4 MHz. When operating at a lower frequency, the increase in three input clock periods must be added to the specified width. Data strobe width varies according to the instruction being executed.
7. Address strobe and data strobe to data in valid delay times represent memory system access times and are given for a 4 MHz input frequency.
8. All timing references assume 2.0 V for a logic "1" and 0.8 V for a logic "0".
9. All output ac parameters use test load 2.

*Timings are preliminary and subject to change.

Pages 274-278 (Pages 16-20)

The timing tables for this page have been revised and expanded to include the 6 MHz timing. Corrected versions of the tables follow.

SCC Read and Write Timing (Page 274)

No.	Symbol	Parameter	4 MHz Min(ns)	4 MHz Max(ns)	6 MHz Min(ns)	6 MHz Max(ns)	Notes*
1	TwPCl	PCLK Low Width	105	2000	70	1000	
2	TwPCh	PCLK High Width	105	2000	70	1000	
3	TfPC	PCLK Fall Time		20		10	
4	TrPC	PCLK Rise Time		20		15	
5	TcPC	PCLK Cycle Time	250	4000	165	2000	
6	TsA(WR)	Address to $\overline{WR}$ ↓ Setup Time	80		80		
7	ThA(WR)	Address to $\overline{WR}$ ↓ Hold Time	0		0		
8	TsA(RD)	Address to $\overline{RD}$ ↓ Setup Time	80		80		
9	ThA(RD)	Address to $\overline{RD}$ ↑ Hold Time	0		0		
10	TsIA(PC)	$\overline{INTACK}$ to PCLK ↑ Setup Time	0		0		
11	TsIAi(WR)	Intack to $\overline{WR}$ ↓ Setup Time	200		200		1
12	ThIA(WR)	$\overline{INTACK}$ to $\overline{WR}$ ↑ Hold Time	0		0		
13	TsIAi(RD)	Intack to $\overline{RD}$ ↓ Setup Time	200		200		1
14	ThIA(RD)	$\overline{INTACK}$ to $\overline{RD}$ ↑ Hold Time	0		0		
15	ThIA(PC)	$\overline{INTACK}$ to PCLK ↑ Hold Time	100		100		
16	TsCEl(WR)	$\overline{CE}$ Low to $\overline{WR}$ ↓ Setup Time	0		0		
17	ThCE(WR)	$\overline{CE}$ to $\overline{WR}$ ↑ Hold Time	0		0		
18	TsCEh(WR)	$\overline{CE}$ High to $\overline{WR}$ ↓ Setup Time	100		70		
19	TsCEl(RD)	$\overline{CE}$ Low to $\overline{RD}$ ↓ Setup Time	0		0		1
20	ThCE(RD)	$\overline{CE}$ to $\overline{RD}$ ↑ Hold Time	0		0		1
21	TsCEh(RD)	$\overline{CE}$ High to $\overline{RD}$ ↓ Setup Time	100		70		1
22	TwRDl	$\overline{RD}$ Low Width	390		250		1
23	TdRD(DRA)	$\overline{RD}$ ↓ to Read Data Active Delay	0		0		
24	TdRDr(DR)	$\overline{RD}$ ↑ to Read Data Not Valid Delay	0		0		
25	TdRDf(DR)	$\overline{RD}$ ↓ to Read Data Valid Delay		250		180	
26	TdRD(DRz)	$\overline{RD}$ ↑ to Read Data Float Delay		70		45	2

NOTES:
1. Parameter does not apply to Interrupt Acknowledge transactions.
2. Float delay is defined as the time required for a ±0.5 V change in the output with a maximum dc load and minimum ac load.

SCC Cycle Timing (Page 275)

No.	Symbol	Parameter	4 MHz Min(ns)	4 MHz Max(ns)	6 MHz Min(ns)	6 MHz Max(ns)	Notes*
27	TdA(DR)	Address Required Valid to Read Data Valid Delay		590		420	
28	TwWRl	$\overline{WR}$ Low Width	390		250		
29	TsDW(WR)	Write Data To $\overline{WR}$ ↓ Setup Time	0		0		
30	ThDW(WR)	Write Data to $\overline{WR}$ ↑ Hold Time	0		0		
31	TdWR(W)	$\overline{WR}$ ↓ to Wait Valid Delay		240		200	4
32	TdRD(W)	$\overline{RD}$ ↓ to Wait Valid Delay		240		200	4
33	TdWRf(REQ)	$\overline{WR}$ ↓ to W/$\overline{REQ}$ Not Valid Delay		240		200	
34	TdRDf(REQ)	$\overline{RD}$ ↓ to W/$\overline{REQ}$ Not Valid Delay		240		200	
35	TdWRr(REQ)	$\overline{WR}$ ↑ to $\overline{DTR}$/$\overline{REQ}$ Not Valid Delay		5TcPC +300		5TcPC +250	
36	TdRDr(REQ)	$\overline{RD}$ ↑ to $\overline{DTR}$/$\overline{REQ}$ Not Valid Delay		5TcPC +300		5TcPC +250	
37	TdPC(INT)	PCLK ↓ to $\overline{INT}$ Valid Delay		500		500	4
38	TdIAi(RD)	$\overline{INTACK}$ to $\overline{RD}$ ↓ (Acknowledge) Delay					5
39	TwRDA	$\overline{RD}$ (Acknowledge) Width	285		250		
40	TdRDA(DR)	$\overline{RD}$ ↓ (Acknowledge) to Read Data Valid Delay		190		180	
41	TsIEI(RDA)	IEI to $\overline{RD}$ ↓ (Acknowledge) Setup Time	120		100		
42	ThIEI(RDA)	IEI to $\overline{RD}$ ↑ (Acknowledge) Hold Time	0		0		
43	TdIEI(IEO)	IEI to IEO Delay Time		120		100	
44	TdPC(IEO)	PCLK ↑ to IEO Delay		250		250	
45	TdRDA(INT)	$\overline{RD}$ ↓ to $\overline{INT}$ Inactive Delay		500		500	4
46	TdRD(WRQ)	$\overline{RD}$ ↑ to $\overline{WR}$ ↓ Delay for No Reset	30		15		

No.	Symbol	Parameter	4 MHz Min(ns)	4 MHz Max(ns)	6 MHz Min(ns)	6 MHz Max(ns)	Notes*
47	TdWRQ(RD)	$\overline{WR}$ ↑ to $\overline{RD}$ ↓ Delay for No Reset	30		30		
48	TwRES	$\overline{WR}$ and $\overline{RD}$ Coincident Low for Reset	250		250		
49	Trc	Valid Access Recovery Time	6TcPC		6TcPC		
			+200		+130		3

NOTES:

3. Parameter applies only between transactions involving the SCC.
4. Open-drain output, measured with open-drain test load.
5. Parameter is system dependent. For any SCC in the daisy chain, TdIAi(RD) must be greater than the sum of TdPC(IEO) for the highest priority device in the daisy chain, TsIEI(RDA) for the SCC, and TdIEIf(IEO) for each device separating them in the daisy chain.

* Timings are preliminary and subject to change.

SCC General Timing (Page 276)

No.	Symbol	Parameter	4 MHz Min(ns)	4 MHz Max(ns)	6 MHz Min(ns)	6 MHz Max(ns)	Notes*
1	TdPC(REQ)	PCLK ↓ to $\overline{W}/\overline{REQ}$ Valid Delay		250		250	
2	TdPC(W)	PCLK ↓ to Wait Inactive Delay		350		350	
3	TsRXC(PC)	$\overline{RxC}$ ↑ to PCLK ↑ Setup Time	50		50		1,4
4	TsRXD(RXCr)	RxD to $\overline{RxC}$ ↑ Setup Time (X1 Mode)	0		0		1
5	ThRXD(RXCr)	RxD to $\overline{RxC}$ ↑ Hold Time (X1 Mode)	150		150		1
6	TsRXD(RXCf)	RxD to $\overline{RxC}$ ↓ Setup Time (X1 Mode)	0		0		1,5
7	ThRXD(RXCf)	RxD to $\overline{RxC}$ ↓ Hold Time (X1 Mode)	150		150		1,5
8	TsSY(RXC)	$\overline{SYNC}$ to $\overline{RxC}$ ↑ Setup Time	-200		-200		1
9	ThSY(RXC)	$\overline{SYNC}$ to $\overline{RXC}$ ↑ Hold Time	3TcPC		3TcPC		
			+200		+200		1
10	TsTXC(PC)	$\overline{TxC}$ ↓ to PCLK ↑ Setup Time	0		0		2,4
11	TdTXCf(TXD)	$\overline{TxC}$ ↓ to TxD Delay (X1 Mode)		300		300	2
12	TdTXCr(TXD)	$\overline{TxC}$ ↑ to TxD Delay (X1 Mode)		300		300	2,5
13	TdTXD(TRX)	TxD to $\overline{TRxC}$ Delay (Send Clock Echo)					
14	TwRTXh	$\overline{RTxC}$ High Width	180		180		
15	TwRTXl	$\overline{RTxC}$ Low Width	180		180		
16	TcRTX	$\overline{RTxC}$ Cycle Time	400		400		
17	TcRTXX	Cystal Oscillator Period	250	1000	250	1000	3
18	TwTRXh	$\overline{TRxC}$ High Width	180		180		
19	TwTRXl	$\overline{TRxC}$ Low Width	180		180		
20	TcTRX	$\overline{TrxC}$ Cycle Time	400		400		
21	TwEXT	$\overline{DCD}$ or $\overline{CTS}$ Pulse Width	200		200		
22	TwSY	$\overline{SYNC}$ Pulse Width	200		200		

NOTES:

1. RxC is $\overline{RTxC}$ or $\overline{TRxC}$, whichever is supplying the receive clock.
2. TxC is $\overline{TRxC}$ or $\overline{RTxC}$, whichever is supplying the transmit clock.
3. Both $\overline{RTxC}$ and $\overline{SYNC}$ have 30 pF capacitors to ground connected to them.
4. Parameter applies only if the data rate is one-fourth the PCLK rate. In all other cases, no phase relationship between $\overline{RxC}$ and PCLK or $\overline{TxC}$ and PCLK is required.
5. Parameter applies only to FM encoding/decoding.

*Timings are preliminary and subject to change.

SCC System Timing (Page 278)

No.	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	Units	Notes*
1	TdRXC(REQ)	$\overline{RxC}$ ↑ to $\overline{W}/\overline{REQ}$ Valid Delay	8	12	8	12	TcPC	2
2	TdRXC(W)	$\overline{RxC}$ ↑ to Wait Inactive Delay	8	12	8	12	TcPC	1,2
3	TdRXC(SY)	$\overline{RxC}$ ↑ to $\overline{SYNC}$ Valid Delay	4	7	4	7	TcPC	2
4	TdRXC(INT)	$\overline{RxC}$ ↑ to $\overline{INT}$ Valid Delay	10	16	10	16	TcPC	1,2
5	TdTXC(REQ)	$\overline{TxC}$ ↓ to $\overline{W}/\overline{REQ}$ Valid Delay	5	8	5	8	TcPC	3
6	TdTXC(W)	$\overline{TxC}$ ↓ to Wait Inactive Delay	5	8	5	8	TcPC	1,3
7	TdTXC(DRQ)	$\overline{TxC}$ ↓ to $\overline{DTR}/\overline{REQ}$ Valid Delay	4	7	4	7	TcPC	3
8	TdTXC(INT)	$\overline{TxC}$ ↓ to $\overline{INT}$ Valid Delay	6	10	6	10	TcPC	1,3
9	TdSY(INT)	$\overline{SYNC}$ Transition to $\overline{INT}$ Valid Delay	2	6	2	6	TcPC	1
10	TdEXT(INT)	$\overline{DCD}$ or $\overline{CTS}$ Transition to $\overline{INT}$ Valid Delay	2	6	2	6	TcPC	1

NOTES:

1. Open-drain output, measured with open-drain test load.
2. $\overline{RxC}$ is $\overline{RTxC}$ or $\overline{TRxC}$, whichever is supplying the receive clock.
3. $\overline{TxC}$ is $\overline{TRxC}$ or $\overline{RTxC}$, whichever is supplying the transmit clock.

*Timings are preliminary and subject to change.

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In Figure 10, "Counter/Timer Waveforms," the time constant line is incorrect between TC-2 and 1. A corrected version of the art follows.

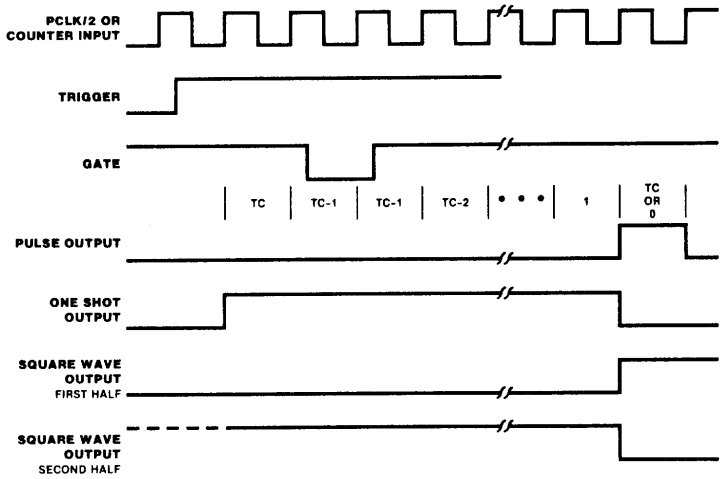

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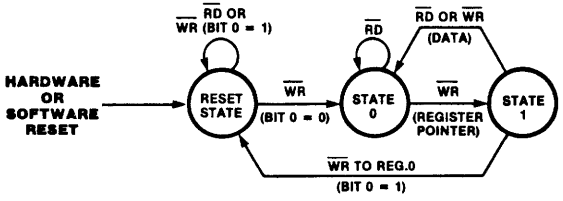
Figure 11, "State Machine Operation," is incorrect. A corrected version of the art follows.



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In Figure 13, "Port Specification Registers," Port Mode Specification Registers, Addresses should read:

100000A Port A
101000 Port B

Delete "Partial" from the parentheses; and change "PTS2" to "PTSO."

In Port Handshake Specifications Registers, the Addresses should read:

100001 Port A
101001 Port B

In Port Command and Status Registers, the Address should read:

001000 Port A
101001 Port B

In parentheses delete "Write" and add "Partial Write."

The format for this register is incorrect. A corrected version of the art follows.

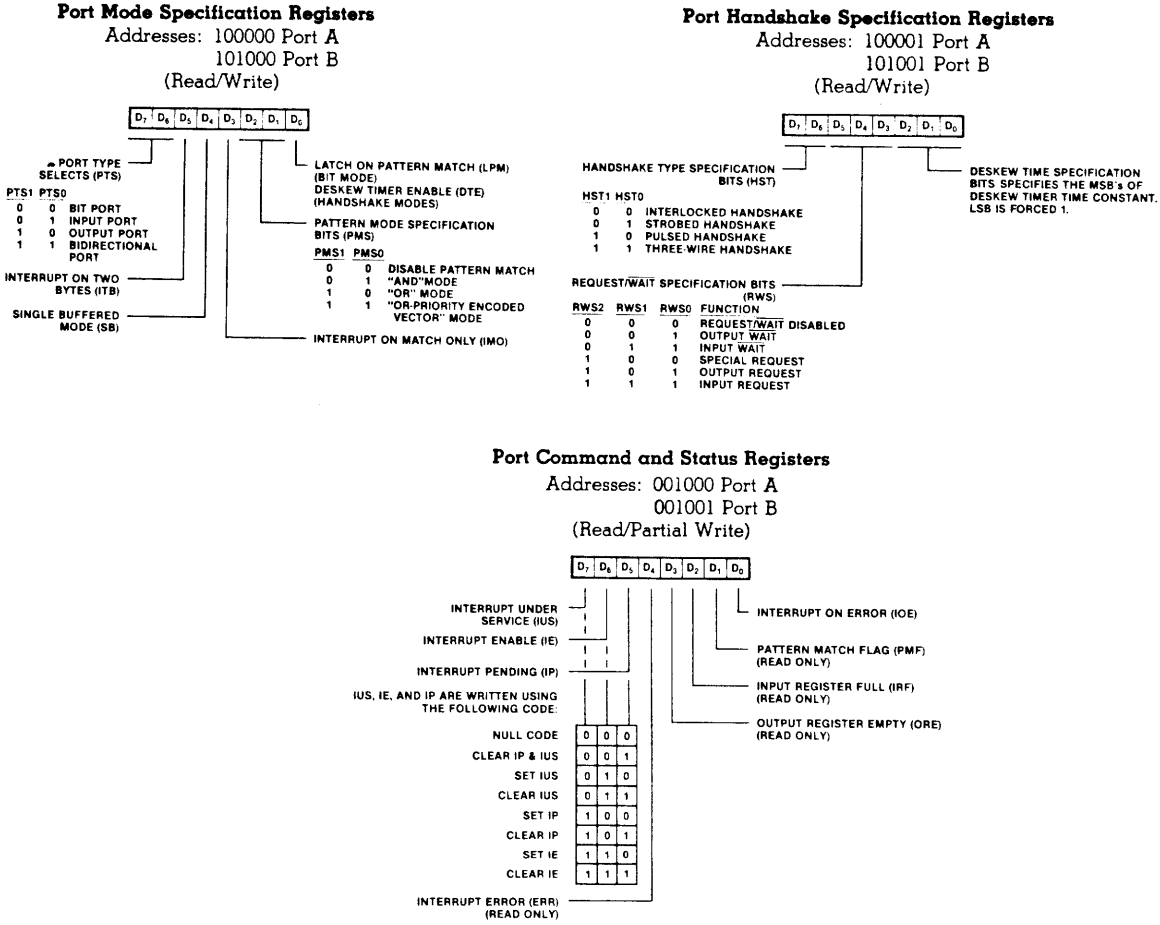

Figure 13. Port Specification Registers

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In Figure 17, "Counter/Timer Registers," the Counter/Timer Mode Command and Status Registers, the Address should read:

001010 Counter/Timer 1
001011 Counter/Timer 2
001100 Counter/Timer 3

In the same figure, Counter/Timer Mode Specifications Registers, the Addresses should read:

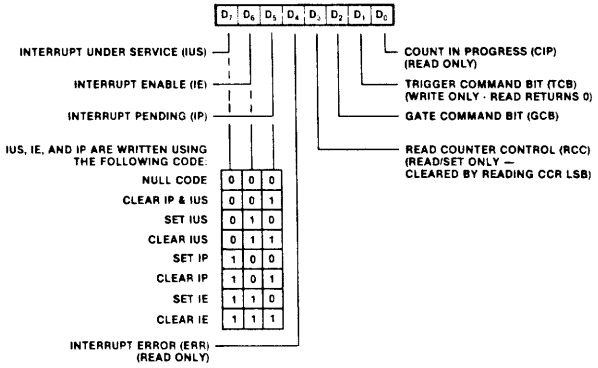
011100 Counter/Timer 1
011101 Counter/Timer 2
011110 Counter/Timer 3

Also, DSC1 should read DCS1.

A corrected version of the art follows.

Counter/Timer Command and Status Registers

Addresses: 001010 Counter/Timer 1
001011 Counter/Timer 2
001100 Counter/Timer 3
(Read/Partial Write)



Counter/Timer Mode Specification Registers

Addresses: 011100 Counter/Timer 1
011101 Counter/Timer 2
011110 Counter/Timer 3
(Read/Write)

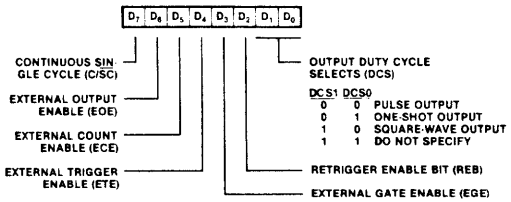


Figure 17. Counter/Timer Registers

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In the **Register Address Summary:**

Delete AD_7-AD_0 in all cases.
Delete the XX at the end of each address in all cases.

In **Most Often Accessed Registers** change Counter/Timer Control to Counter/Timer Command and Status in all cases. A corrected version of the table follows.

Register Address Summary

Main Control Registers

Address	Register Name
000000	Master Interrupt Control
000001	Master Configuration Control
000010	Port A's Interrupt Vector
000011	Port B's Interrupt Vector
000100	Counter/Timer's Interrupt Vector
000101	Port C's Data Path Polarity
000110	Port C's Data Direction
000111	Port C's Special I/O Control

Most Often Accessed Registers

Address	Register Name
001000	Port A's Command and Status
001001	Port B's Command and Status
001010	Counter/Timer 1's Command and Status
001011	Counter/Timer 2's Command and Status
001100	Counter/Timer 3's Command and Status
001101	Port A's Data (can be accessed directly)
001110	Port B's Data (can be accessed directly)
001111	Port C's Data (can be accessed directly)

Counter/Timer Related Registers

Address	Register Name
010000	Counter/Timer 1's Current Count-MSBs
010001	Counter/Timer 1's Current Count-LSBs
010010	Counter/Timer 2's Current Count-MSBs
010011	Counter/Timer 2's Current Count-LSBs
010100	Counter/Timer 3's Current Count-MSBs
010101	Counter/Timer 3's Current Count-LSBs
010110	Counter/Timer 1's Time Constant-MSBs
010111	Counter/Timer 1's Time Constant-LSBs
011000	Counter/Timer 2's Time Constant-MSBs
011001	Counter/Timer 2's Time Constant-LSBs
011010	Counter/Timer 3's Time Constant-MSBs
011011	Counter/Timer 3's Time Constant-LSBs
011100	Counter/Timer 1's Mode Specification
011101	Counter/Timer 2's Mode Specification
011110	Counter/Timer 3's Mode Specification
011111	Current Vector

Port A Specification Registers

Address	Register Name
100000	Port A's Mode Specification
100001	Port A's Handshake Specification
100010	Port A's Data Path Polarity
100011	Port A's Data Direction
100100	Port A's Special I/O Control
100101	Port A's Pattern Polarity
100110	Port A's Pattern Transition
100111	Port A's Pattern Mask

Port B Specification Registers

Address	Register Name
101000	Port B's Mode Specification
101001	Port B's Handshake Specification
101010	Port B's Data Path Polarity
101011	Port B's Data Direction
101100	Port B's Special I/O Control
101101	Port B's Pattern Polarity
101110	Port B's Pattern Transition
101111	Port B's Pattern Mask

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In **DC Characteristics** the Maximum rating for symbol I_{CC} should read 200.

Pages 298-304
(Pages 18-24)

The timing tables for these pages have been revised and expanded to include the 6 MHz timing. Corrected versions of the tables follow.

CIO CPU Interface Timing (Page 298)

No.	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	Units	Notes*
1	TcPC	PCLK Cycle Time	250	4000	165	4000	ns	
2	TwPCh	PCLK Width (High)	105	2000	70	2000	ns	
3	TwPCl	PCLK Width (Low)	105	2000	70	2000	ns	
4	TrPC	PCLK Rise Time		20		10	ns	
5	TfPC	PCLK Fall Time		20		15	ns	
6	TsIA(PC)	$\overline{INTACK}$ to PCLK ↑ Setup Time	100		100		ns	
7	ThIA(PC)	$\overline{INTACK}$ to PCLK ↑ Hold Time	0		0		ns	
8	TsIA(RD)	$\overline{INTACK}$ to $\overline{RD}$ ↓ Setup Time	200		200		ns	1
9	ThIA(RD)	$\overline{INTACK}$ to $\overline{RD}$ ↑ Hold Time	0		0		ns	
10	TsIA(WR)	$\overline{INTACK}$ to $\overline{WR}$ ↓ Setup Time	200		200		ns	
11	ThIA(WR)	$\overline{INTACK}$ to $\overline{WR}$ ↑ Hold Time	0		0		ns	
12	TsA(RD)	Address to $\overline{RD}$ ↓ Setup Time	80		80		ns	
13	ThA(RD)	Address to $\overline{RD}$ ↑ Hold Time	0		0		ns	
14	TsA(WR)	Address to $\overline{WR}$ ↓ Setup Time	80		80		ns	
15	ThA(WR)	Address to $\overline{WR}$ ↑ Hold Time	0		0		ns	
16	TsCEl(RD)	$\overline{CE}$ Low to $\overline{RD}$ ↓ Setup Time	0		0		ns	1
17	TsCEh(RD)	$\overline{CE}$ High to $\overline{RD}$ ↓ Setup Time	100		70		ns	1
18	ThCE(RD)	$\overline{CE}$ to $\overline{RD}$ ↑ Hold Time	0		0		ns	1
19	TsCEl(WR)	$\overline{CE}$ Low to $\overline{WR}$ ↓ Setup Time	0		0		ns	
20	TsCEh(WR)	$\overline{CE}$ High to $\overline{WR}$ ↓ Setup Time	100		70		ns	
21	ThCE(WR)	$\overline{CE}$ to $\overline{WR}$ ↑ Hold Time	0		0		ns	
22	TwRDl	$\overline{RD}$ Low Width	390		250		ns	1
23	TdRD(DRA)	$\overline{RD}$ ↓ to Read Data Active Delay	0		0		ns	
24	TdRDf(DR)	$\overline{RD}$ ↓ to Read Data Valid Delay		250		180	ns	
25	TdRDr(DR)	$\overline{RD}$ ↑ to Read Data Not Valid Delay	0		0		ns	
26	TdRD(DRz)	$\overline{RD}$ ↑ to Read Data Float Delay		70		45	ns	2
27	TwWRl	$\overline{WR}$ Low Width	390		250		ns	
28	TsDW(WR)	Write Data to $\overline{WR}$ ↓ Setup Time	0		0		ns	
29	ThDW(WR)	Write Data to $\overline{WR}$ ↑ Hold Time	0		0		ns	
30	Trc	Valid Access Recovery Time	1000*		650*		ns	3
		CIO Interrupt Timing						
31	TdPM(INT)	Pattern Match to $\overline{INT}$ Delay (Bit Port)		2		2	TcPC +ns	
32	TdACK(INT)	$\overline{ACKIN}$ to $\overline{INT}$ Delay (Port with Handshake)		10		10	TcPC +ns	4
33	TdCI(INT)	Counter Input to $\overline{INT}$ Delay (Counter Mode)		2		2	TcPC +ns	
34	TdPC(INT)	PCLK to $\overline{INT}$ Delay (Timer Mode)		3		3	TcPC +ns	
		CIO Interrupt Acknowledge Timing						
35	TsIA(RDA)	$\overline{INTACK}$ to $\overline{RD}$ ↓ (Acknowledge) Setup Time	350		250		ns	5
36	TwRDA	$\overline{RD}$ (Acknowledge) Width	350		250		ns	
37	TdRDA(DR)	$\overline{RD}$ ↓ (Acknowledge) to Read Data Valid Delay		250		180	ns	
38	TdIA(IEO)	$\overline{INTACK}$ ↓ to IEO ↓ Delay		350		250	ns	5
39	TdIEI(IEO)	IEI to IEO Delay		150		100	ns	5
40	TsIEI(RDA)	IEI to $\overline{RD}$ ↓ (Acknowledge) Setup Time	100		70		ns	5
41	ThIEI(RDA)	IEI to $\overline{RD}$ ↑ (Acknowledge) Hold Time	100		70		ns	
42	TdRDA(INT)	$\overline{RD}$ ↓ (Acknowledge) to $\overline{INT}$ ↑ Delay		600		600	ns	

NOTES:

1. Parameter does not apply to Interrupt Acknowledge transactions.
2. Float delay is measured to the time when the output has changed 0.5 V with minimum ac load and maximum dc load.
3. Trc is the specified number or 3 TcPC, whichever is longer.
4. The delay is from $\overline{DAV}$ ↓ for 3-Wire Input Handshake. The delay is from DAC ↓ for 3-Wire Output Handshake.
5. The parameters for the devices in any particular daisy chain must meet the following constraint: The delay from $\overline{INTACK}$ ↓ to $\overline{RD}$ ↓ must be greater than the sum of TdIA(IEO) for the highest priority peripheral, TsIEI(RDA) for the lowest priority peripheral, and TdIEI(IEO) for each peripheral separating them in the chain.

*Timings are preliminary and subject to change. All timing references assume 2.0 V for a logic "1" and 0.8 V for a logic "0".

CIO Handshake Timing (Page 300)

No.	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	Units	Notes*
1	TsDI(ACK)	Data Input to $\overline{ACKIN}$ ↓ Setup Time	0		0		ns	
2	ThDI(ACK)	Data Input to $\overline{ACKIN}$ ↓ Hold Time--Strobed Handshake					ns	
3	TdACKf(RFD)	$\overline{ACKIN}$ ↓ to RFD ↓ Delay	0		0		ns	
4	TwACKl	$\overline{ACKIN}$ Low Width--Strobed Handshake					ns	
5	TwACKh	$\overline{ACKIN}$ High Width--Strobed Handshake					ns	
6	TdRFDr(ACK)	RFD ↑ to $\overline{ACKIN}$ ↓ Delay	0		0		ns	
7	TsDO(DAV)	Data Out to $\overline{DAV}$ ↓ Setup Time	25		20		ns	1
8	TdDAVf(ACK)	$\overline{DAV}$ ↓ to $\overline{ACKIN}$ ↓ Delay	0		0		ns	
9	ThDO(ACK)	Data Out to $\overline{ACKIN}$ ↓ Hold Time	2		2		TcPC	
10	TdACK(DAV)	$\overline{ACKIN}$ ↓ to $\overline{DAV}$ ↑ Delay	2		2		TcPC	
11	ThDI(RFD)	Data Input to RFD ↓ Hold Time--Interlocked Handshake	0		0		ns	
12	TdRFDf(ACK)	RFD ↓ to $\overline{ACKIN}$ ↑ Delay Interlocked Handshake	0		0		ns	
13	TdACKr(RFD)	$\overline{ACKIN}$ ↑ ($\overline{DAV}$ ↑) to RFD ↑ Delay--Interlocked and 3-Wire Handshake	0		0		ns	
14	TdDAVr(ACK)	$\overline{DAV}$ ↑ to $\overline{ACKIN}$ ↑ (RFD ↑)--Interlocked and 3-Wire Handshake	0		0		ns	
15	TdACK(DAV)	$\overline{ACKIN}$ ↑ (RFD ↑) to $\overline{DAV}$ ↓ Delay--Interlocked and 3-Wire Handshake	0		0		ns	
16	TdDAVIf(DAC)	$\overline{DAV}$ ↓ to DAC ↑ Delay--Input 3-Wire Handshake	0		0		ns	
17	ThDI(DAC)	Data Input to DAC ↑ Hold Time--3-Wire Handshake	0		0		ns	
18	TdDACOr(DAV)	DAC ↑ to $\overline{DAV}$ ↑ Delay--Input 3-Wire Handshake	0		0		ns	
19	TdDAVIr(DAC)	$\overline{DAV}$ ↑ to DAC ↓ Delay--Input 3-Wire Handshake	0		0		ns	
20	TdDAVOf(DAC)	$\overline{DAV}$ ↓ to DAC ↑ Delay--Output 3-Wire Handshake	0		0		ns	
21	ThDO(DAC)	Data Output to DAC ↑ Hold Time--3-Wire Handshake	2		2		TcPC	
22	TdDACIr(DAV)	DAC ↑ to $\overline{DAV}$ ↑ Delay--Output 3-Wire Handshake	2		2		TcPC	
23	TdDAVOr(DAC)	$\overline{DAV}$ ↑ to DAC ↓ Delay--Output 3-Wire Handshake	0		0		ns	

NOTES:
1. This time can be extended through the use of deskew timers.

*Timings are preliminary and subject to change.

All timing references assume 2.0 V for a logic "1" and 0.8 V for a logic "0".

CIO Counter/Timer Timing (Page 302)

No.	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	Units	Notes*
1	TcCI	Counter Input Cycle Time	500		330		ns	
2	TCIh	Counter Input High Width	230		150		ns	
3	TwCIl	Counter Input Low Width	230		150		ns	
4	TfCI	Counter Input Fall Time		20		15	ns	
5	TrCI	Counter Input Rise Time		20		15	ns	
6	TsTI(PC)	Trigger Input to PCLK ↓ Setup Time (Timer Mode)					ns	1
7	TsTI(CI)	Trigger Input to Counter Input ↓ Setup Time (Counter Mode)					ns	1
8	TwTI	Trigger Input Pulse Width (High or Low)					ns	
9	TsGI(PC)	Gate Input to PCLK ↓ Setup Time (Timer Mode)					ns	1
10	TsGI(CI)	Gate Input to Counter Input ↓ Setup Time (Counter Mode)					ns	1
11	ThGI(PC)	Gate Input to PCLK ↓ Hold Time (Timer Mode)					ns	1
12	ThGI(CI)	Gate Input to Counter Input ↓ Hold Time (Counter Mode)					ns	1

No.	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	Units	Notes*
13	TdPC(CO)	PCLK to Counter Output Delay (Timer Mode)					ns	
14	TdCI(CO)	Counter Input to Counter Output Delay (Counter Mode)					ns	

NOTES:
1. These parameters must be met to guarantee trigger or gate are valid for the next counter/timer cycle.

*Timings are preliminary and subject to change. All timing references assume 2.0 V for a logic "1" and 0.8 V for a logic "0".

CIO Request/Wait Timing (Page 303)

No.	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	Units	Notes*
1	TdRD(REQ)	$\overline{RD}$ ↓ to REQ ↓ Delay					ns	
2	TdRD(WAIT)	$\overline{RD}$ ↓ to $\overline{WAIT}$ ↓ Delay					ns	
3	TdWR(REQ)	$\overline{WR}$ ↓ to REQ ↓ Delay					ns	
4	TdWR(WAIT)	$\overline{WR}$ ↓ to $\overline{WAIT}$ ↓ Delay					ns	
5	TdPC(REQ)	PCLK ↓ to REQ ↑ Delay					ns	
6	TdPC(WAIT)	PCLK ↓ to $\overline{WAIT}$ ↑ Delay					ns	
7	TdACK(REQ)	$\overline{ACKIN}$ ↓ to REQ ↑ Delay					TcPC +ns	1
8	TdACK(WAIT)	$\overline{ACKIN}$ ↓ to $\overline{WAIT}$ ↑ Delay					TcPC +ns	1

NOTES:
1. The delay is from DAV ↓ for 3-Wire Input Handshake. The delay is from DAC ↓ for 3-Wire Output Handshake.

*Timings are preliminary and subject to change. All timing references assume 2.0 V for a logic "1" and 0.8 V for a logic "0".

CIO Reset Timing

1	TdRD(WR)	Delay from $\overline{RD}$ ↑ to $\overline{WR}$ ↓ for No Reset	50		50		ns	
2	TdWR(RD)	Delay from $\overline{WR}$ ↑ to $\overline{RD}$ ↓ for No Reset	50		50		ns	
3	TwRES	Minimum Width of $\overline{RD}$ and $\overline{WR}$ both Low for Reset	250		250		ns	

*Timings are preliminary and subject to change. All timing references assume 2.0 V for a logic "1" and 0.8 V for a logic "0".

CIO Miscellaneous Port Timing (Page 304)

No.	Symbol	Parameter	4 MHz Min	4 MHz Max	6 MHz Min	6 MHz Max	Units	Notes*
1	TrI	Any Input Rise Time		100		100	ns	
2	TfI	Any Input Fall Time		100		100	ns	
3	Tw1's	1's Catcher High Width	250		170		ns	1
4	TwPM	Pattern Match Input Valid (Bit Port)	750		500		ns	
5	TsPMD	Data Latched on Pattern Match Setup Time (Bit Port)	0		0		ns	
6	ThPMD	Data Latched on Pattern Match Hold Time (Bit Port)	1000		650		ns	

NOTES:
1. If the input is programmed inverting, a Low-going pulse of the same width will be detected.

*Timings are preliminary and subject to change. All timing references assume 2.0 V for a logic "1" and 0.8 V for a logic "0".

Z8590 UPC
Product Specification

Page 310 (Page 6) — Same as Page 238.

Page 314 (Page 10) — In the **Opcode Map,** Upper Nibble F, Lower Nibbles 0 and 1 should read 8,5 Execution and Pipeline Cycles rather than 6,7.

Page 316
(Page 12)

Same as Page 244.

R247 P3M
Port 3 Mode Register
UPC register address (Hex): F7

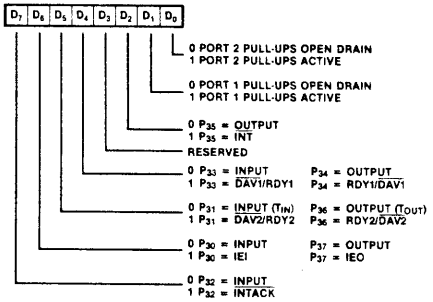


Figure 12. Port Mode Registers

Page 320
(Page 16)

The timing tables on this page have been revised and expanded to include the 6 MHz timing. A corrected version of the tables follow.

UPC Master CPU Interface Timing (Page 320)

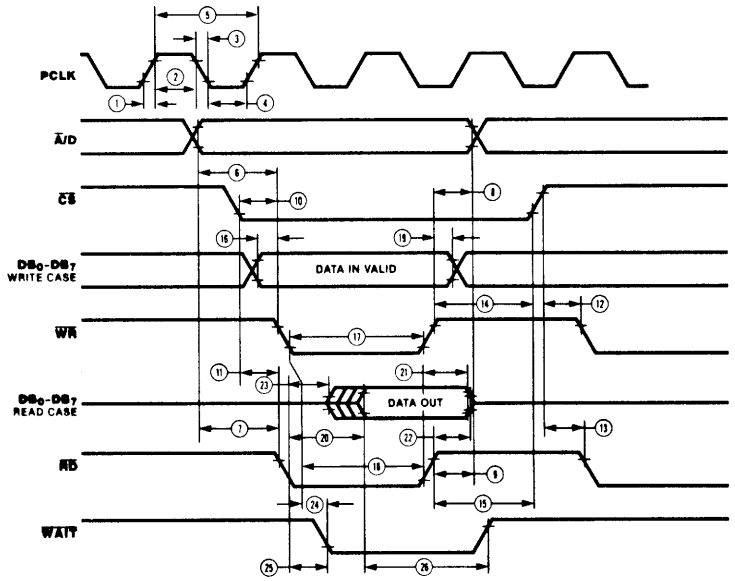
No.	Symbol	Parameter	4 MHz Min(ns)	4 MHz Max(ns)	6 MHz Min(ns)	6 MHz Max(ns)	Notes*
1	TrC	Clock Rise Time		20		15	
2	TwCh	Clock High Width	105	1855	70	1855	
3	TfC	Clock Fall Time		20		10	
4	TwCl	Clock Low Width	105	1855	70	1855	
5	TpC	Clock Period	250	2000	165	2000	
6	TsA/D(WR)	A/D to $\overline{WR}$ ↓ Setup Time	80		80		
7	TsA/D(RD)	A/D to $\overline{RD}$ ↓ Setup Time	80		80		
8	ThA/D(WR)	A/D to $\overline{WR}$ ↑ Hold Time	30		25		
9	ThA/D(RD)	A/D to $\overline{RD}$ ↑ Hold Time	30		25		
10	TsCSf(WR)	$\overline{CS}$ ↓ to $\overline{WR}$ ↓ Setup Time	0		0		
11	TsCSf(RD)	$\overline{CS}$ ↓ to $\overline{RD}$ ↓ Setup Time	0		0		
12	TsCSr(WR)	$\overline{CS}$ ↑ to $\overline{WR}$ ↓ Setup Time	60		60		
13	TsCSr(RD)	$\overline{CS}$ ↑ to $\overline{RD}$ ↓ Setup Time	60		60		
14	ThCS(WR)	$\overline{CS}$ to $\overline{WR}$ ↓ Hold Time	0		0		
15	ThCS(RD)	$\overline{CS}$ to $\overline{RD}$ ↓ Hold Time	0		0		
16	TsDI(WR)	Data in to $\overline{WR}$ ↓ Setup Time	0		0		
17	Tw(WR)	$\overline{WR}$ Low Width	390		250		
18	Tw(RD)	$\overline{RD}$ Low Width	390		250		
19	ThWR(DI)	Data in to $\overline{WR}$ ↑ Hold Time	0		0		
20	TdRD(DI)	Data Valid from $\overline{RD}$ ↓ Delay					1
21	ThRD(DI)	Data Valid to $\overline{RD}$ ↑ Hold Time	0		0		
22	$TdRD(DI_Z)$	Data Bus Float Delay from $\overline{RD}$ ↑		70		45	
23	$TdRD(DB_A)$	$\overline{RD}$ ↓ to Read Data Active Delay	0		0		
24	TdWR(W)	$\overline{WR}$ ↓ to $\overline{WAIT}$ ↓ Delay		150		150	
25	TdRD(W)	$\overline{RD}$ ↓ to $\overline{WAIT}$ ↓ Delay		150		150	
26	TdDI(W)	Data Valid to $\overline{WAIT}$ ↑ Delay	0		0		
		UPC Interrupt Acknowledge Transactions					
27	TsACK(RD)	$\overline{INTACK}$ ↓ to $\overline{RD}$ ↓ Setup Time	90		80		2
28	TdRD(DI)	$\overline{RD}$ ↓ to Vector Valid Delay		255		180	
29	ThRD(ACK)	$\overline{RD}$ ↑ to $\overline{INTACK}$ ↑ Hold Time	0		0		
30	ThIEI(RD)	IEI to $\overline{RD}$ ↑ Hold Time	100		100		
31	TwRDl	$\overline{RD}$ (Acknowledge) Low Width	255		250		
32	TdIEI(IEO)	IEI to IEO Delay		120		100	
33	TsIEI(RD)	IEI to $\overline{RD}$ ↓ Setup Time	150		120		
34	$TdACK_f(IEO)$	$\overline{INTACK}$ ↓ to IEO ↓ Delay		250		250	
35	$TdACK_r(IEO)$	$\overline{INTACK}$ ↑ to IEO ↑ Delay		250		250	

NOTES:
1. This parameter is dependent on the state of the UPC at the time of master CPU access.
2. In case where daisy chain is not used.
3. The timing characteristics given reference 2.0 V as High and 0.8 V as Low.
4. All output ac parameters use test load 1.

*Timings are preliminary and subject to change.

Page 321
(Page 17)

In the **Master CPU Interface Timing** the top trace is incorrect. Lines DB_0-DB_7 Write Case and DB_0-DB_7 Read Case have Data In and Data Out Valid reversed. A corrected version of the art follows.



Page 322
(Page 18)

The timing tables on this page have been revised and expanded to include the 6 MHz timing. A corrected version of the tables follow.

UPC Handshake Timing (Page 322)

No.	Symbol	Parameter	4 MHz Min(ns)	4 MHz Max(ns)	6 MHz Min(ns)	6 MHz Max(ns)	Notes*
1	TsDI(DA)	Data in Setup Time	0		0		
2	ThDA(DI)	Data in Hold Time	230		230		
3	TwDA	Data Available Width	175		175		1,2
4	TdDAL(RY)	Data Available Low to Ready Delay Time	20 0	175	20 0	175	1,2 2,3
5	TdDAH(RY)	Data Available High to Ready Delay Time	0	150	0	150	1,2 2,3
6	TdDO(DA)	Data Out to Data Available Delay Time	50		50		2
7	TdRY(DA)	Ready to Data Available Delay Time	0	205	0	205	2

UPC Reset Timing

No.	Symbol	Parameter	4 MHz Min(ns)	4 MHz Max(ns)	6 MHz Min(ns)	6 MHz Max(ns)	Notes*
1	TdRDQ(WR)	Delay from RD ↑ to WR ↓ for No Reset	40		35		
2	TdWRQ(RD)	Delay from WR ↑ to RD ↓ for No Reset	50		35		
3	TwRES	Minimum Width of WR and RD both Low for Reset	250		250		4

UPC RAM Version Program Memory Timing

No.	Symbol	Parameter	4 MHz Min(ns)	4 MHz Max(ns)	6 MHz Min(ns)	6 MHz Max(ns)	Notes*
1	TwMAS	Memory Address Strobe Width	60		55		5
2	TdA(MAS)	Address Valid to Memory Address Strobe ↑ Delay	30		30		5
3	TdMR/W (MAS)	Memory Read/Write to Memory Address Strobe ↑ Delay	30		30		5
4	TdMDS(A)	Memory Data Strobe ↑ to Address Change Delay	60		60		
5	TdMDS (MR/W)	Memory Data Strobe ↑ to Memory Read/Write Not Valid Delay	80		75		
6	Tw(MDS)	Memory Data Strobe Width (Write Case)	160		110		6
7	TdDO(MDS)	Data Out Valid to Memory Data Strobe ↓ Delay	30		30		5
8	TdMDS(DO)	Memory Data Strobe ↑ to Data Out Change Delay	30		30		5
9	Tw(MDS)	Memory Data Strobe Width (Read Case)	230		230		6
10	TdMDS(DI)	Memory Data Strobe ↓ to Data In Valid Delay		160		130	7
11	TdMAS(DI)	Memory Address Strobe ↑ to Data In Valid Delay		280		220	7
12	ThMDS(DI)	Memory Data Strobe ↑ to Data In Hold Time	0		0		
13	TwSY	Instruction Sync Out Width	160		100		
14	TdSY(MDS)	Instruction Sync Out to Memory Data Strobe Delay	200		160		
15	TwI	Interrupt Request via Port 3 Input Width	100		100		

NOTES:

1. Input Handshake.
2. Test Load 1.
3. Output Handshake.
4. Internal reset signal is 1/2 to 2 clock from external reset condition.
5. Delay times are specified for an input clock frequency of 4 MHz. When operating at a lower frequency, the increase in input clock period must be added to the specified delay time.
6. Data strobe width is specified for an input clock frequency of 4 MHz. When operating at a lower frequency, the increase in three input clock periods must be added to the specified width. Data strobe width varies according to the instruction being executed.
7. Address strobe and data strobe to data in valid delay times represent memory system access times and are given for a 4 MHz input frequency.
8. All timing references assume 2.0 V for a logic "1" and 0.8 V for a logic "0".
9. All output ac parameters use test load 2.

*Timings are preliminary and subject to change.

Page 329

Figure 2 should be entitled "Z8601 MCU Pin Assignments."

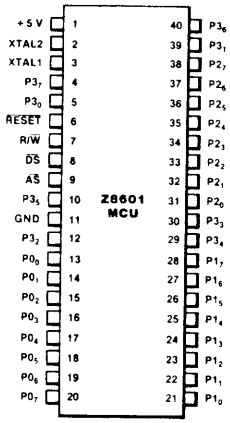


Figure 2. Z8601 MCU Pin Assignments

Page 340

In the **Opcode Map,** Upper Nibble F, Lower Nibbles 0 and 1 should read 8,5 Execution and Pipeline Cycles rather than 6,7.

Page 342

In **External I/O or Memory Read and Write Timing** the Minimum value of Number 2 should read 70; the Maximum value of Number 3 should read 360.

Z8 Family of Microcomputers Z8611/Z8612/Z8613 Product Specification

Page 353

The part number in the photograph should read "Z8613".

Page 358

Same as Page 340 above.

Page 360

Same as Page 342 above.

Z8 Family Z8681 Microcomputers Product Brief

Pages 366-367 (Page 2)

Switch the titles for Figures 3 and 4.

Page 369

Delete the number "3" from the chapter heading.

Z6132 4K x 8 Quasi-Static RAM Product Specification

Page 375 (Page 5)

The following changes should be made in the **AC Electrical Characteristics** table:

Number	Z6132-3[7] Min (ns)	Z6132-3[7] Max (ns)	Z6132-4 Min (ns)	Z6132-4 Max (ns)	Z6132-5 Min (ns)	Z6132-5 Max (ns)	Z6132-6 Min (ns)	Z6132-6 Max (ns)
1					750		900	
11			-10		-10		-10	
15	15	45	15	55	15	65	15	75
16	15	45	15	55	15	65	15	75

Page 376 (Page 6)

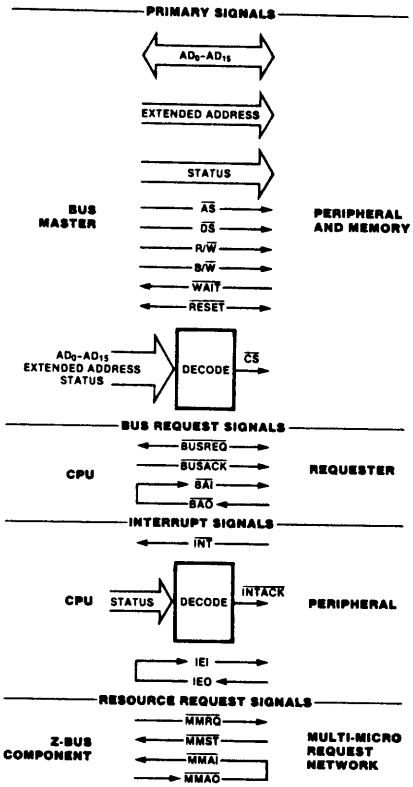
In **Power-Up,** the second sentence should read as follows:

> Moreover, the 6132 requires thirty-two selected or deselected memory cycles before proper operation is attained.

Z-BUS Component
Interconnect Summary

Page 381

In Figure 1, "Z-BUS Signals," delete CLOCK. A corrected version of the art follows.



Page 383

Delete the Clock entry.

Page 384

Delete the Clock entry in the table.

Delete note #14.

Insert after note #13:

$\overline{\square}$ = No connection

Page 389

Delete all **Bus Requests** text and Figure 7, "Bus Request Protocol." Add the following text and corrected art:

BUS REQUESTS

Figure 6a shows how the bus request lines connect bus requesters and the CPU on a Z-BUS. Figure 7 shows the states of the bus request mechanism as the Z-BUS is acquired, used, and released.

To generate transactions on the bus, a bus requester must gain control of the bus by making a bus request. This is done by pulling down $\overline{\text{BUSREQ}}$. A bus request can be made in either of two cases:

- $\overline{\text{BUSREQ}}$ is initially High and $\overline{\text{BAI}}$ is High, indicating that the bus is controlled by the CPU and no other requester is requesting the bus.

- $\overline{\text{BAI}}$ is High and the requester had wanted to request the bus at the time of the last Low to High transition of $\overline{\text{BUSREQ}}$. This insures that a module will not be locked out indefinitely by a higher priority bus requester.

After $\overline{\text{BUSREQ}}$ is pulled Low, the Z-BUS CPU relinquishes the bus and indicates this condition by making $\overline{\text{BUSACK}}$ Low. The Low on $\overline{\text{BUSACK}}$ is propagated through the $\overline{\text{BAI}}/\overline{\text{BAO}}$ daisy chain (Figure 6a). BAI follows BAO for components not requesting the bus, and any component requesting the bus holds its $\overline{\text{BAO}}$ High, thereby locking out all lower priority requesters. A bus requester gains control of the bus when its $\overline{\text{BAI}}$ input goes Low. When it is ready to relinquish the bus, it stops pulling BUSREQ Low and allows BAO to follow $\overline{\text{BAI}}$. This permits lower priority devices that made simultaneous requests to gain control of the bus. When all simultaneously requesting devices have relinquished the bus, and the Low on $\overline{\text{BAI}}/\overline{\text{BAO}}$ has propagated to the lowest priority requester, $\overline{\text{BUSREQ}}$ goes High, returning control of the bus to the CPU.

The CPU responds to the High on $\overline{\text{BUSREQ}}$ by driving $\overline{\text{BUSACK}}$ High. The High on $\overline{\text{BUSACK}}$ is propagated down the $\overline{\text{BAI}}/\overline{\text{BAO}}$ daisy chain, thus allowing bus requesters to make new bus requests. Because high priority bus requesters can pull $\overline{\text{BUSREQ}}$ Low before low priority devices have a High on $\overline{\text{BAI}}$, a way is needed for low priority devices to request the bus when $\overline{\text{BUSREQ}}$ is Low. That is provided by the rule that a requester may request the bus if $\overline{\text{BAI}}$ is High and it had wanted the bus at the time the last Low to High transition on $\overline{\text{BUSREQ}}$.

As soon as $\overline{BUSREQ}$ is pulled Low by any requester, each of the other requesters on the bus drives $\overline{BUSREQ}$ Low and continues to do so until it drives its $\overline{BAO}$ output Low. This provides a handshake between the CPU and the bus requesters by insuring that $\overline{BUSREQ}$ will not go High until the CPU's acknowledgement of $\overline{BUSACK}$ has reached every requester. Bus requesters can therefore run asynchronously to the CPU. This rule also allows the bidirectional $\overline{BUSREQ}$ line to be buffered using the logic shown in Figure 6b. This logic is similar to the logic inside a bus requester that keeps $\overline{BUSREQ}$ Low when it has initially been pulled Low by a different requester.

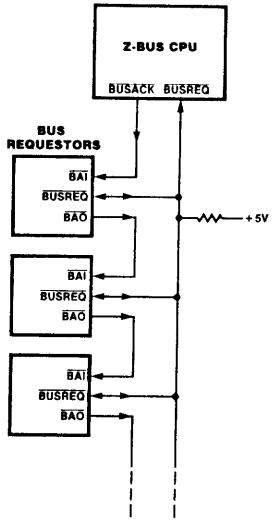


Figure 6a. Bus Request Connections

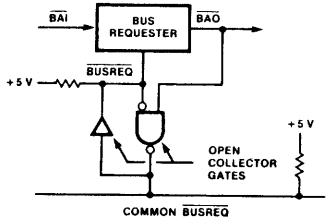


Figure 6b. Bus Request Line Buffering

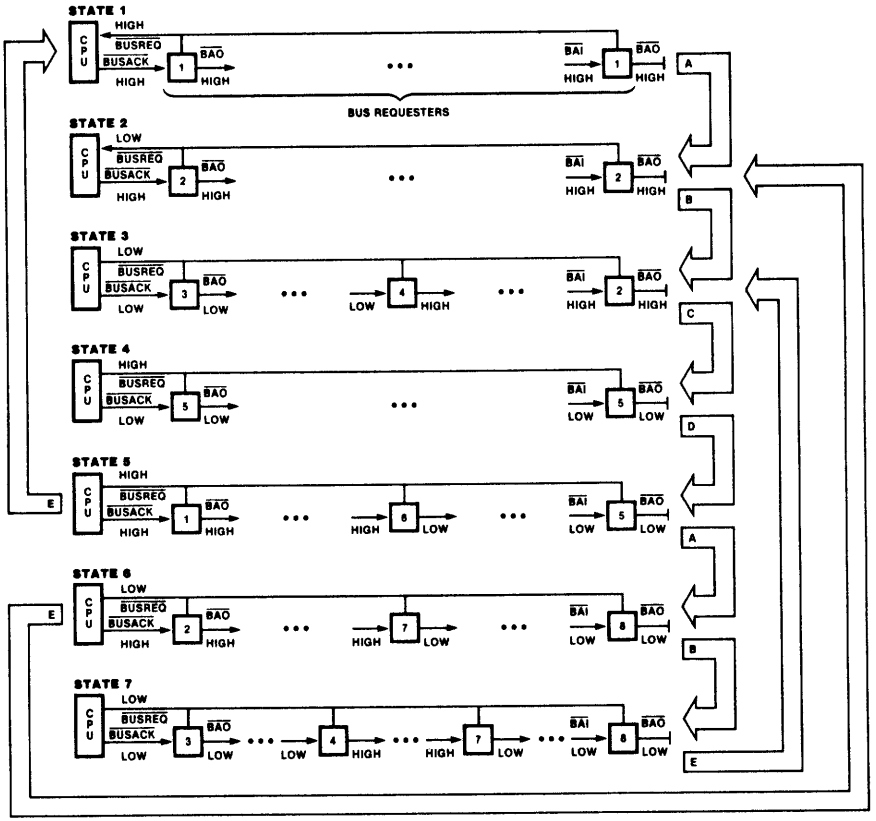


Figure 7. Bus Request Mechanism States

BUS STATE LEGEND

1. The CPU owns the bus and no one is requesting it.
2. A bus requester has requested the bus by pulling $\overline{\text{BUSREQ}}$ Low, but the CPU has not responded.
3. A Low from the CPU's $\overline{\text{BUSACK}}$ is propagating down the $\overline{\text{BAI}}/\overline{\text{BAO}}$ daisy chain. Bus requesters are using the bus.
4. The Low from $\overline{\text{BUSACK}}$ has propagated to the end of the daisy chain causing all bus requesters to release $\overline{\text{BUSREQ}}$, which floats High. The CPU has not yet acknowledged return of the bus.
5. The CPU acknowledges the High on $\overline{\text{BUSREQ}}$ with a High on $\overline{\text{BUSACK}}$ which propagated down the $\overline{\text{BAI}}/\overline{\text{BAO}}$ daisy chain.
6. Some device whose BAI input is High requests the bus by pulling $\overline{\text{BUSREQ}}$ Low. The CPU has not yet responded with a Low on $\overline{\text{BUSACK}}$.
7. The CPU has responded to a Low on $\overline{\text{BUSREQ}}$ with a Low on $\overline{\text{BUSACK}}$. The previous High state on $\overline{\text{BUSACK}}$ is still propagating down the $\overline{\text{BAI}}/\overline{\text{BAO}}$ daisy chain.

TRANSITION LEGEND

A. A bus requester requests the bus by pulling down on $\overline{\text{BUSREQ}}$.
B. The CPU responds to $\overline{\text{BUSREQ}}$ by pulling down $\overline{\text{BUSACK}}$.
C. The Low from $\overline{\text{BUSACK}}$ propagates to the end of the $\overline{\text{BAI}}/\overline{\text{BAO}}$ daisy chain, causing all the bus requesters to let $\overline{\text{BUSREQ}}$ rise.
D. The CPU responds to $\overline{\text{BUSREQ}}$ High by driving $\overline{\text{BUSACK}}$ High.
E. The High from $\overline{\text{BUSREQ}}$ propagates to the end of the $\overline{\text{BAI}}/\overline{\text{BAO}}$ daisy chain.

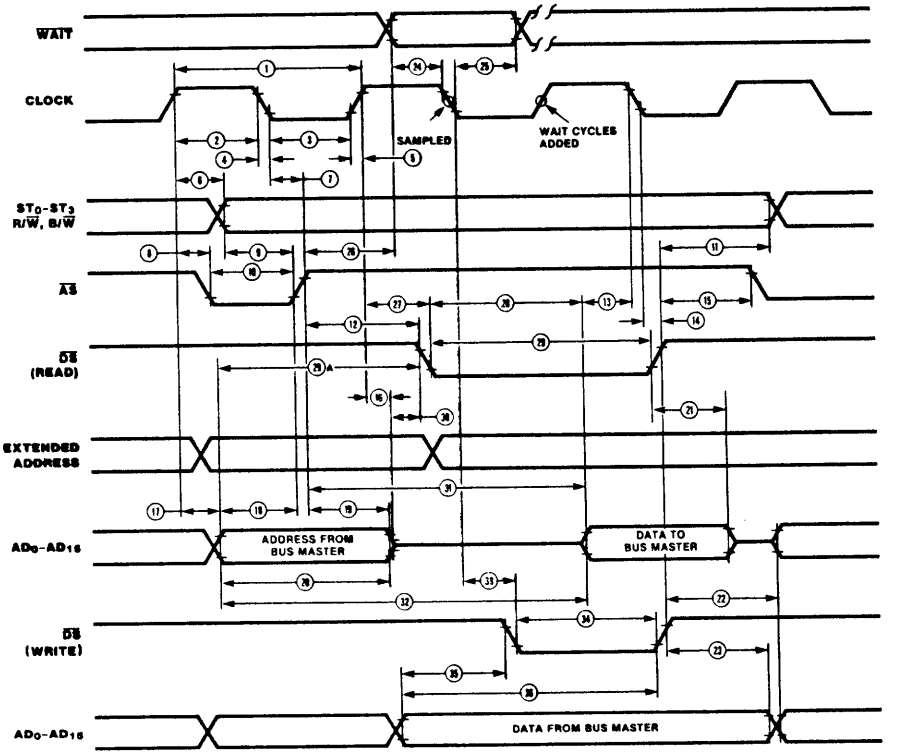
BUS REQUESTER LEGEND

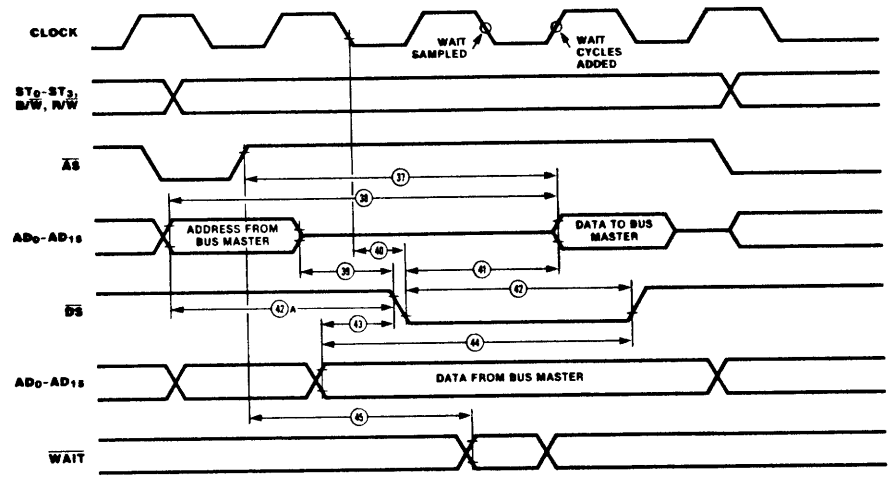
1. Requester does not want bus and is not pulling $\overline{\text{BUSREQ}}$ Low.
2. Requester may or may not want bus; it is pulling $\overline{\text{BUSREQ}}$ Low in either case.
3. Requester is not pulling $\overline{\text{BUSREQ}}$ Low; if it wants control of the bus, it must wait for $\overline{\text{BUSREQ}}$ and $\overline{\text{BAI}}$ to rise before requesting the bus.
4. Requester is either using the bus or propagating the Low on its $\overline{\text{BAI}}$ input. It will stop driving $\overline{\text{BUSREQ}}$ when its $\overline{\text{BAO}}$ output goes Low. If its wants to use the bus, but did not want to at the time $\overline{\text{BUSREQ}}$ and $\overline{\text{BAI}}$ were last High or $\overline{\text{BUSREQ}}$ went from Low to High, then it must wait for $\overline{\text{BUSREQ}}$ and $\overline{\text{BAI}}$ to rise before requesting and using the bus.
5. Requester is not pulling $\overline{\text{BUSREQ}}$ Low. If it wants to use the bus, it must wait for its $\overline{\text{BAI}}$ to become High before requesting the bus.
6. Requester is propagating the High on its $\overline{\text{BAI}}$ input. If it wants the bus it will pull $\overline{\text{BUSREQ}}$ Low.
7. Requester is propagating the High on its BAI input.
8. Requester is not pulling $\overline{\text{BUSREQ}}$ Low. If it wanted the bus at the time $\overline{\text{BUSREQ}}$ went from Low to High, it may request the bus when its $\overline{\text{BAI}}$ input rises; otherwise if it wants the bus, it must wait for $\overline{\text{BUSREQ}}$ to rise.

Figure 7 (continued). Bus Request Mechanism States

Page 392

The **Bus Master Timing** and **I/O Transaction Timing** diagrams lack parameters 29A and 42A, respectively. Corrected versions of the art follow.





A corrected version of **Bus Master Timing Parameters** follows.

Z-BUS Bus Master Timing Parameters (Page 393)

No.	Symbol	Parameter	4 MHz Min(ns)	4 MHz Max(ns)	6 MHz Min(ns)	6 MHz Max(ns)	Notes
		All Transactions					
1	TpC	Clock Period	250	2000	165	2000	
2	TwCh	Clock High Width	105		70		
3	TwCl	Clock Low Width	105		70		
4	TfC	Clock Fall Time		20		10	
5	TrC	Clock Rise Time		20		15	
6	TdC(S)	Clock ↑ to Status Valid Delay		110		85	
7	TdC(ASr)	Clock ↓ to $\overline{AS}$ ↑ Delay		90		80	
8	TdC(ASf)	Clock ↑ to $\overline{AS}$ ↓ Delay		80		60	
9	TdS(AS)	Status Valid to $\overline{AS}$ ↑ Delay	50		30		
10	TwAS	$\overline{AS}$ Low Width	80		55		
11	TdDS(S)	$\overline{DS}$ ↑ to Status Not Valid Delay	75		55		
12	TdAS(DS)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ Delay	80	2095	55		3
13	TsDR(C)	Read Data to Clock ↓ Setup Time	30		20		
14	TdC(DS)	Clock ↓ to $\overline{DS}$ ↑ Delay		70		65	
15	TdDS(AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay	70		35		
16	TdC(Az)	Clock ↑ to Address Float Delay		65		55	
17	TdC(A)	Clock ↑ to Address Valid Delay		100		75	
18	TdA(AS)	Address Valid to $\overline{AS}$ ↑ Delay	50		35		1
19	TdAS(A)	$\overline{AS}$ ↑ to Address Not Valid Delay	70		45		1
20	TwA	Address Valid Width	150		85		
21	ThDR(DS)	Read Data to $\overline{DS}$ ↑ Hold Time	0		0		
22	TdDS(A)	$\overline{DS}$ ↑ to Address Active Delay	80		45		
23	TdDS(DW)	$\overline{DS}$ ↑ to Write Data Not Valid Delay	50		45		
24	TsW(C)	$\overline{WAIT}$ to Clock ↓ Setup Time	50		30		2,5
25	ThW(C)	$\overline{WAIT}$ to Clock ↓ Hold Time	10		10		2,5
		Memory Transactions					
26	TdAS(W)	$\overline{AS}$ ↑ to $\overline{WAIT}$ Required Valid		90		45	
27	TdC(DSR)	Clock ↓ to $\overline{DS}$ (Read) ↓ Delay		120		85	
28	TdDSR(DR)	$\overline{DS}$ (Read) ↓ to Read Data Required Valid		200		130	
29	TwDSR	$\overline{DS}$ (Read) Low Width		250	185		
29A	TdA(DS)	Address Valid to $\overline{DS}$ ↓ Delay	180		110		
30	TdAz(DSR)	Address Float to $\overline{DS}$ (Read) ↓ Delay	0		0		
31	TdAS(DR)	$\overline{AS}$ ↑ to Read Data Required Valid		360		220	
32	TdA(DR)	Address Valid to Read Data Required Valid		410		305	
33	TdC(DSW)	Clock ↑ to $\overline{DS}$ (Write) ↓ Delay		95		80	
34	TwDSW	$\overline{DS}$ (Write) Low Width	160		110		
35	TdDW(DSWf)	Write Data Valid to $\overline{DS}$ (Write) ↓ Delay	50		35		
36	TdDW(DSWr)	Write Data Valid to $\overline{DS}$ (Write) ↑ Delay	230		195		
		I/O Transactions					
37	TdAS(DR)	$\overline{AS}$ ↑ to Read Data Required Valid		610		385	
38	TdA(DR)	Address Valid to Read Data Required Valid		660		470	
39	TdAz(DSI)	Address Float to $\overline{DS}$ (I/O) ↓	0		0		
40	TdC(DSI)	Clock ↓ to $\overline{DS}$ (I/O) ↓		120		90	
41	TdDSI(DR)	$\overline{DS}$ (I/O) ↓ to Read Data Required Valid		330		210	
42	TwDSI	$\overline{DS}$ (I/O) Low Width	400		255		
42a	TdA(DSI)	Address Valid to $\overline{DS}$ (I/O) ↓ Delay	180		110		
43	TdDW(DSIf)	Write Data to $\overline{DS}$ (I/O) ↓ Delay	50		35		
44	TdDW(DSIr)	Write Data to $\overline{DS}$ (I/O) ↑ Delay	480		320		
45	TdAS(W)	$\overline{AS}$ ↑ to $\overline{WAIT}$ Required Valid		340		210	

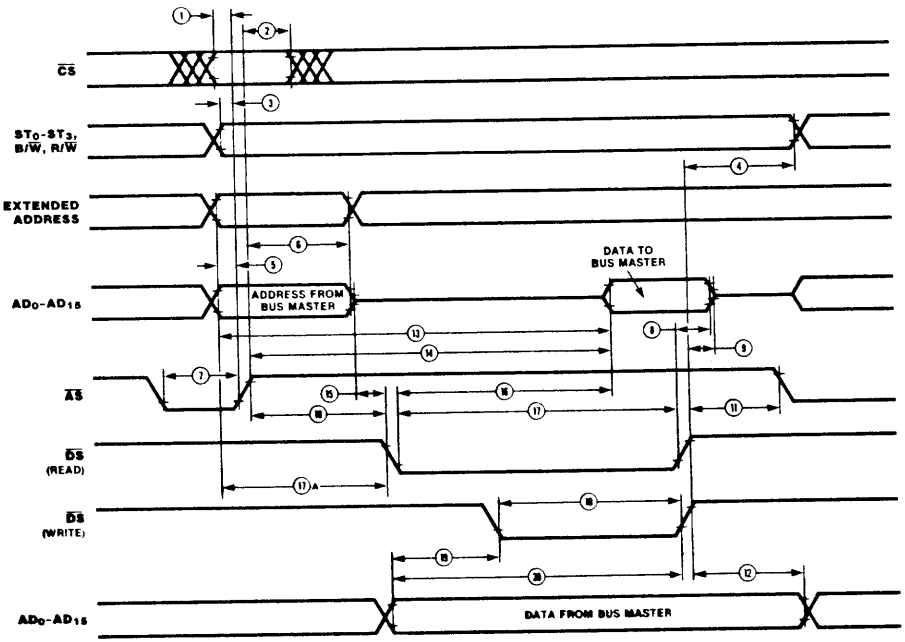
No.	Symbol	Parameter	4 MHz Min(ns)	4 MHz Max(ns)	6 MHz Min(ns)	6 MHz Max(ns)	Notes
		Interrupt-Acknowledge Transactions					
46	TdAS(DSA)	$\overline{AS}$ ↑ to $\overline{DS}$ (Acknowledge) ↓ Delay	960		690		
47	TdC(DSA)	Clock ↑ to $\overline{DS}$ (Acknowledge) ↓ Delay		120		85	
48	TdDSA(DR)	$\overline{DS}$ (Acknowledge) ↓ to Read Data Required Valid		455		295	
49	TwDSA	$\overline{DS}$ (Acknowledge) Low Width	485		315		
50	TdAS(W)	$\overline{AS}$ ↑ to Wait Required Valid		840		540	
51	TdDSA(W)	$\overline{DS}$ (Acknowledge) ↓ to Wait Required Valid		185		120	

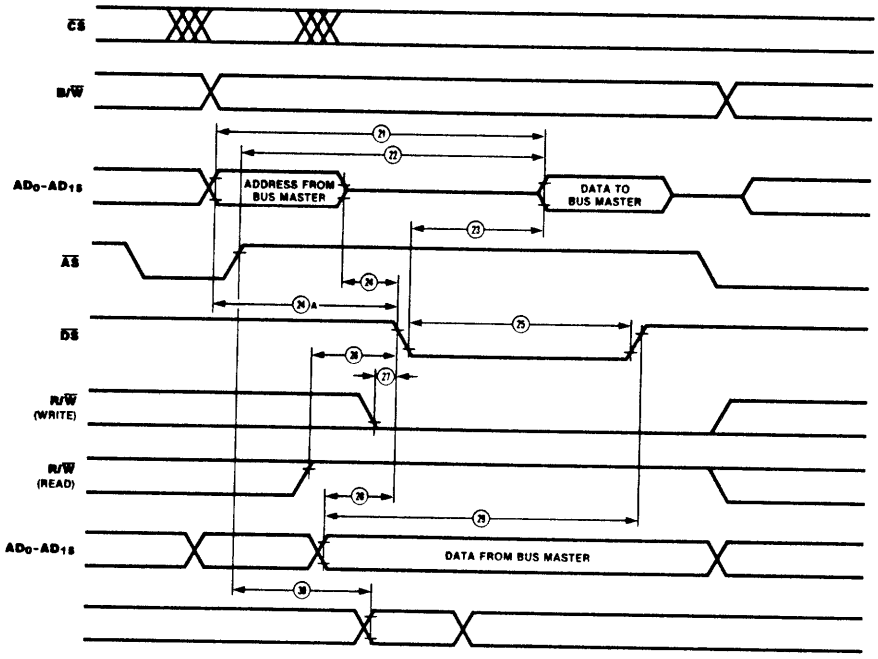
NOTES:

1. Timing for extended addresses is CPU dependent; however, extended addresses must be valid at least as soon as addresses are valid on AD_0-AD_{15} and must remain valid at least as long as addresses are valid on AD_0-AD_{15}.
2. The exact clock cycle that wait is sampled on depends on the type of transaction; however, wait always has the given setup and hold times to the clock.
3. The maximum value for TdAS(DS) does not apply to Interrupt-Acknowledge Transactions.
4. Except where otherwise stated, maximum rise and fall times for inputs are 200 ns.
5. The setup and hold times for $\overline{WAIT}$ to the clock must be met. If $\overline{WAIT}$ is generated asynchronously to the clock, it must be synchronized before input to a bus master.

Page 394

Add to the **Memory and Peripheral Timing** and **I/O Transaction Timing** diagrams parameters 17A and 24A, respectively. A corrected version of these diagrams follows.





Page 395

A corrected version of **Memory and Peripheral Timing Parameters** follows.

Z-BUS Memory and Peripheral Timing Parameters (Page 395)

No.	Symbol	Parameter	4 MHz Min(ns)	4 MHz Max(ns)	6 MHz Min(ns)	6 MHz Max(ns)	Notes
		All Transactions					
1	TsCS(AS)	$\overline{CS}$ to $\overline{AS}$ ↑ Setup Time	0		0		1
2	ThCS(AS)	$\overline{CS}$ to $\overline{AS}$ ↑ Hold Time	60		40		1
3	TsS(AS)	Status to $\overline{AS}$ ↑ Setup Time	20		0		2
4	ThS(DS)	Status to $\overline{DS}$ ↑ Hold Time	55		40		
5	TsA(AS)	Address to $\overline{AS}$ ↑ Setup Time	30		10		1
6	ThA(AS)	Address to $\overline{AS}$ ↑ Hold Time	50		30		1
7	TwAS	$\overline{AS}$ Low Width	70		50	0	
8	TdDS(DR)	$\overline{DS}$ ↑ to Read Data Not Valid Delay	0				
9	TdDS(DRz)	$\overline{DS}$ ↑ to Read Data Float Delay		70	45		
10	TdAS(DS)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ Delay	60	2095	40		5
11	TdDS(AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay	50		25		
12	ThDW(DS)	Write Data to $\overline{DS}$ ↑ Hold Time	30		20		1
		Memory Transactions					
13	TdA(DR)	Address Required Valid to Read Data Valid Delay		320		255	
14	TdAS(DR)	$\overline{AS}$ ↑ to Read Valid Delay		270		170	
15	TdAz(DSR)	Address Float to $\overline{DS}$ (Read) ↓ Delay	0		0		
16	TdDSR(DR)	$\overline{DS}$ (Read) ↓ to Read Data Valid Delay		110		80	
17	TwDSR	$\overline{DS}$ (Read) Low Width	240		180		
17A	TdA(DS)	Address to $\overline{DS}$ ↓ Setup	160		100		
18	TwDSW	$\overline{DS}$ (Write) Low Width	150		105		
19	TsDW(DSWf)	Write Data to $\overline{DS}$ (Write) ↓ Setup Time	30		20		
20	TsDW(DSWr)	Write Data to $\overline{DS}$ (Write) ↑ Setup Time	210		180		

Z-BUS Memory and Peripheral Timing Parameters (Page 395)

No.	Symbol	Parameter	4 MHz Min(ns)	4 MHz Max(ns)	6 MHz Min(ns)	6 MHz Max(ns)	Notes
		I/O Transactions					
21	TdA(DR)	Address Required Valid to Read Data Valid Delay		570		420	
22	TdAS(DR)	$\overline{AS}$ ↑ to Read Data Valid Delay		520		335	
23	TdDSI(DR)	$\overline{DS}$ (I/O) ↓ to Read Data Valid Delay		250		180	
24	TdAz(DSI)	Address Float to $\overline{DS}$ (I/O) ↓ Delay	0		0		
24A	TdA(DSI)	Address to DS (I/O)↓ Setup	160		100		
25	TwDSI	$\overline{DS}$ (I/O) Low Width	390		250		
26	TsRWR(DSI)	R/$\overline{W}$ (Read) to $\overline{DS}$ (I/O) ↓ Setup Time	100		100		
27	TsRWW(DSI)	R/$\overline{W}$ (Write) to $\overline{DS}$ (I/O) ↓ Setup Time	0		0		
28	TsDW(DSIf)	Write Data to $\overline{DS}$ (I/O) ↓ Setup Time	30		20		
29	TsDW(DSIr)	Write Data to $\overline{DS}$ (I/O) ↑ Setup Time	460		305		
30	TdAS(W)	$\overline{AS}$ ↑ to $\overline{WAIT}$ Valid Delay	195		160		
		Interrupt-Acknowledge Transactions					
31	TsIA(AS)	$\overline{INTACK}$ to $\overline{AS}$ ↑ Setup Time	0		0		
32	ThIA(AS)	$\overline{INTACK}$ to $\overline{AS}$ ↑ Hold Time	250		250		
33	TdAS(DSA)	$\overline{AS}$ ↑ to $\overline{DS}$ (Acknowledge) ↓ Delay	940		675		
34	TdDSA(DR)	$\overline{DS}$ (Acknowledge) ↓ to Read Delay Valid Delay	365		245		
35	TwDSA	$\overline{DS}$ (Acknowledge) Low Width	475		310		
36	TdAS(IEO)	$\overline{AS}$ ↓ to IEO ↓ Delay					3,4
37	TdIEIf(IEO)	IEI to IEO Delay					4
38	TsIEI(DSA)	IEI to $\overline{DS}$ (Acknowledge) ↓ Setup Time					4

NOTES:

1. Parameter does not apply to Interrupt Acknowledge Transactions.
2. Does not cover R/$\overline{W}$ for I/O Transactions.
3. Applies only to a peripheral which is pulling $\overline{INT}$ Low at the beginning of the Interrupt Acknowledge Transaction.
4. These parameters are device dependent. The parameters for the devices in any particular daisy chain must meet the following constraint: for any two peripherals in the daisy chain, TdAS(DSA) must be greater than the sum of TdAS(IEO) for the higher priority peripheral, TsIEI(DSA) for the lower priority peripheral, and TdIEIf(IEO) for each peripheral separating them in the daisy chain.
5. The maximum value for TdAS(DS) does not apply to Interrupt Acknowledge Transactions.
6. Except where stated otherwise, maximum rise and fall times for inputs are 200 ns.

Z80 RMB RAM Memory Board
Product Description

Page 451

In **Ordering Information** the Part Number for the Z80 RMB/32 32K RAM Memory Board should read:

05-0104-00.

Z80 MDC Z80 Memory and
Disk Controller Board
Product Description

Page 469

In **Ordering Information** the Part Number for the Z80 MDC/32 32K Memory and Disk Controller should read:

05-6209-00.

Page 471

Delete **Zilog** before Development Systems.

Z8 Software Development Product Description

Page 499

Delete the Z-LINK entry and insert the following:

> **Linker.** ZLINK links assembled modules into a single-load module. ZLINK resolves any external references between separately assembled modules, so that the load module produced is relocatable. It also allows the reordering and combining of named sections between modules. ZLINK permits a symbolic specification of the program entry point in the Command line and, on request, produces a detailed map for program documentation.

Delete the **LOAD/SEND** heading and substitute **Program Transfer.**

Delete the **Z-PROG** heading and substitute **PROM PROGRAMMING.**

Add to the **Description** of **Part No.** 07-3363-02 the following:

> Prerequisites
> PDS 8000 Series
> ZDS 1/40 or 1/25
> MCZ-1 Series
> RIO

Z8000 Software Development Package Product Description

Page 501

In **Overview** the first two sentences should read:

> The Z8000 Software Development Package consists of five utility programs which aid and simplify the development of Z8000 programs. PLZ/ASM from Zilog's PLZ family bring all the advantages of modular programming to the Z8000 software developer and ensure transportability to future processors.

Delete the hyphen in "Z-PROG" in sentence 3.

Delete the **LINKER** text and substitute the **LINKER** text from page 499 in this DCN.

In **Imager** sentences one, two and three should read:

> The IMAGER accepts multiple linked object files from ZLINK and translates them into absolute code. IMAGER can then either store the absolute code in a disk file or leave it in system memory. IMAGER supports segmented and nonsegmented code.

Delete **LOAD/SEND** and add **PROGRAM TRANSFER.**

Delete the **Z-PROG** heading and substitute **PROM Programming.**

Add to the **Description** of **Part No.** 07-3310-01 the following:

Prerequisites
PDS 8000 Series
ZDS 1/40
MCZ-1 Series
RIO

Page 503

Change Page Heading to:

Z8000™
Cross-Software
Package Version II

Page 504

In **Product Description,** paragraph 2, the third sentence should read:

The C compiler presently generates both segmented and nonsegmented code.

In **Ordering Information,** the Part Number should read:

06-0086-01.

Under **Software (continued)** the sentence should read:

All software is distributed on one reel of magnetic tape recorded at 1600 BPI.

Under **Documentation** delete the second and third entries.

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