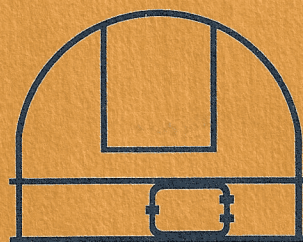DIGITAL & TEST INSTRUMENTS

ASTRODOMES & ENVIRONMENTAL ENCLOSURES

INSTRUCTION MANUAL

SOLID STATE DIGITAL CLOCK

MODEL D12MDRNS-BCDP-M237

SERIAL NOS. 200-210

PARABAM, INC.

WARRANTY

Parabam, Inc., warrants each instrument to be free of defects in material and workmanship, that each is of the agreed designation or specification, and makes no other warranty, expressed or implied.

Our liability under this warranty is limited to repair or replacement of instruments which, upon our authorization, have been returned, prepaid, to the factory within one year of shipment to the original purchaser, and are found by us to be defective. Transistors, tubes, semiconductors, choppers, and bulbs are exempted from this warranty, but are subject to the warranties of their respective manufacturers.

Instruments out of warranty will be serviced at cost plus a small handling charge when sent prepaid to our factory upon authorization. Serviced instruments will be returned FOB, Compton, California.

Parabam, Inc., reserves the right to make changes in design at any time without incurring any obligation to retrofit units previously purchased.

All claims incurred under this warranty are void if the instrument covered by this warranty has been modified or tampered with in any way.

CONTENTS

SECTION 1

GENERAL DESCRIPTION

BASIC FUNCTION

The Parabam Model "D" Digital Clock accumulates clock pulses to provide
a logic output and/or visual numerical displays of elapsed time or real
time.

PRIMARY COMPONENTS

The digital clock is a completely solid state device employing silicon semi-
conductor logic. Plug-in printed circuit modules are used for the BCD
counter stages (unidirectional or bidirectional), BCD/decimal conversion
circuits, lamp drivers, frequency dividers, control logic circuits, and for
the smaller components of the regulated power supply. Larger components
of the power supply are assembled on a single plate.

PHYSICAL DATA

The 19" rack panel of the clock is 5-1/4" high and has EIA standard notching.
The enclosed cabinet extends 15" behind the panel. Front/access to the PC
modules and panel components is provided by swinging out the hinged panel
section. Receptacles at the rear of the chassis provide connection to any
logic output and/or remote visual displays.

SUMMARY OF SPECIFICATIONS - Model D12MDRNS-BCDP-M237

Time Base:

Derived from internal oscillator. Timing stability within
±0.5 seconds per day.

Time Range:

01 Month, 01 Day, 00 Hours, 00 Minute, 00 Seconds to
12:31:2359:59. Leap Year switch permits February days-
count of 29.

Visual Display:

Five remote 2- unit Nixie bezel and filter assemblies connected
to chassis by 20-foot cable.

Logic Output:

31 bits of date/time data in BCD 8421 form with logic "1"
= +12 volts at 1200 ohms source impedance (load 2 ma max.)
and logic "0" = 0 volts (sink 3 ma max.)

SECTION 2

INSTALLATION

UNPACKING

No more than normal care need be exercised in unpacking the
digital clock. A preliminary visual check should be made for
evidence of damage in transit.   In the event of suspected damage,
a report should be made out immediately for both the carrier
and Parabam, Inc.,

INSTALLATION LOCATION

A properly ventilated location should be selected for permanent
installation. Additional factors to be considered are ease of
operation and maintenance accessibility.

INTERCONNECTIONS

    1.   Actuate power switch to off and connect unit
             to 115 volts, 60 cycle line power.

    2.   Connect to readout equipment and/or remote
             displays as referenced on the Block Interconnect
             Diagram for the specific clock model.

SECTION 3

OPERATION

OPERATIONAL TESTS

When the digital clock is initially installed it should be checked in the following manner to insure that it has not been operationally damaged in transit.

(1)   Actuate Start/Stop switch to Stop position and turn power on. The time count should be zero.

(2)   Actuate each Time Set pushbutton. Observe that each decade count increments once per actuation without introducing a transfer count into the following decade. Confirm also that any logic output corresponds to the visual display. Repeat this procedure for each decade.

(3)   To check the transfer of all decades, set the clock just below its maximum count, actuate the Start/Stop switch to Start and observe the transition to zero or to its minimum count.

NORMAL OPERATION

Set Start/Stop switch to stop, set in desired start time, then start clock the instant real time coincides with the preset start time. Note that the first time count transition occurs a full least count after starting.

SECTION 4

THEORY OF OPERATION

GENERAL

The Block Interconnect Diagram shows the elements of the Digital
Clock (with detail drawings referenced) and the conversion of the
time base to digital time data is covered in the following paragraphs.

Model: D12MDRNS-BCDP-M237

Block Interconnect Drawing: No. 45792

SPECIAL FEATURE

Frequency Divider Module AD60SI-504(Part No. 45128-504)provides a
20 microsecond + 12 volt 1 pps clock pulse that is outputted to Pin #31
of receptacle J15 for externally providing a "time sample inhibit" signal.
Count transitions are triggered at the trailing edge of this pulse and trans-
ition time is approximately 0.3 microseconds per counter stage.

STANDARD FLIP-FLOP

The figure below shows the schematic of the flip-flop module used in the frequency divider and in the BCD counters. It uses two silicon PNP transistors, employs -12 volt logic, and is triggered by a positive-going signal (for example, -12 volts to ground or ground to +12 volts) having a rise of 5 volts per microsecond or better. Logic is such that a "set" condition produces -12 volts on the A output and a "reset" condition produces -12 volts on the $\overline{A}$ output and grounds the A output.
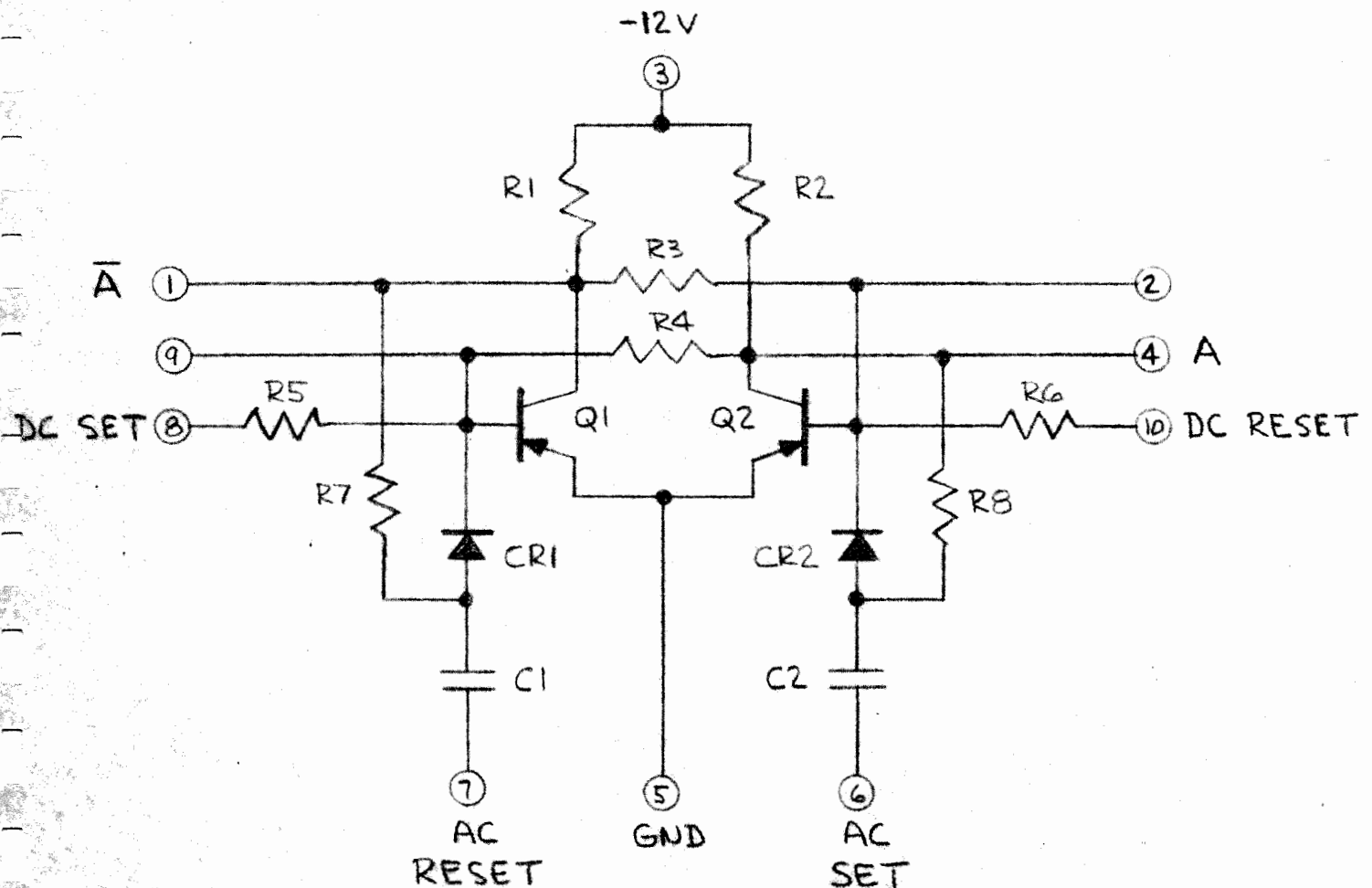
FREQUENCY DIVIDER

60 cycle voltage is converted to a square wave by means of a Schmitt-Trigger on the AD60S in order to drive the divider flip-flops. Six flip-flops and a one-shot multi-vibrator are utilized to obtain the required division of 60 pps to 1 pps. Output of the one-shot provides the normal clock pulse and provides feedback to the binary 4 flip-flop so that the natural binary division by 64 is advanced by four counts.

Stopping the time count is accomplished by holding the flip-flops of the frequency divider in the "reset" or zero condition. This insures that the first clock pulse occurs one full second after each start.

UNIDIRECTIONAL BCD DIVIDE-10 COUNTER

The BCD $\div$ 10 counter employs four flip-flops logically interconnected to count 0 through 9 rather than the natural binary 0 - 15. This is accomplished by allowing the counter to count 0 through 9 then forcing a transition from 9 to 0 rather than allowing the 0 to 10 transition. Note that after an input of 8 pulses the $\overline{8}$ output of the FF4 inhibits the set input of FF2. The ninth pulse merely sets FF1 but the tenth pulse resets FF4 as well as FF1. FF2 and FF3 remain in the reset condition, and the counter returns to the zero condition.

UNIDIRECTIONAL BCD DIVIDE-6 COUNTER

The $\div$ 6 counter employs the same logic as the $\div$ 10 counter except that the forced transition is from 5 to 0. The sixth input pulse resets FF1, the output of FF1 resets FF4, and attempts to set FF2. However, the $\overline{4}$ output of FF4 inhibits the set input of FF2 and the counter returns to the zero condition.

UNIDIRECTIONAL 00 to 23 HOURS-COUNT LOGIC

Units and tens of hours are accumulated with a $\div$ 10 counter and a $\div$ 3 counter logically arranged to count 00 to 23 and then return to 00 on receipt of the 24th input pulse. The combination operates conventionally until the 20th pulse sets FF2 of the $\div$ 3 counter. Then the $\overline{A}$ output of this flip-flop inhibits the set inputs of FF3 and FF4 of the $\div$ 10 counter. The 21st, 22nd and 23rd input pulses serve to set FF1 and FF2 of the $\div$ 10 counter. The 24th pulse resets these two flip-flops, the output of FF2 resetting FF2 of the $\div$ 3 counter but not affecting FF3. Thus both counters return to the zero condition.

UNIDIRECTIONAL COUNTER DECADE PRESET & INHIBIT

Actuation of the set switch associated with a counter stage simultaneously grounds the preset input line and opens the output line to prevent a transition pulse to the following stage. Multiple pulses caused by switch contact bounce are eliminated by virtue of the fast discharge of C2 (producing the required positive-going preset pulse) through 47 ohm resistor R43 and the relatively slow recharge time constant through 1.0 megohm resistor R42.

BUFFERED BCD OUTPUT

Each counter flip-flop output is amplified with a transistor stage and the BCD output of the clock is the output of the buffer stages. The buffered output of each counter also serves as the input to the BCD/decimal conversion matrix that controls the lampdrivers of that stage.

BCD/DECIMAL 0 - 9 DECODER

Eight transistor stages buffer the four flip-flops and provide current amplification. The BCD and BCD-complement outputs are then decoded by a biquinary matrix consisting essentially of nine diodes and twelve transistors. The logic of this matrix is traight-forward and is illustrated in the following table in which the "false" condition is shown by a bar over the numeral.

Decimal	Binary				
0	$\overline{1}$	$\overline{2}$	$\overline{4}$	$\overline{8}$	
1	1	$\overline{2}$	$\overline{4}$	$\overline{8}$	
2	$\overline{1}$	2	$\overline{4}$		8 not possible
3	1	2	$\overline{4}$		8 not possible
4	$\overline{1}$	$\overline{2}$	4		8 not possible
5	1	$\overline{2}$	4		8 not possible
6	$\overline{1}$	2	4		8 not possible
7	1	2	4		8 not possible
8	$\overline{1}$			8	2 & 4 not possible
9	1			8	2 & 4 not possible

One of the ten output transistors, Q1 through Q10, will conduct to provide current to the appropriate lamp of the visual display or to provide base current to the associated power transistor of the Multiple Lampdriver Module. The biquinary scheme in effect decodes only the binary 2-4-8 digits so that two of ten outputs will occur. The binary "1" then determines the correct one of the two.

BCD/DECIMAL 0 - 5 DECODER

The logic and circuitry is essentially identical to that of the 0 - 9 decoder.
Eight driver transistors are employed but only two diodes are required.

Decimal	Binary			
0	$\overline{1}$	$\overline{2}$	$\overline{4}$	
1	1	$\overline{2}$	$\overline{4}$	
2	$\overline{1}$	2		4 not possible
3	1	2		4 not possible
4	$\overline{1}$		4	2 not possible
5	1		4	2 not possible

CALENDAR LOGIC

The basic logic involved here is to:

(1)   Decode the BCD output of the units-months and tens-months counter stages to derive a signal for each month 01 - 12.

(2)   Combine the 12 month signals to obtain three signals representing a 30-day month, a 31-day month, and February.

(3)   Decode the BCD output of the units-days and tens-days counter stages to derive three signals representing the day of the month as the 31st, 30th, or 28th (29th when Leap Year Switch actuated).

(4)   Combine the days-in-month signals with the days-of-month signals to control the output of the tens-hours counter stage. Normally this output will merely advance the days count by one but it will reset the days-count to 01 when the two logic signals indicate the preceding day as the last of the month.

The months-count increments each time to the tens-days count resets to zero. However, at the end of December, the transition to 13 is sensed and used to reset the count to 01 within a few microseconds.

MONTH BUFFER MODULE

This circuitry buffers the BCD output of the months counter stages and generates the BCD complement. The module also contains an AND gate and one-shot that serve to sense the count transition to 13 and provide a pulse to reset the count to 01.

MONTH DECODE MODULE

Circuitry associated with transistors Q1 thru Q12 accept the months-count in BCD form from the Month Buffer Module and decode it to decimal form 01 to 12. The Q13 AND gate output is the 31-day month signal. The Q15 AND gate output is the 30-day month signal. The output of Q14 represents February.

MONTH END MODULE

Inputs to this module are the three days-in-month signals, the units-days (UD) digits $\overline{UD1}$ and UD8, the tens-days (TD) digits TD1 and TD2, and the output of the tens-hours counter stage. Digit UD1 is generated by transistor Q14 stage.

The output of transistor Q2 is the "31st day" signal, which is ANDed with the "31 day month" input to provide, from Q3, one "last day of month" signal. The output of Q5 is the "30th day" signal, which is ANDed with the "30 day month" input to provide, from Q6, another "last day of month" signal. The output of Q8 is the "28th/29th day" signal and it is ANDed with the "February" input to provide the remaining "last day of month" signal.

With no last-day signals present, the output of the tens-hours counter stage will pass through to the input of the units-days counter. With any last-day signal present, the OR gate formed by R11 and CR33-CR35 will inhibit the transfer pulse and the Q11 OR gate stage will be enabled so that the transfer pulse will, instead, trigger the Q12-Q13 one-shot circuit. The pulse output of the one-shot then resets the days-count to 01.

POWER SUPPLY

Transformer T1 delivers 14-0-14 vrms to bridge rectifiers CR 1 through CR4 and the two rectified voltages are then filtered and series-regulated in a conventional manner by transistors Q1 and Q7 and zener diodes CR5 and CR6. The resultant regulated ± 12 volts provides power to all logic circuits within the digital clock.

The circuitry of transistors Q3, Q4, Q5 and Q6 serves to zero the time-count each time power is turned on.

The Nixie display is energized by the +200 volts derived from transformer T2, rectifiers CR7-CR10, and capacitor C4.

The two nickel-cadmium batteries B1 and B2 are normally kept on charge as shown and the power failure relay is normally energized. Upon line power failure, the relay drops out and the clock logic circuits are kept energized by the ±12 volts from the batteries.

SECTION 5

MAINTENANCE

GENERAL

Isolation of any trouble within the digital clock is made easy because of
the sequential nature of its operation. The visual readout will, in all prob-
ability, indicate the decade stage where a fault exists and whether the trouble
is restricted to a particular digit of that decade. The clock requires no ad-
justments or preventive maintenance.

TEST EQUIPMENT

(1)   A reliable oscilloscope having a triggered and calibrated time base
        and a frequency response that will allow observation of pulse rise
        times on the order of one microsecond.

(2)   A sensitive (20,000 ohm/volt) voltmeter.

PARTS REPLACEMENT

No special procedures are required for replacement of any components of
the digital clock. However, identical components should be used and ex-
cessive heat should be avoided in the soldering of semi-conductors.

ACCESS TO COMPONENTS

The hinged front panel of the digital clock allows access to all of the plug-in
printed circuit modules and to the front panel components. In order to service
the power supply chassis or any oscillator, batteries, or relays, merely un-
screw and remove the chassis top cover plate.

CIRCUIT TROUBLESHOOTING

Section 7 of this manual contains all circuit schematics and wiring diagrams.
All electrical components and functional mechanical components are described
in detail in the Parts Lists of Section 6. In conjunction with the Theory of
Operation Section, this data should be used for isolation of any trouble and
correcting it at the module or component level. In the event of trouble within
a PC module, it is recommended that the module be replaced with a spare
and that the defective unit be returned to the contractor for repair.

SECTION 6

PARTS LISTS

ELECTRICAL PARTS LIST

MODEL D12MDRNS-BCDP-M237 DIGITAL CLOCK

Item	Reference Designation	Qty Assy.	Description	Manufacturer	Part No.
1.	S1	1	4PST Toggle Switch	Cutler-Hammer	7661-K6
2.	S2, S3	1	SPDT Toggle Switch	Arrow-Hart	21350-EH
3.	S4-S11	8	PB Switch DPDT	Microswitch	2PB11-T12
4.	–	5	Digital Indicator Assy, NL8422 Nixie Tubes	National Elect.	NL-BEZ-59-2
5.		1	Oscillator, 12 vdc. Oven 115 vac. Output 60 Hz.	Gibbs Mfg.	518
6.		1	Printed Circuit Module: Power Supply - BPM12E2-4R	Parabam	34857
7.		1	Printed Circuit Module: Frequency Divider - AD60S-504	Parabam	45128-504
8.		3	Printed Circuit Module: Counter ABD10P-NLD	Parabam	45065
9.		2	Printed Circuit Module: Counter ABD6P-NLD	Parabam	45066
10.		1	Printed Circuit Module: Counter ABD10UHP-NLD	Parabam	45067
11.		1	Printed Circuit Module: Counter ABD3P-NLD	Parabam	45068
12.		1	Printed Circuit Module: Counter ABD10P-NLD-M198A	Parabam	45158-502
13.		1	Printed Circuit Module: Counter ABDT(MD)P-NLD	Parabam	45789
14.		1	Printed Circuit Module: Control A-MBM	Parabam	44964
15.		1	Printed Circuit Module: Control MDM	Parabam	44049

ELECTRICAL PARTS LIST

MODEL D12MDRNS-BCDP-M237 DIGITAL CLOCK

Item	Reference Designation	Qty. Assy.	Description	Manufacturer	Part No.
16.		1	Printed Circuit Module: Control A-MEM	Parabam	44966
	PM12E3-P200	1	Power Supply Plate Assy	Parabam	35056-500
17.	T1	1	Transformer 115/28V 1 Amp.	Triad	F202U
18.	T2	1	Transformer 115/50V	Stancor	P8181
19.		1	Line Filter	Cornell-Dubilier	IF-54
20.	Q7	1	Power Transistor	Motorola	IN1539
21.	C1, C2	2	Capacitor, 3800 MF, 25 VDC	Mallory	CG382U25C1
22.	C4	1	Capacitor 20 MF, 450 VDC	Cornell-Dubilier	BR20-450
			Standby Power-Plate Assembly	Parabam	35797
23.	T3	1	Transformer 115/40	Triad	F90X
24.	B1, B2	2	Nickel-Cadmium Battery, 12v, 500MAH	Gould	12V/500BH
25.	K1	1	Relay, 115 vac, 4C Cont.	Parelco	R10E1-Y4-115 VAC
26.	-	10	Rectifier	Solitron	HG-70

SECTION 7

DRAWINGS

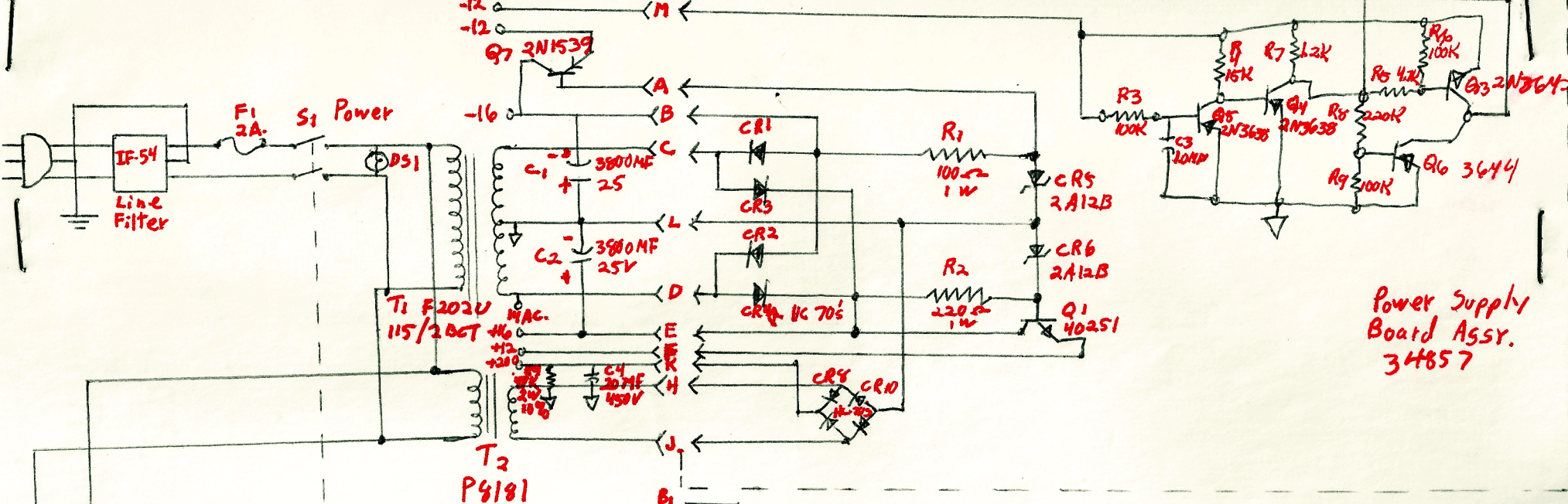### DIGITAL CLOCK MODEL D12MDRNS-BCDP-M237

The following drawings are included with and form a part of this Instruction Manual.
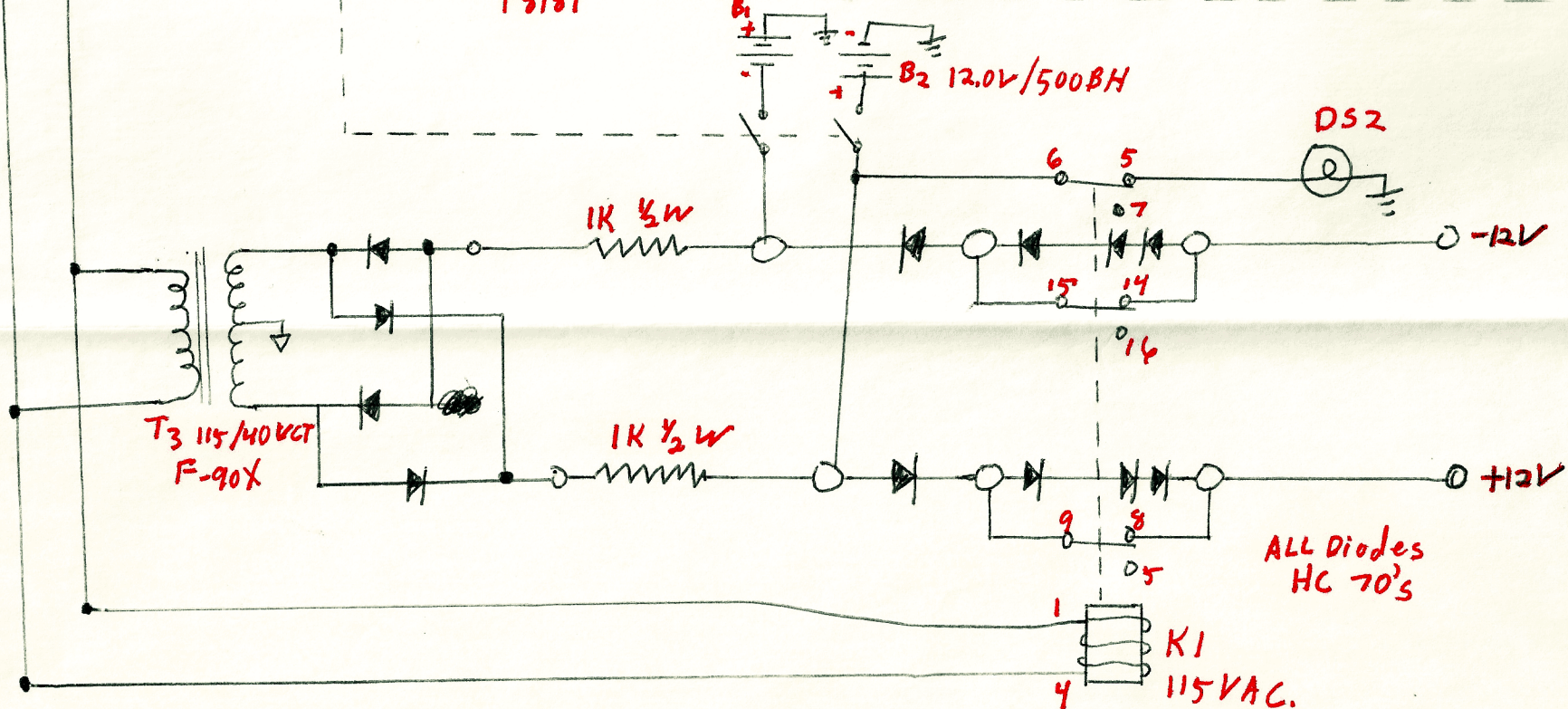
Counter Reset input
Zero turn-on

Power Supply Board Assy. 34857

Power Supply PM12E3-P200
+ PM 12- Batt

35795