Nu Machine System Diagnostic Unit
General Description
2242829-0001

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This manual provides detailed information about the Texas Instruments Nu Machine(TM)* System Diagnostic Unit (SDU). It is primarily directed to the system programmer and provides some information for the installation personnel.

Information in this manual is divided into the following sections:

Section

1. General--Contains physical and functional descriptions that acquaint the user with the hardware components and capabilities of the Nu Machine SDU.

2. Installation--Outlines procedures for unpacking the Nu Machine SDU from its shipping container, installing the board in the Nu Machine chassis, and performing diagnostics.

3. Operation--Describes the board and front panel light-emitting diodes (LEDs), the back control panel rotary switch, and the reset switch and signals.

4. Programming--Presents information for use by programmers on the function of the SDU and defines the Multibus(R)** address space and NuBus(TM)* address space reserved for SDU use.

Appendix

A. P1 Pin Assignments--Shows the standard NuBus pin assignments on P1.

B. P2 Pin Assignments--Shows the Multibus pin assignments on P2.

C. P3 Pin Assignments--Shows the input/output (I/O) pin assignments on P3.

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* Nu Machine and NuBus are trademarks of Texas Instruments Incorporated.

** Multibus is a registered trademark of Intel Corporation.

D. Serial Port Pin Assignments--Shows the remote and local serial port pin assignments.

E. Multibus Compliance Levels--Describes the Multibus attributes supported by the SDU.

Reference Documents

The following documents contain additional information related to SDU design. These documents cover NuBus and Multibus specifications, detailed programming and implementation information on some components, and interface requirements for SDU I/O.

TITLE	PART NUMBER
NuBus Specification	2242825-0001
iAPX 86, 88 User's Manual (Intel)	
Intel Component Data Catalog	
Motorola Microprocessor Data Manual	
Multibus Specification (Intel) or IEEE Standard Microcomputer System Bus Specification (IEEE Std 796-1983)	9800683
AP-28A (Intel)	
EIA-RS-232C	
QIC-02 Interface Specification (Rev. D, 9/23/82)	
Nu Generation Computer System Architecture Specification	2236632-0001
Nu Machine Diagnostic User Manual	2244479-0001
Nu Machine Rack Module, General Description	2242821-0001
Nu Machine Office Module, General Description	2242822-0001
Nu Machine Unpacking and Inventory Guide	2244492-0001

Nu Machine Installation Manual	2242824-0001
Nu Machine SDU Operating System User Manual	2242811-0001
Nu Machine SDU Operating System Implementation Description	2242812-0001
Nu Machine SDU Operating System Driver Design Guide	2242813-0001
Nu Machine SDU Development System, User Guide	2242815-0001
Nu Machine SDU Development System, Assembler Reference Manual	2242816-0001

Notation

The following notational conventions have been used throughout this document.

Ones and Zeros
Signal or bit names that end with an asterisk (*) are active low. Names that do not end with an asterisk (*) are active high. Low means logic 0; high means logic 1.

Reset
The four SDU reset functions are:

- NuBus RESET*
- Multibus INIT*
- an SDU reset signal
- a tape controller reset signal

Each of these signals will be referred to by its complete name, such as NuBus RESET*, unless the context makes it clear which of the preceding reset signals is intended.

Numbers
Bit 0 of a byte is the least significant bit, and bit 7 is the most significant bit. Byte numbering is similar to bit numbering. For example, in a 16-bit halfword, bit 7 of byte 0 is adjacent to bit 0 of byte 1. Words are 32 bits.

The hexadecimal symbol (0x) precedes each hexadecimal number throughout this document. A bit represented by X within a hexadecimal number can range in value from 0x0 to 0xF.

1.1 General

This manual provides unpacking, installation, testing, and operating information for the Texas Instruments Nu Machine (TM)* System Diagnostic Unit (SDU) board (see Figure 1-1). This section contains functional and physical descriptions to acquaint the user with the hardware components and capabilities of the Nu Machine SDU.

1.2 Purpose of Equipment

The SDU provides many one-per-system functions and smart front-end and diagnostic capabilities. Since these functions are concentrated on the SDU, rather than on separate central processing unit (CPU) cards, the system is able to support multiple processors without conflict. The SDU Monitor, the PROM-resident portion of the SDU Operating System, provides a flexible system-boot environment.

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* Nu Machine is a trademark of Texas Instruments Incorporated.

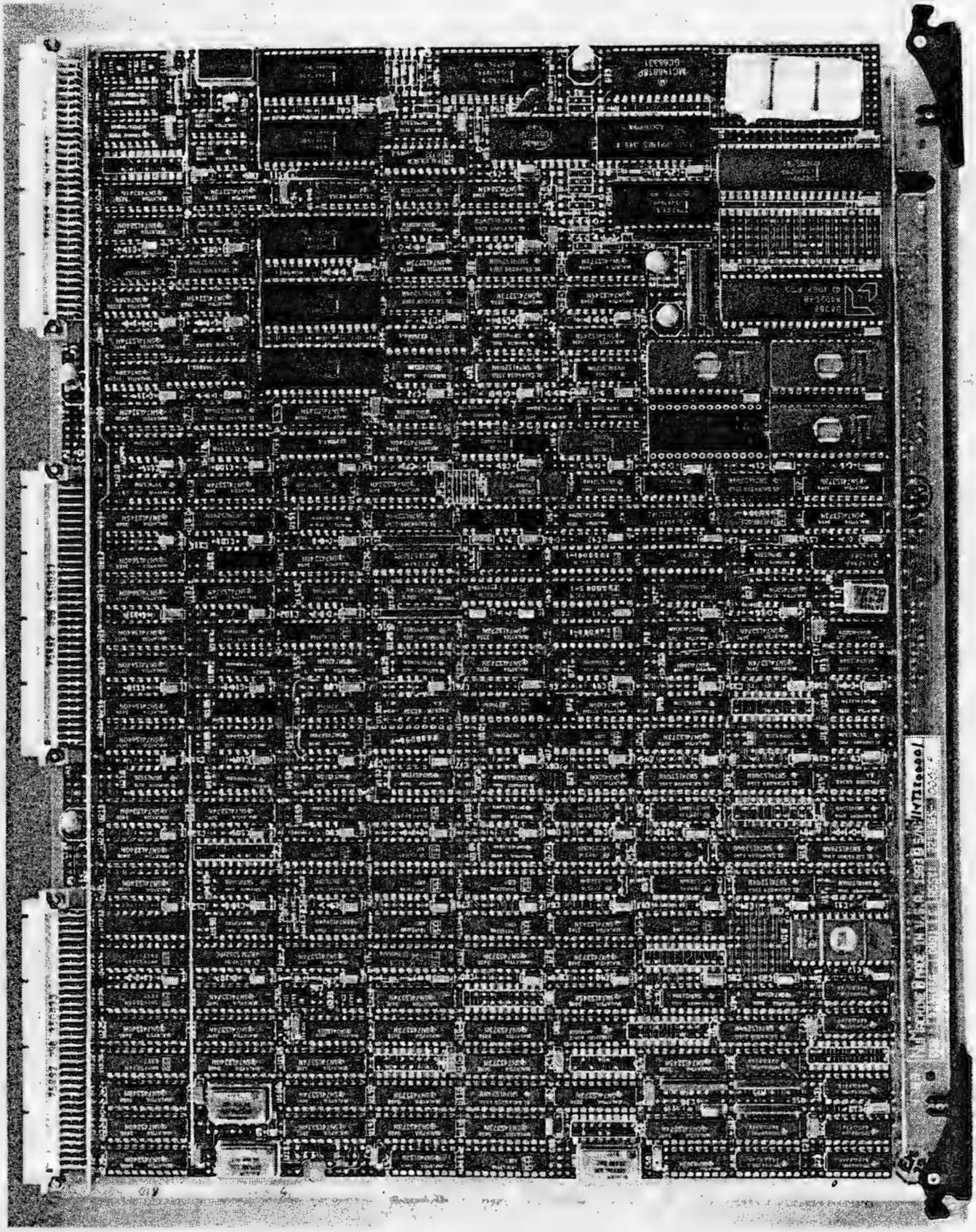

Figure 1-1. Nu Machine System Diagnostic Unit Board.

1.3 Equipment Description

The SDU is an 8088-based, single printed wiring board (PWB) microprocessor system with additional special purpose hardware to interface to the NuBus (TM)* architecture and provide required system utilities. Figure 1-2 shows the major hardware subsections and interfaces with other Nu Machine system components. The following paragraphs describe the major SDU components.

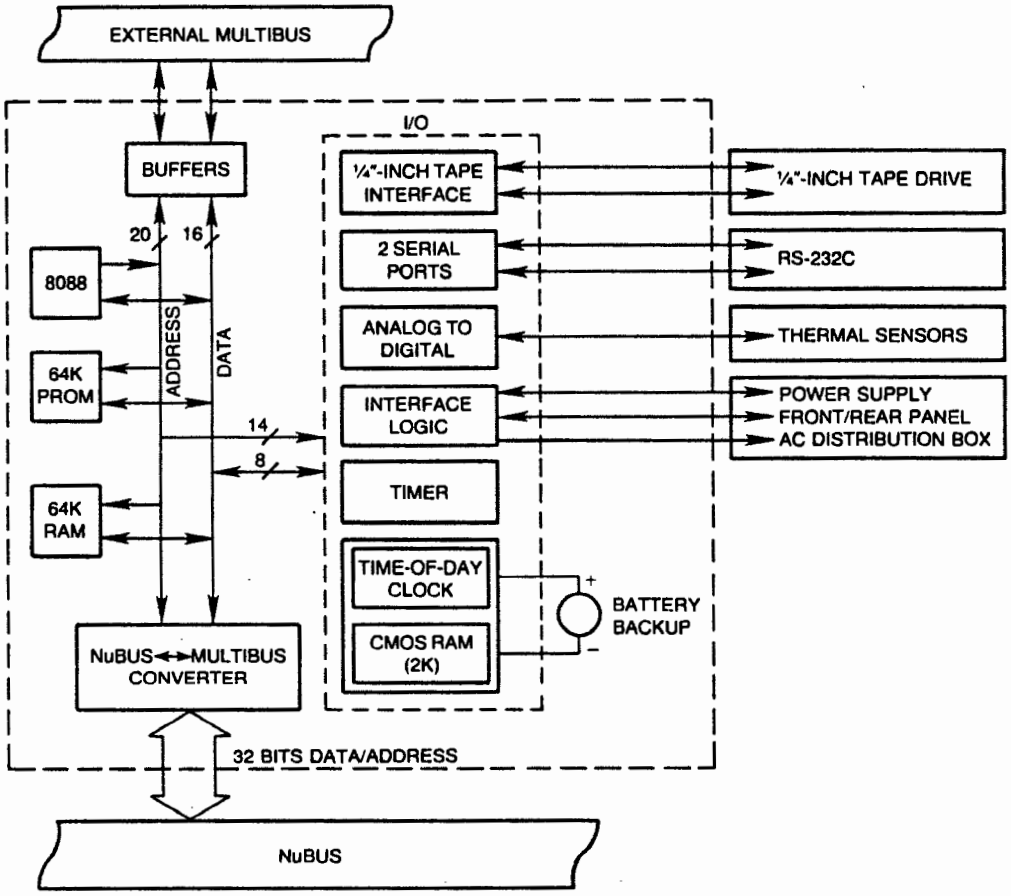

Figure 1-2. SDU Block Diagram and System Interfaces.

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* NuBus is a trademark of Texas Instruments Incorporated.

1.3.1 8088 and Related Hardware

The 8088 microprocessor system is the heart of the SDU. It consists of the following:

- 8088 microprocessor -- The 8088 specifications and interface are described in the Intel Component Data Catalog.

- Reset circuits -- The board-level SDU reset signal initializes internal registers to the power-up state and also resets the on-board 8088. The SDU reset signal is driven active by any of the following:

  1. The operator pressing the back panel reset button. A resistor capacitor (RC) circuit then holds the SDU reset signal low for about 3 milliseconds.

  2. The power supply generating an active 5 volts dc out-of-tolerance signal. If the SDU sends a high or low margin signal to the power supply, the dc out-of-tolerance signal is ignored.

  3. The remote serial port detecting a line break character while the back panel switch is at 0, 2, 3, or 4

  4. The on-board deadman timer triggering while the back panel switch is at 2. The timer triggers if the switch panel register, Multibus (R)* address 0x1C084, is not read once every one-half second.

- Clock generation circuits -- The 8088 clock is derived from a 14.7456 megahertz crystal giving the 8088 an effective clock rate of 4.9152 megahertz.

- Multibus time-out logic -- The Multibus time-out logic generates a READY signal to the 8088 as well as a time-out interrupt if an operation takes more than 3 milliseconds to complete.

- 64K bytes of ROM

- Programmable interrupt controllers -- Three programmable interrupt controllers (PICs) provide a flexible interface between the 8088 and devices

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* Multibus is a registered trademark of Intel Corporation.

requiring real-time servicing. The three PICs (PIC0, PIC1, and PIC2) are configured as a master PIC (PIC0) and two slave PICs (PIC1 and PIC2) as described in the 8259A data sheet. Paragraph 4.2.15, Interrupt Controllers, details the operation of the 8259A.

- 64K bytes of dynamic RAM
- Multibus interface logic

1.3.2 Configuration ROM

The SDU has a 2K-byte configuration ROM and a configuration register residing on the NuBus. The contents and format of the configuration ROM are described in the Nu Generation Computer System Architecture Specification. The configuration register implements only the on-board LED bit.

1.3.3 Internal Multibus

The SDU is built around an internal Multibus. The I/O/Data Bus and CMOS/Data Bus, extensions of the internal Multibus, reduce drive requirements for the various buses. The external Multibus is also an extension of the internal Multibus. The buffers between the internal Multibus and external Multibus provide isolation and meet the loading requirements of the Multibus. (The relationship between the internal Multibus, external Multibus, and the SDU board is explained in Paragraph 4.2.7, Control-Status Register 0. Multibus attributes supported by the SDU are discussed in Appendix E, Multibus Compliance Levels.)

1.3.4 NuBus and Multibus Interface

The SDU interfaces to and enables two-way conversions between the NuBus and Multibus.

1.3.5 Front/Back Control Panel Interface

Three lines from the SDU drive the front panel LEDs. Four lines into the SDU indicate the mode selector position on the back panel rotary switch. A single input from the back control panel resets the SDU.

1.3.6 Serial Communications

Two asynchronous RS-232C ports support data rates to 19.2K baud.

1.3.7 1/4-Inch Tape Interface

A QIC-02 streaming tape drive interface provides system backup capability and diagnostic loading media.

1.3.8 Power Supply Interface

Two signal lines from the power supply to the SDU indicate the 5 volts and ac power status. A line from the SDU to the

power supply enables the SDU to margin the +5 volt supply above and below nominal.

1.3.9 AC Shutdown

A line from the SDU to the ac distribution box enables the SDU to shut off the ac power in emergency situations.

1.3.10 Thermal Sensors

Five inputs from the optional external thermal sensors to an analog-to-digital converter are provided.

1.4 Specifications

Table 1-1 lists the physical, electrical, and environmental specifications for the SDU board.

Table 1-1. SDU Board Specifications

CHARACTERISTIC	SPECIFICATION
Ambient Temperature:	
Operating	10 to 35 degrees C
Storage	-40 to 65 degrees C
Ambient Humidity:	
Operating	15 to 80% (noncondensing)
Storage	5 to 95% (noncondensing)
Altitude:	
Operating	-300 to 3,000 meters (-990 to 10,000 feet)
Storage	-300 to 12,000 meters (-990 to 40,000 feet)
Shock:	
Operating	15g for 11 ms
Storage	25g for 11 ms
Vibration:	
Operating	.5g rms, random
Storage	.75g rms, random
Power	48 W
Current:	
+5 V	9 A
+12 V	150 mA
-12 V	120 mA

1.5 Functional Description

The following paragraphs describe the function of the major Nu Machine SDU components.

1.5.1 Bus Conversion

The NuBus/Multibus converter resides on the SDU. Bus conversion in both directions is done by hardware mapping logic and does not require 8088 microprocessor intervention. The two buses run independently until one bus accesses the other. Under certain circumstances, a NuBus card can attempt to access the Multibus at the same time that a Multibus card is accessing the NuBus. The SDU prevents a lockup by giving the NuBus a "Try Again Later" response and allowing the Multibus cycle to complete. The following two paragraphs describe the conversions in more detail.

1.5.1.1 NuBus-to-Multibus Conversion The Multibus memory space and I/O space (as described in Paragraphs 4.3.1 and 4.3.2, respectively) are completely contained within the SDU NuBus slot space. Thus, there is a direct correlation between NuBus addresses and the accessed Multibus addresses.

The Multibus memory space can be accessed with byte, halfword, and word operations. Byte and halfword operations on the NuBus are translated into byte and halfword operations on the Multibus. Word operations on the NuBus are translated into two halfword operations on the Multibus with the lower halfword transfer occurring first.

The Multibus I/O space can be accessed in one of two different address ranges. In one range, byte, halfword, or word transfers can access the Multibus I/O space but only the low byte of each NuBus word is valid data. In the other range, byte, halfword, and word transfers are all supported across the interface.

When a NuBus access of either the Multibus memory or I/O space occurs, the following sequence of events occurs:

1. START* on the NuBus accesses the Multibus.
2. The SDU bus translation logic initiates arbitration for the Multibus.
3. The SDU bus translation logic acquires the Multibus.
4. The Multibus operation (or operations for 32 bits) occurs as per the Multibus Specification.

5. The SDU returns XACK* on the Multibus.

6. The SDU does an ACK cycle on the NuBus.

The SDU detects bus locks on the NuBus and asserts the Multibus signal LOCK* if a NuBus-to-Multibus translation is in progress. Thus, indivisible transfers are supported across the bus interface.

1.5.1.2 Multibus-to-NuBus Conversion Multibus-to-NuBus conversions are similar in sequence to NuBus-to-Multibus conversions. The following sequence of events occur:

1. The address map is initialized (see Paragraph 4.2.3) to point to the desired NuBus page.

2. Multibus master initiates Multibus transfer (upper ten bits of Multibus address select map entry).

3. Valid bit (bit 23) of map entry indicates a NuBus access.

4. The SDU bus translation logic initiates arbitration for the NuBus.

5. The SDU acquires NuBus mastership.

6. The NuBus operation is initiated by a START cycle as explained in the NuBus Specification.

7. The addressed slave on the NuBus responds with an ACK*.

8. The SDU bus translation logic generates XACK* on the Multibus.

If the Multibus signal LOCK* is active when a Multibus-to-NuBus conversion is performed, the NuBus is locked until LOCK* is inactive.

1.5.1.3 Interrupt Translation The SDU can translate Multibus interrupts into NuBus interrupts. The SDU's 8088 microprocessor receives all Multibus interrupts in a non-bus-vectored fashion (explained in the Multibus Specification). When programmed, the 8088 can respond to Multibus interrupts by writing to an arbitrary NuBus address (or addresses). Since NuBus interrupts are specifically addressed writes with the least significant bit set to 1, the Multibus interrupt can be translated into a NuBus interrupt.

The SDU can also translate NuBus interrupts into Multibus non-bus-vectored interrupts. On the SDU, the Multibus address space is contained within the NuBus address space. The Multibus interrupt register, which lies in this Multibus address space, can drive any of the eight Multibus interrupt lines active. Therefore, NuBus writes to the Multibus interrupt register which have the least significant bit set to 1 are translated into Multibus interrupts.

1.5.2 NuBus Central Features

1.5.2.1 System Clock The SDU is the source of the 75 percent duty cycle, 10 megahertz system clock (CLK*), to which all bus operations are synchronized. Under software control, the system clock rate can be increased or decreased by 7 percent for diagnostic purposes.

1.5.2.2 Time-Out Recovery The SDU optionally provides NuBus time-out recovery by monitoring the time between the START* and ACK* control signals. If more than the programmed number of clock cycles (up to 256) occur, the SDU asserts the ACK* signal with the appropriate TM0 and TM1 code for a time-out.

1.5.3 Nonvolatile Features

The SDU contains 2K bytes of battery backed-up CMOS RAM. This memory is used to store the system configuration information in a nonvolatile manner. The SDU also provides a battery backed-up time-of-day clock.

1.5.4 1/4-Inch Tape Interface

The SDU contains a 1/4-inch streaming tape drive interface. This feature provides low-cost transportable media for the Nu Machine. Since this interface is on the SDU, only the SDU, power supply, and tape drive must be functioning properly to load the diagnostic routines from the 1/4-inch tape drive.

1.5.5 Interval Timer

The SDU contains a programmable timer for generating periodic events to specific CPUs. The timer can be used for many important system functions, such as process scheduling.

1.5.6 Debug/Diagnostic Facilities

The SDU provides the NuBus system operator with several diagnostic tools. The SDU Monitor of the SDU Operating System allows a terminal on either serial port to read and write bus locations and to initiate and execute SDU

self-diagnostics. The NuBus diagnostic hardware verifies bus integrity.

1.5.7 System Status Display

On power-up, the SDU first runs a self-test, then a bus test, and finally individual board tests. The SDU uses the front panel LEDs to summarize the results of the tests; the detailed results can be read using the system console. An LED on each board is automatically turned on at power-up and is turned off by the SDU after the board-specific diagnostic passes.

1.5.8 Serial Ports

The SDU contains two serial communications ports, either of which can be used as the smart front panel/remote diagnostics port, depending on the position of the diagnostic rotary switch. Otherwise, they are both available as general-purpose serial ports.

1.5.9 Power Supply Interface

The interface to the power supply includes several lines in addition to the actual current-carrying cables. These lines are ACPF, DCOT, MARGIN, and ACOFF. The SDU provides the system interface to these lines. ACPF (ac power fail) is generated by the power supply. The SDU then posts events to the installed CPUs so that they can take appropriate action. DCOT (dc out of tolerance) indicates that the +5 volt supply is out of tolerance +/-5 percent. When this signal is active, the SDU generates a system reset. MARGIN is the SDU signal by which the +5 volt supply margin can be increased or decreased by 7 percent. ACOFF is a signal from the SDU to the ac distribution box by which the SDU can shut off the ac power.

1.5.10 System Bootstrap

The SDU Monitor of the SDU Operating System boots automatically upon power-up. The SDU then determines the location of the system console, either serial port or high resolution display, from the position of the rotary switch. This allows the system to be manually reset, reinitialized, or rebooted via SDU Monitor control. Refer to the Nu Machine SDU Operating System User Manual for the command descriptions.

The SDU can fully and automatically boot the Nu Machine Operating System when the rotary switch is properly set. The rotary switch positions are explained in both the Nu Machine Rack Module, General Description and the Nu Machine Office Module, General Description.

2.1 General

This section provides information and procedures for unpacking the SDU from its shipping container and installing it in a Nu Machine (TM)* system chassis. When the SDU is shipped in a chassis as part of a complete system, refer to the Nu Machine Unpacking and Inventory Guide for unpacking procedures.

This section covers installation details of the SDU board only. The procedures assume that the user has a fundamental knowledge of basic hand tools and cabling techniques, but they do not require a detailed understanding of computer hardware or software.

2.2 Unpacking/Packing the SDU Board

Upon receipt of the container, inspect it to ensure that no damage has occurred. If any damage is found, note the damage on the bill of lading and file claim against the carrier, if applicable. Photograph any damages to the equipment container.

CAUTION

The Nu Machine systems contain static-sensitive electronic components. To avoid damage to these components, ensure that you are well grounded before removing or handling the printed circuit boards.

Use a static-control system consisting of a static-control floor or table mat and a static-control wrist strap. These are commercially available. If you do not have a static-control system, you can discharge any accumulated static charge by touching a grounded object prior to handling a board.

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It is imperative that you do not place the printed circuit board on top of its shipping bag. The conductive external surface of this bag will short the SDU board's energized pins on contact, resulting in a corrupted CMOS RAM. Always store or transport a printed circuit board inside its protective package.

After completion of the preliminary inspection, perform the following steps to remove the board from its container and prepare the computer for installation.

NOTE

Do not discard any packing materials until unpacking, inspection, and inventory are complete.

1. Remove the top cushion pad or other packing material.
2. Obtain the packing list. Inventory the items received against the packing list.
3. Pack all shipping materials into the original shipping container and store the container for reshipment of the unit.
4. Inspect the SDU board and components for signs of damage that may have occurred during shipment. If damage has occurred, notify the carrier immediately.

To repack the unit, reverse the above procedure using the original packing material.

2.3 SDU Installation Procedures

The following paragraphs describe the preparation and installation of the Nu Machine SDU board.

WARNING

Ensure that the chassis ac power cord is disconnected from ac power during installation. Failure to observe this precaution could result in severe electrical shock.

1. Select the chassis slot for the SDU board. The SDU board must be installed in either slot 13, 14,or 15, whichever is the highest priority NuBus (TM)* slot in the chassis. Since the SDU generates clock signals for both the NuBus and Multibus (R)** interfaces, the selected slot must have a NuBus in the P1 position and, if the system is equipped with Multibus, a Multibus in the P2 position.

2. Install a 1 high by 1 wide connector plate assembly (TI P/N 2235471-0001) to provide the jack for the P3 board connector to plug into. Lower the I/O back panel to access the back chassis framework. Push the connector plate assembly into the selected chassis slot hole directly below the motherboard. Secure the assembly to the back chassis framework with screws.

3. Returning to the front of the chassis, slide the board into the selected chassis slot. Hold the board so that the inserter/ejector tabs on the front corners of the board are pushed out and the board components are to the right. When the board is fully inserted, the inserter/ejector tabs will snap over the board's locking pins to prevent it from vibrating out of the chassis.

4. For standard Nu Machine systems, install the Multibus priority jumper (TI P/N 2220779-0001) on pin A31 and pin B31 in P2 slot 15. Note that the SDU slot position can affect the jumper setting. As a rule, install the jumper on the first slot (either 14 or 15) which is the Multibus master. If the jumper is not installed in the correct slot, the Multibus cannot be enabled.

5. An SDU paddle board (TI P/N 2235465-0001) must be mounted on the P3 connector plate assembly which was installed in the step 2 above. To connect the SDU paddle board to the other system components, the SDU cables in Table 2-1 are required. Note that the cable length and part number can vary depending on the Nu Machine system. Consult your local sales representative for exact ordering information. Refer

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** Multibus is a registered trademark of Intel Corporation.

to the Chassis Section of the Nu Machine Installation Manual for the SDU paddle board and interface cable installation procedures.

Table 2-1. Required SDU Cables

CABLE NAME	TI PART NUMBER
SDU Front Panel	2235232
SDU Rear Panel	2235233
SDU Serial Interface	2235416
SDU Power Supply	2235418
SDU Ac Power Control	2235419

3.1 General

This section describes SDU operation after installation in the chassis with appropriate peripherals and mass storage devices.

3.2 Fault Indication LED

The SDU card has a red LED mounted on its front edge. This LED should come on at power-up and go out at the successful completion of the SDU configuration ROM diagnostic.

3.3 Front Panel LEDs

There are three LEDs on the front panel that indicate the results of the SDU self-diagnostics. The green RUN LED, when lit, indicates that the processor has resumed execution after the self-diagnostics are successfully completed. The red ATTN LED goes out when the self-diagnostics are successfully completed. The red SET-UP LED goes out if the battery-powered SDU CMOS RAM is correctly initialized. A full explanation of self-diagnostics is given in Paragraph 3.6.

3.4 Back Panel Rotary Switch

The back panel rotary switch has five mode selector positions labeled 0 through 4. Each switch position selects a preprogrammed boot sequence device, system console, and data rates for the serial ports. If the battery-powered CMOS RAM is not set up, then default boot parameters must be used. Refer to either the Nu Machine (TM)* Rack Module, General Description or the Nu Machine Office Module, General Description for mode selector position information.

3.5 Reset Pushbutton and Signals

A reset pushbutton is located on the back panel of the chassis. This pushbutton resets the board-level SDU reset

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signal which initializes internal registers to the power-up state and also resets the on-board 8088.

NuBus (TM)* RESET* and Multibus (R)** INIT*, standard reset signals, are generated by the SDU but do not reset any SDU functions. These signals are driven active at SDU power-up and by explicitly resetting them through the SDU monitor. Setting the NuBus reset bit and the Multibus reset bit in control-status register 1 (CSR1) will be discussed in Paragraph 4.2.6.

Tape RESET* is the reset signal for the 1/4-inch tape interface. This signal is only driven active through the SDU Monitor. Setting the tape reset bit in CSR1 will be discussed in Paragraph 4.2.6.

3.6 Self-Diagnostics

The SDU automatically performs self-diagnostics at power-up. Manually resetting the system via the INIT command runs the same self-diagnostics. Besides the following self-diagnostics description, additional information can be found in the Nu Machine Diagnostic User Manual.

At reset, the SDU Monitor turns on all three front panel LEDs (ATTN, SET-UP and RUN) and then tests the on-board RAM. The monitor halts if the RAM test fails and leaves all LEDs lighted. If the RAM test passes, the monitor tests the:

- Programmable interrupt controller (PIC)
- Bus time-out register (BTO)
- Interrupt register
- Map RAM
- CMOS RAM CRC

Table 3-1 depicts the results of the self-test diagnostics indicated by the front panel LEDs. When the ATTN and SET-UP LEDs are out and the RUN LED is on, a >> prompt will appear

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** Multibus is a registered trademark of Intel Corporation.

on the SDU monitor console device indicating that the SDU and its operating system are operational.

If the ATTN LED remains on, the power-up self-test was not successfully completed. In this case, refer to the troubleshooting flow chart in either Nu Machine Rack Module, Field Theory and Maintenance or Nu Machine Office Module, Field Theory and Maintenance for help.

If the SET-UP LED remains on, the battery-powered SDU RAM was not correctly initialized. Refer to the section on system power-up in either the Nu Machine Rack Module, General Description or the Nu Machine Office Module, General Description for help.

Table 3-1. Self-Diagnostics Results

LEDs ON	CMOS RAM CRC PASSED	ALL OTHER TESTS PASSED
All	No	No
SET-UP only	No	Yes
None	Yes	No
RUN only	Yes	Yes

4.1 General

This section describes the SDU Multibus(R)* and NuBus (TM)** address spaces. If the programmer wishes to alter the 8088 software or investigate 8088 capabilities, begin by referring to the Nu Machine** SDU Development System User Guide.

4.2 Multibus Address Space Definition

The Multibus is a non-multiplexed, asynchronous bus which supports 8-bit and 16-bit data transfers. Multibus addresses are twenty bits long, providing one megabyte of address space. Multibus operation is explained in the IEEE Standard Microcomputer System Bus Specification (IEEE Std 796-1983).

Table 4-1 is a partial breakdown of the Multibus address space reserved for SDU use. The low 64K bytes of the SDU address space are RAM and the high 64K bytes are ROM.

Table 4-1. Multibus Address Space

FUNCTION	ADDRESS RANGE	COMMENTS
SDU RAM	0x00000-0x0FFFF	64K bytes
SDU Register Space	0x10000-0x1FFFF	Sparsely implemented, multifunction area
SDU ROM	0xF0000-0xFFFFF	64K bytes, byte addressable

The SDU register space (0x10000-0x1FFFF) contains the various control registers and special functions implemented

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on the SDU. Table 4-2 details the addresses and related functions in the SDU register space.

Table 4-2. SDU Register Space Definition

FUNCTION	ADDRESS RANGE	COMMENTS
Address map	0x18000-0x18FFF	1024-entry page map
Front panel LEDs/ac shutdown	0x1C080	
Back panel switch	0x1C084	Read only
CSR1	0x1C088	See CSR desc.
CSR0	0x1C08C	See CSR desc.
A/D converter	0x1C100-0x1C11C	Read only
CMOS TOD chip	0x1C120,0x1C124	See M146818 desc.
Remote serial port	0x1C150,0x1C154	See Intel 8251A desc.
Local serial port	0x1C158,0x1C15C	See Intel 8251A desc.
Interval timer #1	0x1C160-0x1C16C	See Intel 8253 desc.
Interval timer #0	0x1C170-0x1C17C	See Intel 8253 desc.
Time-out register	0x1C180	NuBus time-out preset
1/4-inch tape interface	0x1C1A0 and 0x1C600-0x1C7FF	See Cipher Tape Manual
Bus integrity registers	0x1C1A8-0x1C1BC	
Interrupt controller #0	0x1C1C0,0x1C1C4	See Intel 8259A desc.
Interrupt controller #1	0x1C1C8,0x1C1CC	See Intel 8259A desc.
Interrupt controller #2	0x1C1D0,0x1C1D4	See Intel 8259A desc.
Multibus interrupt register	0x1C1E0-0x1C1FC	8-bit addressable latch
CMOS RAM	0x1E000-0x1FFFC	2K byte RAM, low byte only

The following paragraphs describe each address space and corresponding memory-mapped function in detail.

4.2.1 SDU ROM

The Multibus addresses from 0xF0000 to 0xFFFFF access the SDU ROM. This ROM contains the SDU Monitor of the SDU Operating System and certain drivers associated with SDU functions. Refer to the SDU Operating System User Manual for detailed SDU ROM information. The ROM consists of up to four 27128 EPROMS and Multibus interface logic. Each 27128 contains 16K bytes of information. Table 4-3 relates ROM address ranges to board locations. The SDU ROM can only be accessed in bytes; 16-bit accesses will not provide meaningful data.

Table 4-3. ROM Address Allocation

ROM NUMBER	ADDRESS RANGE	REFERENCE LOCATION
1	0xF0000-0xF3FFF	U43
2	0xF4000-0xF7FFF	U6
3	0xF8000-0xFBFFF	U42
4	0xFC000-0xFFFFF	U5

The 27128s have a 200 nanosecond access time but the actual SDU ROM response time is between 300 and 400 nanoseconds due to logic and synchronization delays.

4.2.2 SDU RAM

The SDU RAM is accessed by the Multibus addresses 0x00000 through 0x0FFFF. The RAM consists of eight 4164 64K byte by 1-bit dynamic RAMs, an 8203 dynamic RAM controller, Multibus interface logic, a PAL state machine, and termination resistors. The PAL state machine and the interface logic translate a 16-bit operation into two byte operations (low byte first); so the RAM supports Multibus transfers of both sizes. The 8203 automatically refreshes the DRAMs. The bus cycle time to read or write the RAM is between approximately 500 and 750 nanoseconds. However, if a refresh cycle is in progress, the cycle will be delayed as required. Some areas of the SDU RAM are reserved for the SDU Monitor. The SDU Operating System Implementation Description details RAM allocation.

4.2.3 Address Map

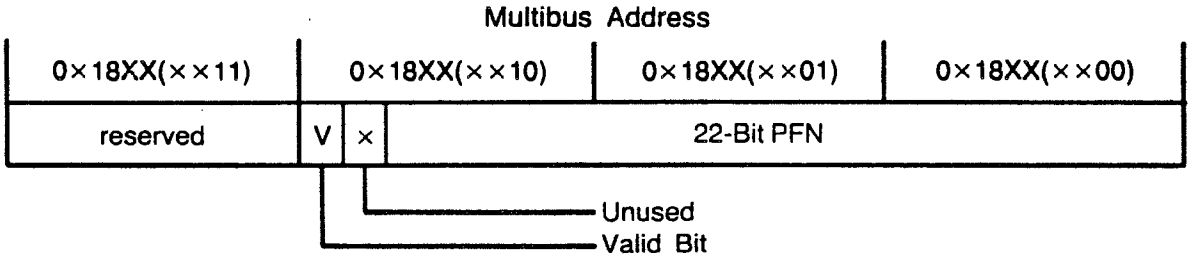
Conversion of Multibus cycles into NuBus cycles requires mapping 20-bit addresses into 32-bit addresses. The SDU translates an arbitrary Multibus address into a NuBus address using a 24-bit by 1024-word static RAM array. Figure 4-1 depicts the format of this array.

The array is accessed by Multibus addresses 0x18000 through 0x18FFF. Each map entry consists of four bytes; the most significant byte is unimplemented.

Bits 0 through 21 are used as page pointers in the NuBus address space during Multibus-to-NuBus translation. Bit 22 is unused. Bit 23, the valid bit, is set when a map entry contains a valid page (1024 bytes) pointer and cleared when the entry does not contain a valid page pointer.

The address map is readable and writable over the NuBus. Only byte transactions are performed; 16-bit operations are not supported.

The address map contains undefined data at power-up. Valid bits in the map may or may not be set. All map entries must be set to a known assigned value prior to setting bit 1 in CSR0 for the NuBus interface. Failure to do so will result in spurious accesses to the NuBus during transfers to valid Multibus addresses.



NOTE:
PFN = Page Frame Number

Figure 4-1. Address Map Format.

Figure 4-2 shows how Multibus addresses are translated into NuBus addresses using the map. The upper 10 bits of the Multibus address select one of the 1024 map entries. If the valid bit is set in the selected map entry, the Multibus operation is translated into a NuBus operation. The lower 22 bits of the selected map entry are used as the most significant bits of the NuBus address. The lower 10 bits of the NuBus address are the same as the lower 10 bits of the Multibus address.

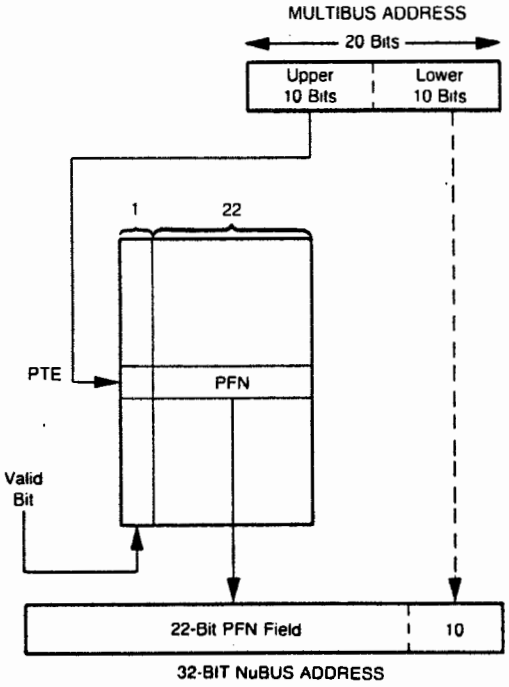


Figure 4-2. Translation Definition.

Each map entry corresponds to a fixed page of Multibus addresses. For example, the map entry at locations 0x184C8, 0x184C9, and 0x184CA always corresponds to Multibus addresses 0x4C800 through 0x4CBFF. Care should be taken so that implemented Multibus addresses do not have the valid bit set in the corresponding map entry.

4.2.4 Front Panel LEDs

Multibus address 0x1C080 accesses the register for the front panel LEDs. This is a write only register; reading the register results in undefined data.

This register is one byte wide but only four bits are meaningful. Bits 0, 1, and 2 each correspond to a different front panel LED. The LED bits drive the front panel when they are 0. Thus, writing 1 to a particular bit position turns the corresponding LED off. Bit 7, the ac shutdown bit, turns the power off when it is 1. Thus, writing 0x80 to address 0x1C080 will cause the ac power to go off.

This register is cleared at power-up or SDU reset, enabling ac power and driving all three LEDs on. Figure 4-3 shows each bit position function for this register.

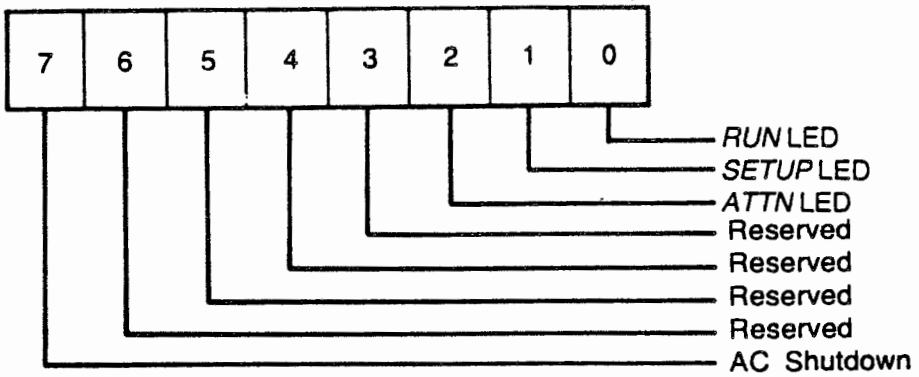


Figure 4-3. LED Register.

4.2.5 Back Panel Switch

The status of the back panel switch positions and the current NuBus slot position of the SDU are determined by reading Multibus address 0x1C084. This register can only be read; writing to this location has no effect.

The lower four bits (bits 0 to 3) convey the position of the back panel rotary switch. Table 4-4 shows the relationship between the five switch positions and bits 0 to 3 of 0x1C084. The upper four bits (bits 4 to 7) correspond to the NuBus slot identification lines ID0 to ID3. Figure 4-4 shows the switch register's bit positions and functions.

The back panel switch positions select both software and hardware options. The software options are described in both the Nu Machine Rack Module, General Description and the Nu Machine Office Module, General Description. Switch positions 0, 2, 3, and 4 enable the remote serial port to generate the SDU reset signal when it receives a break character; switch position 1 disables this function. Switch position 2 enables the on-board deadman timer; all other switch positions disable this function. Refer to Paragraph 1.3.1, 8088 and Related Hardware, for more information on the deadman timer.

Table 4-4. 1C084 Bit Patterns

SWITCH POSITION	SWITCH3	SWITCH2	SWITCH1	SWITCH0
0	1	1	1	1
1	1	1	1	0
2	1	1	0	1
3	1	0	1	1
4	0	1	1	1

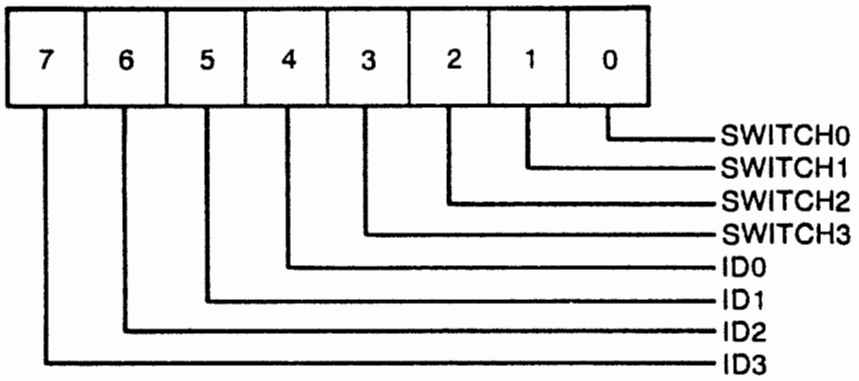


Figure 4-4. Switch Register.

4.2.6 Control-Status Register 1

Multibus address 0x1C088 accesses a multipurpose control and status register. This register is both readable and writable, but the data read is not always the same as the data written. This register is cleared at power-up and at SDU reset. Figures 4-5 and 4-6 show each bit position function in CSR1 for both reads and writes.

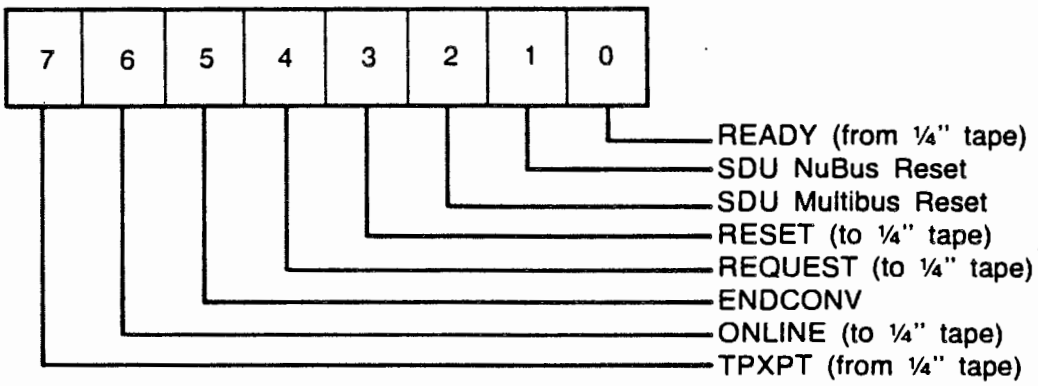


Figure 4-5. CSR1 Read Format.

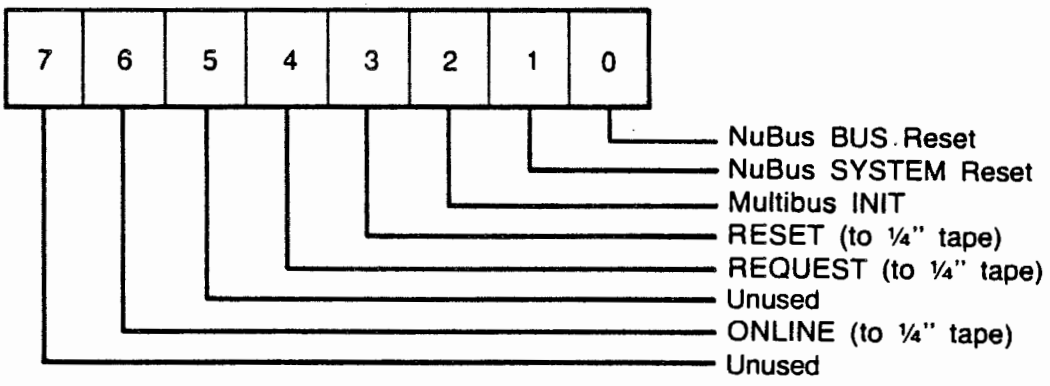


Figure 4-6. CSR1 Write Format.

Bits 0, 3, 4, 6, and 7, when read, convey the status of some 1/4-inch tape interface control lines. Bits 3, 4, and 6, when written, drive corresponding bits on the tape interface. These bits are all active high.

The QIC-02 Interface Specification explains the meaning of these tape interface control lines. Note that all SDU tape

control and status bits are inverted from the corresponding bits shown in the QIC-02 Specification. For example, writing 1 to CSR1 bit 6 will cause the QIC-02 signal ONLINE* to go active (low). If CSR1 is read and bit 7 is 1, an exception condition exists and the signal EXCEPTION* from the tape is active (low).

Writing 1 to bit 0 drives the signal NuBus RESET* active for a single bus cycle.

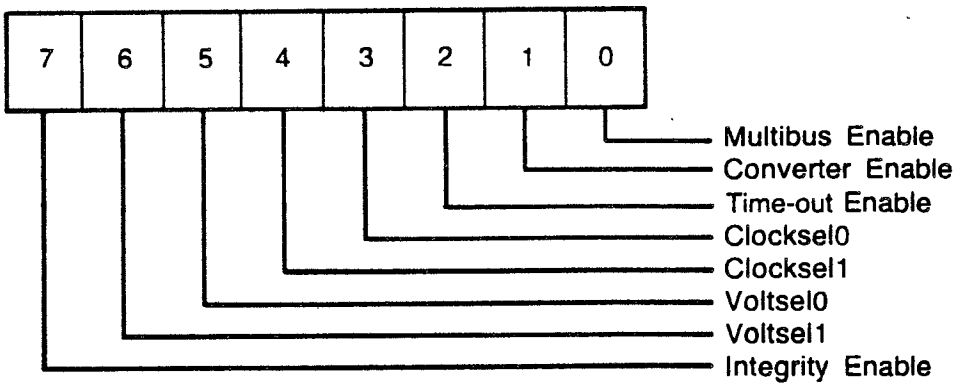
Writing 1 to bit 1 drives NuBus RESET* active; it remains active until 0 is written to this bit. When read, this bit conveys the state of bit 1 but not necessarily the state of NuBus RESET*.

Bit 2 is similar to bit 1, except that it drives Multibus INIT* active. Reading this bit does not necessarily convey the state of INIT*.

Bit 5 is a status flag from the SDU analog-to-digital (A/D) converter which, when active high, indicates that the A/D converter has completed a conversion and the A/D output is valid. Bits 5 and 7 are not connected on the register output; writing data to them has no effect.

4.2.7 Control-Status Register 0

Multibus address 0x1C08C is a second multipurpose control and status register. This register is readable and writable, and the read data indicates the state of each written bit. This register is cleared at power-up and at SDU reset. Figure 4-7 summarizes each bit's function in CSR0.



Notes:

1)

Clocksel1	Clocksel0	Bus Clock
0	0	10 MHz
0	1	9 MHz
1	0	11 MHz
1	1	Off-board source

2)

Voltsel1	Voltsel0	+5 V dc status
0	0	Normal
0	1	Margin high
1	0	Margin low
1	1	Transition

Figure 4-7. Control-Status Register 0.

Bit 0 of CSR0 is the Multibus enable bit. When this bit is 1, the interface between the SDU internal Multibus and the external Multibus is enabled. Under these conditions, the internal Multibus and external Multibus are effectively one Multibus, and the interface is transparent for all address, data, control, interrupt, and arbitration lines.

When this bit is 0, the internal Multibus and external Multibus become separated. At this point, activity on the one has no effect on the other. The SDU continues to drive the external Multibus timing signals (CCLK* and BCLK*), although all other interface connections are severed, until the Multibus priority input is forced on. Attempts to access the external Multibus when this interface is disabled result in Multibus time-outs; the target slave is not affected and no transfer acknowledge occurs.

Bit 1 of CSR0 is the converter enable bit. This bit enables conversions in both directions between the Multibus and

NuBus. When this bit is 0, the SDU is effectively isolated from the NuBus. Attempts to access the NuBus when this bit is 0 result in Multibus time-outs; no NuBus transaction can be initiated.

Note that CSR0 is cleared at power-up and at SDU reset. Therefore, the bus interfaces previously discussed are both disabled and must be explicitly enabled.

Bit 2 of CSR0 enables the SDU to generate NuBus time-outs. The time-out period depends on the value in the time-out register. If this bit is 0, time-outs on the NuBus must be generated by some other system component. Refer to Paragraph 4.2.12, Time-Out Register, for more details.

Bits 3 and 4 of CSR0 select the rate at which the SDU drives the NuBus clock. Figure 4-7 shows the clock rate selected by the various bit patterns. At power-up or SDU reset the normal 10 megahertz clock rate is selected. The 9 megahertz and 11 megahertz clock rates are for diagnostic purposes only and should not be used in normal operation. These clock rates are intended to stress the system and demonstrate operational tolerances. If both bit 3 and bit 4 are high, an off-board clock source, if connected, is selected.

Bits 5 and 6 of CSR0 select the voltage level of the system's +5 volts dc supply. Figure 4-7 shows the voltage level selected by each bit pattern. Note that when the voltage is changed from a marginal to normal value, both bits 5 and 6 should be in a transition state of 1 for no less than 500 milliseconds before clearing them. This period allows the power supply to return to its normal output without enabling the dc out-of-tolerance signal. Failure to go through this transition state can result in spurious SDU resets.

Bit 7 of CSR0 enables SDU diagnostic registers to drive and sense the level of NuBus lines. Paragraph 4.2.14, Bus Integrity Registers, details the relationship between the integrity registers and particular NuBus signals. When bit 7 of CSR0 is 1, the contents of the integrity registers are statically and unconditionally enabled onto the NuBus. Therefore, this bit should only be turned on when the NuBus is in a diagnostic state and, preferably, with NuBus RESET* active.

4.2.8 A/D Converter

The SDU board has an 8-channel A/D converter which could be used for sensing levels of external thermal sensors. The reference inputs to the A/D are GND and +5. Thus, 0x00

indicates that the selected channel is connected to ground or a very low voltage. 0xFF indicates that the channel is connected to a +5 or higher voltage.

To select a channel and read the digitized value:

- Arbitrary data is written to the Multibus address of the desired channel. This initiates the analog signal digitization corresponding to that channel.
- When the signal ENDCONV (bit 5 of CSR1) goes active (high), the digitized data is available from the A/D.
- The digital value is retrieved from the A/D by reading any valid A/D address.

Table 4-5 shows the relationship between Multibus addresses and A/D channels. Note that A/D channel selection occurs on write cycles only, and any A/D address can be used to read the data.

Table 4-5. A/D Converter Addresses

MULTIBUS ADDRESS	A/D CHANNEL	I/O PINS
0x1C100	0	P003 A12
0x1C104	1	P003 B9
0x1C108	2	P003 B10
0x1C10C	3	P003 B11
0x1C110	4	Ground
0x1C114	5	P003 B13
0x1C118	6	P003 B14
0x1C11C	7	+5 volts dc

4.2.9 CMOS TOD Chip

The SDU battery-powered time-of-day chip is a Motorola MC146818. The MC146818 data sheet gives a complete chip description and programming information. The MC146818 can be viewed as an array with 64 byte registers with addresses from 0 to 63. The first 14 bytes (0 to 13) have special purposes, while the remaining 50 bytes are general purpose. Data transfer to this chip requires two bus transactions: writing the register's address to Multibus address 0x1C124, then reading/writing data from/to Multibus address 0x1C120.

4.2.10 RS-232C Serial Ports

The SDU has two RS-232C serial communications ports: the remote serial port and the local serial port. Each serial port consists of an 8251A programmable communications

interface (PCI) and interface logic for receiving and driving RS-232C levels. Both ports operate in asynchronous mode only. The remote serial port drives the SDU reset signal active if a break character is detected on the received data input while the back panel switch is in position 0, 2, 3, or 4. Each serial port is connected to a 25-pin, D-shell connector on the Nu Machine back I/O panel. The remote port is connected to a male connector; the local port is connected to a female connector. Refer to either the Nu Machine Rack Module, General Description or the Nu Machine Office Module, General Description for details on the SDU paddle card and its interface cable to the serial ports.

Appendix D shows the relationship between D-shell pin assignments and 8251A signals. Two Multibus addresses are associated with each port: 1) a command register for initialization, setting control parameters, and reading status, and 2) a data register for reading/writing received/transmitted data. The 8251A data sheet gives detailed programming information. Table 4-6 shows the Multibus addresses for accessing serial port registers.

Table 4-6. Multibus Addresses to Serial Port Registers

MULTIBUS ADDRESS	DESCRIPTION
0x1C150	Remote serial port data register
0x1C154	Remote serial port command/status register
0x1C158	Local serial port data register
0x1C15C	Local serial port command/status register

4.2.11 Programmable Interval Timers

Two Intel 8253 Programmable Interval Timers (PITs) are used on the SDU: PIT0 and PIT1. Each PIT has three timers on it each with an input clock rate of 1.2288 megahertz. The 8253 data sheet gives detailed programming information. Table 4-7 shows the relationship of Multibus addresses to PIT registers and each PIT's function.

Table 4-7. PIT Address Map

MULTIBUS ADDRESS	REGISTER DEFINITION	COUNTER FUNCTION
0x1C160	PIT1 counter #0	Periodic interrupt #0
0x1C164	PIT1 counter #1	Periodic interrupt #1
0x1C168	PIT1 counter #2	Periodic interrupt #2
0x1C16C	PIT1 mode	None
0x1C170	PIT0 counter #0	Remote serial port rate generator
0x1C174	PIT0 counter #1	Local serial port rate generator
0x1C178	PIT0 counter #2	Unused
0x1C17C	PIT0 mode	None

PITs operating as periodic interrupts go to interrupt controller #1 at interrupt levels 4, 5, and 6 (refer to Paragraph 4.2.15, Interrupt Controllers). PITs operating as rate generators drive the receive and transmit clocks of the serial ports. Note that the rate generator PITs must be programmed in the square wave rate generator mode.

The serial data rate is determined by both PIT0 and the 8251A programming. For example, suppose a 9600 baud rate is required, and the 8251A is in 16X mode. Since clock input is 16 times the data rate, the 8251A should have a clock rate of 153600 (16 X 9600) hertz, and the PIT should be programmed to divide the input clock rate (1.2288 megahertz) by 8 (1228800/8 = 153600).

4.2.12 Time-Out Register

Multibus address 0x1C180 accesses the NuBus time-out register on the SDU. This register is both readable and writable. Setting this register to 0 establishes the maximum NuBus time-out period of 25.6 microseconds. Shorter time-out periods (from 0 to 25.6 microseconds) are achieved by writing numbers greater than 0 into this register. For example, if 0x80 is written into the time-out register, the NuBus time-out is set to 12.8 microseconds. This register is cleared at power-up and on SDU resets. Note that NuBus time-outs are only enabled by setting the time-out bit (bit 2) in CSR0.

4.2.13 1/4-Inch Tape Interface

The SDU 1/4-inch tape interface is memory-mapped in Multibus address space. The tape interface state machine translates reads of Multibus address 0x1C1A0 into tape status reads. Writes to this address are translated into command transfers to the tape drive. Multibus addresses in the range from

0x1C600 to 0x1C7FF are translated into string data transfers to or from the tape drive. Only byte transfers are supported.

The tape interface control signals RESET*, ONLINE*, and REQUEST* are determined by bits in CSR1. Paragraph 4.2.6, CSR1, relates these control signals and bit positions. The control signal XFER* is driven by a PAL state machine, which translates Multibus control lines into XFER* and vice versa. The status lines EXCEPTION* and READY* can be sensed by reading CSR1 or received as interrupts on PIC0. The signals DIRC* and ACK* from the tape are used strictly by the tape interface state machine.

For a complete description of the SDU 1/4-inch tape interface, refer to the QIC-02 Interface Specification Rev. D (9/23/82).

4.2.14 Bus Integrity Registers

The SDU can statically drive NuBus signal lines and then read the status of these lines to determine if any NuBus signals are shorted high, low, or together. The bus integrity registers statically and unconditionally drive the NuBus if the integrity enable bit (bit 7) in CSR0 is 1. Therefore, the integrity logic should only be activated if the NuBus is quiescent, preferably with the SDU holding NuBus RESET* active. The integrity logic is in six Multibus address space registers. Each of these registers is readable and writable. If the NuBus signal lines are not shorted, the data read should be the data written. Table 4-8 shows which Multibus address accesses which integrity register.

Table 4-8. Integrity Registers

MULTIBUS ADDRESS	REGISTER NUMBER
0x1C1A8	0
0x1C1AC	1
0x1C1B0	2
0x1C1B4	3
0x1C1B8	4
0x1C1BC	5

Figures 4-8 through 4-13 show the relationship between NuBus signal names and bit positions for each of the integrity registers.

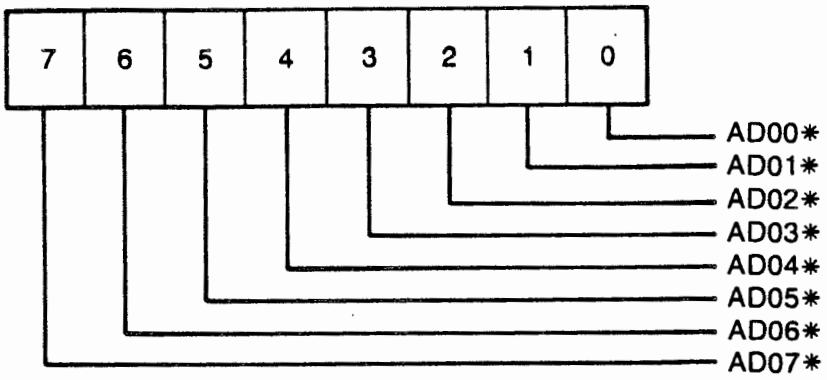


Figure 4-8. Integrity Register 0.

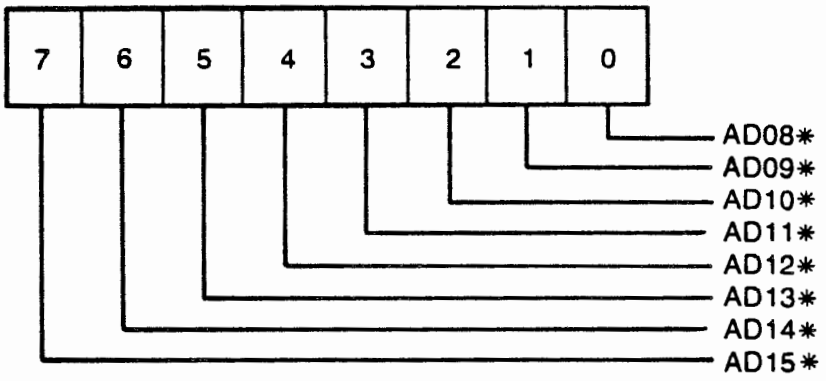


Figure 4-9. Integrity Register 1.

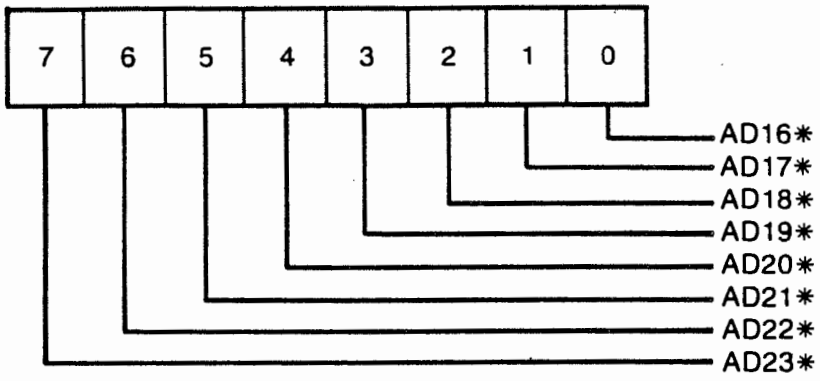


Figure 4-10. Integrity Register 2.

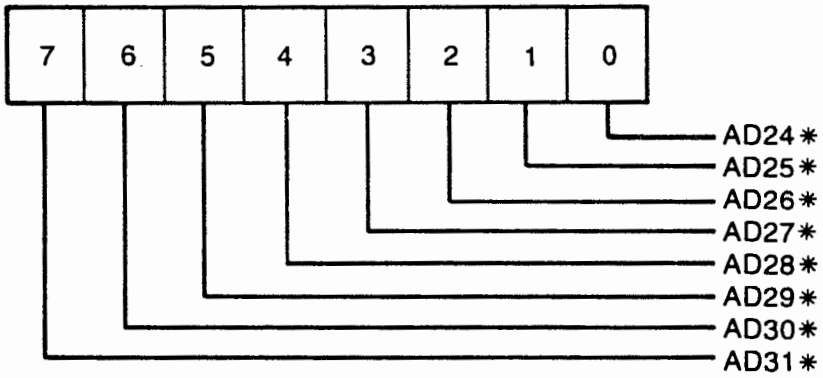


Figure 4-11. Integrity Register 3.

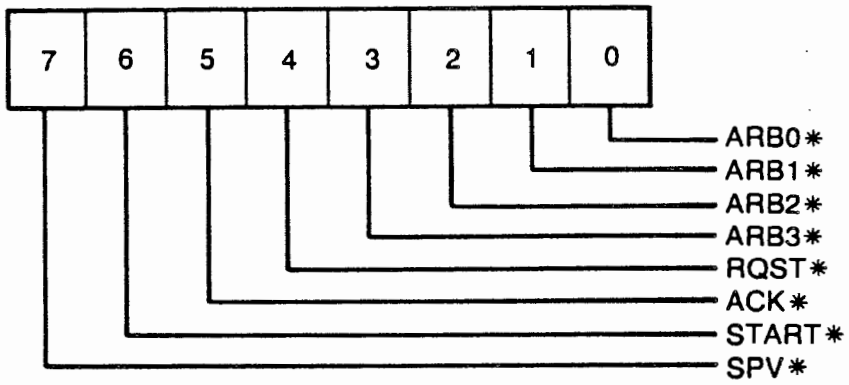


Figure 4-12. Integrity Register 4.

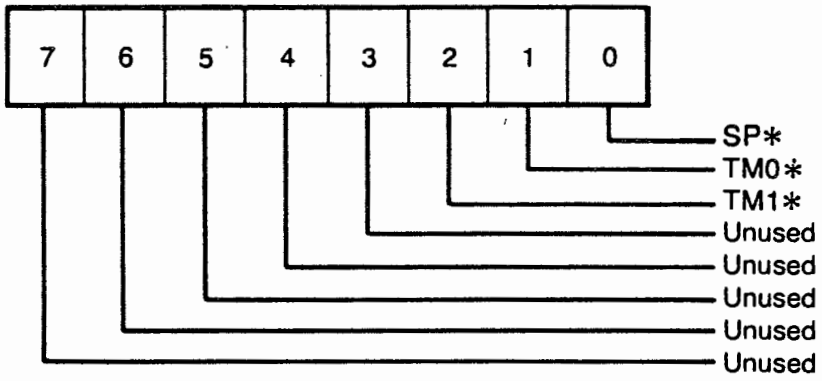


Figure 4-13. Integrity Register 5.

4.2.15 Interrupt Controllers

The SDU has three 8259A programmable interrupt controllers (PICs) which generate interrupts to the 8088. Two of them operate in the slave mode (PIC1, PIC2) and the third (PIC0) operates in the master mode. Detailed programming information is in the 8259A data sheet. The interrupts are

individually maskable, and the priority is also programmable. The interrupt requests can also be programmed to sense either edges (low-to-high transitions) or high levels on the PIC inputs. Table 4-9 through Table 4-11 relate each PIC interrupt number to its interrupt function.

Table 4-9. PIC0 Interrupt Functions

INTERRUPT #	SIGNAL	DESCRIPTION
0	MULTITO*	Multibus time-out
1	TIMEOUT*	NuBus time-out
2	TPXPT*	1/4-inch tape EXCEPTION* input
3	TPRDY*	1/4-inch tape READY* input
4	ACLOINT*	Ac power fail from power supply
5	RSVD*	Reserved
6	PIC2INT*	Interrupt from slave PIC2
7	PIC1INT*	Interrupt from slave PIC1

The MULTITO signal indicates that a Multibus time-out has occurred. Multibus time-outs are generated if the 8088 does not access a bus for longer than 3 milliseconds. Thus, MULTITO will go active if the 8088 executes a halt instruction or if the 8088 is denied Multibus access for longer than the time-out period. Note that Multibus time-outs do not cause any transfer acknowledge on the Multibus. The Multibus does not support error acknowledgment.

The SDU generates a NuBus time-out when the time-out enable bit in CSR0 is 1 and either: 1) A START* cycle occurs on the NuBus and an ACK* cycle has not occurred for longer than the programmed time-out period, or 2) RQST* has been active but a START* has not occurred for longer than the programmed time-out period. In the first situation, the SDU generates an ACK* with a bus time-out code on the TMx* lines. In the second case, the SDU generates an idle cycle to reinitiate arbitration. A time-out interrupt indicates one of these cases.

The TPXPT interrupt indicates an exception condition from the 1/4-inch tape controller. This interrupt is asserted at the high-to-low transition of the EXCEPTION* signal from the tape controller. Refer to the QIC-02 Interface Specification for implications of activity on this line.

TPRDY is similar to TPXPT except that it indicates that the READY* signal on the 1/4-inch tape interface has made a high-to-low transition.

ACLOINT indicates that the ac power to the +5 volt power supply is below a specified level. This interrupt is asserted whenever the power supply ACLO line goes from the low-to-high state.

The slave interrupt controllers, PIC1 and PIC2 are cascaded through the master interrupt controller PIC0. The slave interrupt controllers generate PIC1INT and PIC2INT interrupts to the master. These interrupts indicate that there is an active input on one or more of the respective interrupt lines.

Table 4-10. PIC1 Interrupt Functions

INTERRUPT #	SIGNAL	DESCRIPTION
0	RXRDY0*	Remote serial port receive ready
1	TXRDY0*	Remote serial port transmit ready
2	RXRDY1*	Local serial port receive ready
3	TXRDY1*	Local serial port transmit ready
4	PITINT0*	Periodic interrupt 0
5	PITINT1*	Periodic interrupt 1
6	PITINT2*	Periodic interrupt 2
7	Spare	

RXRDY0 is a signal from the remote serial port indicating that a character is in the receive buffer and ready for processing. This signal is connected directly to pin 14 of the 8251A associated with the remote serial port.

TXRDY0 is a signal from the remote serial port indicating that the transmitter is ready to accept a data character. This signal is connected directly to pin 15 of the 8251A associated with the remote serial port.

RXRDY1 and TXRDY1 are similar to RXRDY0 and TXRDY0 except that they pertain to the local serial port rather than the remote serial port.

PITINT0, PITINT1, and PITINT2 are all interrupt inputs from PIT1. These general system timers can generate interrupts from once every 1.62 microseconds to once every 53 milliseconds. Paragraph 4.2.11, Programmable Interval Timers, gives more information on the interrupt timer.

Table 4-11. PIC2 Interrupt Functions

INTERRUPT #	SIGNAL	DESCRIPTION
0	LOCALINT0*	Multibus interrupt 0
1	LOCALINT1*	Multibus interrupt 1
2	LOCALINT2*	Multibus interrupt 2
3	LOCALINT3*	Multibus interrupt 3
4	LOCALINT4*	Multibus interrupt 4
5	LOCALINT5*	Multibus interrupt 5
6	LOCALINT6*	Multibus interrupt 6
7	LOCALINT7*	Multibus interrupt 7

The inputs to PIC2 are driven by a three-state buffer. The inputs to the buffer are the Multibus interrupt lines INT0* through INT7*. The buffer is activated only when the Multibus enable bit (bit 0) of CSR0 is 1.

The PICs are programmed by writing initialization command words (ICWs) and operation control words (OCWs), as required, into the PIC. Details on these control words and the programming sequence are in the 8259A data sheet. Note in the data sheet a signal, A0, which differentiates between the first ICW (or OCW) and subsequent control words. In the SDU implementation, the signal A0 is driven by Multibus address bit #2 (MADDR02). Table 4-12 relates Multibus addresses and each PIC's control word locations.

Table 4-12. PIC Addresses

MULTIBUS ADDRESS	FUNCTION	CONTROLLER NUMBER
0x1C1C0	ICW1, OCW1	PIC0
0x1C1C4	ICW2-ICW4,OCW2-OCW3	PIC0
0x1C1C8	ICW1, OCW1	PIC1
0x1C1CC	ICW2-ICW4,OCW2-OCW3	PIC1
0x1C1D0	ICW1, OCW1	PIC2
0x1C1D4	ICW2-ICW4,OCW2-OCW3	PIC2

4.2.16 Multibus Interrupt Register

The Multibus has eight interrupt lines (INT0* to INT7*). The SDU can sense any of these lines through PIC2 as described in the preceding paragraph and can drive any of these lines. Each interrupt has a corresponding Multibus address as Table 4-13 shows.

Table 4-13. Interrupt Addressing

MULTIBUS ADDRESS	MULTIBUS INTERRUPT LEVEL
0x1C1E0	0
0x1C1E4	1
0x1C1E8	2
0x1C1EC	3
0x1C1F0	4
0x1C1F4	5
0x1C1F8	6
0x1C1FC	7

Each Multibus interrupt line can be driven active by writing a byte to the corresponding Multibus address with the least significant data bit set to 1. The interrupt can be cleared by writing 0 to the least significant bit at the same location. The status of the interrupt register can be determined by reading address 0x1C1E0. Each bit of this register corresponds to a particular Multibus interrupt bit. For example, if 0x00 is written to 0x1C1E0 through 0x1C1F0, 0x01 is written to 0x1C1F4, and 0x00 is written to 0x1C1F8 and 0x1C1FC, Multibus interrupt 5 will be active and reading 0x1C1E0 will produce 0x20. This interrupt can be cleared by writing 0x00 to 0x1C1F4. Figure 4-14 shows the format of 0x1C1E0 when it is read.

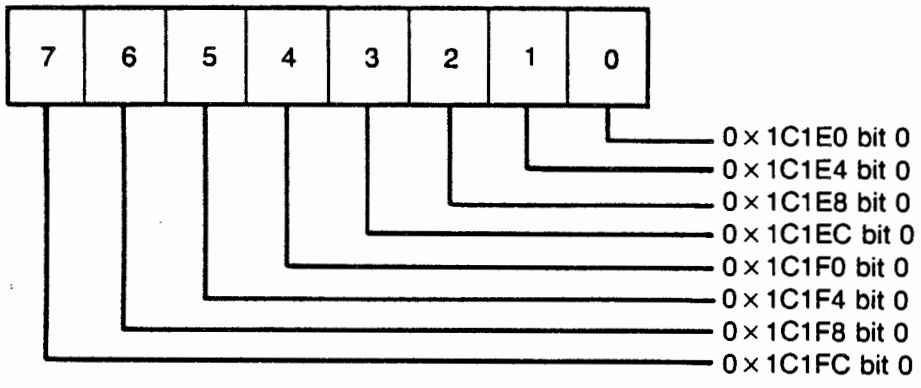


Figure 4-14. 0x1C1E0 Read Format.

4.2.17 CMOS RAM

The SDU battery backed up CMOS RAM is accessed by Multibus addresses 0x1E000 through 0x1FFFC. Only every fourth byte address is a valid RAM address. Thus, byte 0 of the CMOS RAM is at Multibus address 0x1E000, byte 1 is at 0x1E004, and so forth. A total of 2048 byte locations are provided. Figure 4-15 illustrates the CMOS address space. The battery backed up RAM is used to retain system setup and configuration information through power-down cycles. The SDU Operating System User Manual describes the data format stored in the CMOS RAM.

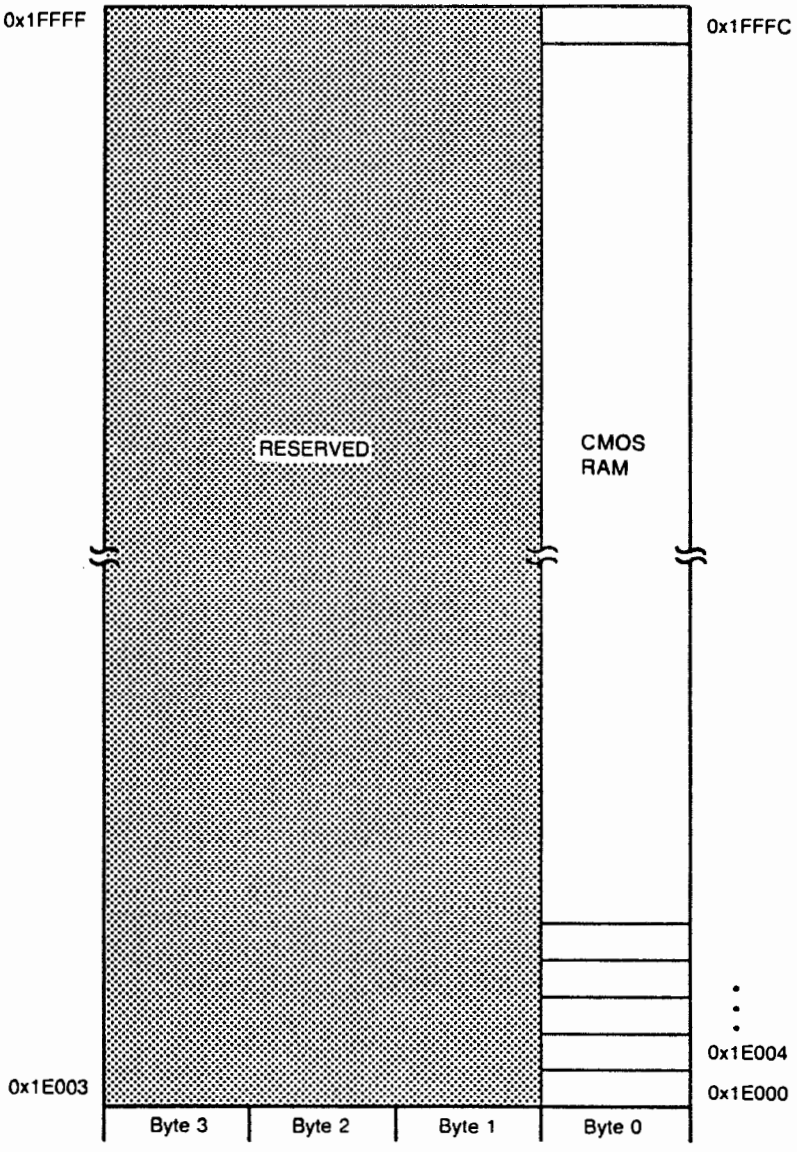


Figure 4-15. CMOS RAM Address Space.

4.3 NuBus Address Space Definition

The SDU is a NuBus slave. All valid SDU addresses are between NuBus address 0xF(ID)000000 and 0xF(ID)FFFFFF, where ID is the SDU hexadecimal slot identification number. The valid address spaces contained within the SDU's NuBus address space consist of three major blocks: Multibus memory space, Multibus I/O space, and configuration space. Figure 4-16 shows the breakdown of the SDU's NuBus addresses.

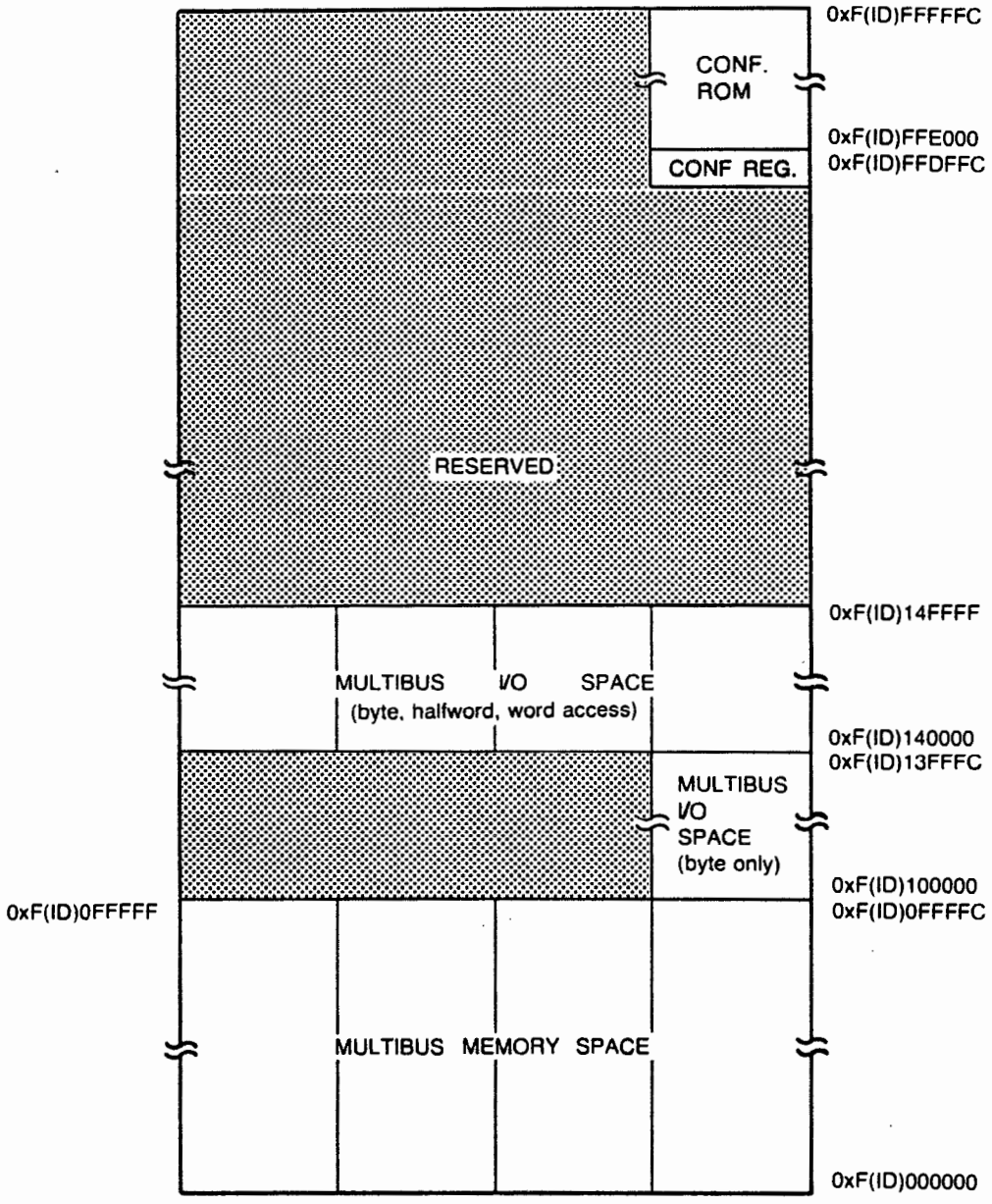


Figure 4-16. SDU NuBus Addresses.

4.3.1 Multibus Memory Space

NuBus addresses 0xF(ID)000000 through 0xF(ID)0FFFFF directly access the Multibus memory space. The addressing is contiguous (no holes). Byte, halfword, and word transfers are supported across the interface. The NuBus address of a Multibus facility is simply the facility's Multibus address appended to 0xF(ID)0... (with AD0* and AD1* adjusted to indicate transfer size). Thus, SDU facilities on the Multibus are all available through the NuBus and have the same operational characteristics (for example, byte access and holes) when viewed through the bus converter as on the Multibus. Note that for any accesses through the NuBus-to-Multibus interface, the converter enable bit (bit 1) of CSR0 must be set to 1--otherwise NuBus time-outs occur.

4.3.2 Multibus I/O Space

Two different mappings access the Multibus I/O space from the NuBus. NuBus addresses 0xF(ID)100000 through 0xF(ID)13FFFC are translated into Multibus I/O operations with only the low byte of each NuBus word mapped into a Multibus I/O port. Thus, the entire Multibus I/O address space is accessible in bytes from the NuBus. Byte, halfword, or word transfers can access the Multibus I/O space in this address range but only the low byte of each NuBus word is valid data. Read operations to this space are mapped into Multibus IORC* operations and writes to this space are mapped into IOWC* operations.

NuBus addresses 0xF(ID)140000 through 0xF(ID)14FFFF are mapped into Multibus I/O operations, as in Multibus memory space mapping, with all byte, halfword, and word transfers supported across the interface. This permits efficient data transfers to I/O locations which support 16-bit operations. Word transfers on the NuBus are translated into two 16-bit Multibus operations. Read operations to this space are mapped into Multibus IORC* operations and writes to this space are mapped into IOWC* operations.

4.3.3 Configuration Space

The configuration space on the SDU is made up of a configuration register and a configuration ROM. The configuration register's standard layout does not provide a reset or enable bit since the SDU performs system boot and is enabled at power-up. Bit 2 is the LED bit. Writing 1 to this bit turns the SDU LED on; writing 0 to this bit turns it off. This bit is turned on at power-up or SDU reset. The configuration register is at address 0xF(ID)FFDFFC.

The 2K-byte configuration ROM is justified to the low byte of each NuBus word. The configuration ROM addresses are 0xF(ID)FFE000 to 0xF(ID)FFFFFC. The configuration ROM

contains board-dependent information and start-up diagnostics. The Nu Generation Computer System Architecture Specification details the contents of this ROM.

4.4 Software Development

Both object and source licenses for the SDU Development System are available, as well as the SDU Operating System source. Contact your local sales representative for further information.

Software development information can be located in the following documents:

TITLE	PART NUMBER
Nu Machine SDU Operating System User Manual	2242811-0001
Nu Machine SDU Operating System Implementation Description	2242812-0001
Nu Machine SDU Operating System Driver Design Guide	2242813-0001
Nu Machine SDU Development System, User Guide	2242815-0001
Nu Machine SDU Development System, Assembler Reference Manual	2242816-0001

The P1 connector detailed in Table A-1 has standard NuBus pin assignments. Signal line characteristics for the NuBus are described in the NuBus Specification.

Table A-1. NuBus Pin Assignments

PIN/ROW	A	B	C
1	-12	-12	RESET*
2	GND	GND	GND
3	SPV*	GND	+5
4	SP*	+5	+5
5	TM1*	+5	TM0*
6	AD1*	+5	AD0*
7	AD3*	+5	AD2*
8	AD5*	-5	AD4*
9	AD7*	-5	AD6*
10	AD9*	-5	AD8*
11	AD11*	-5	AD10*
12	AD13*	GND	AD12*
13	AD15*	GND	AD14*
14	AD17*	GND	AD16*
15	AD19*	GND	AD18*
16	AD21*	GND	AD20*
17	AD23*	GND	AD22*
18	AD25*	GND	AD24*
19	AD27*	GND	AD26*
20	AD29*	GND	AD28*
21	AD31*	GND	AD30*
22	GND	GND	GND
23	GND	GND	RSVD*
24	ARB1*	-5	ARB0*
25	ARB3*	-5	ARB2*
26	ID1*	-5	ID0*
27	ID3*	-5	ID2*
28	ACK*	+5	START*
29	+5	+5	+5
30	RQST*	GND	+5
31	GND	GND	GND
32	+12	+12	CLK*

The Multibus pin assignments are mapped into a DIN connector. Table B-1 shows the Multibus pin assignments on the P2 connector as they appear on the SDU. Multibus signal line characteristics are described in the Multibus Specification.

Table B-1. SDU Multibus Pin Assignments

PIN/ROW	A	B	C
1	AD17*	AD16*	AD15*
2	DAT0*	GND	AD14*
3	DAT2*	GND	DAT1*
4	DAT4*	GND	DAT3*
5	DAT6*	+5	DAT5*
6	DAT8*	+5	DAT7*
7	DATA*	+5	DAT9*
8	DATC*	+5	DATB*
9	DATE*	+5	DATD*
10	ADR0*	+5	DATF*
11	ADR2*	-5	ADR1*
12	ADR4*	GND	ADR3*
13	ADR6*	RSVD*	ADR5*
14	ADR8*	RSVD*	ADR7*
15	ADRA*	-12	ADR9*
16	ADRC*	GND	ADRB*
17	ADRE*	GND	ADRD*
18	INT0*	GND	ADRF*
19	INT2*	GND	INT1*
20	INT4*	+12	INT3*
21	INT6*	RSVD*	INT5*
22	INTA*	RSVD*	INT7*
23	CCLK*	GND	AD13*
24	CBRQ*	+5	AD12*
25	BHEN*	+5	AD11*
26	AACK*	+5	AD10*
27	XACK*	+5	INH2*
28	IORC*	+5	INH1*
29	MRDC*	GND	IOWC*
30	BUSY*	GND	MWTC*
31	BPRN*	GND	BREQ*
32	BCLK*	INIT*	BPRO*

The P3 pin assignments are used for I/O. Tables C-1 through C-3 describe the signals on this connector.

Table C-1. P3 Row A

PIN/ROW	SIGNAL	DESCRIPTION
A01	TPDAT0*	1/4-inch tape data bit 0
A02	TPDAT2*	1/4-inch tape data bit 2
A03	TPDAT4*	1/4-inch tape data bit 4
A04	TPDAT6*	1/4-inch tape data bit 6
A05	TPDIR*	1/4-inch tape DIRC* control line
A06	TPACK*	1/4-inch tape ACK* control line
A07	TPRDY*	1/4-inch tape READY* control line
A08	Open	
A09	SWITCH0	Back panel switch bit 0
A10	SWITCH2	Back panel switch bit 2
A11	RSVD	Reserved
A12	ADCCH0	A/D channel 0
A13	LED0	RUN LED on front panel
A14	LED2	ATTN LED on front panel
A15	GND	Logic ground
A16	Open	
A17	TXD0	Remote serial port transmit data
A18	DTR0	Remote serial port data terminal ready
A19	CTS0	Remote serial port clear to send
A20	TXD1	Local serial port transmit data
A21	DTR1	Local serial port data terminal ready
A22	CTS1	Local serial port clear to send
A23	GND	Logic ground
A24	Open	
A25	ACPF	Ac powerfail signal from power supply
A26	DCOT	Dc out-of-tolerance from power supply
A27	Open	
A28	MARG2	Margin control to power supply
A29	Open	
A30	PWROFF	Ac shutdown to ac distribution box
A31	GND	Logic ground
A32	Open	

Table C-2. P3 Row B

PIN/ROW	SIGNAL	DESCRIPTION
B01	TPXPT*	1/4-inch Tape EXCEPTION* control line
B02	GND	Logic ground
B03	GND	Logic ground
B04	Open	
B05	Open	
B06	Open	
B07	BFTPRST*	1/4-inch tape RESET* control line
B08	Open	
B09	ADCCH1	A/D channel 1
B10	ADCCH2	A/D channel 2
B11	ADCCH3	A/D channel 3
B12	GND	Logic ground
B13	ADCCH5	A/D channel 5
B14	ADCCH6	A/D channel 6
B15	ADCCH7	A/D channel 7
B16	GND	Logic ground
B17	Open	
B18	Open	
B19	GND	Logic ground
B20	Open	
B21	Open	
B22	Open	
B23	GND	Logic ground
B24	Open	
B25	Open	
B26	Open	
B27	Open	
B28	Open	
B29	Open	
B30	GND	Logic ground
B31	GND	Logic ground
B32	Open	

Table C-3. P3 Row C

PIN/ROW	SIGNAL	DESCRIPTION
C01	TPDAT1*	1/4-inch tape data bit 1
C02	TPDAT3*	1/4-inch tape data bit 3
C03	TPDAT5*	1/4-inch tape data bit 5
C04	TPDAT7*	1/4-inch tape data bit 7
C05	BFTPXFER*	1/4-inch tape XFER* control line
C06	BFTPRQST*	1/4-inch tape REQUEST* control line
C07	BFTPONLINE*	1/4-inch tape ONLINE* control line
C08	Open	
C09	SWITCH1	Back panel switch bit 1
C10	SWITCH3	Back panel switch bit 3
C11	RSVD	Reserved
C12	EXTRST*	Back panel reset switch
C13	LED1	SETUP LED on front panel
C14	RSVD	Reserved
C15	RSVD	Reserved
C16	Open	
C17	RTS0	Remote serial port request to send
C18	RXD0	Remote serial port received data
C19	DSR0	Remote serial port data set ready
C20	RTS1	Local serial port request to send
C21	RXD1	Local serial port received data
C2	DSR1	Local serial port data set ready
C23	GND	Logic ground
C24	Open	
C25	Open	
C26	Open	
C27	Open	
C28	Open	
C29	Open	
C30	Open	
C31	Open	
C32	Open	

The 1/4-inch tape interface signal line characteristics are described in the QIC-02 Interface Specification. The back control panel switch inputs to the SDU are all pulled up to +5 volts through 1K ohm resistors on the SDU. These signals are typically either open or shorted to ground by the external switch. The A/D channel inputs are high impedance inputs to an A/D converter. Locations for resistors in parallel with the A/D are provided on-board to facilitate voltage divider or controlled current circuitry.

The front panel LED outputs are driven by a 74S241 buffer. The LEDs turn on when these signal lines are driven low.

The LEDs should be connected to +5 volts through a current limiting resistor.

The serial port signal lines are all at standard RS-232C levels. The ac powerfail, dc out-of-tolerance, and margin signals are all determined by the power supply.

Normally, ac powerfail is logic 0. With ac removal, the powerfail signal goes to logic 1 at least 3 milliseconds before loss of dc output. On ac turn-on, this signal remains high until the output is in regulation.

Normally, dc out-of-tolerance is logic 0. When the output is under or over voltage by 5 percent, dc out-of-tolerance goes to logic 1. When the output goes back to within tolerance, this signal remains high for 100 to 500 milliseconds.

The SDU has the capability to margin the power supply by +/-7 percent. The system margin checking driver circuit is on the SDU board.

The ac shutdown signal is an open-collector output capable of sinking 10 milliamps. Signal levels up to 30 volts can be tolerated on this line.

Appendix D SERIAL PORT PIN ASSIGNMENTS

Table D-1. Remote Serial Port Pin Assignments

PIN/ROW	RS-232C DESIGNATION	SDU NAME	8251A PIN
1	Frame ground (AA)	Chassis ground	
2	Transmitted data (BA)	TXD	19
3	Received data (BB)	RXD	3
4	Request to send (CA)	RTS	23
5	Clear to send (CB)	CTS	17
6	Data set ready (CC)	Not used	
7	Signal ground (AB)	Logic ground	
8	Data carrier detect (CF)	DSR	22
9	Not used		
10	Not used		
11	Not used		
12	Not used		
13	Not used		
14	Not used		
15	Transmitter clock (DB)	Not used	
16	Not used		
17	Receiver clock (DD)	Not used	
18	Not used		
19	Not used		
20	Data terminal ready	DTR	24
21	Not used		
22	Not used		
23	Not used		
24	Not used		
25	Not used		

Note:

Connector is a 25-pin, D-shell, male connector.

Table D-2. Local Serial Port Pin Assignments

PIN/ROW	RS-232C DESIGNATION	SDU NAME	8251A PIN
1	Frame ground (AA)	Chassis ground	
2	Received data (BB)	RXD	3
3	Transmitted data (BA)	TXD	19
4	Clear to send (CB)	CTS	17
5	Request to send (CA)	RTS	23
6	Data set ready (CC)	Pull-up	
7	Signal ground (AB)	Logic ground	
8	Data terminal ready	DTR	24
9	Not used		
10	Not used		
11	Not used		
12	Not used		
13	Not used		
14	Not used		
15	Receiver clock (DD)	Not used	
16	Not used		
17	Transmitter clock (DB)	Not used	
18	Not used		
19	Not used		
20	Data carrier detect (CF)	DSR	22
21	Not used		
22	Not used		
23	Not used		
24	Not used		
25	Not used		

Note:

Connector is a 25 pin, D-shell, female connector.

Appendix E MULTIBUS COMPLIANCE LEVELS

The Multibus Specification allows optional levels of compliance in several areas. This section describes Multibus attributes supported by the SDU.

Data Path The SDU supports a 16-bit data path on the Multibus. Byte swapping techniques are used to allow both 8-bit and 16-bit cards to work in the system.

Memory Address Path The SDU supports a 20-bit Multibus memory address path. Multibus cards using 16-bit or 24-bit addressing may not be compatible.

I/O Address Path The SDU supports a 16-bit I/O address path but does not act as an I/O slave. 8-bit I/O address path slaves are supported.

Interrupt Attributes The SDU supports only nonbus-vectored interrupts over the Multibus.

Multibus Arbitration The SDU supports the Multibus daisy chain priority resolution scheme and drives CCLK* and BCLK* on the Multibus. CCLK* is driven at 10 megahertz but BCLK* (arbitration clock) is driven at 5 megahertz to permit up to seven potential masters on the Multibus. The SDU has two potential masters on it--the 8088 and the NuBus converter.

USER'S RESPONSE SHEET

Manual Title: Nu Machine System Diagnostic Unit, General Description (2242829-0001)

Manual Date: August 1, 1984 Date of this Letter: _____

User's Name: _____ Telephone: _____

Company: _____ Office/Department: _____

Street Address: _____

City/State/Zip Code: _____

Please list any discrepancy found in this manual by page, paragraph, figure, or table number in the following space. If there are any other suggestions that you wish to make, feel free to include them. Thank you.

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