M2361A

Mini-Disk Drive
Customer Engineering Manual

FUJITSU

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CHAPTER 1 GENERAL DESCRIPTION

1.1 General Description

1.1.1 General description

The M2361A Disk Drive is a compact state-of-the-art moving head disk drive with a storage capacity of up to 689 megabytes (unformatted) in a very compact package. It uses Winchester type heads and platters, allowing higher recording density, data transfer rate, and greater reliability, while offering a faster access time. The media is non-removable. This drive is appropriate for large capacity, high speed data storage in an online and/or batch system.

Higher cost performance and improved reliability can be achieved in computer systems that utilize M2361A disk drives.

The drive is designed to meet the following standards:
1. UL478 Electronic Data Processing Unit and Systems.
2. CSA C22.2 No. 154-1983 Data Processing Equipment.
3. IEC 435.
4. FCC Part 15 Sub Part J Class A.
5. VDE 0871 Class B.

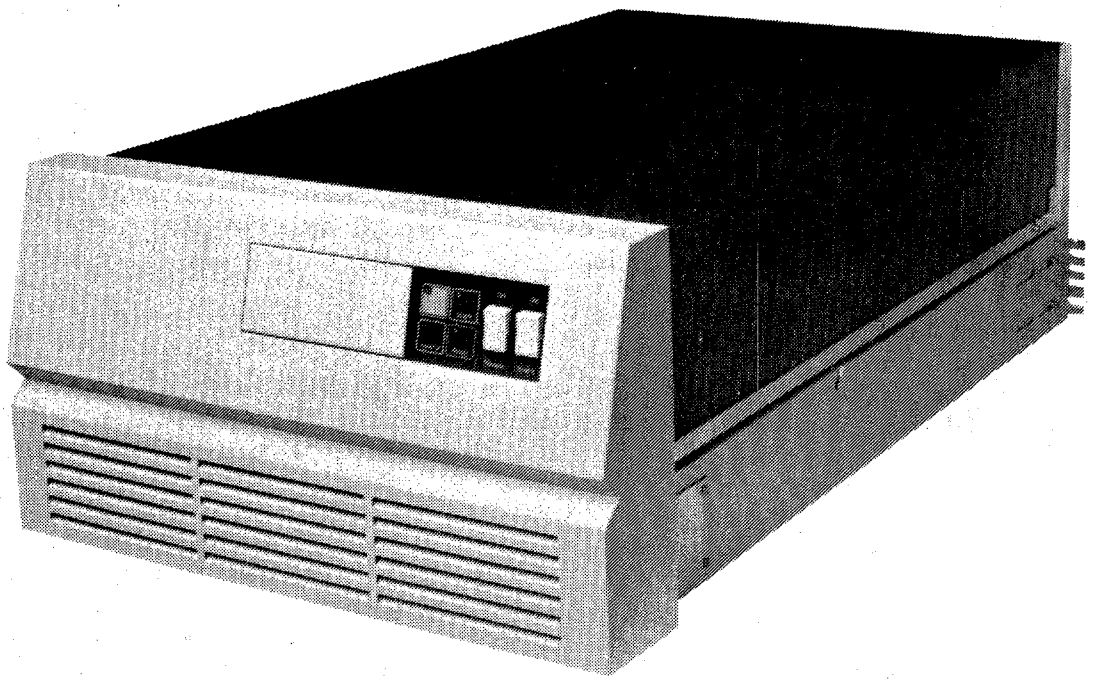


Figure 1.1.1 External view of M2361A

1.1.2 Features

(1) Large capacity and high performance

- 689 megabytes of unformatted data can be stored on six disks.

- The M2361A disk drive provides exceedingly high performance characteristics such as 2.458 megabytes per second data transfer, 18 milliseconds average access time, and 8.33 milliseconds average latency time.

(2) Compact size

The disk drive unit configured with Disk Enclosure (DE), DC power supply and LSI circuits, is available for mounting in a standard 19-inch rack.

(3) High reliability

The disk enclosure includes a rotary actuator, a direct-drive spindle motor, the magnetic heads, disks and carriage. A completely sealed self-contained airflow system is used within the DE to assure a clean environment for low-flying heads, thus ensuring very high reliability.

(4) High serviceability

- The DE can easily be removed for replacement in the field by CE.

- The display panel appears when the sub-panel is opened.
  This panel allows;
  . Drive address setting
  . Drive status display
  . Drive sector count setting
  As a result, except for parts replacement, the drive need not be pulled out from the 19" rack.

(5) Maintenance-free

The M2361A disk drive requires substantially reduced maintenance because of the completely sealed DE, a direct-drive DC spindle motor and highly reliable printed circuit boards.

(6) Auto actuator lock

The rotary actuator is locked by means of a plunger magnet to prevent the head from moving across the disk surface during transportation. The plunger magnet unlocks automatically immediately after the AC power is supplied.

(7) Other features

- High recording density with state-of-the-art technology
  A recording density of more than 10^7 bits per square inch is achieved with the advanced head and disk.

- Low power consumption
  Less than 0.64 KVA is required despite the large storage capacity.

- Dual channel feature
  This option permits two controllers to access the same disk drive so that a file can be shared by two different systems.

- Modified SMD Interface
  The interface signals between the controller and the disk drive are partially modified from the standard SMD interface to agree with higher track capacity and higher maintainability.

The following are the major modified items.

(1) Data transfer rate
(2) Track capacity
(3) Timing of Read/Write operation
(4) Addition of Tag 4 and Tag 5

1.2 Specifications

1.2.1 Physical specifications

Table 1.2.1 Physical specifications

Item	Conditions	Specifications
Dimension	Height	10.4" (264 mm)
	Width	19" (483 mm)
	Depth	28" (710 mm)
Weight*		143 lbs (65 kg)

* Excluding slide guide

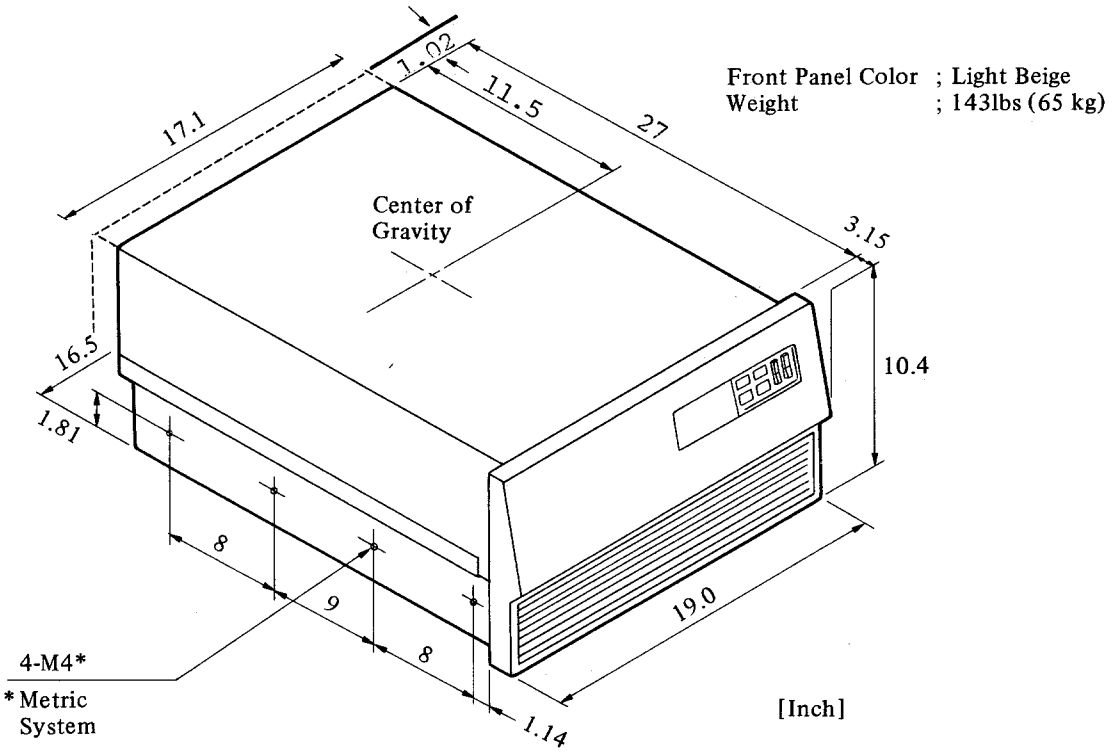


Figure 1.2.1 Physical specifications

1.2.2 Environmental specifications

Table 1.2.2 Environmental specifications

Environment	Storage or transmit in packaged form		On Site Non-operating	Operating Office Environment
Temperature	Within 24 hours	More than 24 hours	23°F-140°F (-5°C-60°C) Max. change 18°F/hour (10°C/hour)	50°F-104°F (10°C-40°C) Max. change 18°F/hour (10°C/hour) Each drive must be used within the range of 31°F (17°C) in all its life. for example 64°F-95°F (18°C-35°C)
	-40°F-140°F (-40°C-60°C) Max. change 36°F/hour (20°C/hour)	23°F-140°F (-5°C-60°C) Max. change 18°F/hour (10°C/hour)		
Humidity	5%-95% RH Non-condensing		20%-80% RH Max. change 10%/hour Non-condensing	
Vibration	3G (when locked for shipment)		0.2G (5-50 Hz) 1G (50-500 Hz)	
Shock	5G (Max. 30 ms)		3G (Max. 10 ms)	2G (Max. 10 ms)
Altitude	40,000 FT (12,000 m)		10,000 FT (3,000 m)	
Dust	0.168 mg/m^3 (Stearic Acid Standard)			
Air flow	———			2.5 m^3/min.
Acoustics	———			60 dB A

* $°C = \frac{5}{9}(°F-32)$

1.2.3 Power requirements

Table 1.2.3 Power requirements (Typical values)

Voltage (Vac±10%)	Frequency (Hz±2Hz)	Current (Aac)		Power Consumption (kVA)	Heat dissipation	
		Starting*	Running		Kcal/hour	BTU/hour
100	50/60	7.8/7.3	6.0/5.7	0.60/0.57	470/440	1,800/1,700
120		6.5/6.3	4.8/4.6	0.57/0.55	440/430	1,700/1,600
200		4.3/3.8	3.1/3.0	0.62/0.60	480/470	1,900/1,800
220		4.1/3.6	2.9/2.8	0.64/0.62	500/480	2,000/1,900
240		4.0/3.5	2.6/2.5	0.62/0.60	480/470	1,900/1,800

* Worst case transient with a maximum of 40 amps for less than 1/2 cycle of input AC power. Refer to Figure 1.2.2.

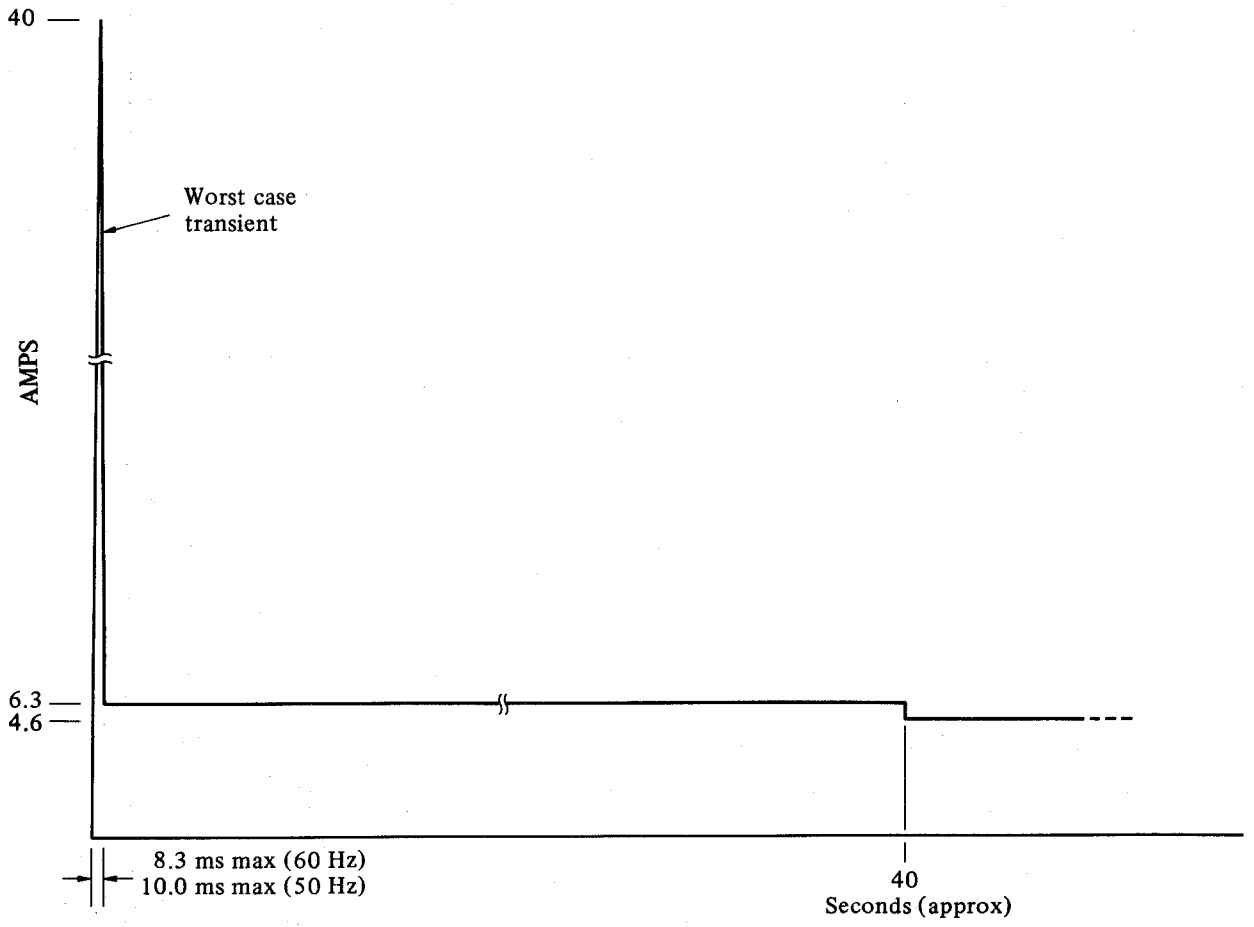
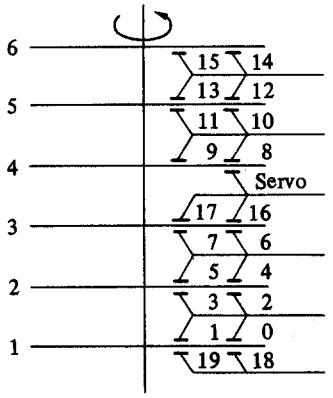


Figure 1.2.2 AC start/run current curve (6.3 amps and 4.6 amps are for 120 Volt 60 Hz case)

1.2.4 Data recording specifications

Table 1.2.4 Data recording specifications

Capacity	/Drive (MB)	689.8 (Unformatted)
	/Track (KB)	40,960 (Unformatted)
Configuration of Disks and Heads		
Rotational Speed (RPM)		3,600 ± 2%
Latency (ms)		8.33
Disk	Diameter (Inch)	10.5
	Number	6
Heads	/Drive	20 + 1 (Servo)
	/Surface	2
Cylinders		842
Data Transfer Rate (MB/sec)		2.458
Positioning Time (ms)	Maximum	35
	Average	18
	Minimum	5.5
Track Density (TPI)		880
Bit Density (BPI)		18,610
Data Coding	on interface	NRZ
	on disk surface	RLL Code

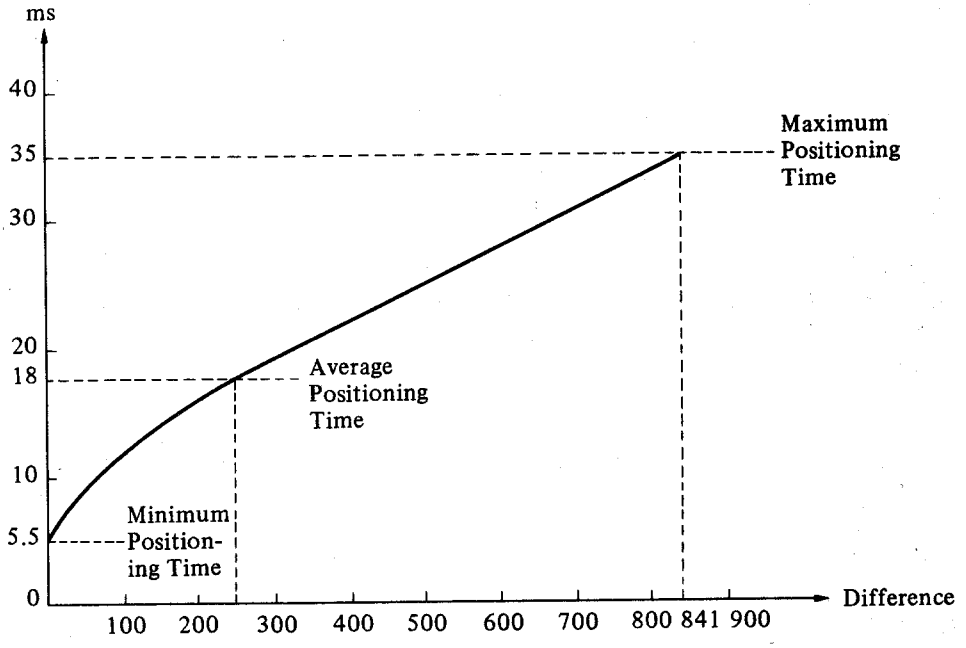


Figure 1.2.3 Positioning time vs. difference

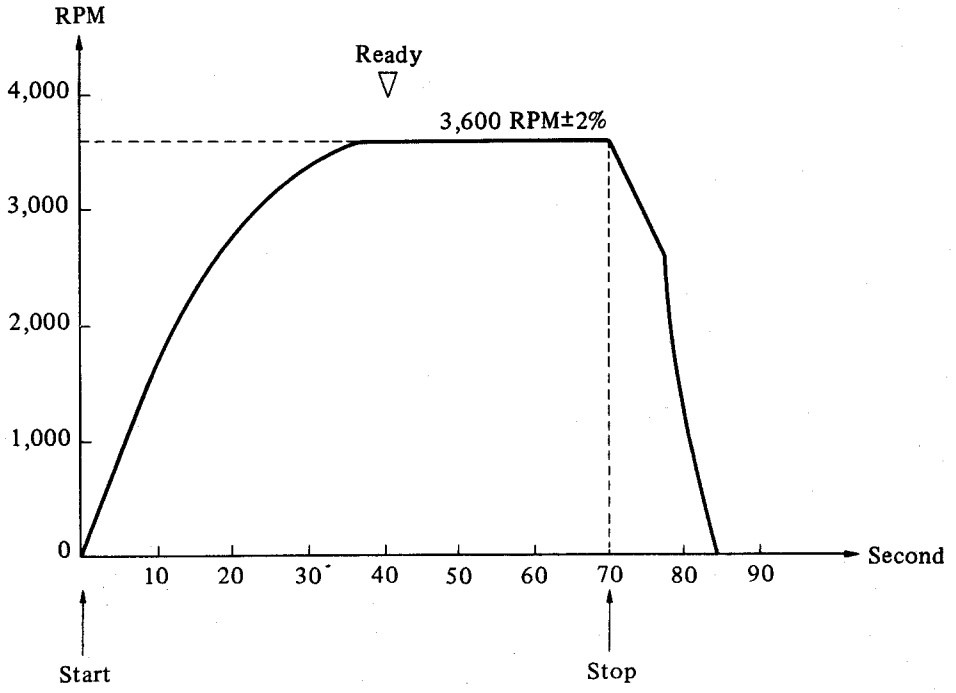


Figure 1.2.4 Spindle start/stop time

1.2.5 Reliability

(1) Mean time between failure (MTBF)

The MTBF is defined as follows:

$$\text{MTBF} = \frac{\text{Estimated Operating Hours}}{\text{Number of Equipment Failures}}$$

The MTBF shall exceed 20,000 hours (design value). Estimated operating hours should not include any maintenance time. Equipment failure means any stoppage or substandard performance of the equipment because of equipment malfunction, excluding that caused by operator error, cable failure, or other failure not due to the equipment. To establish a meaningful MTBF, operating hours must be greater than 6,000 hours and shall include field performance data from all field sites.

For the purpose of this specification, equipment failures are defined as those failures necessitating repair or replacement on an unscheduled basis.

(2) Mean time to repair (MTTR)

The mean time to repair shall not exceed 0.5 hour. It is defined as the time for an adequately trained and competent service technician to diagnose and correct a malfunction.

(3) Preventive maintenance time

The air filter should be cleaned or replaced at one year intervals, or as required.

(4) Component Life

The M2361A provides a useful life of five (5) years before factory overhaul or replacement is required.

(5) Power Less

Data integrity is assured in the event of a power loss (data is not assured during write operation).

1.2.6 Data integrity

The following error rates assume that the M2361A is being operated within specification. Errors caused by media defects or equipment failures are excluded.

(1) Read errors

Prior to determination of a read error rate, the data shall have been verified as written correctly and all media defects flagged.

- Recoverable Error Rate
  A recoverable read error is one which can be read correctly within four retries when reading on track, and should not exceed ten per 10^{11} bits.

- Unrecoverable Error Rate
  An unrecoverable read error is one which cannot be read correctly within five retries and should not exceed ten per 10^{14} bits.

  Retry routine; after 4 times of re-reading with and without offset, RTZ must be performed.

(2) Positioning error rate

The positioning error which can be corrected within one retry should not exceed one per 10^{7} seeks.

(3) Quality standards of media at shipment (Summary)

- The number of defects per DE shall not exceed 700.

- The number of defects per track shall not exceed 4.

- The number of defective tracks per DE shall not exceed 45. (A track containing two or more defects is defined as a defective track.)

- Physical head 0 and 1 at cylinder 0 should be perfect tracks.

1.3 Configuration

1.3.1 Configuration

The basic configuration of the drive and its functional block diagram are shown in Figure 1.3.1 and 1.3.2, respectively. Connection between units in the drive is also shown in Figure 1.3.3.

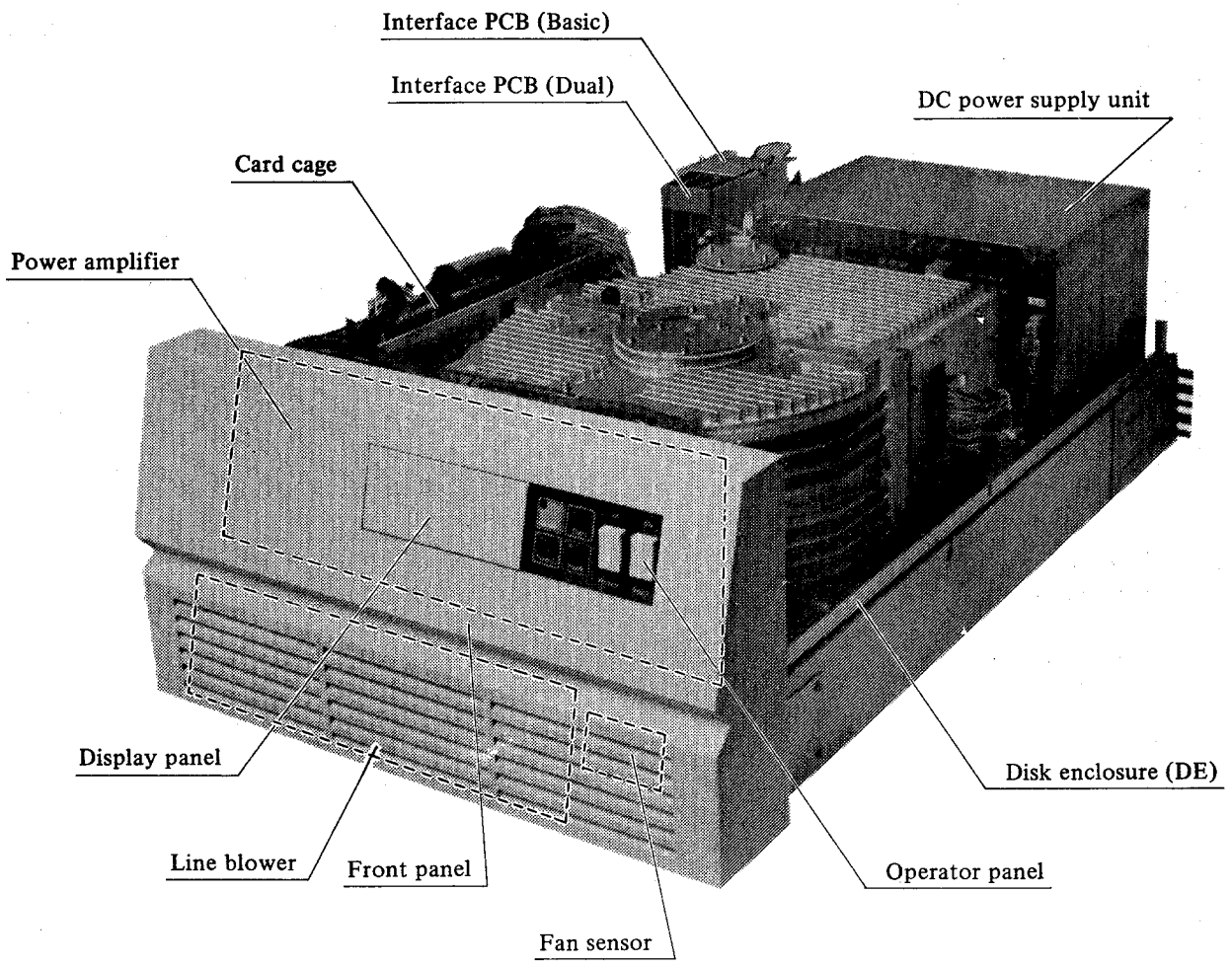


Figure 1.3.1 Mechanical configuration

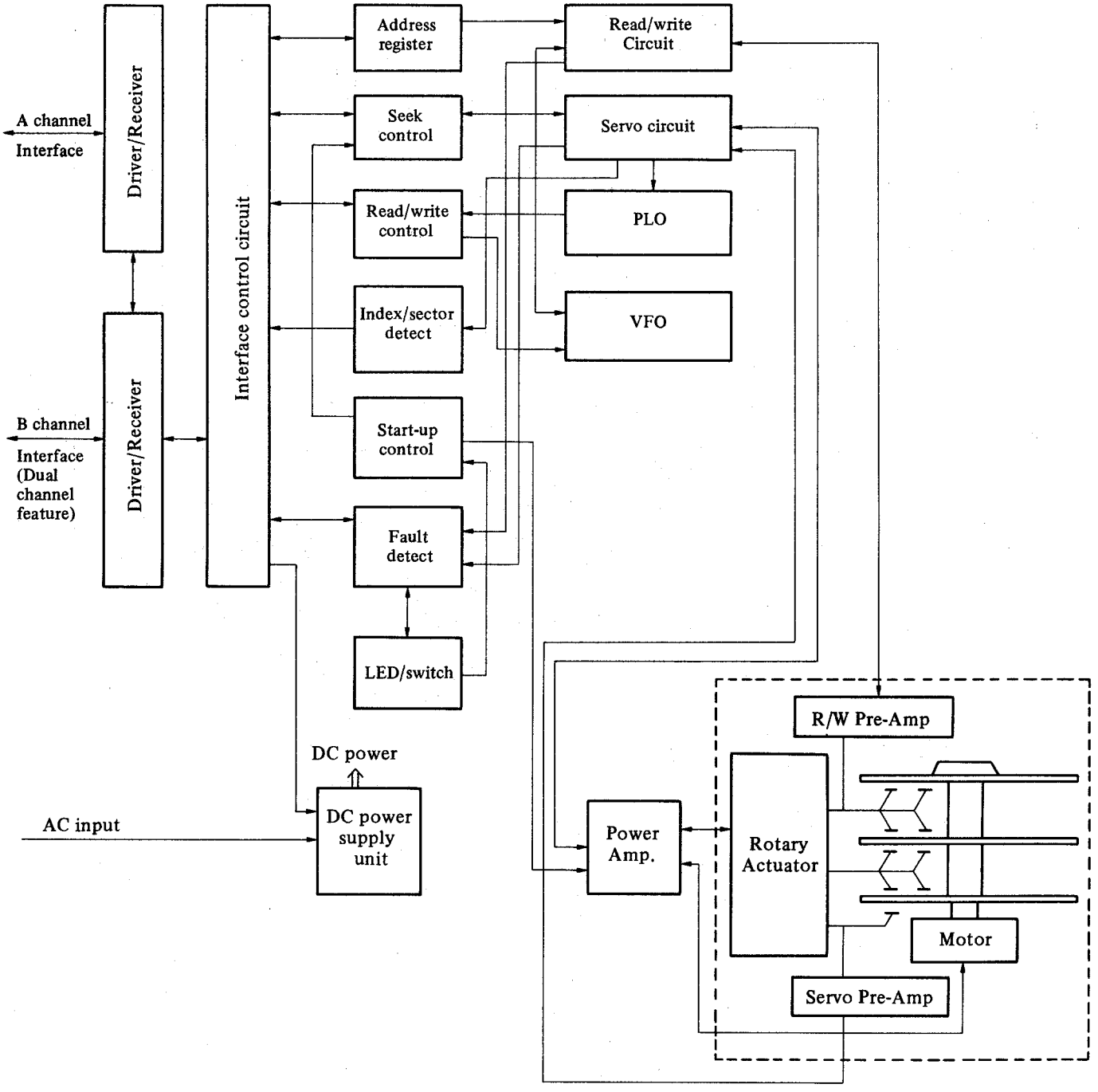


Figure 1.3.2 Functional block diagram

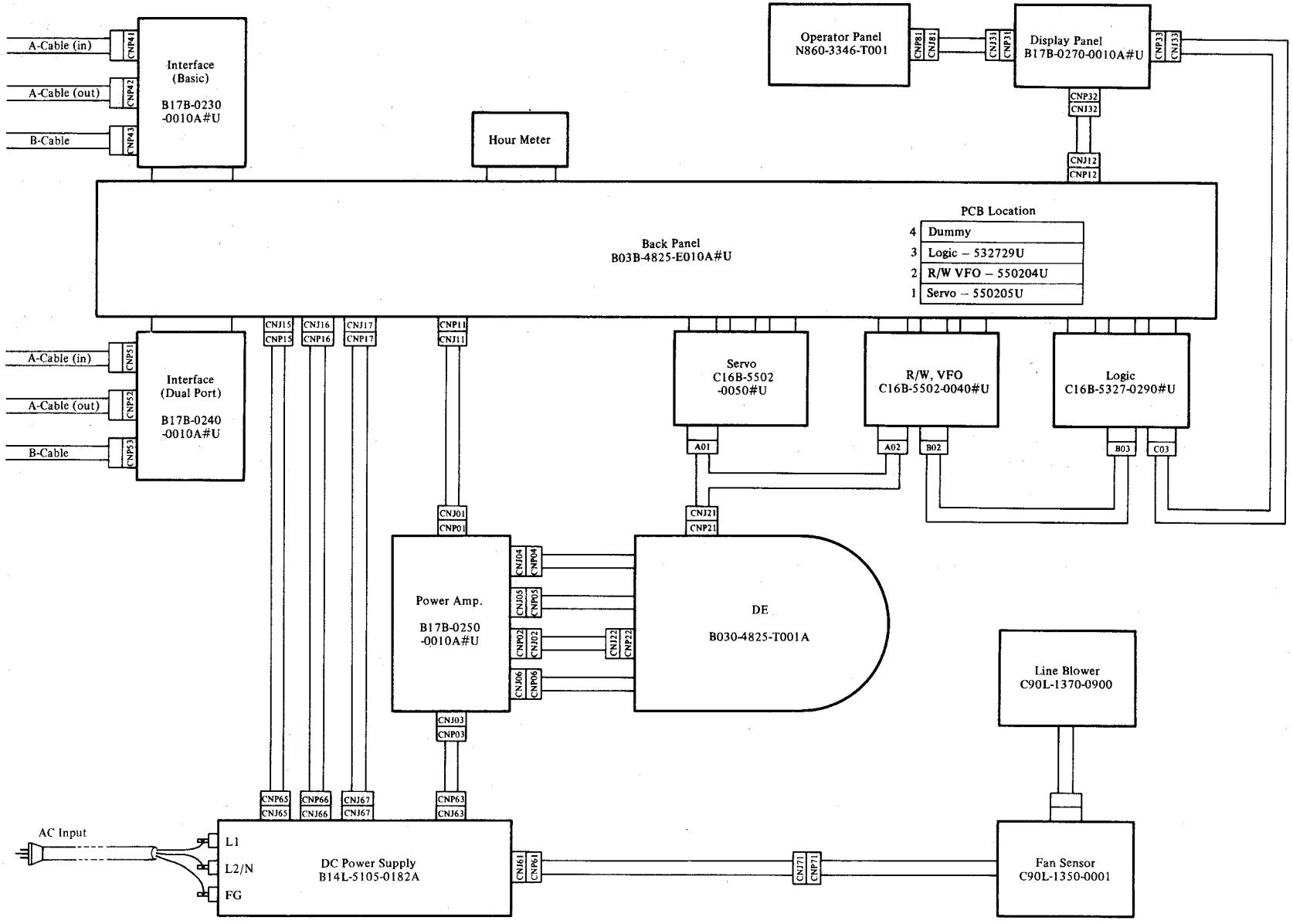
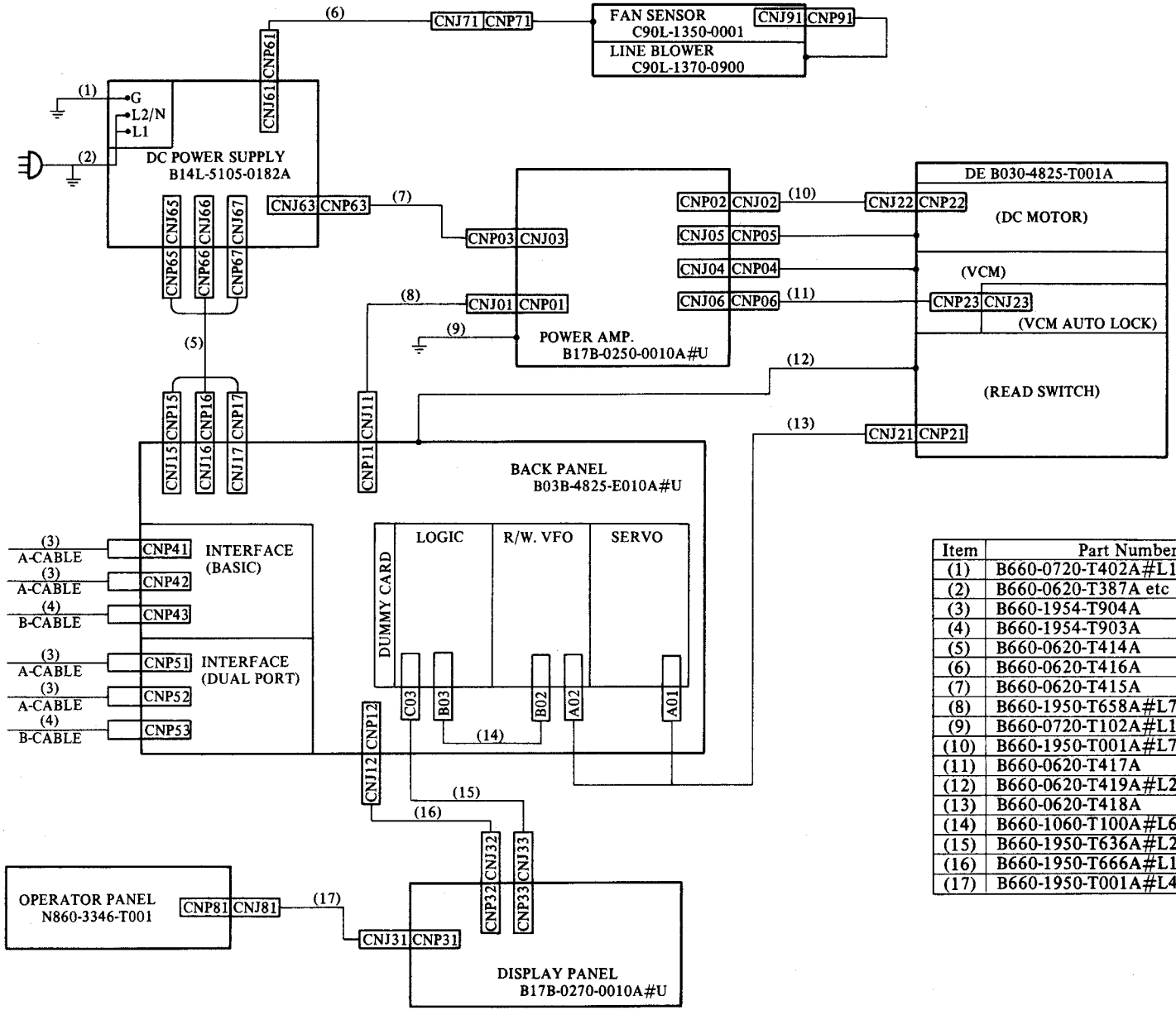


Figure 1.3.3 Connection diagram



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(4)	B660-1954-T903A
(5)	B660-0620-T414A
(6)	B660-0620-T416A
(7)	B660-0620-T415A
(8)	B660-1950-T658A#L720R0
(9)	B660-0720-T102A#L100R0
(10)	B660-1950-T001A#L700R0
(11)	B660-0620-T417A
(12)	B660-0620-T419A#L220R0
(13)	B660-0620-T418A
(14)	B660-1060-T100A#L60R00
(15)	B660-1950-T636A#L220R0
(16)	B660-1950-T666A#L110R1
(17)	B660-1950-T001A#L430R0

Figure 1.3.4 Internal connection diagram

1.3.2 Options

(1) Option list

Table 1.3.1 Option list

No.	Name	Specification	Remark	
1	A-Cable	B660-1954-T904A	Max. 30 m	Cable length can be specified in 0.5 m increments.
2	B-Cable	B660-1954-T903A	Max. 15 m	
3	Power Cable B	B660-0620-T387A #3.0 m	L = 3 m	UL/CSA Recognized 200/220/240 V
4	Power Cable B	B660-0620-T387A #5.0 m	L = 5 m	
5	Power Cable C	B660-1055-T033A	L = 2.5 m	UL/CSA Recognized 100/120 V
6	Power Cable D	B660-1055-T034A	L = 3.5 m	
7	Power Cable E	B660-1055-T035A	L = 4.5 m	
8	Line Terminator	B03L-4790-0003A	Note that two line terminators are required in dual port system.	
9	Interface Circuit (Dual Part)	B17B-0240-0010A #U	Permits two controllers to access the same drive.	
10	Slide Guide	B03B-4825-D020A		
11	Hour Meter	B61L-0140-0011A #10000	10,000 hours	
12				
13				

*Check with your local sales office for lengths available.

Note that A- and B-Cable length must be specified by adding comment behind the cable specification.

Example: B660-1954-T904A #10.5 m (10.5 meters)

(2) Specifications of cables and connectors

Table 1.3.2 Cables and connectors

	Cable		Connector (Supplier)	
	Specification	Supplier	Drive Side	Cable Side
A-Cable (60-Pin)	Zo = 100 ± 10Ω 28 AWG 7 Strands 100 FT. Max.	FUJITSU	FUJITSU FCN-704P060-AU/M	FUJITSU FCN-707B060-AU/B
			3M 3372-1003LCSB	3M 3334-6500 and 3448-3060
B-Cable (26-Pin)	Zo = 100 ± 10Ω 28 AWG 7 Strands 50 FT. Max.	FUJITSU	FUJITSU FCN-705P026-AU/M	FUJITSU FCN-707B026-AU/B
			3M 3429-1003LCSB	3M 3399-6500 and 3448-3026
Power Cable B	See Figure 1.3.5			
Power Cable C∿E	See Figure 1.3.6			

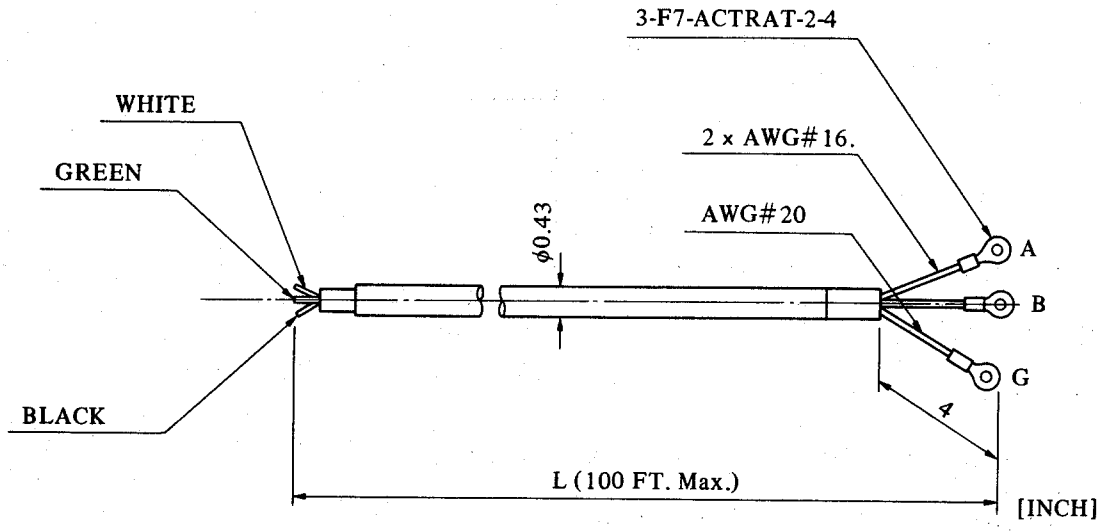


Figure 1.3.5 Power cable B

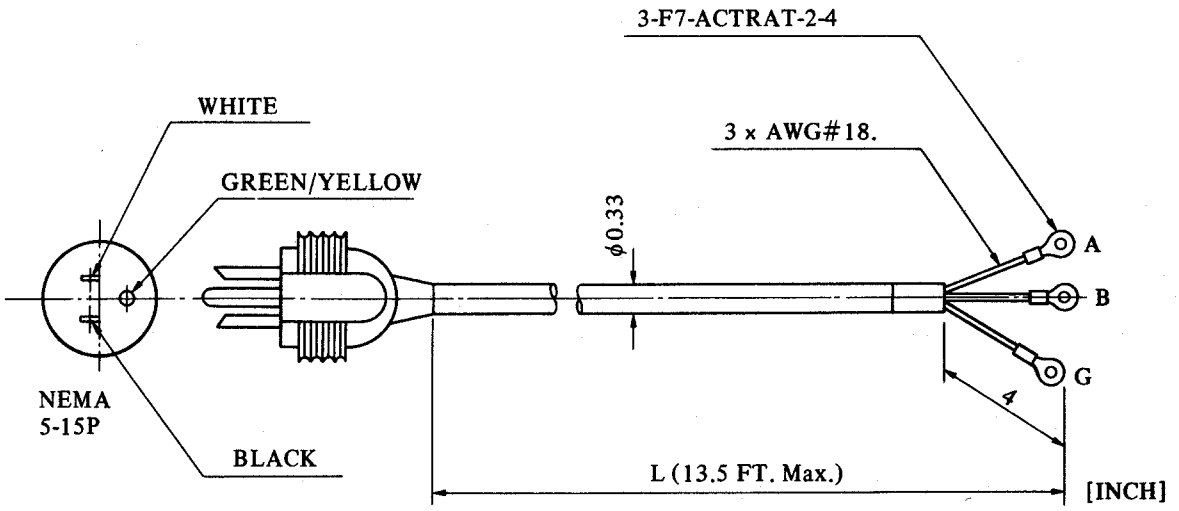


Figure 1.3.6 Power cable C ∿ E

CHAPTER 2 INSTALLATION

2.1 General Description

This section describes storage, unpacking, installation, and cabling of the M2361A when shipped separately, and shipping precautions when the unit is delivered as a system.

2.2 Storage

When the drive is stored for a prolonged period, avoid locations where the environment is extreme. Stored units should be properly packed and can be stored stacked vertically, two high. When the temperature difference between storage (or shipping) and the unpacking environment exceeds 20°C (36°F), the unit should be allowed to remain in packaged form for more than 3 hours to avoid condensation when unpacking.

2.3 Unpacking

The M2361A is shipped in a carton surrounded by shock absorber as shown in Figure 2.3.1. Note: the shipping carton is intended to be reuseable.

(1) Store and open the carton on a flat surface, ensure that the top of the box, indicated by "This Side Up" signs, is oriented correctly.

Note: Don't store in the upside-down position.

(2) Take out the upper pad.

(3) Lift the M2361A out of the box by means of the nylon bands.

Note: Move the disk drive slowly and carefully to prevent unnecessary shock.
Don't grasp the front panel or cover of the unit to lift.

(4) Store packing material for possible future use.

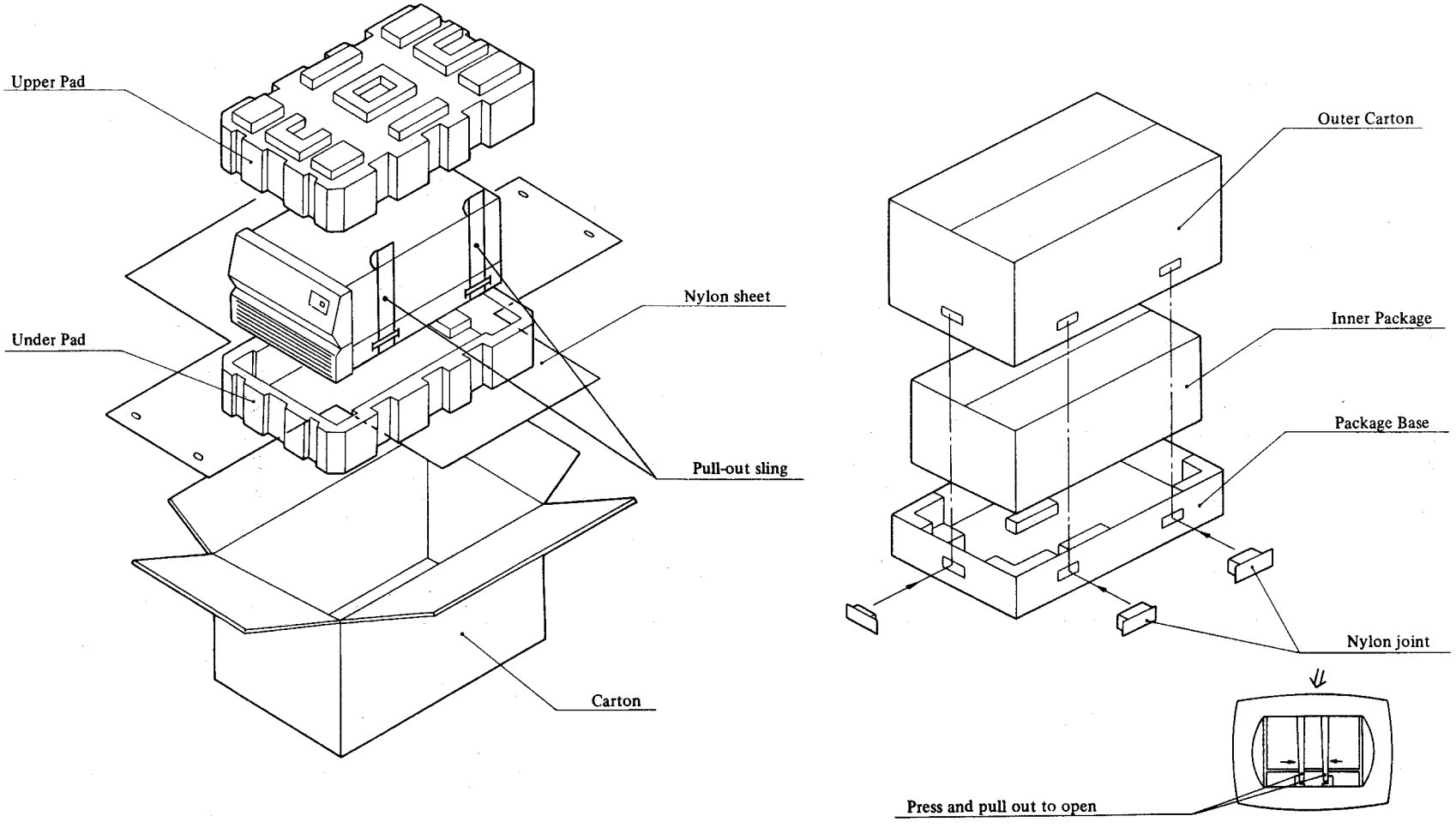


Figure 2.3.1 Exterior view and construction of carton

2.4 Visual Inspection

After unpacking, check the following.

(1) There should be no scratches, dents, nor other damage that mars appearance and integrity.

(2) All parts should be firmly fixed, there should be no loose screw, etc.

(3) The attachments and options should be as ordered.

2.5 Installation

This unit can be slide-mounted in a standard 19-inch rack or built into a system cabinet.

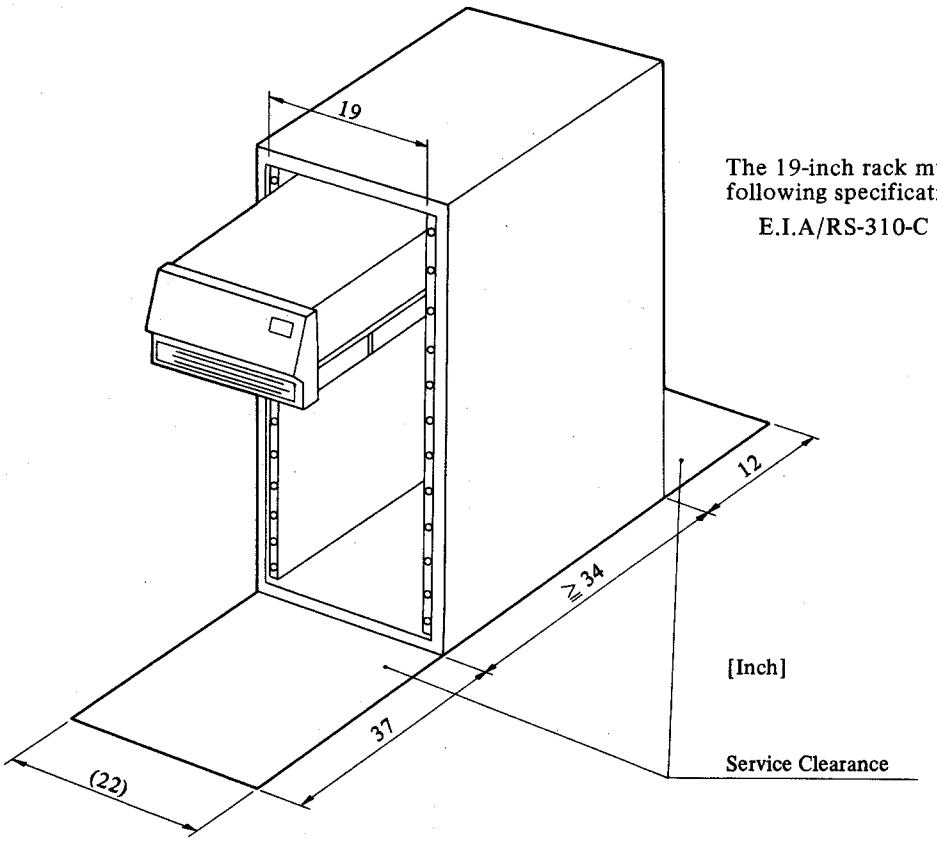


Figure 2.5.1 Installation in the 19-inch rack

2.5.1 Slide-mounting instructions

Installation procedures are illustrated in Figure 2.5.2.

(1) Extend the slide guide and release from the slide rail.

(2) Install the slide guide in the 19-inch rack or cabinet.

(3) With both the slide guides installed and extended, lift the drive with slide rails already attached onto the extended guides. Be sure the rails are correctly seated and latched in the guides.

Note: The drive weighs approximately 143 lbs (65 kg), and requires at least two people to install.

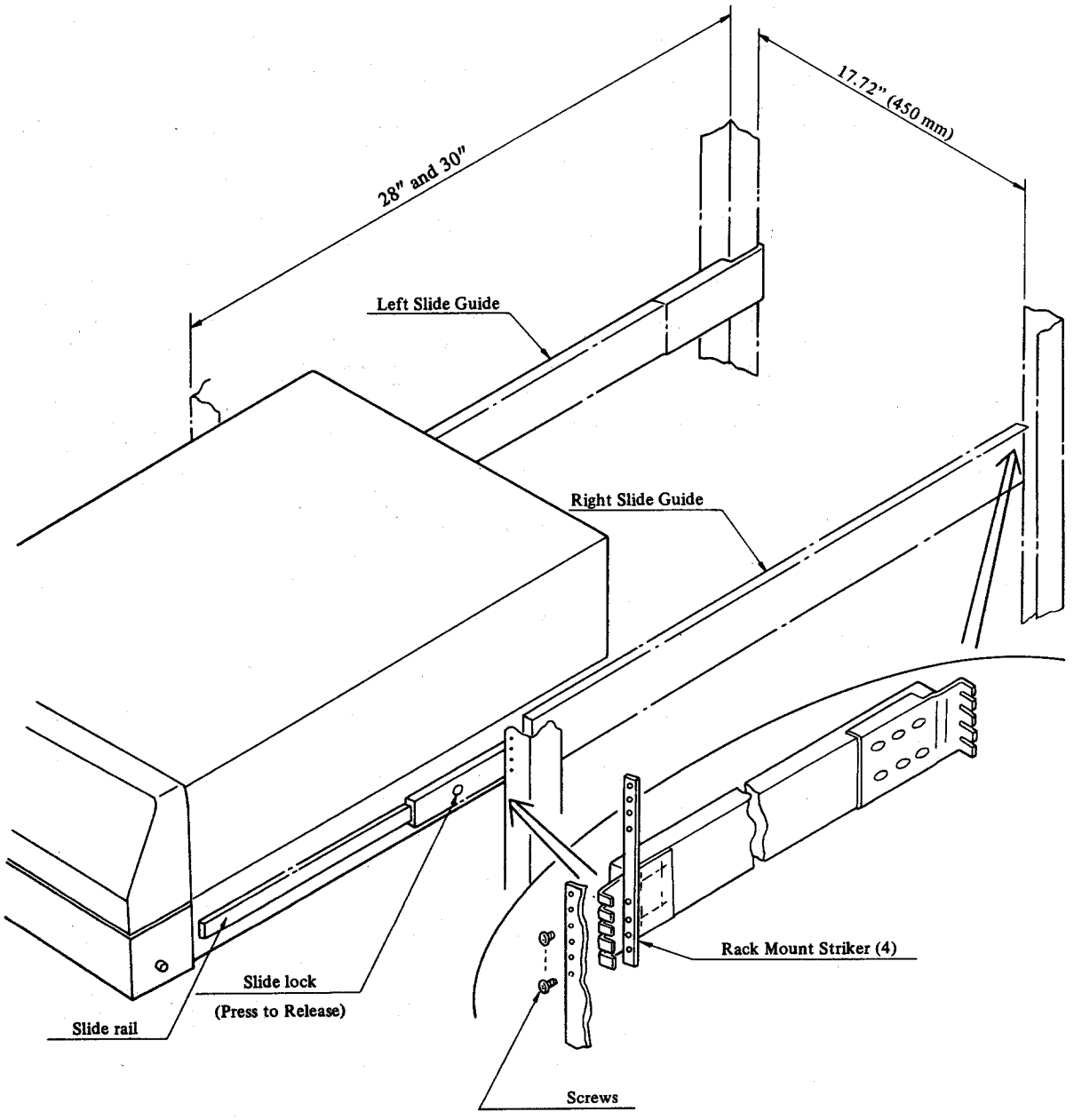


Figure 2.5.2 Rack mount installation

2.5.2 Cooling

(1) Cooling system of drive unit

The drive has been designed so that it is able to work at the environmental temperature 104°F (40°C) without any additional cooling fan.

The drive is cooled by a centralized cooling system a line blower. The air is sucked in through the air vents on the front cover, passes through the air filter and the line blower, and is blown uniformly over the entire DE, card cage, power amplifier, and interface PCBs.

The air which passes through the card cage cools the DC power supply and the air which passes over the DE cools interface PCBs, and is discharged.

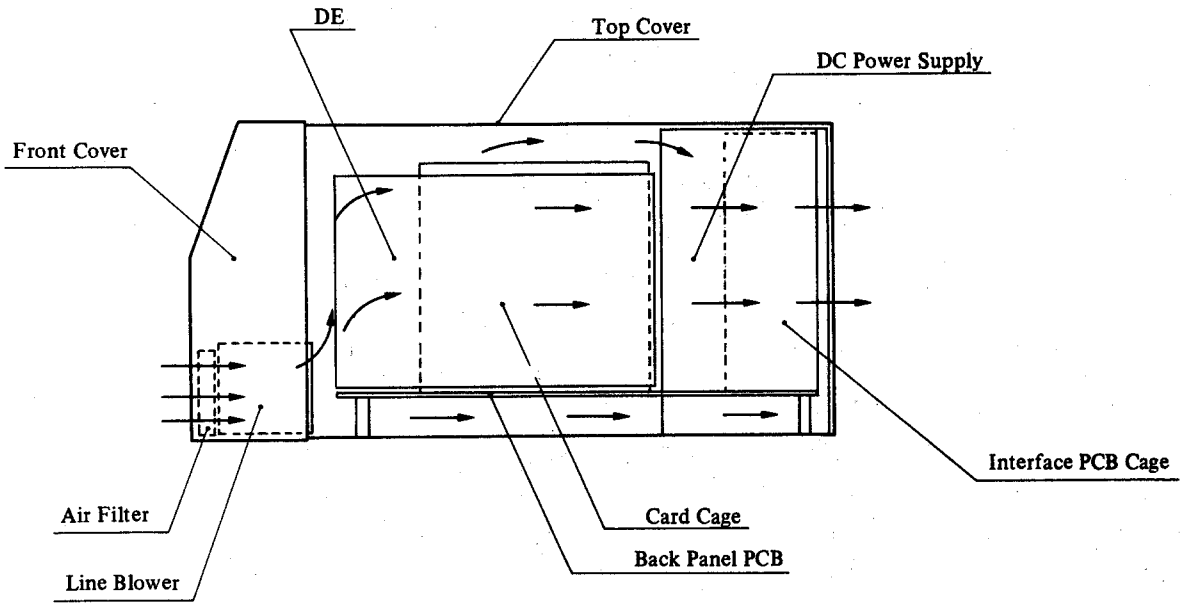


Figure 2.5.3 Cooling system

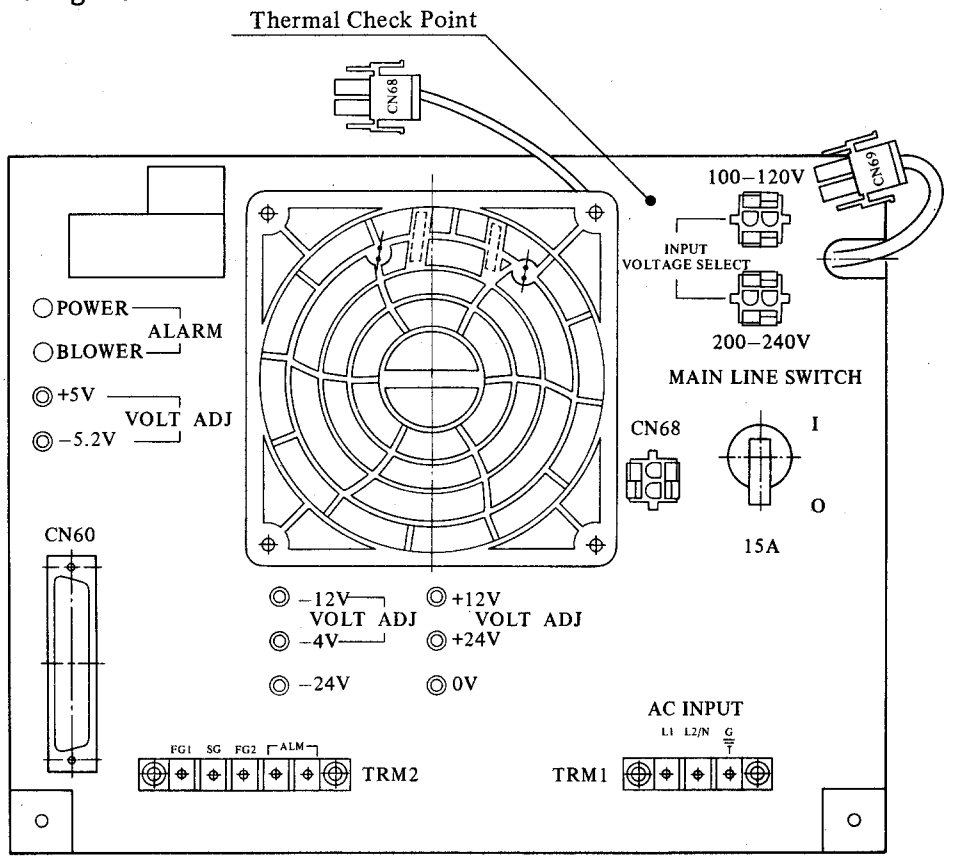
(2) Thermal check point

The air flow will be less than the naked drive if it is installed in the rack. The cooling condition can be confirmed by taking the surface temperature of the DC Power supply.

Table 2.5.1 Thermal Condition

Maximum surface Temperature (Tc)	Condition
55°C	At random seeking. Even on max. environmental temperature (40°C)

If the temperature is not kept under this condition, the drive cannot work and will be damaged.



(Rear View of the DC Power Supply)

Figure 2.5.4 Thermal check point

(3) Additional cooling fan

If the temperature at the thermal check point cannot be kept under the specified condition when the drive is installed in a rack, the additional fan must be mounted in the back of the rack.

Check the air flow of the whole cooling system of the rack by measuring the temperature of the thermal check point.

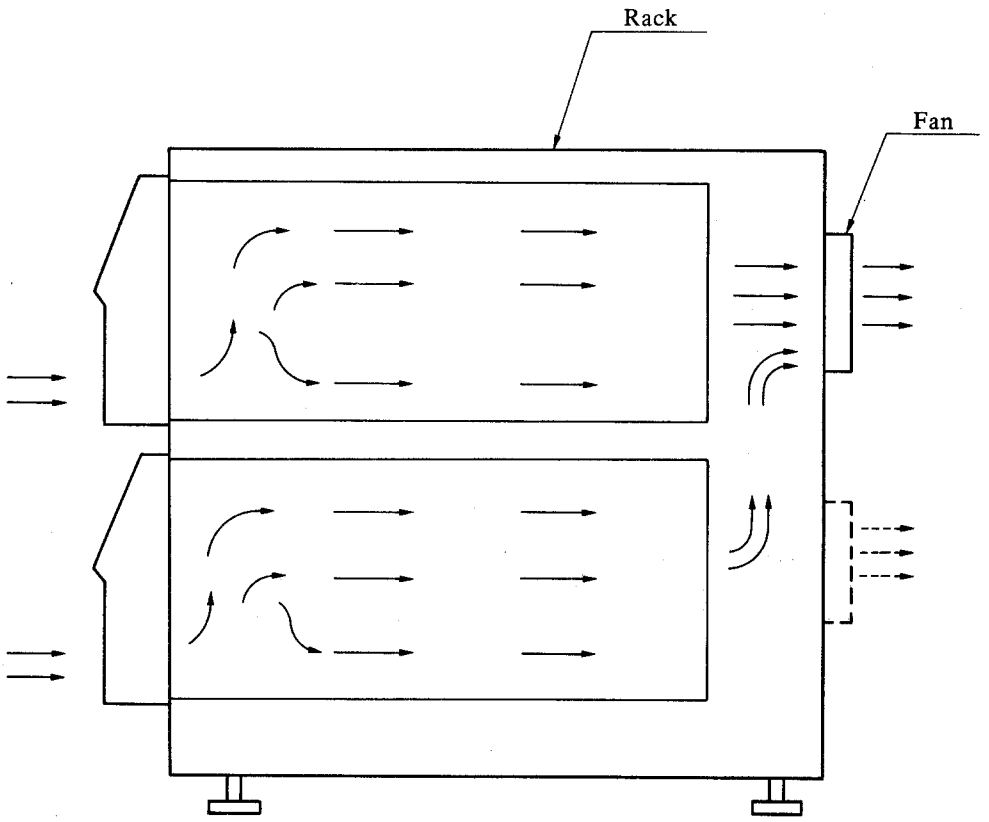


Figure 2.5.5 Example of additional cooling fan

2.6 Mounting of Options

2.6.1 Dual channel option mounting

1 Remove the 2 screws "A" holding the interface PCB fixture. (See Figure 2.6.1)

2 Insert the dual channel option (Dual port Interface PCB) into the right side connector in the interface card cage.

3 Mount the interface PCB fixture by using the 2 screws "A".

4 Connect the interface cables. (Refer to Section 2.7.3)

5 If necessary, mount the line terminator. (Refer to Section 2.6.4)

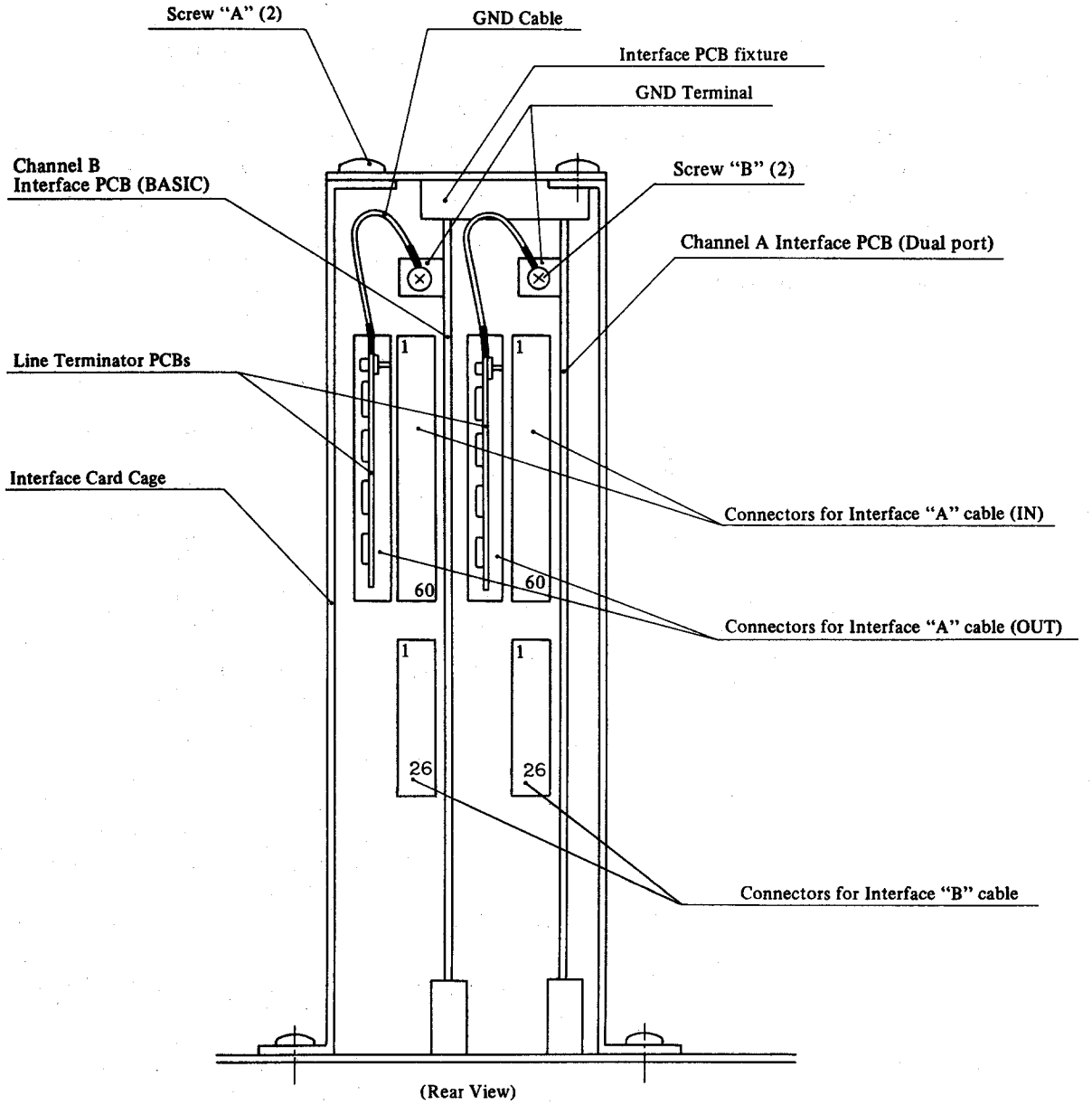


Figure 2.6.1 Mounting the dual channel option

2.6.2 Slide guide mounting

The slide guide assembly consists of a pair of right and left slide guides. Mount the slide guide assembly on the 19-inch rack as follows.

(1) Loosen the 2 nuts holding the bracket in the back, so that it moves back and forth. (See Figure 2.6.2)
The slide guide assembly can be mounted in the 19-inch rack with a depth of mounting pitch 28 inches and 30 inches.

(2) Install right and left slide guides in the 19-inch rack. Tighten the bracket mounting nuts after adjusting bracket location to fit it to the depth of the mounting pitch.

(3) If necessary release the slide rail from the slide guide by pressing the slide lock.

(4) Attach the right and left slide rails to the drive unit using the 4 screws "A".

(5) Lift the drive unit and insert its slide rails into the guide rails mounted in the 19-inch rack. Be sure the rails are correctly seated and latched in the guides.

Note: The drive weighs approximately 143 lbs (65 kg), and requires at least two people to install.

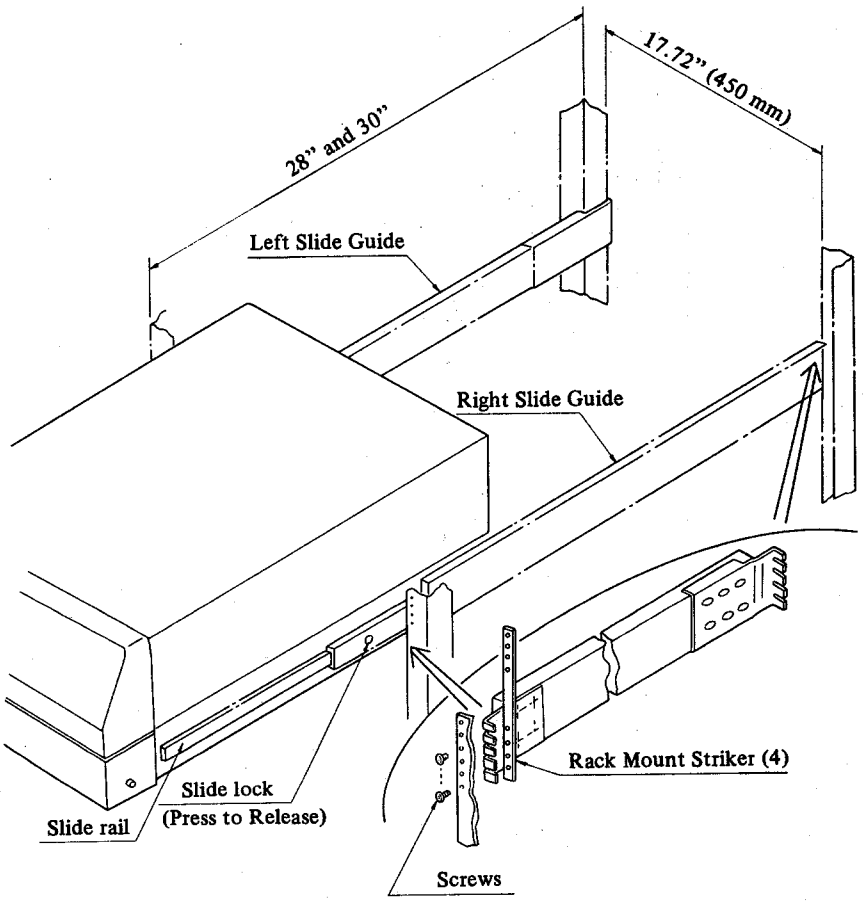


Figure 2.6.2 Rack mount installation

2.6.3 Hour meter mounting

Install the hour meter in the connector (TM1) on the back panel.
(See Figure 2.6.3)

Note: 1. The arrow of the hour meter must be the same direction as that on the connector (TM1).

2. If the indicator is fully changed to red, pull out the hour meter and change the direction.

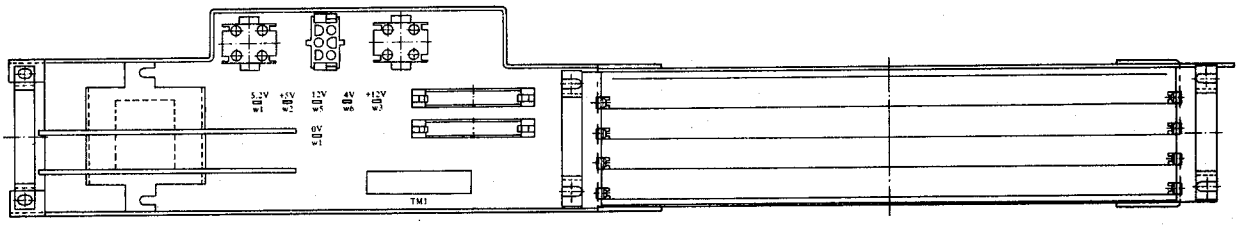


Figure 2.6.3 Back panel PCB

2.6.4 Line terminator mounting

① Install the line terminator PCB in the "out" connector for A-cable of the interface PCB. (See Figure 2.6.1)

② Connect the GND cable of the line terminator PCB to the GND terminal on the interface PCB using the screw "B".

2.7 Cabling

2.7.1 Cables

All cables are connected in the rear of the drive unit.

(1) Cable list

Cables consist of;

a. Interface cables — A-cable — for Data Transfer
B-cable —

b. AC Power cable — Power Cable B for 200-240V

or Power Cable C
or Power Cable D } for 100-120V
or Power Cable E

Table 2.7.1 Cable List

No.	Name	Specification	Remark	
1	A-Cable	B660-1954-T904A	* Max. 30 m	Cable length can be specified in 0.5 m increments.
2	B-Cable	B660-1954-T903A	* Max. 15 m	
3	Power Cable B	B660-0620-T387A #3.0 m	* L = 3 m	UL/CSA Recognized 200-240V
4	Power Cable B	B660-0620-T387A #5.0 m	* L = 5 m	
5	Power Cable C	B660-1055-T033A	* L = 2.5 m	UL/CSA Recognized 100-120V
6	Power Cable D	B660-1055-T034A	* L = 3.5 m	
7	Power Cable E	B660-1055-T035A	* L = 4.5 m	

* Check with your local sales office for lengths available

(2) Specifications of Cables and Connectors

Table 2.7.2 Cables and connectors

	Cable		Connector (Supplier)	
	Specification	Supplier	Drive Side	Cable Side
A-Cable (60-Pin)	Zo = 100 ± 10Ω 28 AWG 7 Strands 100 FT. Max.	FUJITSU	FUJITSU FCN-704P060-AU/M	FUJITSU FCN-707J060-AU/B
			3M 3372-1003LCSB	3M 3334-6500 and 3448-3060
B-Cable (26-Pin)	Zo = 100 ± 10Ω 28 AWG 7 Strands 50 FT. Max.	FUJITSU	FUJITSU FCN-705P026-AU/M	FUJITSU FCN-707J026-AU/B
			3M 3429-1003LCSB	3M 3399-6500 and 3448-3026
Power Cable B	See Figure 2.7.1			
Power Cable C&D	See Figure 2.7.2			

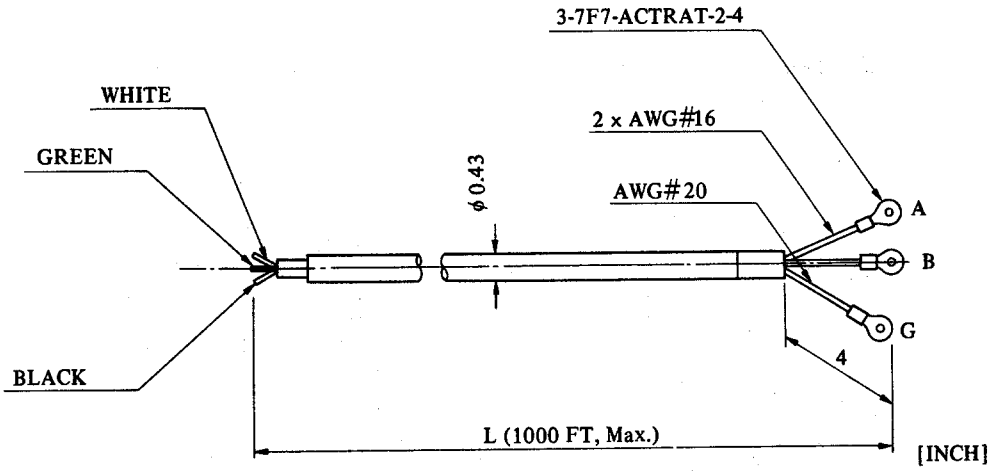


Figure 2.7.1 Power cable B

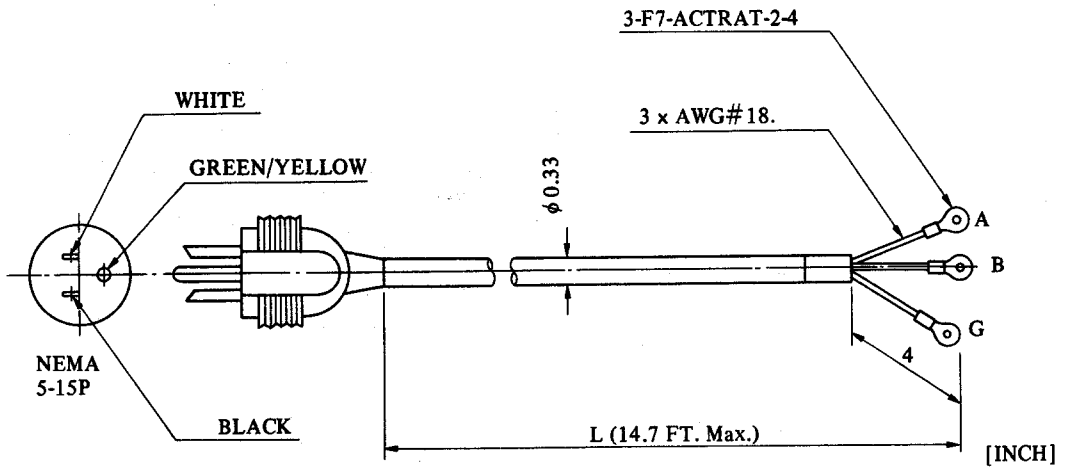


Figure 2.7.2 Power Cable C ∿ E

2.7.2 Power cable connection

(1) Loosen the 2 screws "A" holding the cable clamp. (See Figure 2.7.3)

(2) Insert the power cable into the cable clamp.

(3) Connect the 2 power lines to the AC input terminal L1 and L2 using the 2 screws "C".

(4) Connect the GND line to the drive unit FG using the screw "B".

(5) If the AC input voltage is changed, set the connector CN69 on power supply to the proper input voltage. (See Figure 2.7.3)

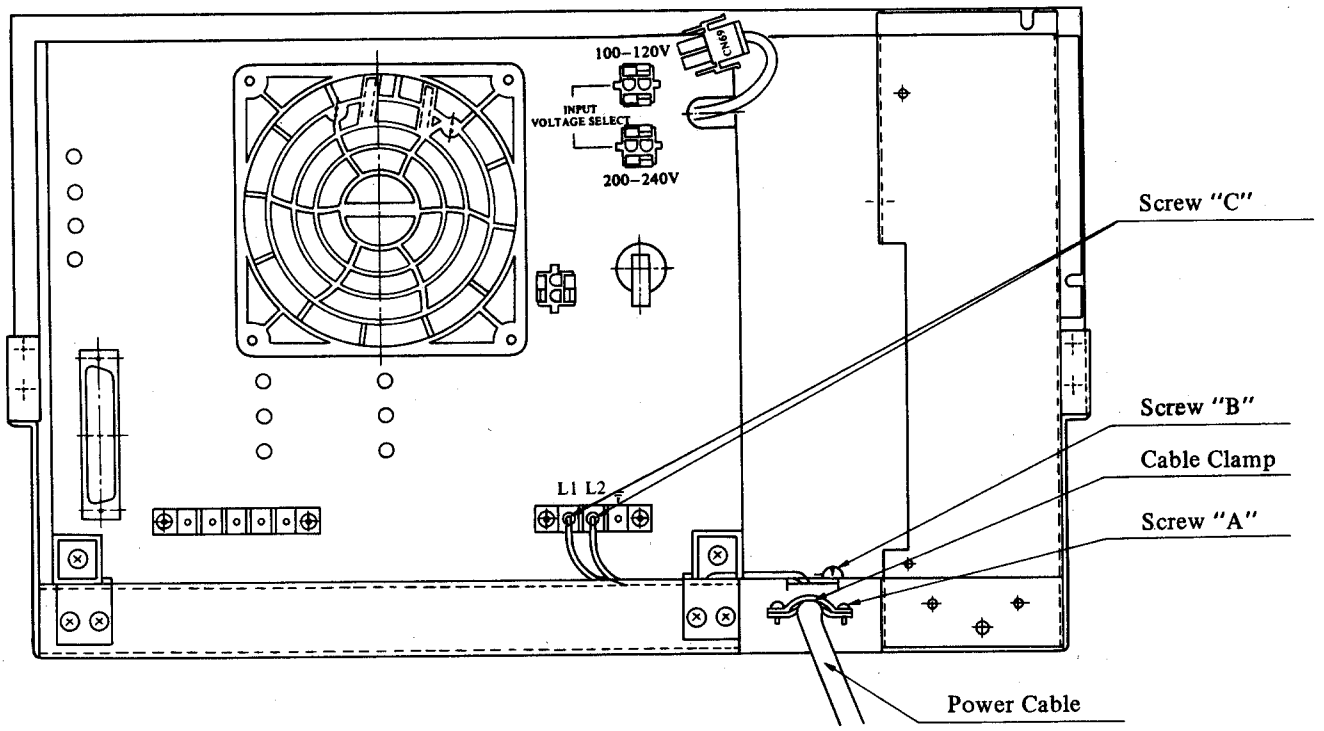


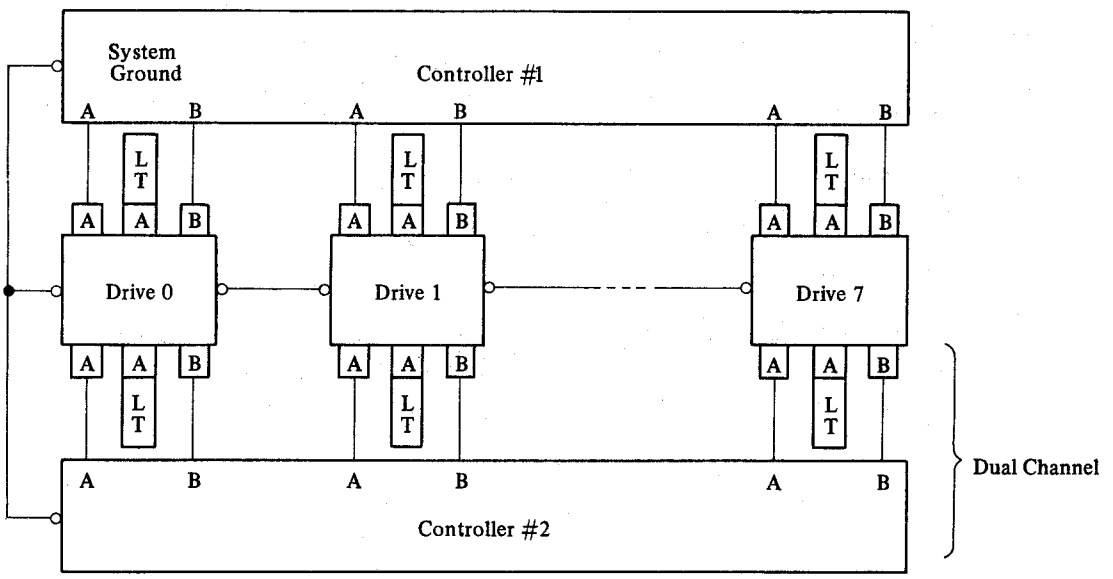
Figure 2.7.3 Power cable connector

2.7.3 Interface cabling

(1) A and B cables (Data transfer interface cables)

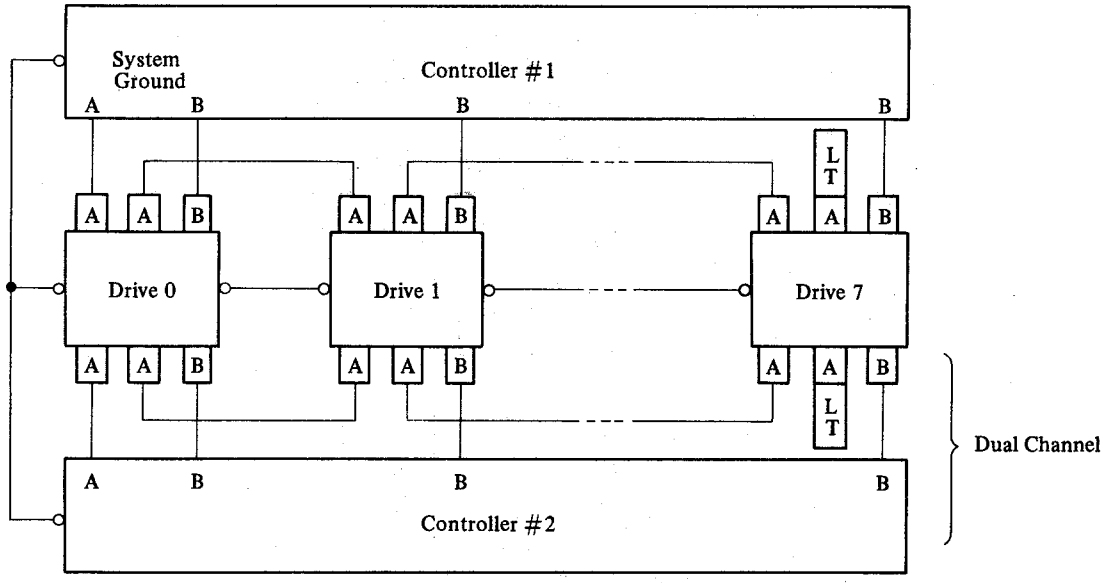
a. Connection

One of the following interface cable configurations must be chosen depending on the feature of the controller.
(Note; Dual Channel Feature is optional.)



Note that Line Terminators (LT) are required in each drive in a radial cable configuration.

Figure 2.7.4 Radial cable configuration



Note that a Line Terminator (LT) is required in the last drive in a daisy-chain cable configuration.

Figure 2.7.5 Daisy-chain cable configuration

b. Cable Mounting (See Figure 2.7.6)

① Remove the 2 screws (A) holding the cable clamp (1).

② Remove the 2 screws (B) holding the cable clamp (2).

③ Connect A-cables to the upper connectors on the interface PCB. The IN A-cable must be connected to the right connector and the OUT A-cable must be connected to the left connector on each interface PCB.

④ Connect B-cable to the lower connector on the interface PCB.

⑤ Clamp A-cable using the clamp (2) for A-cable and the 2 screws (B).

⑥ Clamp B-cable using the clamp (1) for B-cable and the 2 screws (A).

⑦ Connect the GND lines of the interface cables to FG using the screws (C).

⑧ If necessary, install the line terminator PCB in the "out" connector for A-cable of the interface PCB. Connect the GND cable of the line terminator PCB to the GND terminal on the interface PCB using the screw (D).

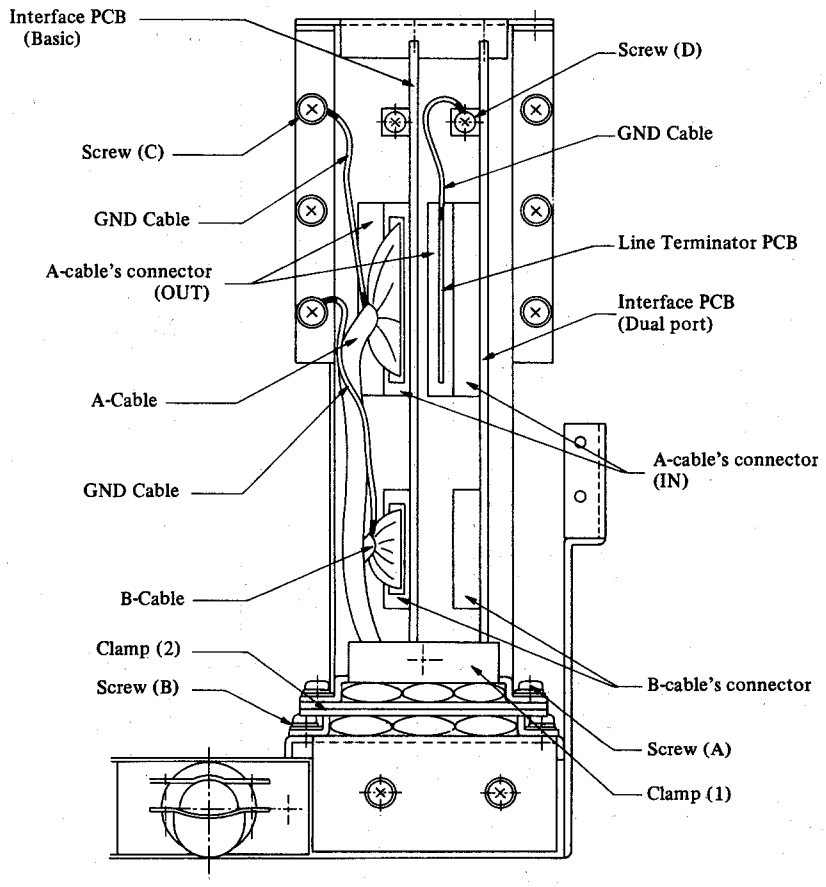


Figure 2.7.6 Cable mounting (Rear view)

2.7.4 System grounding

(1) Definitions of SG, FG1 and FG2.

SG is Signal ground or DC ground and is isolated from AC ground within the drive.
FG1 is Frame ground or AC ground and is a direct short to chassis.
FG2 is a high impedance AC ground, connected to FG1 through a 510 Kohm resistor.
For shipment, SG is connected to FG2 with the shorting plate, as shown in Figure 2.7.7.

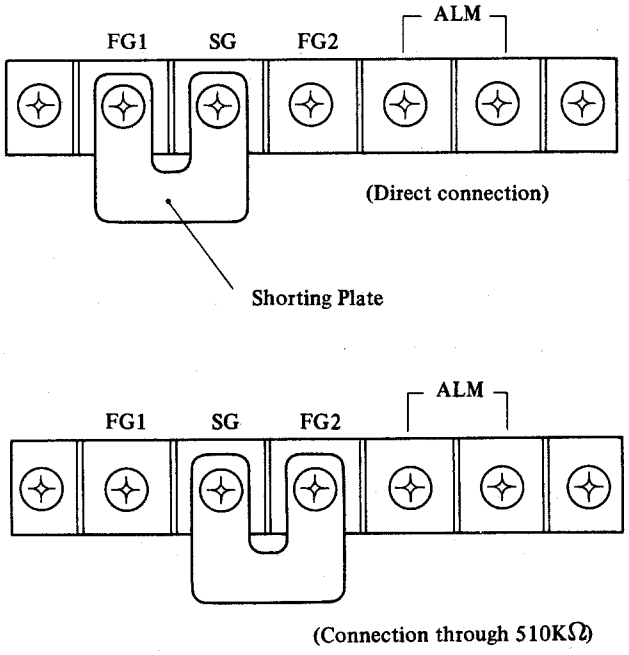


Figure 2.7.7 Connection of FG and SG

(2) Grounding methods

It is always recommended that drives be grounded, and it is required if cable lengths longer than 10 ft. are used or if the drives are connected in the daisy-chain configuration. All grounding should be done with flat braided wire, preferably covered with a jacket or tubing.

Grounding methods very with site and system integration design, and are commonly derived in a trial-and-error fashion. However, three approaches are offered in order of preference:

a. Connect SG to FG1 with the shorting plate. Connect a flat braid wire from SG to controller ground. If daisy-chained, daisy-chain the braid from SG to SG as shown in Figure 2.7.8.

b. Leave SG connected to FG2 (shipping configuration) and connect a flat braid wire to controller ground. If daisy-chained, daisy-chain the braid from SG to SG as shown in Figure 2.7.9.

c. Remove the shorting plate, isolating SG and FG grounds. Connect a flat braid wire from SG to controller ground (preferably DC ground). In this case, the braided wire must be covered to prevent accidental shorting to chassis (AC ground).

(3) AC considerations

a. The controller should always be solidly connected to earth ground. The drives and the system are then grounded through the controller. (The previous three approaches described in (2) above assume the controller is the focal point for commonizing AC and DC ground.)

b. It is always recommended that the drive, controller and CPU share a common AC branch circuit.

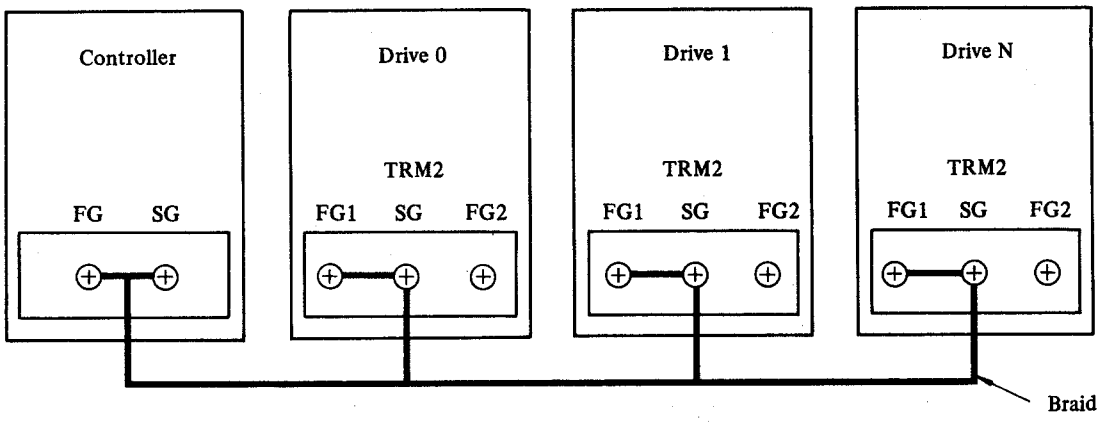


Figure 2.7.8 SG/FG1 common

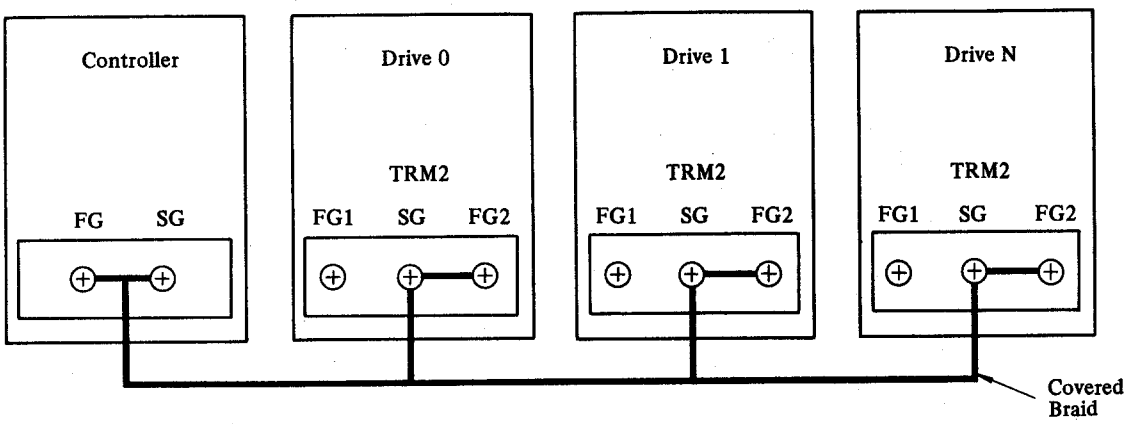


Figure 2.7.9 SG/Hi Z FG2 common

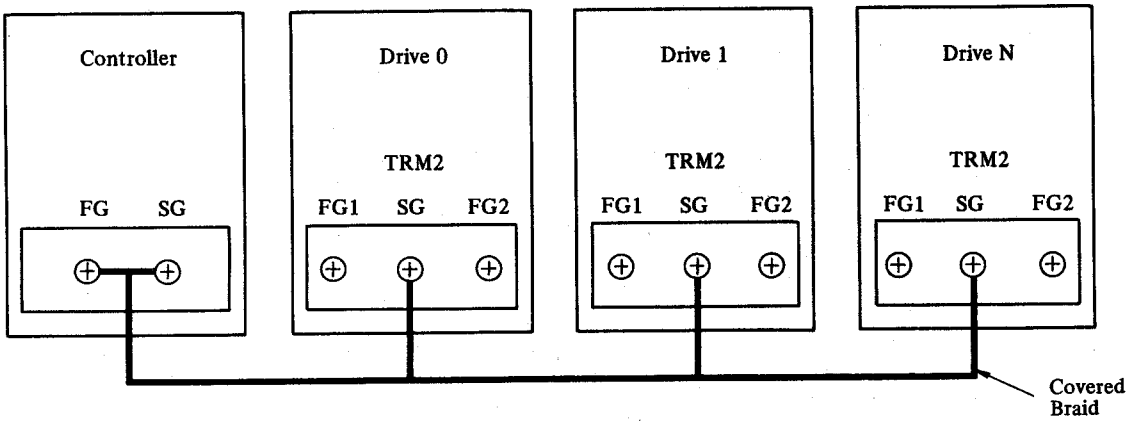


Figure 2.7.10 SG/FG isolated

CHAPTER 3 OPERATION AND CHECKOUT

3.1 General Description

This chapter describes the operation of switches and indicators on the operator panel, the DC power supply unit, display panel and logic PCB as well as cabling information and installation procedures. These switches and indicators are needed not only to operate the drive in a system, but also to display the information necessary for trouble-shooting in the event of drive failure.

3.2 DC Power Supply Unit

3.2.1 Introduction

The DC power supply unit has a fan for cooling. It is also cooled by the airflow from the line blower which cools the entire drive. When the main line switch is turned on, DC power is supplied to this line blower. The main line switch is automatically turned off when it detects an over-current in the AC input.

The power supply can be set for different input voltages by changing the connection on the control panel of the unit. (Refer to Figure 3.2.1.)

3.2.2 Control panel

The control panel of the DC power supply is shown in Figure 3.2.1.

(1) MAIN LINE SWITCH (Non-Fuse Breaker)

Supplies AC power to the unit. If an over current flows in the AC input, it goes off.

(2) POWER ALARM (LED)

If one of following failures occurs, this LED lights.

- Over current or over voltage in the DC output
- Fan alarm
- Over temperature of the DC power supply unit

(3) BLOWER ALARM (LED)

Indicates a failure of the line-blower.

(4) INPUT VOLTAGE SELECT (Connector)

This connector must be connected to the correct position in accordance with the voltage at the AC input.

When the M2361A is shipped, this connector is set to the 100–120 V position. If used at a voltage 200–240, CN69 must be moved to the 200–240 V connection.

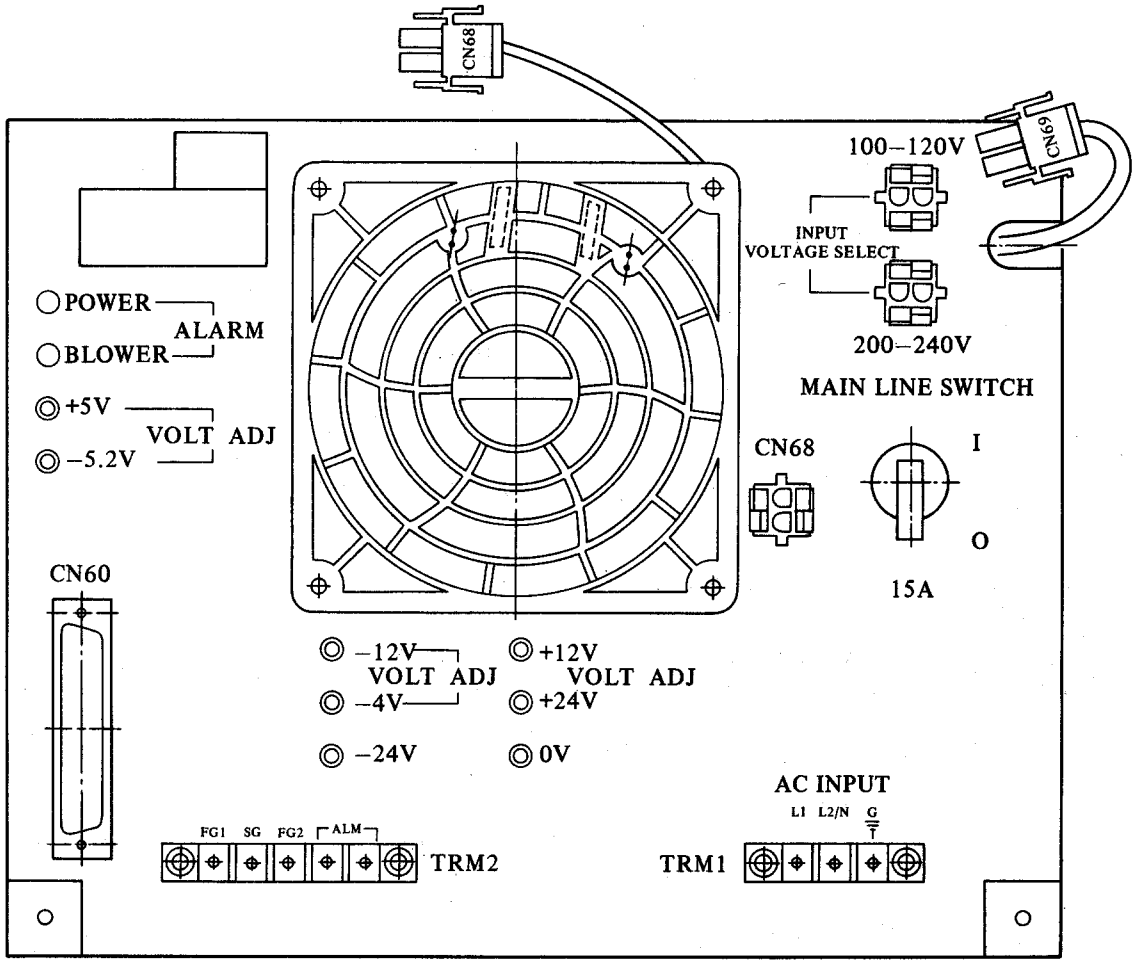


Figure 3.2.1 Control panel of DC power supply unit

(5) TRM 2 (Terminal)

FG1 ..... Frame Ground
SG ..... Signal Ground
FG2 ..... Frame Ground isolated by a 510 KΩ resistor
ALM ..... Alarm output

The Frame Ground and the Signal Ground are completely isolated in the drive. They are connected together only on this terminal with a shorting strap at the time of shipment. It can be removed, depending on system power distribution or system grounding requirements.

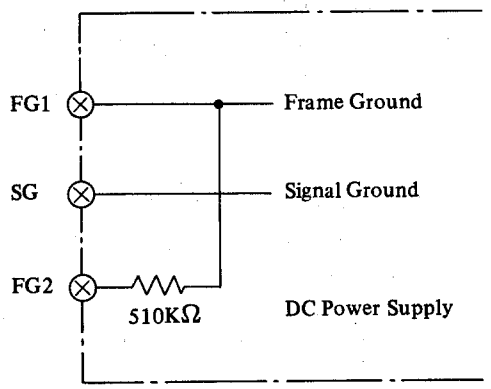


Figure 3.2.2 FG1, FG2 and SG

(6) Volt Adj (Variable Resistors)

Variable resistors are provided to adjust the -5.2, -4, ±12 and +5 Volt DC output within the tolerance specified.

3.2.3 Input conditions

Input conditions of the DC power supply unit are equal to the input conditions of the drive itself, and are listed in table 1.2.3.

The power input cable passes through the cable clamp below the DC power supply unit and is fixed on the terminal (TRM1).

3.2.4 Output conditions

Table 3.2.1 Output conditions

Voltage		Protection		Current	Variable Range (%)	Usage
Vdc	Tolerance (%)	Over-Voltage	Over-Current	Adc		
+5	±5	With	With	5 ∿ 10	±5	PCBs
+12	±5	Without	With	0.3 ∿ 1	±5	
-12	±5	Without	With	0.3 ∿ 1	±5	
-4	±5	Without	With	0.2 ∿ 0.5	±5	
-5.2	±5	With	With	3 ∿ 10	±5	
+24	±10	Without	With	4.3 ∿ 7.2		Line Blower, FAN, Rotary Actuator, Spindle Motor
-24	±10	Without	With	3.3 ∿ 6.2		

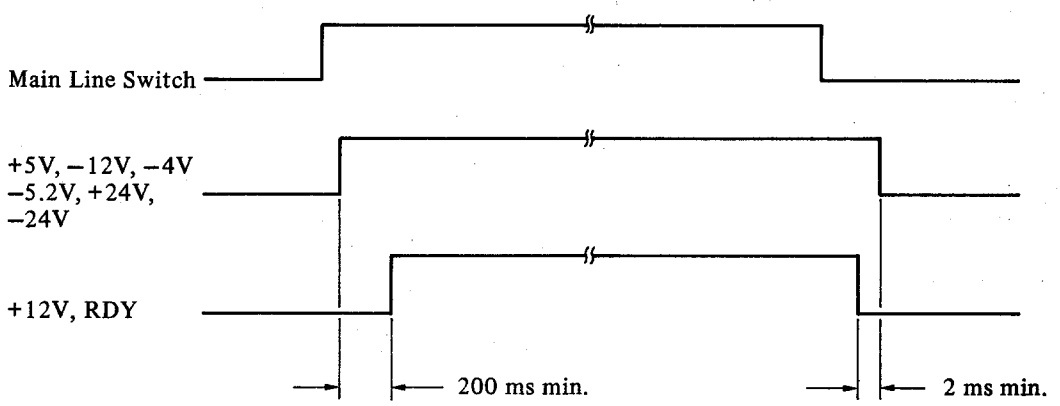


Figure 3.2.3 Output sequence

3.2.5 Alarm detections

The causes of various alarms and what they indicate when they occur are listed in Table 3.2.2.

Table 3.2.2 Indications of alarms

Alarm	Cause	Indication		
		Main Line Sw.	Power Alm LED	Blower Alm LED
Power Alarm	Over current of AC input	Break	-	-
	Over current/voltage of DC output	-	Light	-
	Over temperature of the DC power supply unit	-	Light	-
	Stopping of fan on the DC power supply unit	-	Light	-
Blower Alarm	Stopping of line blower	-	-	Light

3.3 Operator Panel

Switches and indicators on the operator panel are shown in Figure 3.3.1.

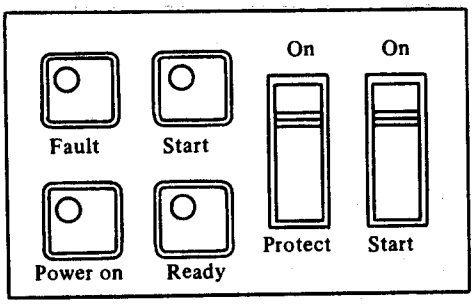


Figure 3.3.1 Operator panel

(1) Start (Switch)

If the Spindle Remote/Local switch on the CE panel behind the front panel is set to Local, it enables rotation of the spindle motor. When the DC motor comes up-to-speed, the heads start Initial Seek operation and stop on cylinder zero. Approximately 40 seconds later the Ready LED lights. The spindle motor stops rotating approximately 15 seconds after the switch is set to the Off position.

When the Remote/Local switch is set to Remote, the spindle motor starts and stops rotating in accordance with the Spindle Sequence Pick/Hold commands issued from the controller if the Start switch is On.

(2) Protect (Switch)

Inhibits Write operation. The write-protect function is enabled by the File Protect Switch on the operator panel, and becomes active while the drive is not selected. If the drive is selected and the write-protect-function is desired, the drive must be momentarily deselected.

(3) Start (LED)

Indicates that the start switch is on. The spindle should begin rotating.

(4) Ready (LED)

Indicates that the spindle has reached the rated speed and no fault condition exists in the drive. It goes off when the heads are seeking to the desired cylinder.

(5) Fault (LED and Switch)

Indicates a Fault condition (i.e., R/W check status). Depressing the indicator switch clears this condition.

(6) Power On (LED)

Indicates that the DC power supply circuit breaker is ON.

3.4 Display Panel

Switches and indicators are provided for aiding maintenance, and are shown in Figure 3.4.1.

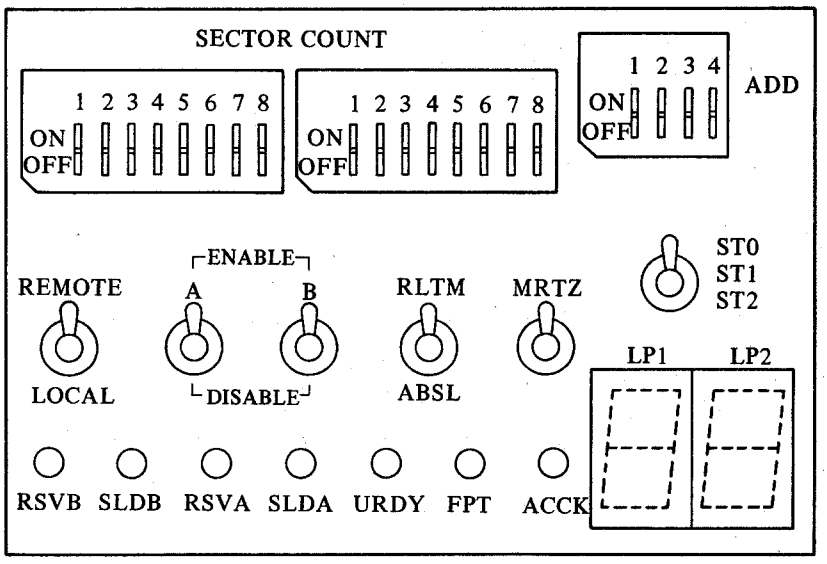


Figure 3.4.1 Display panel

3.4.1 REMOTE/LOCAL switch

When this is set to Remote, the spindle motor starts/stops rotating in accordance with the commands (Spindle Sequence Pick/Hold) issued from the controller. Refer to Figure 3.4.2. When set to Local, rotation is under the control of the Start switch on the operator panel.

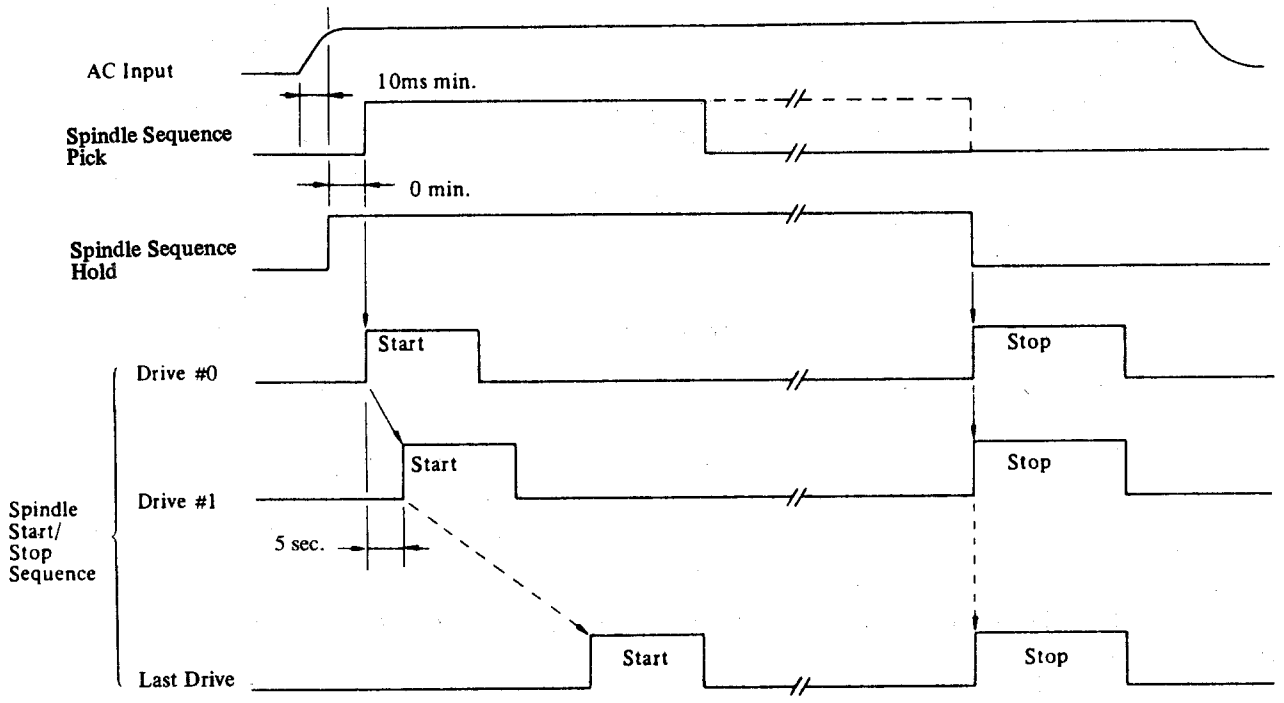


Figure 3.4.2 Spindle sequence pick/hold timing

3.4.2 ENABLE/DISABLE A, B switch

The A-channel, or if the dual port option is used, the B-channel, interface signals can be enabled/disabled.

3.4.3 RLTM/ABSL (Release Timer/Absolute) switch

This switch is functional if the dual port option is provided.

When the switch is in RLTM, reserved status will be released 500 ms after Unit Select Command if the Release Command has not already been isued. When the switch is in ABSL, reserved status can be released only by the Release Command.

3.4.4 MRTZ (Manual RTZ) switch

The head performs RTZ operation when this maintenance-aid switch is pressed.

3.4.5 State switch and state indicators (Toggle switch and 7-segment LEDs)

Two 7-segment LEDs indicate detailed drive states as shown in Table 3.4.1 in accordance with the position of the State Switch.

Table 3.4.1 Status and state

State Switch Position		Upper (ST 0)	Center (ST 1)	Lower (ST 2)
LED \ State / Bit		Write/Read Check State	Access State	DE Sequence State
LP1	1	Index Check	DE Sequence Check	DE Sequence Latch 1
	2	Control Check	Access Timeout Check	DE Sequence Latch 2
	4	Multi Head Check	Over Shoot Check	DE Sequence Latch 4
	8	Head Short Check	Rezero Mode Latch	Hall Alarm
LP2	1	Write Current on Read Check	Servo Latch	Motor At Speed
	2	Write Transition Check	Linear Mode Latch	Inhibit DE Seq. Recycle
	4	Delta I Write Check	Control Latch	Unit Ready
	8	Servo Off-Track	Wait Latch	Access Busy

(1) Write/Read check state (ST 0)

Refer to item (4) of subsection 4.5.4 for detailed description.

(2) Access state (ST 1)

Refer to item (5) of subsection 4.5.4 for detailed description.

(3) DE sequence state (ST 2)

a. DE Sequence Latch 1, 2 and 4

Indicates start/stop status of the DE. Details are described in subsection 4.5.4, Table 4.5.4.

b. Hall Alarm

Indicates that all output signals from the hall-elements used to detect the pole position of the rotor in the spindle motor are high or low level simultaneously.

c. Motor At Speed

Indicates that the spindle motor is rotating at 3,600 RPM ±2%.

d. Inhibit DE Sequence Recycle

Indicates that Run State Good goes false while the DE Sequence Latch is in State 7. Stop sequence of the DE may be inhibited hereafter. Switching off the drive power or pushing the Start switch to Off position clears this state.

e. Unit Ready

Indicates that the drive has reached the rated rotational speed and heads are positioned on track.

f. Access Busy

Indicates that the heads are in motion, i.e., heads are performing Seek, RTZ or Offset operation.

3.4.6 Unit status indicators (LEDs)

Indicate Unit Status as shown in Table 3.4.2. These statuses are also issued to the controller as States 0 to 4 when both Tag 4 and 5 false if this feature is utilized.

Refer to item (2) of subsection 4.5.4 for detailed descriptions of each state.

Table 3.4.2 Unit status indicators

Name of LED	Color of LED	Contents
URDY	Green	Unit Ready
ACCK	Red	Seek Error (Access Check)
FPT	Yellow	Write Protected (File Protect)

3.4.7 Dual port status indicators (LEDs)

Displays channels A and B interface status available if the dual port option is provided, as shown in Table 3.4.3.

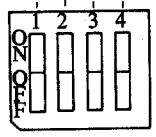
Table 3.4.3 Dual port status

LED name	Signal name	Contents
RSVA	Channel A Reserved	Indicates that the drive is reserved by A-channel.
SLDA	Channel A Selected	Indicates that the drive is selected by A-channel.
RSVB	Channel B Reserved	Indicates that the drive is reserved by B-channel.
SLDB	Channel B Selected	Indicates that the drive is selected by B-channel.

3.4.8 Drive address switch (DIP switches)

Drive logical address 0-7 can be set with these switches in binary code as shown in Figure 3.4.3.

Drive Address	Switch Position			
	1	2	3	4
0	Not Used	OFF	OFF	OFF
1		OFF	OFF	ON
2		OFF	ON	OFF
3		OFF	ON	ON
4		ON	OFF	OFF
5		ON	OFF	ON
6		ON	ON	OFF
7		ON	ON	ON



Switch

Figure 3.4.3 Drive address switch

3.4.9 Sector count switch (DIP switches)

The number of bytes per sector in Fixed Sector Format is determined by the switches according to the following figure and example.

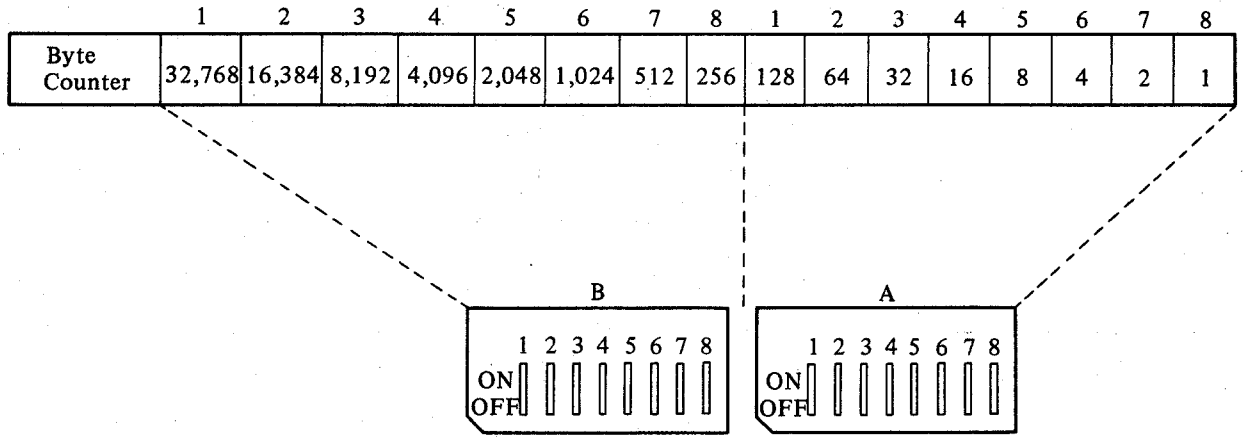


Figure 3.4.4 Sector count switches

Example; 9 Sectors/Track

$$\text{Bytes/Sector} = \frac{\text{Bytes/Track}}{\text{Sectors/Track}} = \frac{40,960}{9} = 4,551.11$$

If the above calculation results in a remainder, round it up to the next integer, i.e., Bytes/Sector = 4,552

Set this figure minus one with jumper plugs to allow the Byte Counter to start counting from zero.

$$4,552-1 = 4,551 = \underbrace{4,096 + 256}_{B} + \underbrace{128 + 64 + 4 + 2 + 1}_{A}$$

Therefore, set 4 and 8 of the B-dip switch and 1, 2, 6, 7 and 8 of the A-dip switch on, and all the rest of the switches off.

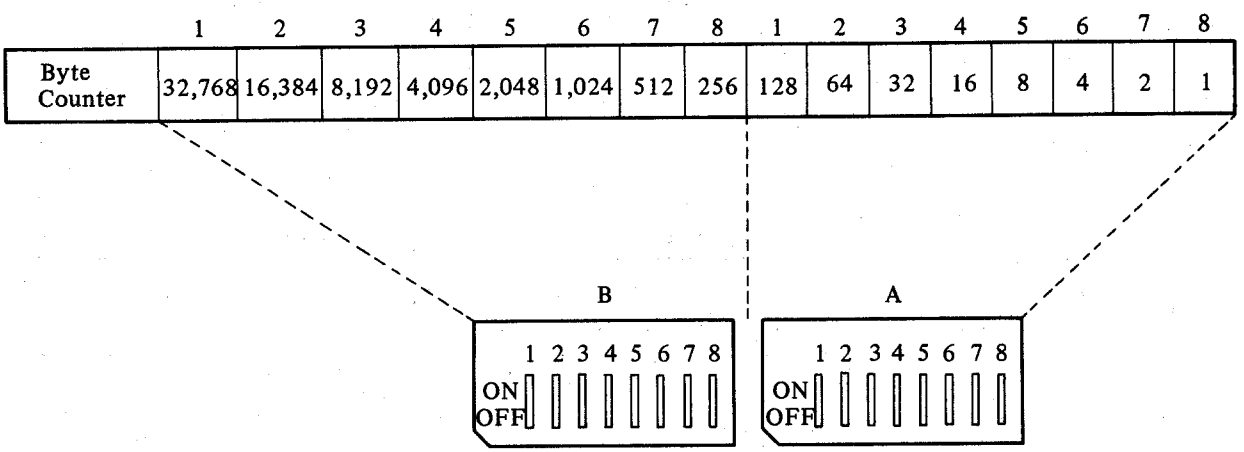
In this case, the number of bytes in the last sector is calculated as follows.

$$40,960 - 8 \times 4,552 = 4,544$$

Namely, the last sector is eight bytes shorter than the others.

Refer to Table 3.4.4 for the settings of DIP switches.

Table 3.4.4 Setting of sector count



Sector Count	A-8	A-7	A-6	A-5	A-4	A-3	A-2	A-1	B-8	B-7	B-6	B-5	B-4	B-3	B-2	B-1	Bytes Per Sect/Last Sect
(2^n)	1	2	4	8	16	32	64	128	256	512	1024	2048	4096	8192	16384	32768	
1	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	OFF	OFF	ON	40960
2	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	OFF	OFF	ON	OFF	20480
3	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	ON	OFF	OFF	13654/13652
4	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	OFF	OFF	ON	OFF	OFF	10240
5	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	OFF	OFF	OFF	8192
6	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	ON	OFF	OFF	OFF	6827/6825
7	ON	ON	OFF	ON	ON	OFF	ON	ON	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	5852/5848
8	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	5120
9	ON	ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	4552/4544
10	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	4096

Table 3.4.4 Setting of sector count - continued

Sector Count	A-8	A-7	A-6	A-5	A-4	A-3	A-2	A-1	B-8	B-7	B-6	B-5	B-4	B-3	B-2	B-1	Bytes Per Sect/Last Sect
(2^n)	1	2	4	8	16	32	64	128	256	512	1024	2048	4096	8192	16384	32768	
11	ON	ON	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	ON	ON	OFF	OFF	OFF	OFF	3724/3720
12	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	3414/3406
13	OFF	ON	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	3151/3148
14	ON	OFF	ON	ON	OFF	ON	ON	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	OFF	2926/2922
15	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	2731/2726
16	ON	ON	ON	ON	ON	ON	ON	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	2560
17	ON	OFF	OFF	ON	OFF	ON	ON	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	2410/2400
18	ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	2276/2268
19	ON	ON	OFF	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	2156/2152
20	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	2048
21	OFF	ON	ON	ON	ON	OFF	OFF	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	1951/1940
22	ON	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	1862/1858
23	OFF	OFF	ON	OFF	ON	ON	ON	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	1781/1778
24	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	1707/1699
25	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	1639/1624
26	ON	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	1576/1560
27	ON	OFF	ON	ON	OFF	ON	ON	ON	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	1518/1492
28	OFF	ON	ON	OFF	ON	ON	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	1463/1459
29	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	1413/1396
30	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	1366/1346

Table 3.4.4 Setting of sector count - continued

Sector Count	A-8	A-7	A-6	A-5	A-4	A-3	A-2	A-1	B-8	B-7	B-6	B-5	B-4	B-3	B-2	B-1	Bytes Per Sect/Last Sect
(2^n)	1	2	4	8	16	32	64	128	256	512	1024	2048	4096	8192	16384	32768	
31	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	1322/1300
32	ON	ON	ON	ON	ON	ON	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	1280
33	ON	OFF	OFF	ON	ON	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	1242/1216
34	OFF	OFF	ON	OFF	ON	ON	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	1205/1195
35	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	1171/1146
36	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	1138/1130
37	ON	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	1108/1072
38	ON	OFF	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	1078/1074
39	OFF	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	1052/1022
40	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	1024
41	ON	ON	ON	OFF	OFF	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	1000/960
42	ON	ON	ON	ON	OFF	OFF	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	976/944
43	OFF	OFF	OFF	ON	ON	ON	OFF	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	953/934
44	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	931/927
45	OFF	ON	ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	911/876
46	OFF	ON	OFF	ON	ON	ON	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	891/865
47	ON	ON	ON	OFF	OFF	ON	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	872/848
48	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	854/822
49	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	836/832
50	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	820/780

Table 3.4.4 Setting of sector count - continued

Sector Count	A-8	A-7	A-6	A-5	A-4	A-3	A-2	A-1	B-8	B-7	B-6	B-5	B-4	B-3	B-2	B-1	Bytes Per Sect/Last Sect
(2^n)	1	2	4	8	16	32	64	128	256	512	1024	2048	4096	8192	16384	32768	
51	ON	ON	OFF	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	804/760
52	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	788/772
53	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	773/764
54	OFF	ON	ON	OFF	ON	ON	ON	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	759/733
55	OFF	OFF	OFF	ON	OFF	ON	ON	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	745/730
56	ON	ON	OFF	ON	ON	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	732/700
57	OFF	ON	ON	ON	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	719/696
58	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	707/661
59	OFF	ON	ON	OFF	ON	ON	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	695/650
60	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	683/663
61	ON	ON	ON	ON	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	672/640
62	OFF	OFF	ON	OFF	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	661/639
63	OFF	ON	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	651/598
64	ON	ON	ON	ON	ON	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	640
65	OFF	ON	ON	OFF	ON	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	631/576
66	OFF	OFF	ON	ON	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	621/595
67	ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	612/568
68	OFF	ON	OFF	ON	ON	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	603/559
69	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	594/568
70	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	586/526

Table 3.4.4 Setting of sector count - continued

Sector Count	A-8	A-7	A-6	A-5	A-4	A-3	A-2	A-1	B-8	B-7	B-6	B-5	B-4	B-3	B-2	B-1	Bytes Per Sect/Last Sect
(2^n)	1	2	4	8	16	32	64	128	256	512	1024	2048	4096	8192	16384	32768	
71	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	577/570
72	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	569/561
73	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	562/496
74	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	554/518
75	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	547/482
76	OFF	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	539/535
77	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	532/528
78	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	526/458
79	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	519/478
80	ON	ON	ON	ON	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	512
81	ON	OFF	OFF	ON	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	506/480
82	ON	ON	OFF	OFF	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	500/460
83	ON	OFF	ON	ON	OFF	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	494/452
84	ON	ON	ON	OFF	OFF	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	488/456
85	ON	OFF	OFF	OFF	OFF	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	482/472
86	OFF	OFF	ON	ON	ON	OFF	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	477/415
87	OFF	ON	ON	OFF	ON	OFF	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	471/454
88	ON	OFF	OFF	OFF	ON	OFF	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	466/418
89	OFF	OFF	ON	ON	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	461/392
90	ON	ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	456/376

Table 3.4.4 Setting of sector count - continued

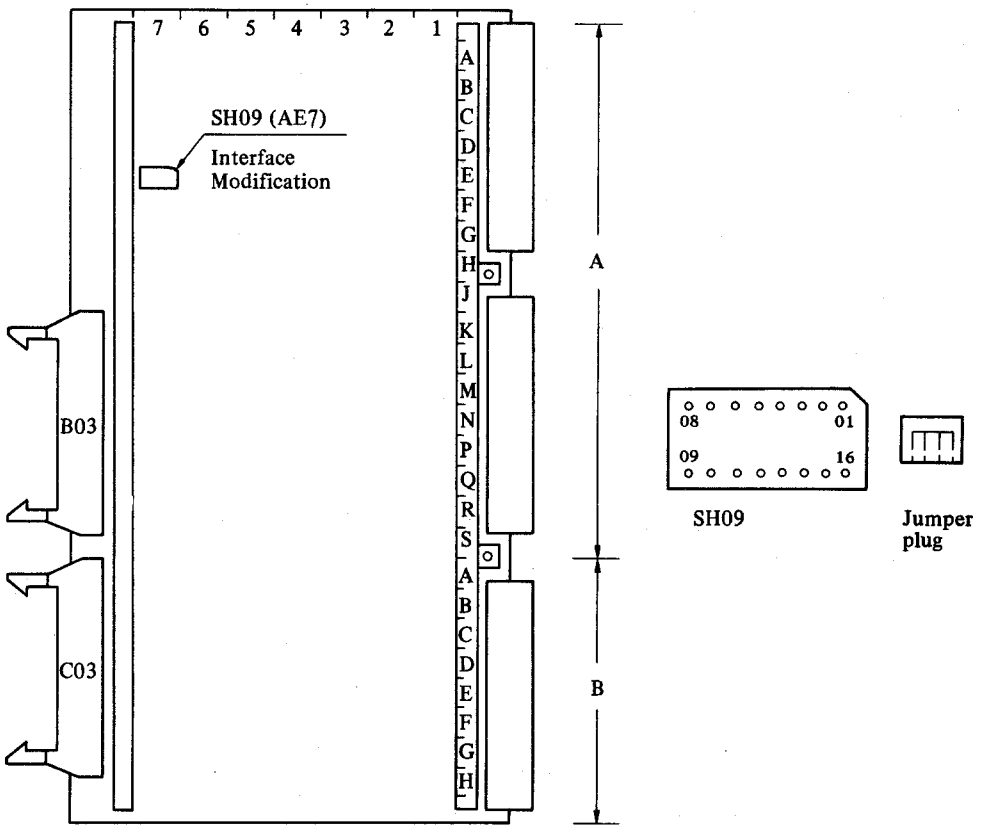
Sector Count	A-8	A-7	A-6	A-5	A-4	A-3	A-2	A-1	B-8	B-7	B-6	B-5	B-4	B-3	B-2	B-1	Bytes Per Sect/Last Sect
(2^n)	1	2	4	8	16	32	64	128	256	512	1024	2048	4096	8192	16384	32768	
91	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	451/370
92	ON	OFF	ON	ON	ON	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	446/374
93	OFF	OFF	OFF	ON	ON	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	441/388
94	ON	ON	OFF	OFF	ON	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	436/412
95	ON	ON	ON	ON	OFF	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	432/352
96	OFF	ON	OFF	ON	OFF	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	427/395
97	OFF	ON	ON	OFF	OFF	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	423/352
98	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	418/414
99	ON	OFF	ON	ON	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	414/388
100	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	410/370
101	ON	OFF	ON	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	406/360
102	ON	OFF	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	402/358
103	ON	OFF	ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	398/364
104	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	394/378
105	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	391/296
106	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	387/325
107	OFF	ON	ON	ON	ON	ON	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	383/362
108	ON	ON	OFF	ON	ON	ON	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	380/300
019	ON	ON	ON	OFF	ON	ON	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	376/352
110	OFF	OFF	ON	OFF	ON	ON	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	373/303

Table 3.4.4 Setting of sector count - continued

Sector Count	A-8	A-7	A-6	A-5	A-4	A-3	A-2	A-1	B-8	B-7	B-6	B-5	B-4	B-3	B-2	B-1	Bytes Per Sect/Last Sect
(2^n)	1	2	4	8	16	32	64	128	256	512	1024	2048	4096	8192	16384	32768	
111	ON	OFF	OFF	OFF	ON	ON	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	370/260
112	ON	OFF	ON	ON	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	366/334
113	OFF	ON	OFF	ON	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	363/304
114	ON	ON	ON	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	360/280
115	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	357/262
116	ON	OFF	OFF	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	354/250
117	OFF	ON	ON	ON	ON	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	351/244
118	ON	ON	OFF	ON	ON	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	348/244
119	OFF	OFF	OFF	ON	ON	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	345/250
120	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	342/262
121	OFF	ON	OFF	OFF	ON	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	339/280
122	ON	ON	ON	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	336/304
123	ON	OFF	ON	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	334/212
124	OFF	ON	OFF	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	331/247
125	ON	ON	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	328/288
126	ON	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	326/210
127	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	323/262
128	ON	ON	ON	ON	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	320

3.5 Logic PCB

Short circuit (SH09) and jumper plugs for changing interface requirements are provided.



( ) indicates location of short circuit on the PCB.

Figure 3.5.1 Interface modification

Table 3.5.1 Interface modification

Item	Pin number to be shortened	Default mode	Function
Incorporate TAG4, 5 Status Capability	03 - 02	o	Enable
	03 - 04		Disable
Operation of Seek End status	06 - 05		Seek End is not issued after Offset Command is reset.
	06 - 07	o	Seek End is issued after Offset Command is reset.
Response of Unit Ready	10 - 09	o	Unit Ready is issued even if the drive is in a fault condition.
	10 - 11		Unit Ready is not issued when the drive is in a fault condition.

CHAPTER 4 THEORY OF OPERATION

4.1 General Description

The operation of the M2361A is divided into three parts. The first part (Section 4.2) describes the mechanical assemblies of the unit. The second part (Section 4.3 and 4.4) describes the magnetic heads and disks. The third part (Section 4.5 and 4.6) describes the interface, servo circuit, R/W control, and other electronic controls.

4.2 Mechanical Assemblies

4.2.1 Disk Enclosure (DE)

(1) Design concept

The mechanical configuration of the DE shown in Figure 4.2.1 was designed to provide a compact, low power consumption, and maintenance-free file with enhanced performance. It features six 10.5 inch diameter disks and a rotary actuator with the fast average positioning time of 18 msec. The rotary actuator is completely balanced statically and dynamically by using a pair of moving coils, thereby avoiding undesired vibration that prolongs settling time.

(2) Spindle and base casting

The primary function of the spindle is to maintain precise and constant rotation of the assembled disks. The accuracy of rotation involves concentricity, precision, thermal and dynamic stability; all of which become more stringent as the track spacing gets tighter.

The dual-supported spindle construction reduces this problem. In this design, the supporting casting is divided into two pieces in a plane parallel to the spindle axis, with one of the divided pieces substantially retaining the rotating bearings. Thus, precise concentricity can be maintained.

With regard to the base casting, it is important to keep the relative dimension between the spindle and rotary actuator very rigid, especially in a dynamic mode. This has been given critical attention as track spacing and access time become smaller and shorter.

In the present drive, the rotary actuator is designed so that the rotating axis is pivoted at both ends, similar to the spindle. A pair of arms are extended from the spindle bearing part to the pivoting element of the rotary actuator. This technique, combined with the high rigidity of the actuator, provides resonant-free seek operation.

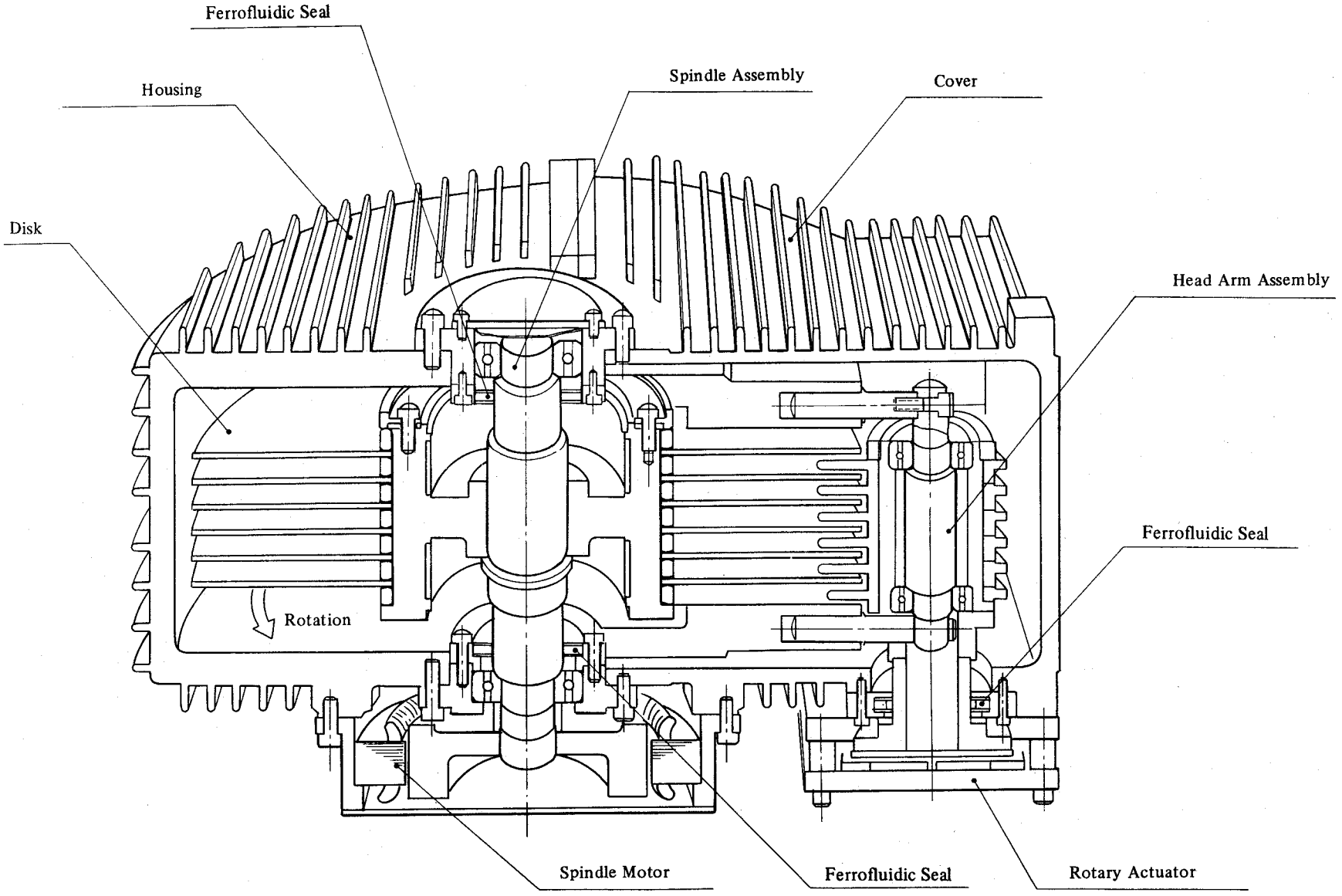


Figure 4.2.1 Cross sectional view of the DE

(3) Air system

The fundamental and important function of the air system is to maintain an ultra-clean environment within the space of the DE to minimize the possibility of head-disk interference. In this DE, a new type of self circulating air system is provided. Features of the system are its simplicity and maintenance free operation. Air flows through the disk spacings from the center to outside of the disks by the pressure difference between them, induced by the rotation of disks. An absolute filter, whose efficiency is 99.97 percent above 0.3 μm particle size dust, is attached within the spindle hub and is rotating with the disks. Particle count goes to nearly zero in a few minutes from the start of rotation. Ferrofluidic seals are adopted to complete the elimination of air contamination.

To enhance the cooling efficiency, the housing is made entirely of aluminum casting with a high heat conductivity, and many fins formed around it. Air circulation is completely symmetrical in the disk stacking direction, and air flow is well intermingled at the inside hub for uniform and efficient cooling around the read/write heads, along with the servo head.

4.2.2 Spindle motor

(1) Features

By adopting the brushless DC spindle motor and connecting the motor directly to the spindle shaft, the following are realized.

- The device becomes compact.
- Pulley and belts are unnecessary, therefore, no maintenance is required.
- Accuracy of rotational speed is improved.
- Vibration is reduced.
- Dynamic braking replaces mechanical brake

(2) Construction

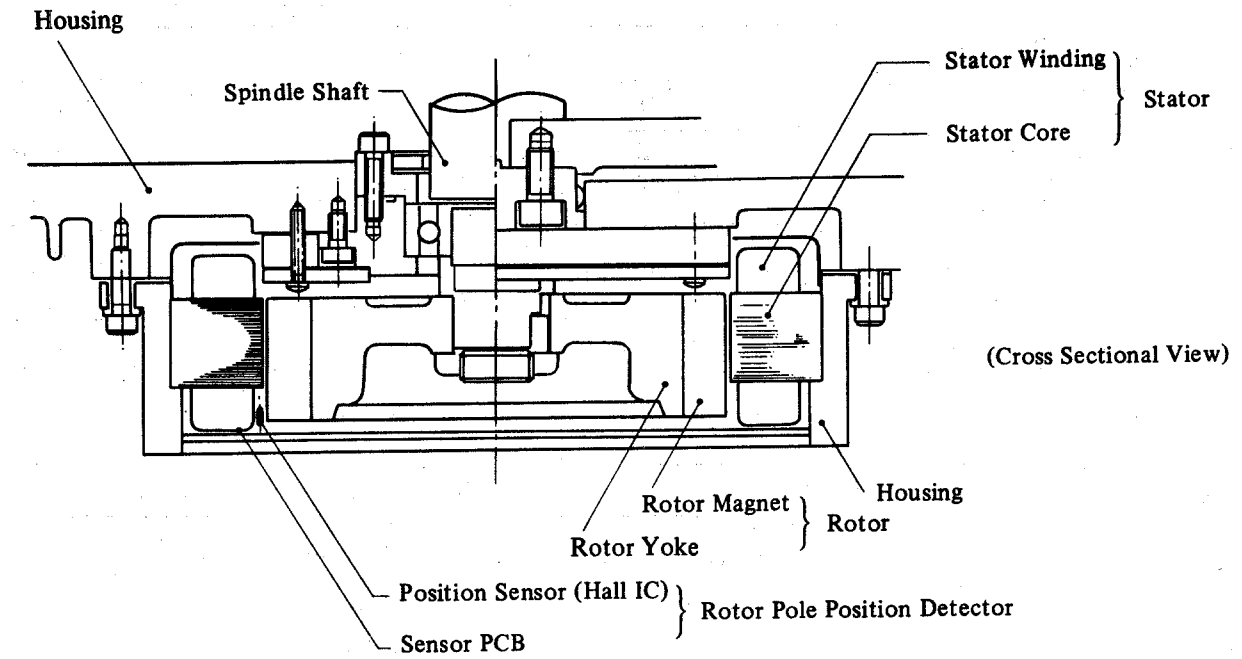
Construction of the motor is shown in Figure 4.2.2. The rotor poles generate torque by the revolving magnetic field, and are connected directly to a single shaft to which magnetic disks are attached. The stator winding generates the above mentioned revolving magnetic field by successively switching the current in it.
The rotor pole position detector determines the switching time of the current in the stator winding by detecting the position of rotor poles. The stator winding and rotor pole position detector are fixed in the motor housing, which is fixed on the DE base.

(3) Specification

Table 4.2.1 Specifications

Output	P	W	120
Rated torque	T	kg-cm	2.7
Rated revolution	N	rpm	3,961
Rated Current	I	A	4.0
Induced voltage constant	Ke	mV/rpm, O/P/phase	8.2
Winding resistance	Ra	Ω/phase at 20°C	1.12
Winding inductance	La	mH/phase	1.7
Winding phase number			3
Number of poles and pole pairs	2P		4
Position sensor		DN6839 Matsushita Electric	

The rated values are 3-phase, half drive (for 120° conduction)



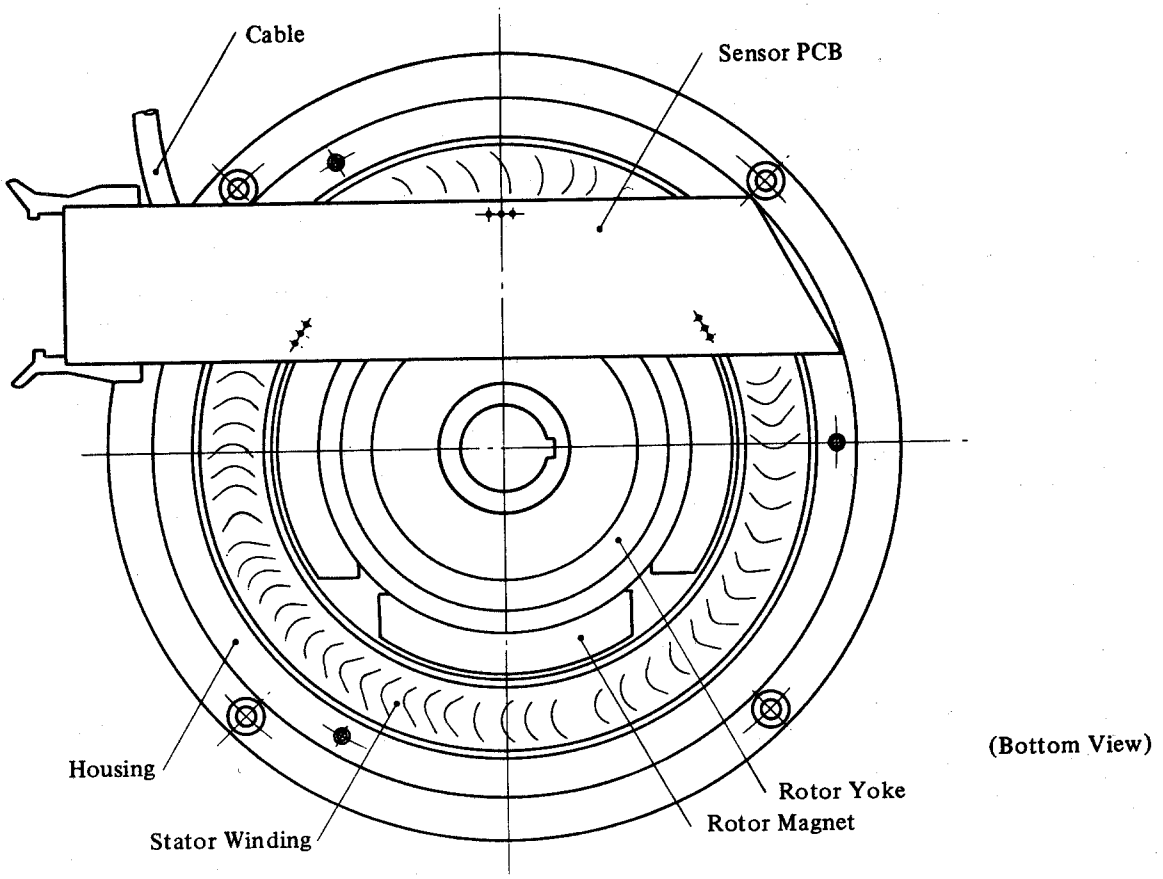


Figure 4.2.2 Construction of the spindle motor

(4) Principle of operation

The brushless DC motor is made by replacing brushes and commutators of the ordinary DC motor with a rotor pole position detector and a semiconductor drive circuit. The schematic circuit of the 3-phase half-wave drive used is shown in Figure 4.2.3. The various waveforms when the DC motor is rotating in the regular direction are shown in Figure 4.2.4. Consequently, in an actual drive, the rotational force is obtained by energizing the windings in the order of C'-C→B'-B→A'-A.

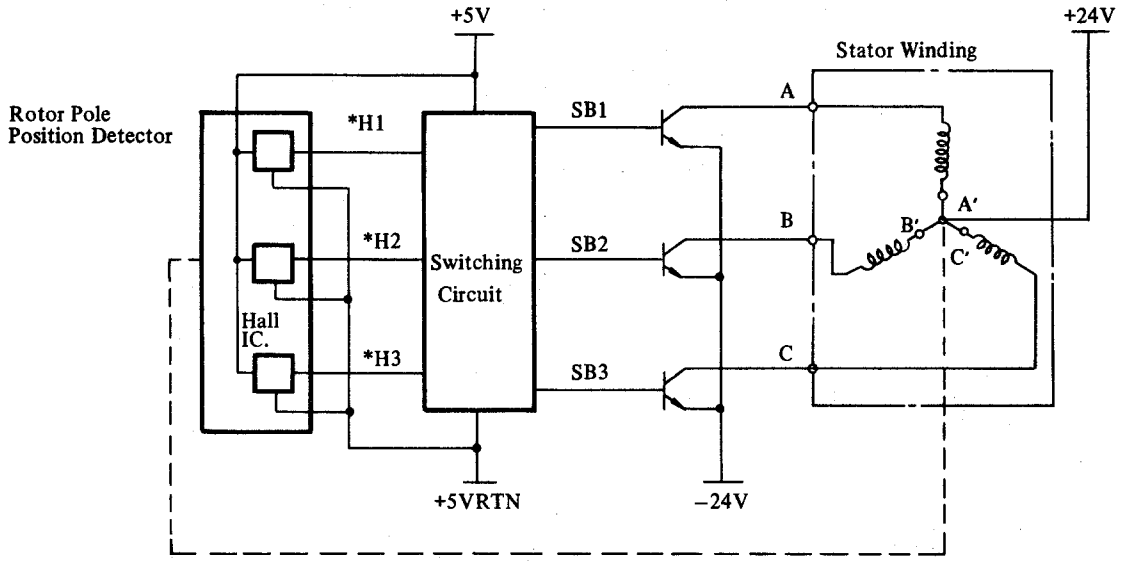


Figure 4.2.3 Schematic diagram of the drive circuit

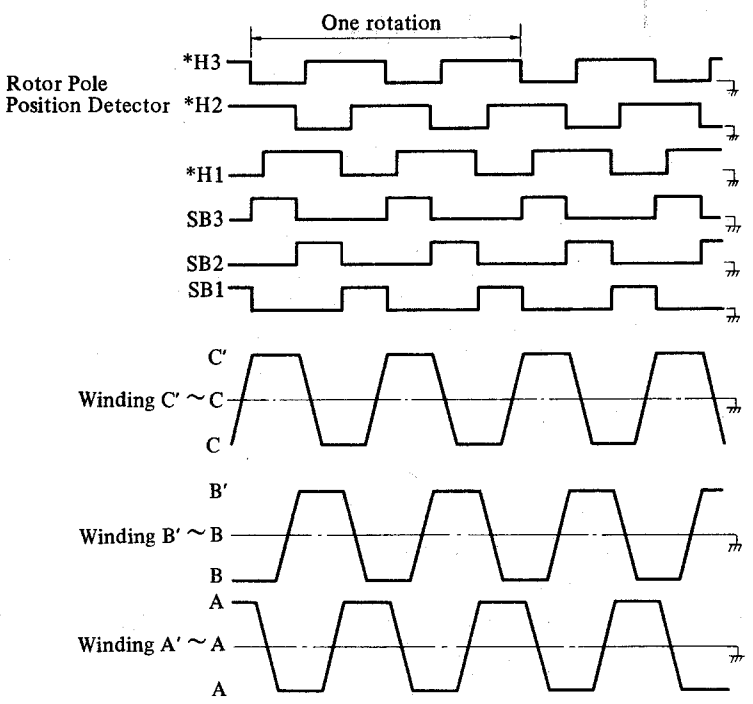


Figure 4.2.4 DC motor waveforms

4.2.3 Rotary actuator

The drive shaft of the head-arm assembly in the DE is coupled directly to a bobbin supporting base to be driven by the rotary actuator outside the DE. A ferrofluidic seal is utilized to separate inside and outside the DE. Two coil-bobbins are attached to the bobbin supporting base, and two magnetic circuits are provided to supply torque to the coil bobbins, moving the head-arm assembly to the desired cylinder within a short access time.

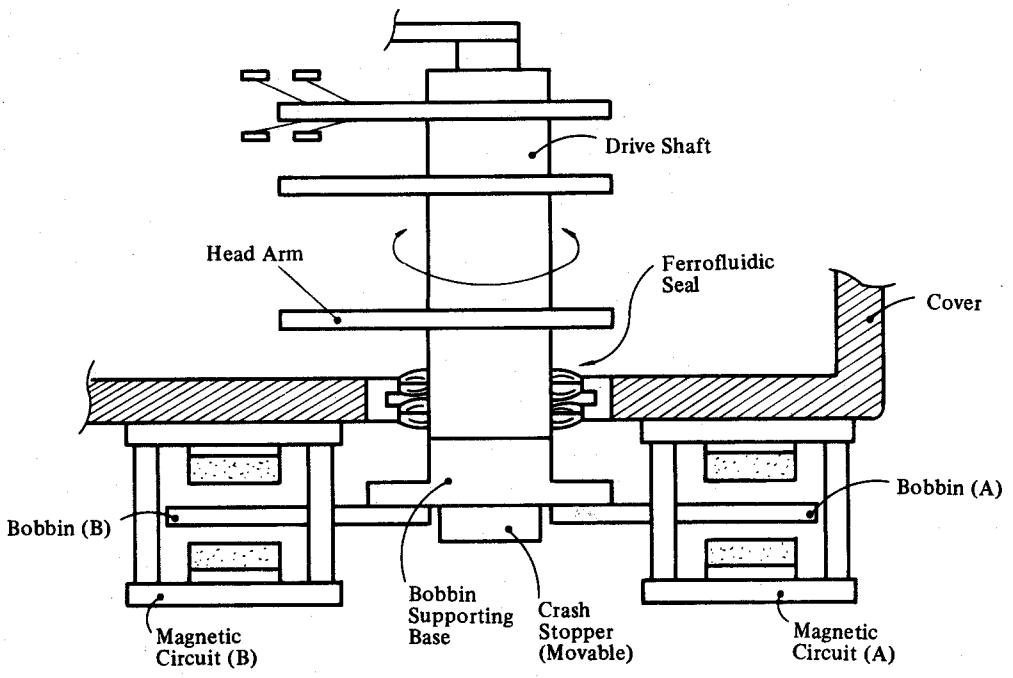


Figure 4.2.5 Construction of the actuator

(1) Magnetic circuit

The pair of magnetic circuits are constructed symmetrically as shown in Figure 4.2.6. Each circuit incorporates four permanent magnets (rare earth magnets) with two magnetic gaps in between. Each magnetic gap contains a uniformly spread magnetic field. The coil bobbin is inserted in it and generates torque proportional to the current in the coil and the intensity of the magnetic field. This torque is sufficient to move the head-arm assembly at the specified speed.

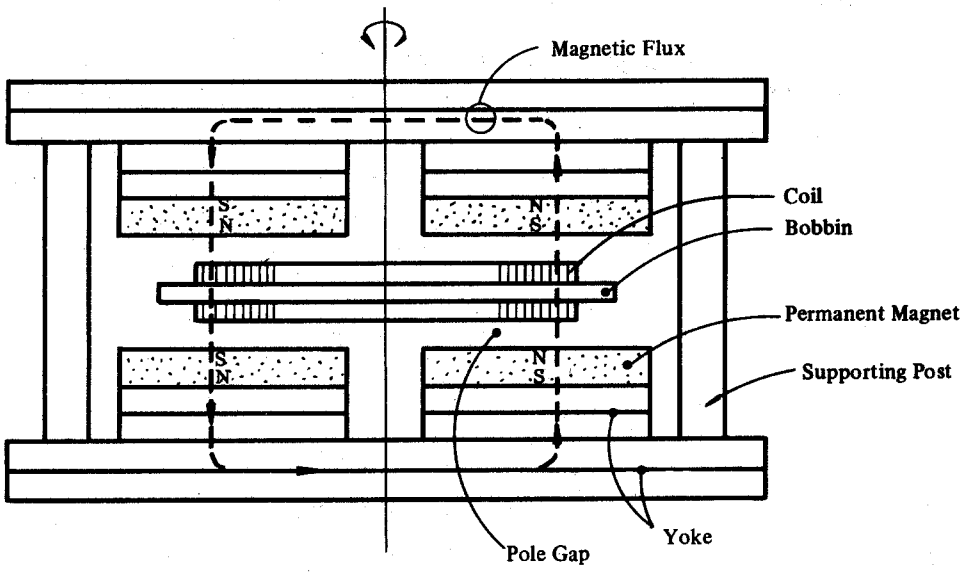


Figure 4.2.6 Magnetic circuit

(2) Drive coil

The two coil bobbins are identical. A pair of flat copper wire coils are attached on the top and bottom of each coil bobbin. The four coils are then connected in series to generate torque in the same direction due to the current flowing in each coil.

(3) Crash stop

The crash stop consists of a moving part attached to the bobbin supporting base and fixed parts on the DE. It determines the movable range of the head-arm assembly, and provides safe deceleration in the event of an uncontrolled seek.

4.2.4 Actuator auto lock

During transportation, all heads must be placed within the CSS zone to prevent damage to the data area. For this purpose, the M2361A has an auto lock mechanism for the rotary actuator outside of the DE. See Figure 4.2.7.

(1) Locked (Power off)

The magnet plunger locks the auto lock arm whenever the power (± 24VDC) is not supplied. The rotary actuator cannot move because its stopper pin is locked in place to the inner stopper.

(2) Unlocked (Power on)

When ±24VDC exists, the magnet plunger pulls the auto lock arm. Then the stopper pin is free and the rotary actuator can move.

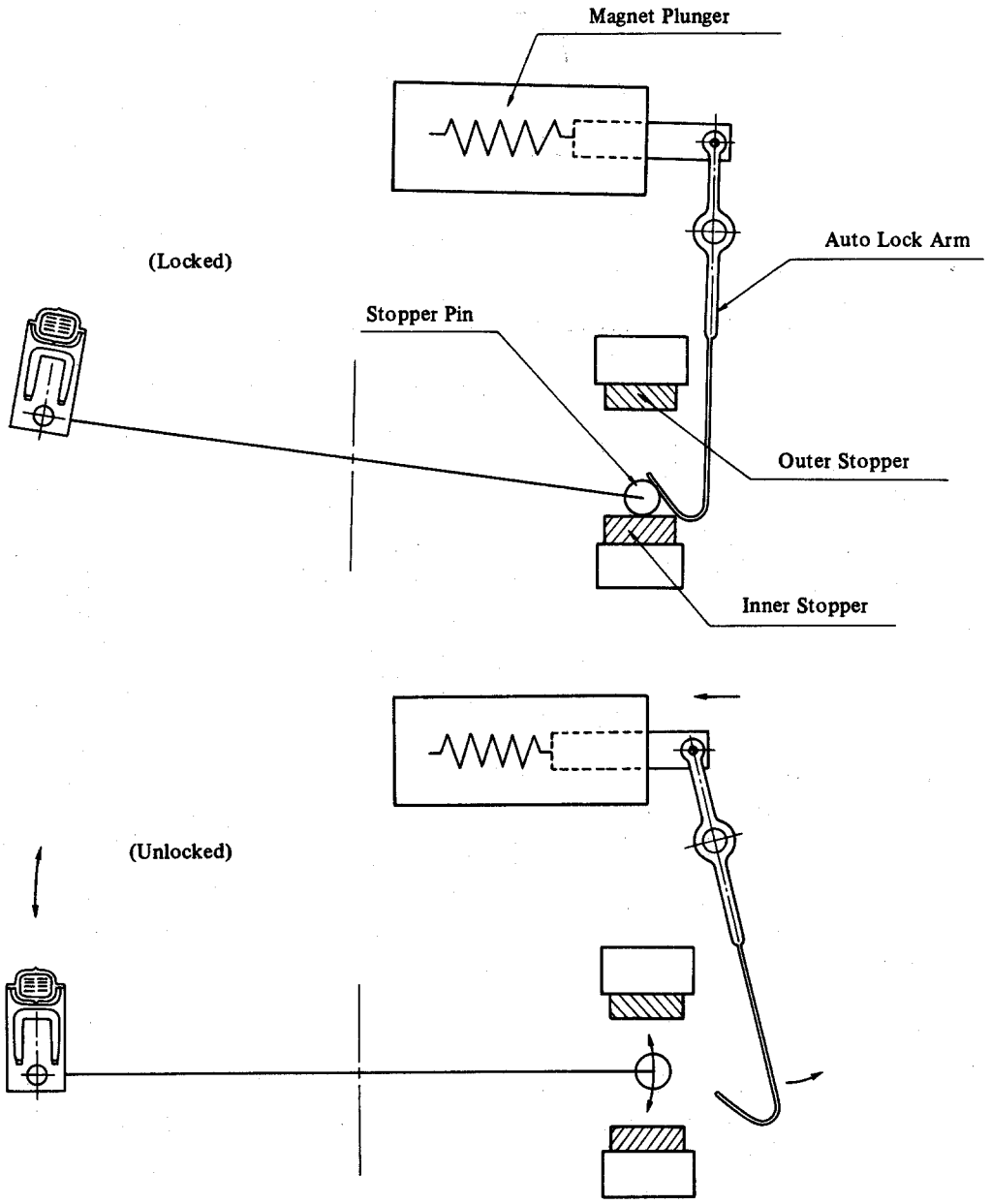


Figure 4.2.7 Actuator auto lock

4.3 Magnetic Head and Disk

4.3.1 Magnetic head

To obtain a high recording density, advanced Winchester type CSS (Contact Start and Stop) heads are used. While the disks are not rotating, the heads rest on the disk surfaces in contact, but when rotation starts, the heads begin to float over the disk surfaces. After the disks reach the specified rotational speed, the heads maintain the flying height with the balanced force of each load spring and the air-bearing between disk surfaces and the head sliders.

Therefore, to prevent wear caused by contact-start/stop, and to achieve minimum but stable flying height, the head is loaded slightly and its slider rails are tapered.

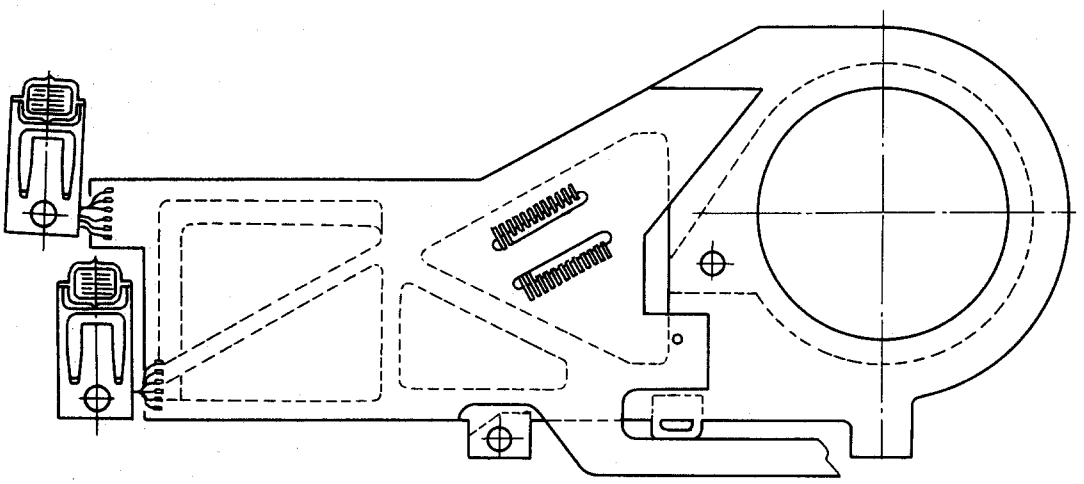


Figure 4.3.1 Head arm assembly
Note: Head Assemblies shown are for the M2351A

To increase the output voltage at high recording density, the core is made from Mn-Zn instead of Ni-Zn which is the commonly used material.

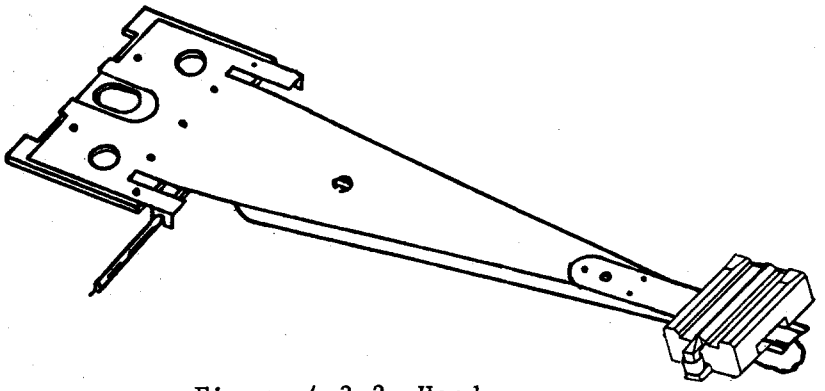


Figure 4.3.2 Head

4.3.2 Magnetic disk

A magnetic disk has a diameter of 10.5 inches (268 mm) and is made of aluminum on which magnetic material is coated. Special coating is provided on the surface of this magnetic material in order to prevent wear caused by repeated contact-start/stop operations.

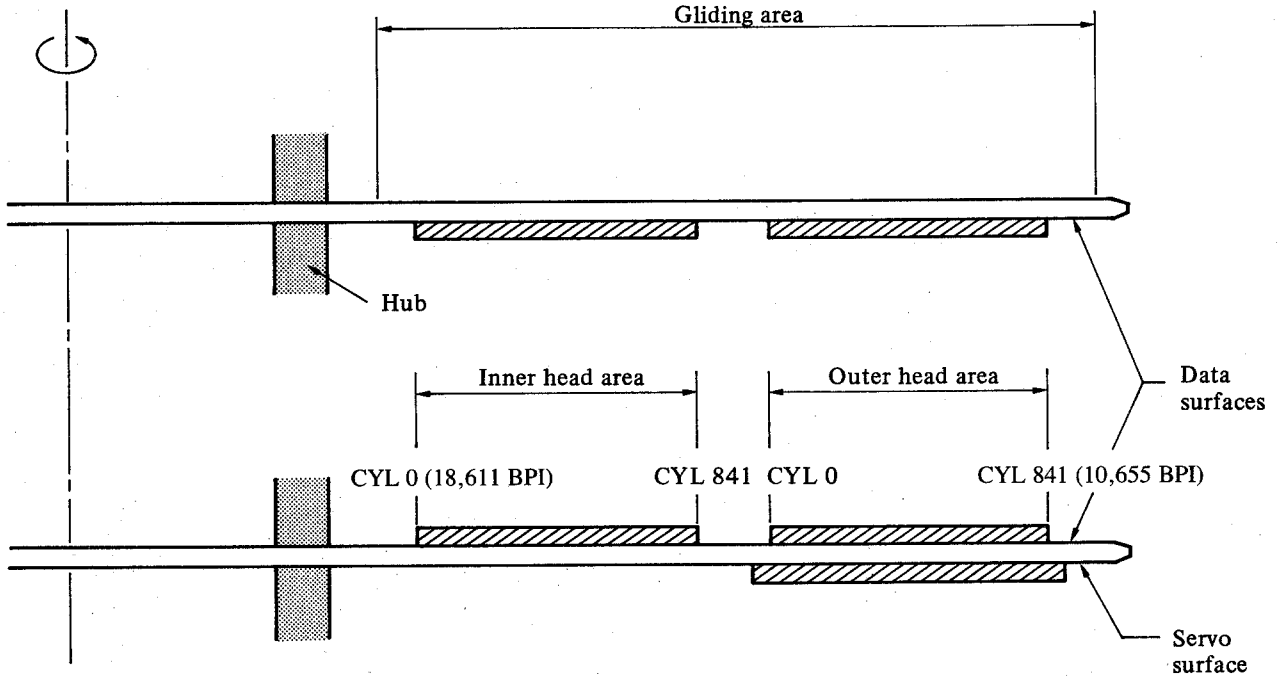


Figure 4.3.3 Data and servo area locations

Though the rotational angle of arm assemblies is constant for all tracks (2.27×10^{-4} radians per track), the track pitch for the inner and outer heads varies as shown in Figure 4.3.4 depending on the mechanical arrangement of the head-arm and the cores.

The track width of the inner head is made wider than that of the outer head to avoid decrease of time margin for the read operation.

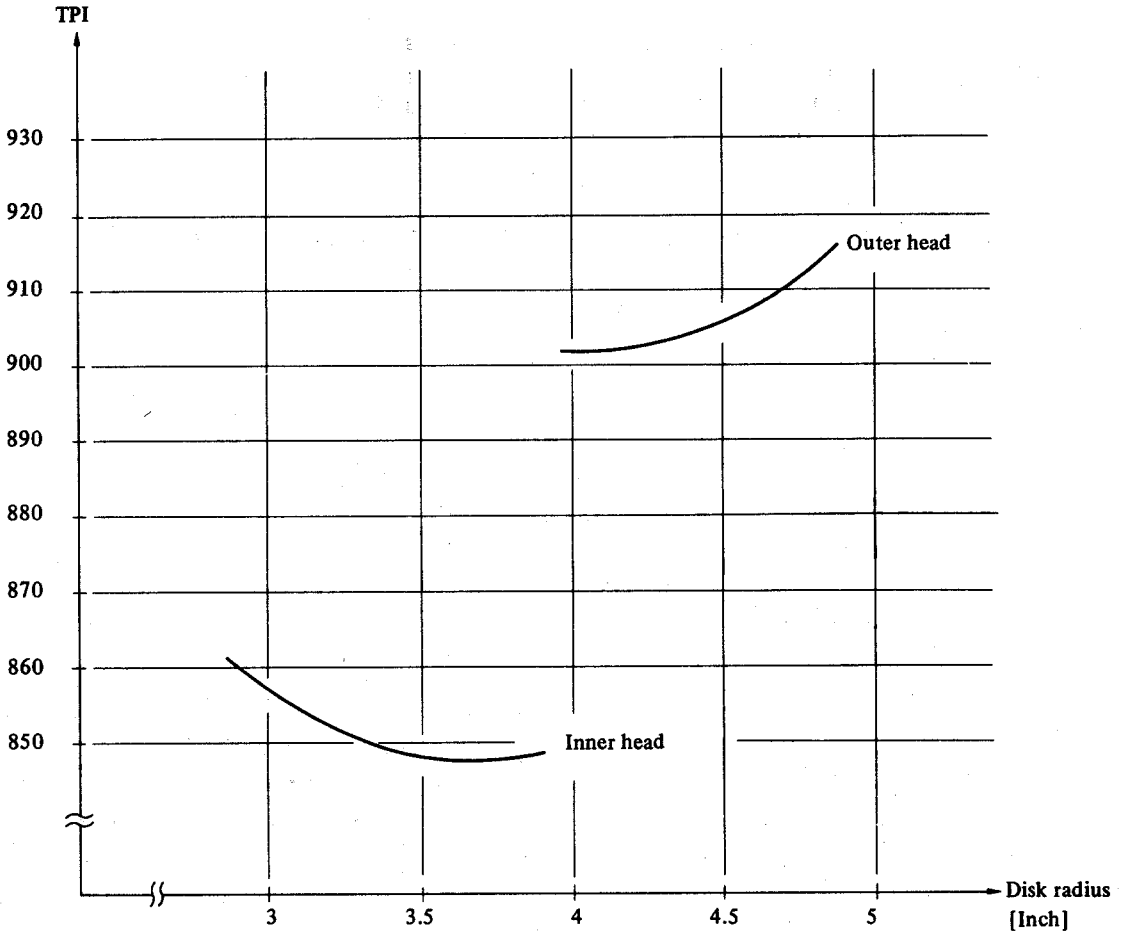


Figure 4.3.4 Track pitch

4.3.3 Servo track format

The servo area is used to store the unique data patterns which generate the track positioning, index, guard band, and clock signals. This data is prerecorded on the disk before the unit is shipped from the factory.

The servo area consists of a combination of 01, 02, E1 and E2 tracks.

The magnetized pattern of servo signal is shown in Figure 4.3.5.

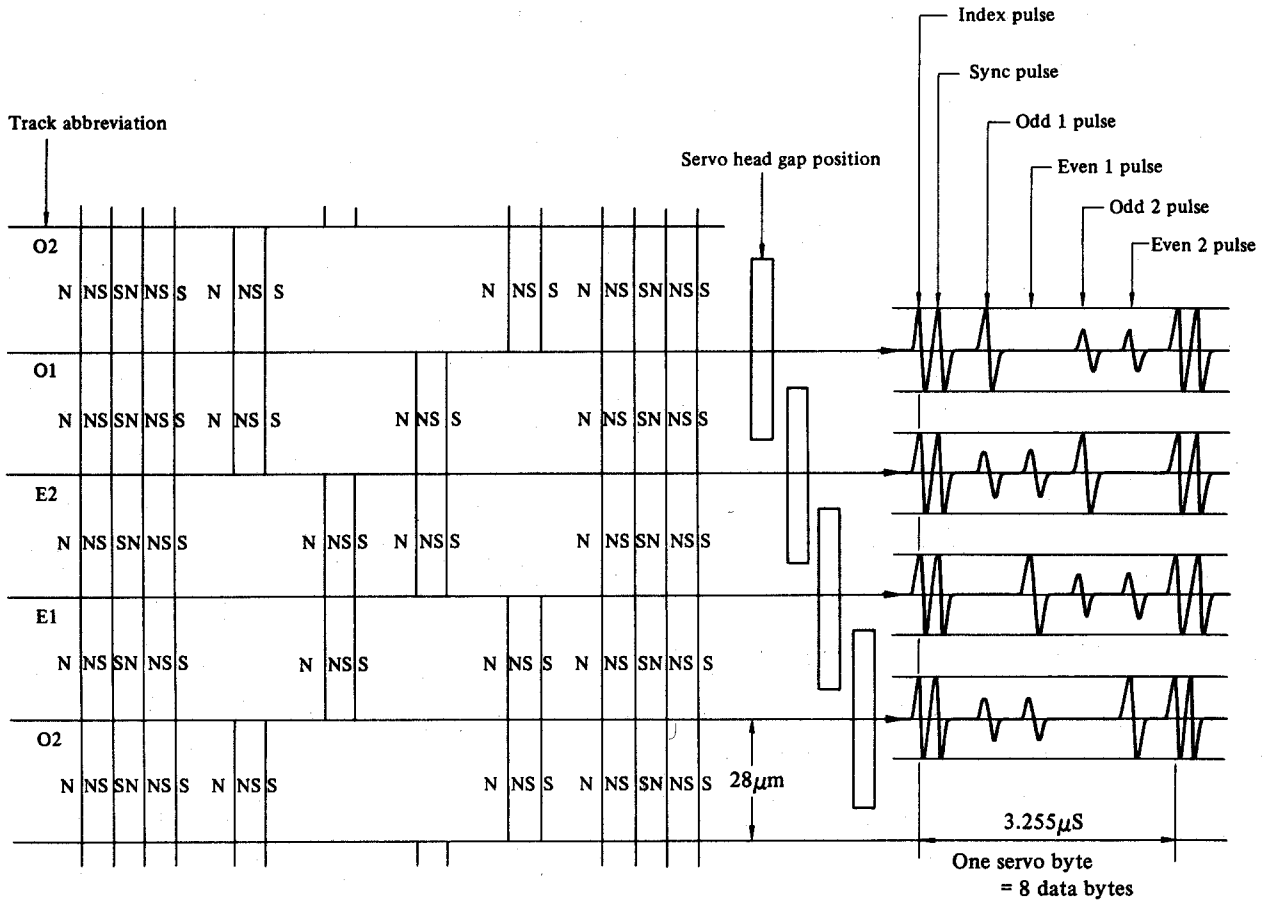
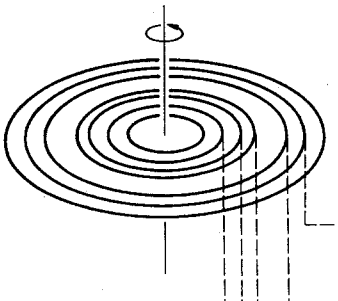
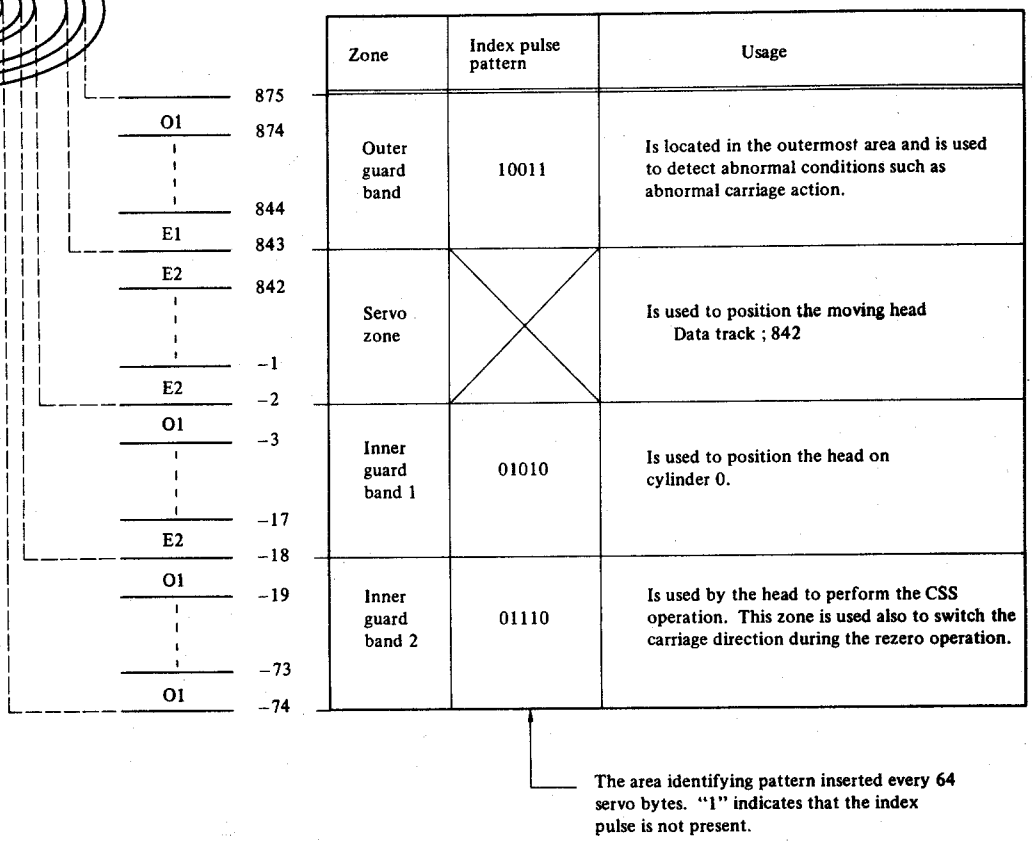


Figure 4.3.5 Magnetized pattern of servo signal and read signal





Zone	Index pulse pattern	Usage
Outer guard band	10011	Is located in the outermost area and is used to detect abnormal conditions such as abnormal carriage action.
Servo zone		Is used to position the moving head Data track ; 842
Inner guard band 1	01010	Is used to position the head on cylinder 0.
Inner guard band 2	01110	Is used by the head to perform the CSS operation. This zone is used also to switch the carriage direction during the rezero operation.

The area identifying pattern inserted every 64 servo bytes. "1" indicates that the index pulse is not present.

Figure 4.3.6 Zone allocation on servo surface

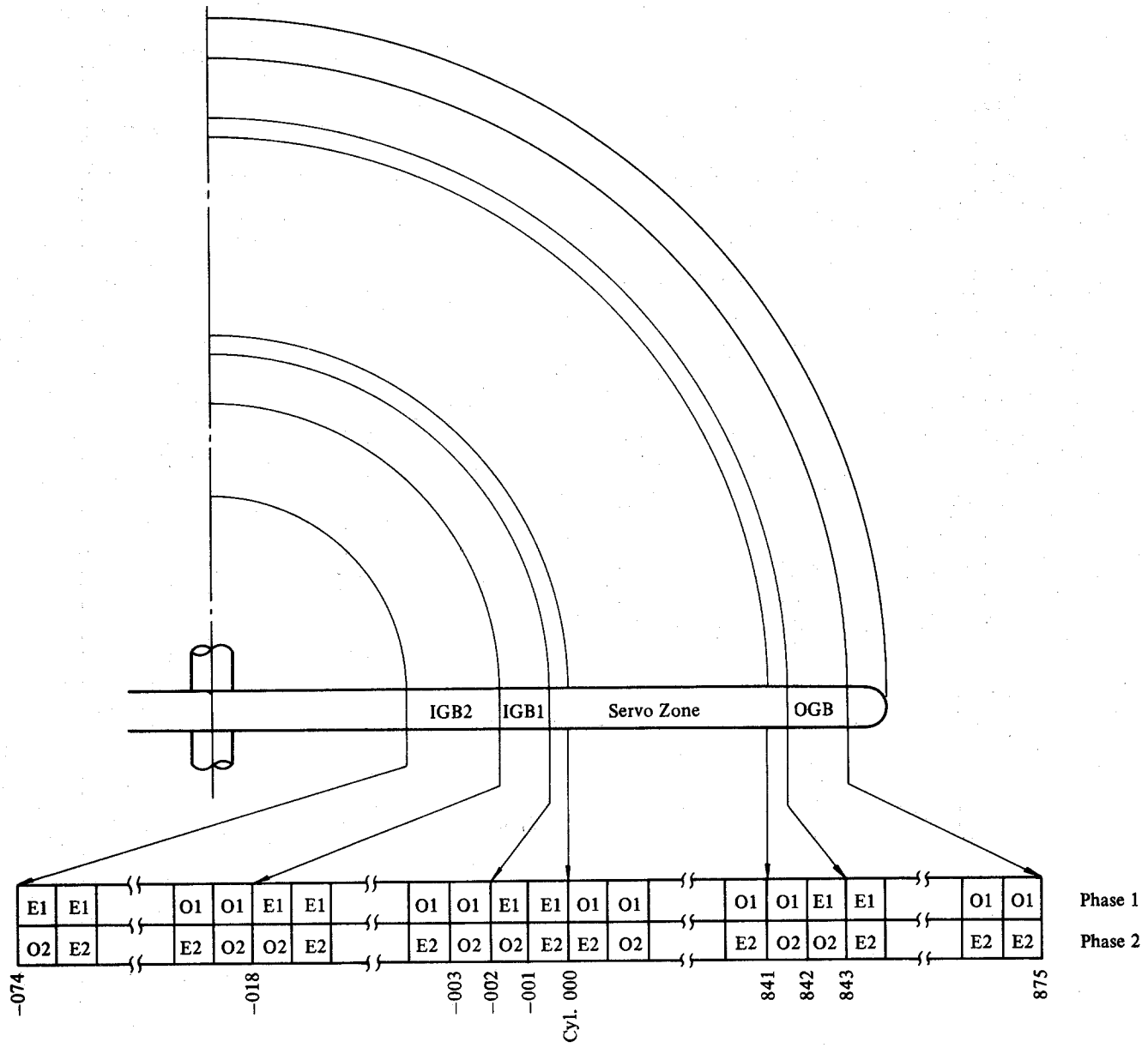


Figure 4.3.7 Servo track configuration

4.4 Data Format

The M2361A can be used with two different formats, i.e., Variable Sector Format and Fixed Sector Format, as determined by the controller. The former contains a 3-Byte DC erased area called an Address Mark (AM) prior to each Address Area (AA) indicating the beginning of a record. Therefore, Data Area (DA) with different lengths in a track can be written or read. On the other hand, every record must have the same length specified by sector length in the Fixed Sector Format.

4.4.1 Format

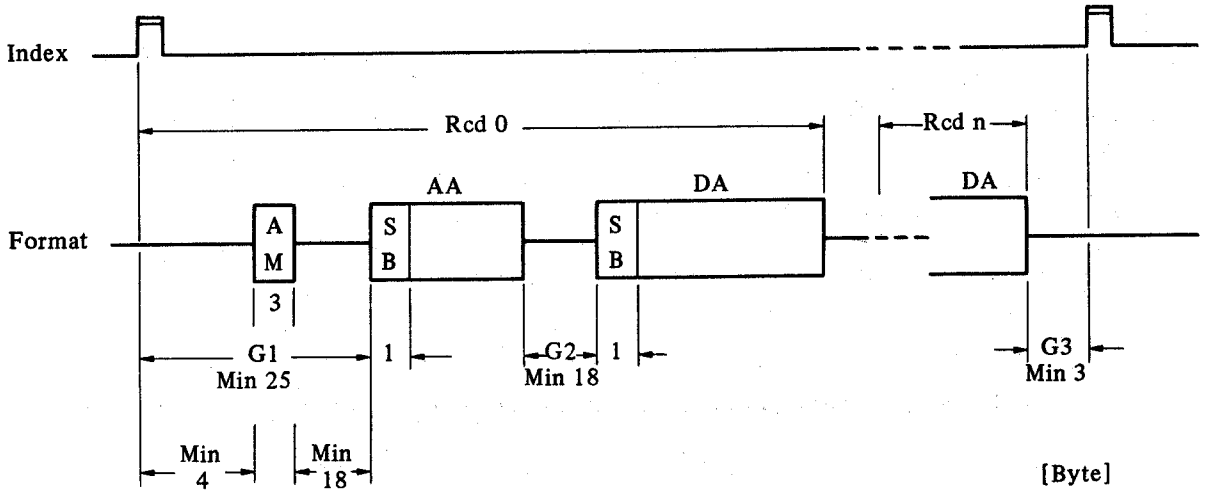


Figure 4.4.1 Variable sector format

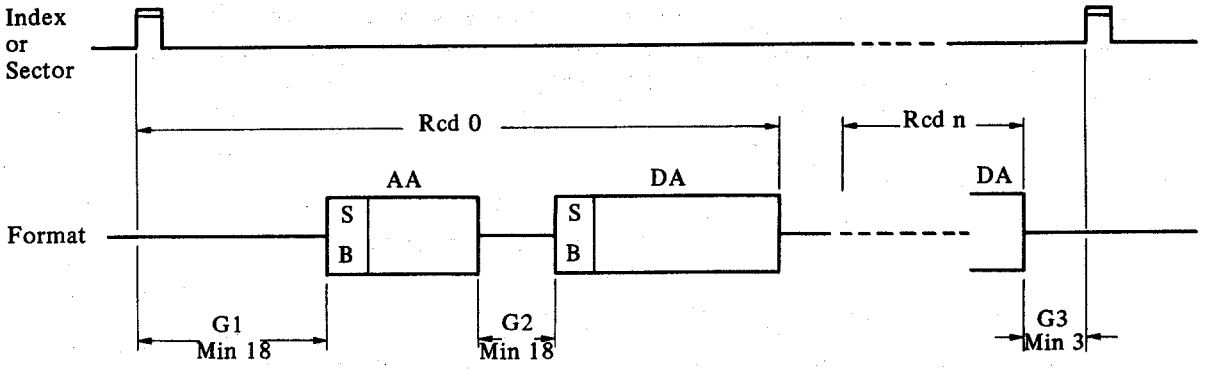


Figure 4.4.2 Fixed sector format

4.4.2 Format parameters

(1) G1, G2, G3 (Gap 1, 2 and 3)

Gaps between adjacent areas. They should be filled with all "0"s.

(2) SB (Sync Byte Pattern)

Indicates the beginning of Address or Data Area.
The pattern for both areas can be varied but the recommended pattern is $(19)_{16}$ or $(0E)_{16}$.

(3) AA (Address Area)

The Address Area should contain the following information;

- Flag Byte to indicate various conditions of the track or sector, i.e., Primary/Alternate track/Sector, Good/Bad track/Sector
- Logical Drive Address
- Cylinder Address
- Head Address
- Sector Address or Record Number
- CRC to check whether the data has been read correctly or ECC to correct the data when a data error has been detected.

(4) DA (Data Area)

The area where the data should be recorded. CRC or ECC must be added.

4.4.3 Track efficiency

Table 4.4.1 shows examples of calculated results of track efficiency in Variable and Fixed Sector Formats. The following assumptions are made for this calculation.

- The length of Address Area including the SB is 8 Bytes.
- All gap lengths used are the shortest in Figures 4.4.1 and 4.4.2.
- The length of the data area is determined using the formula.

  Data Area = SB + DL (Data Length) + CRC
  = 1 + DL + 2 = DL + 3 (Bytes)

- Efficiency = $\frac{\text{DL x (Sector/Track)}}{\text{40,960 (Bytes/Track)}}$ x 100 (%)

Table 4.4.1 Track efficiency

	DL (B)	256	512	1,024	2,048
Variable Sector Format	Sector/Track	128	71	36	19
	Efficiency (%)	80.0	88.8	90.0	95.0
Fixed Sector Format	Sector/Track	128	71	38	19
	Efficiency (%)	80.0	88.8	95.0	95.0

4.4.4 Media specifications

The quality of all tracks are checked, and location and length of media flaws which may affect the reliability of stored data are recorded in the Header Areas of all tracks before the shipment of a drive from the factory. Therefore, by using techniques such as sector/track deallocation or skip displacement, valid data must not be written over known media flaws.

(1) Definition of track quality

Every track is classified into three grades dependent on number of defects on a track. They are:

Perfect track	:	A track containing no defects
Good track	:	A track containing one defect
Defective track	:	A track containing from two to four defects, or a track containing flaws which may contribute to missing AM or false AM. If the track is defective, the high order bit of the first cylinder byte in the Header Area is set to one.

Here, defect is defined as media flaws grouped by the maximum flaw length of 64 bytes. 65 bytes of media flaws are treated as two defects, as an example.

(2) Quality standards of media at shipment

- The number of defects per DE ≦ 700
- The number of defective tracks per DE ≦ 45
- Head 0 and 1 at cylinder 0 are perfect tracks
- There is at least one perfect track and no defective tracks at cylinder 841
- All tracks in fixed-heads area are not defective
- If there is a defect in the region of bytes 14-55 after the index mark, there is no defect in the region of bytes 69-164.
- If there is a defect in the region of bytes 56-104 after the index mark, there is no defect in the region of bytes 14-55 and 116-164.

A DE which does not meet these standards is rejected at its shipment.

(3) Header format

The Header format is divided into two parts. The first part of the format is a Fixed Sector Format, and the second part is a Variable Sector Format. The Fixed Sector Format information is normally included in the first 56 bytes following the index mark. The Variable Sector Format information consists of 49 bytes and normally follows the Fixed Sector information.

Following are rules for the defect recording:

- The position of a defect is listed in bytes (Hex.) after the index mark, +/- 1 byte.
- The length of a defect is in bits (Hex.) +/- 1 bit.
- Unused defect locations are all zeros.
- Every track is recorded with this defect format whether defects exist or not.

- More than one defect on a track causes the track to be flagged as a defective track. The first four media defects on the track are logged.

Figure 4.4.3 shows the format when there are no defects in the first 105 bytes after the index mark.

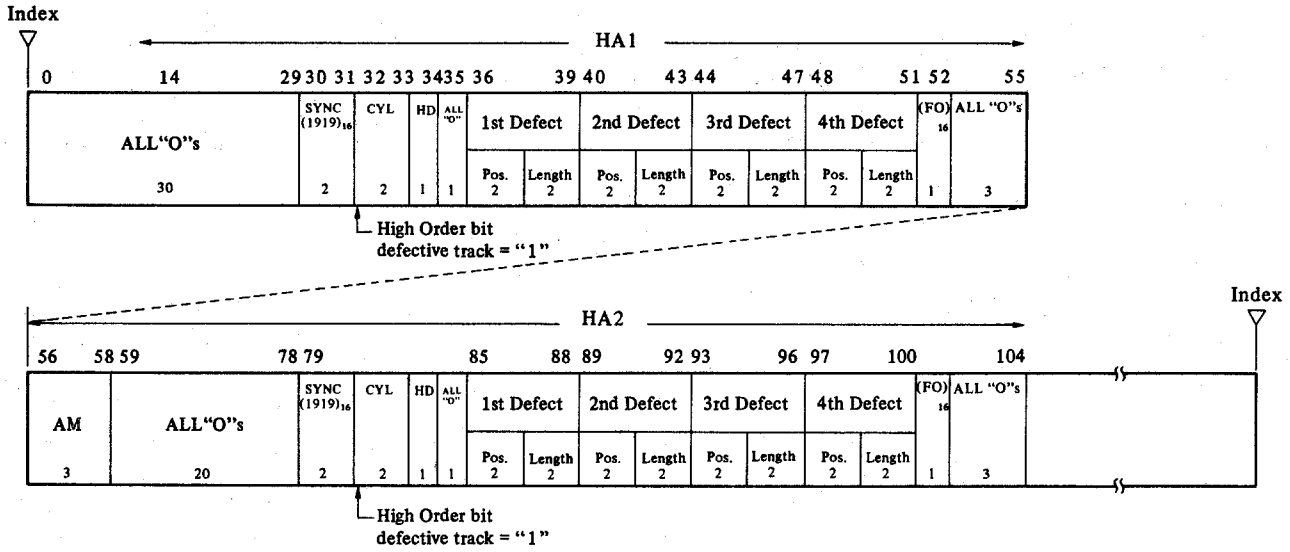


Figure 4.4.3 Format 1

If the beginning of a defect is located in the region of bytes 10 - 55, 60 bytes of zeros are added to Gap 1. Figure 4.4.4 shows an example of this format.

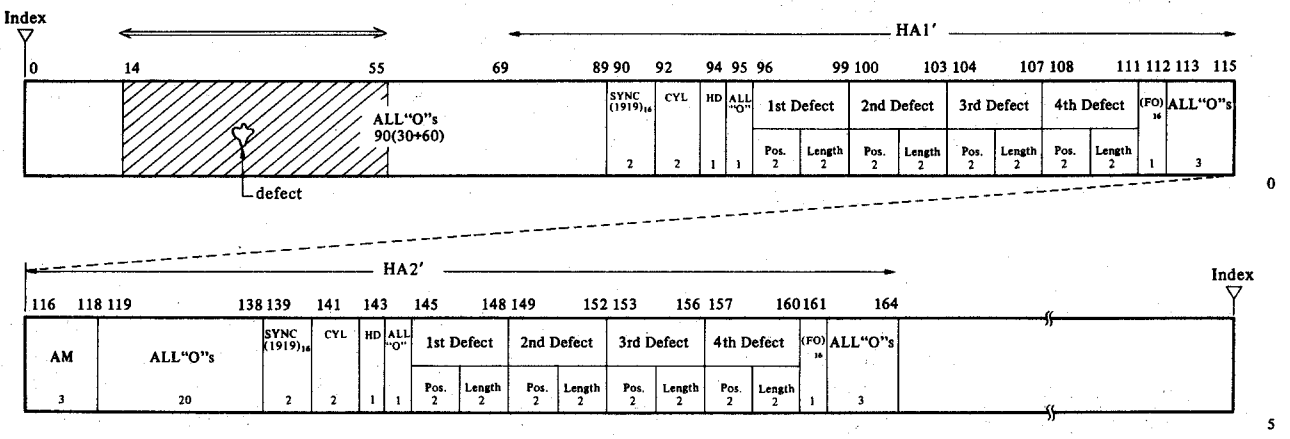


Figure 4.4.4 Format 2

If a defect is located in the region of bytes 56 - 104, the gap before the address mark is increased to 60 bytes. Figure 4.4.5 shows an example of this format.

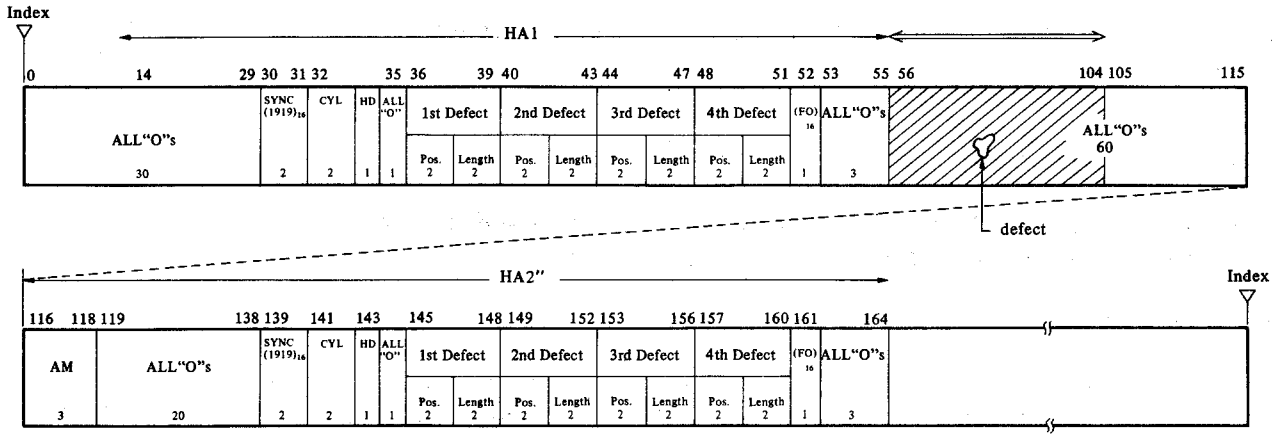


Figure 4.4.5 Format 3

In Figures 4.4.4 and 4.4.5, it is guaranteed that there are no defects in the regions where HA1 and HA2 are newly relocated due to a defect.

(4) Inspection data sheet

The location and length of media flaws are recorded in Header Areas as described in (3), as well as printed out on a sheet which is attached to each drive.

The contents of this sheet are listed below.

- Data (Year: Month: Day)
- Drive type (M2361A)
- Serial number of drive
- Serial number of DE
- Information about flaws
  - Cylinder address
  - Head address
  - Location of flaws in bytes after index mark
  - Length of flaws in bits
- Defective track address (Cylinder/Head address)
- Every perfect head address at cylinder 841
- Total number of defective tracks

4.5 Interface

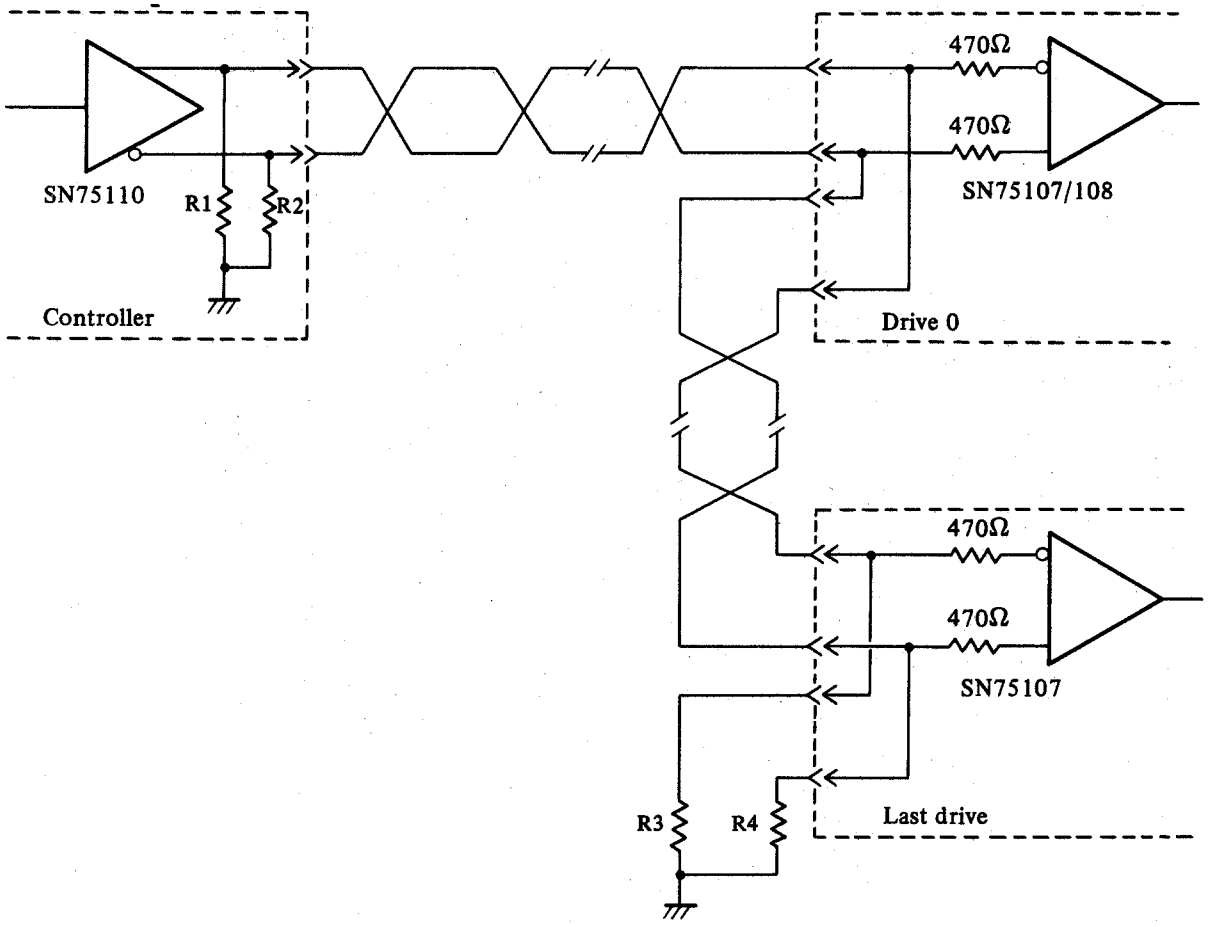
This chapter describes the physical and logical specifications of interface signals between the M2361A and any controller.

4.5.1 Signal transmission driver/receiver

SN75110 Drivers and SN75107/108 Receivers are used to provide a terminated and balanced transmission system.

(1) A-cable

All signals except Open Cable Detect and Power Sequence Pick/Hold signals must be terminated both in the drive and the controller as shown in Figure 4.5.1.



Note; (1) Line terminators are located in the drive and the controller. R1 to R4; 56 Ohms±10%, 1/10W.
(2) The maximum cable length is 100 FT (30 m).

Figure 4.5.1 Balanced transmission of A-cable

For the Open Cable Detect signal, two drivers of SN75110 would be required in parallel without termination to increase the drive current in the interface cable as shown in Figure 4.5.2.

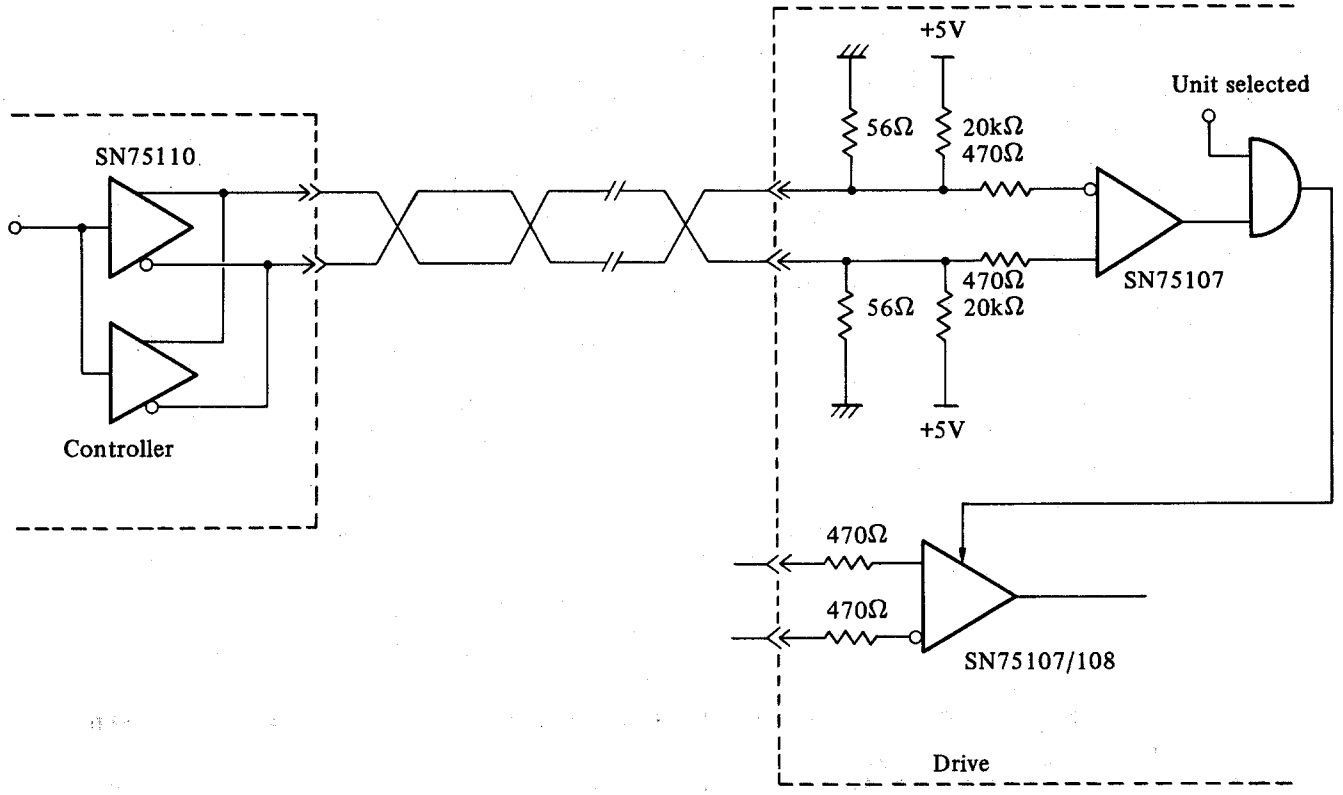


Figure 4.5.2 Open cable detect

Power Sequence Pick and Hold must be set to ground in the controller.

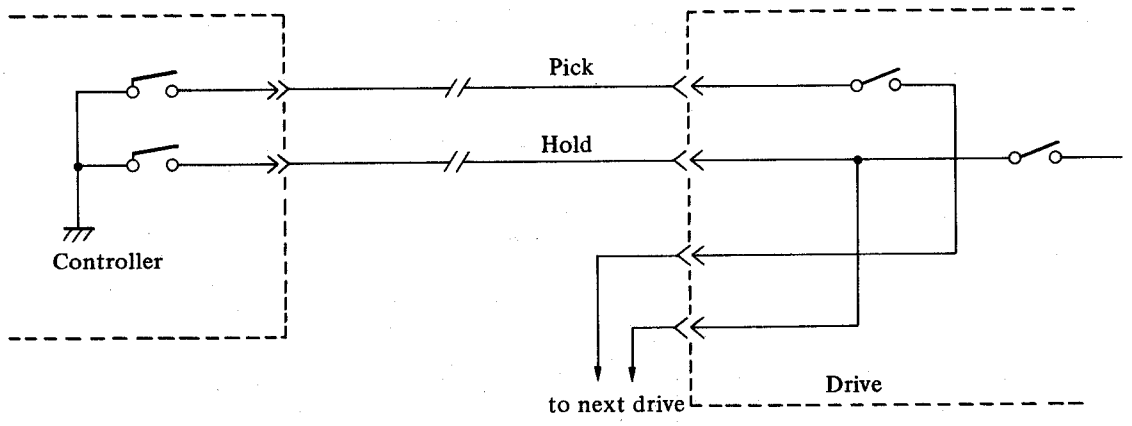
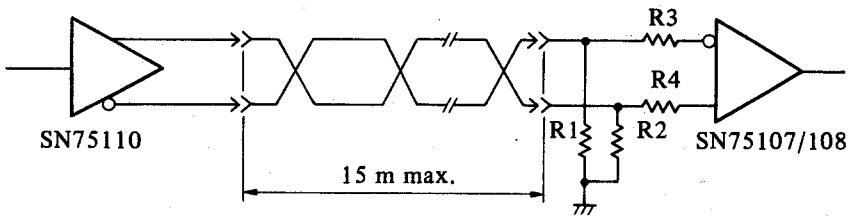


Figure 4.5.3 Power sequence pick/hold

(2) B-cable



Note: 1) The cable shall be flat with characteristic impedance of 100Ω ± 10Ω. Refer to Section 2.5 for cable usage.
2) Line terminators R1 and R2 (82Ω ±5%, 1/10W) are located on the input terminal of the disk drive.
3) Line protectors R3 and R4 (470Ω ±5%, 1/10W) are located on the control unit or the input terminal of the disk drive.
But to improve the reliability of the transmission at the high transfer rate when using ECL logic receivers, the resistors R3 and R4 of the IF WRITE CLOCK, WRITE CLOCK, WRITE DATA, READ CLOCK and READ DATA lines on the control unit and disk drive unit should be eliminated.
4) Time delay of the cable is approximately 5ns/m.
Transfer time and delay of the Receiver (SN75107) is 19ns nominal for both high and low signals.
5) To prevent false operation of the receiver, due to interface disturbances during a power failure of the unit, the bias resistors, as shown below, are used on the controller side for Unit Selected and Seek End signals.
6) Maximum cable length is 15 meters.
7) R5 and R6 (15KΩ ±5%, 1/10W) are used to prevent the receiver output signal from oscillating when input signals are both high as follows:

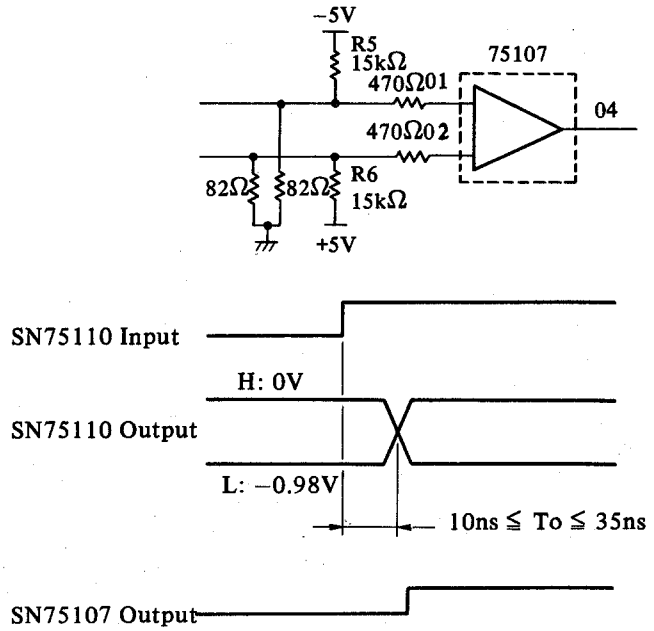


Figure 4.5.4 B-cable driver/receiver

4.5.2 Pin assignment of interface connectors.

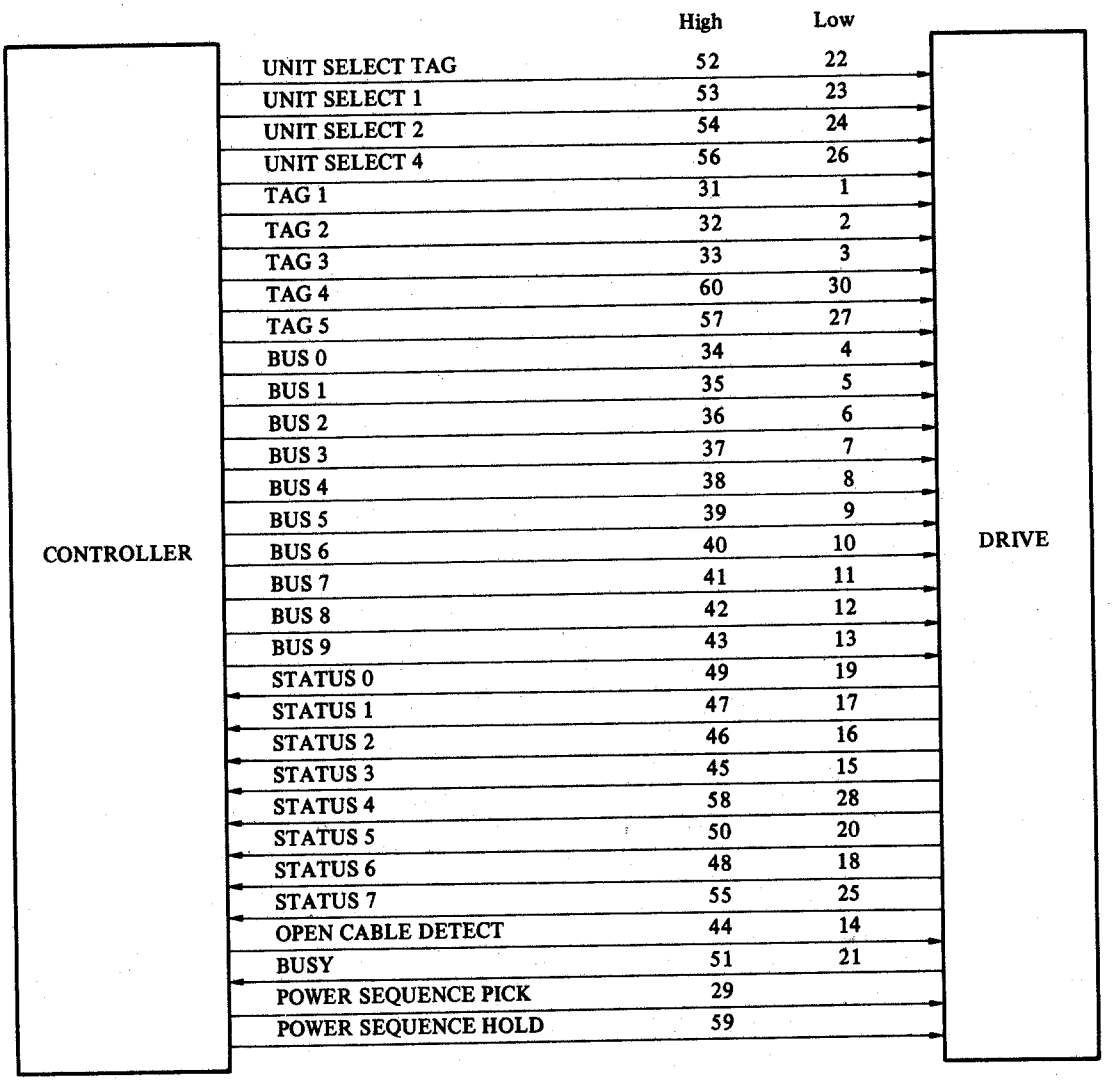


Figure 4.5.5 A-cable

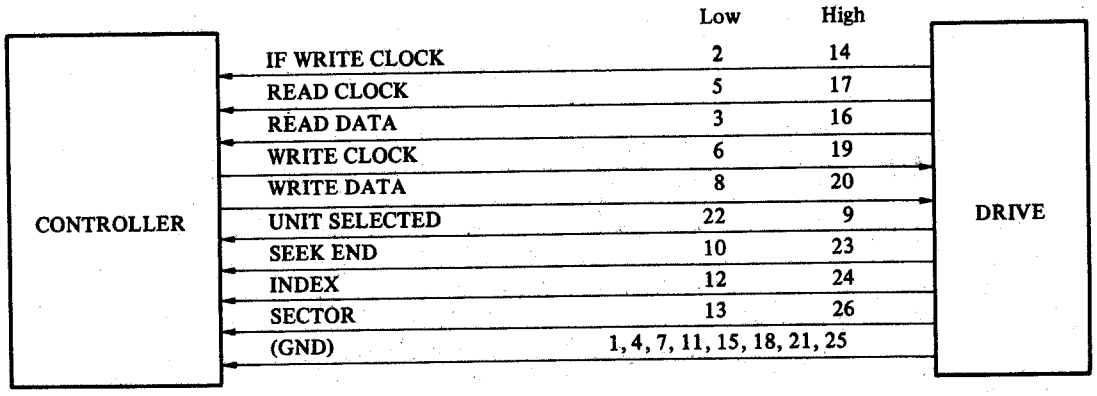


Figure 4.5.6 B-cable

4.5.3 A-cable input signals

(1) Unit Select Tag

This signal gates Unit Select 1, 2 and 4 to select the drive. Refer to timing of Unit Select (Figure 4.5.9 if dual channel option is not installed, or Figure 4.5.29 if dual channel option is installed). Elaboration of the dual channel select operation follows.

Suppose that the dual channel option is installed and the drive has been reserved by Unit Select command from channel-A, the drive is not selectable from channel-B until a Release command will be issued from channel-A or the internal 500 ms re-trigger timer times out. However, Priority Select from channel-B can interrupt the reserved status at any time. (Refer to Figure 4.5.29)

On the other hand, if the dual channel option is installed and the drive has been reserved by a Priority Select command from channel-A, channel-B cannot reserve the drive with Unit Select or Priority Select command until a Release command from channel-A is issued. (Refer to Figure 4.5.30)

(2) Unit Select 1, 2 and 4

These three signals are binary-coded to select the drive and are validated by the leading edge of Unit Select Tag. The logical number of the drive (0 through 7) is selectable by means of a switch located on the PCB (B17B-0270-0010A#U).

Table 4.5.1 Tag/Bus

Bus	Tag 1	Tag 2	Tag 3	(With Unit Select Tag)
	Cylinder Address	Head Address	Control Select	
0	1	1	Write Gate	-
1	2	2	Read Gate	-
2	4	4	Servo Offset Plus	-
3	8	8	Servo Offset Minus	-
4	16	16	Fault Clear	-
5	32	-	AM Enable	-
6	64	-	RTZ	-
7	128	-	-	-
8	256	-	-	-
9	512	-	Release*	Priority Select*

* Dual Channel only.

(3) Cylinder Address (Tag 1)

The cylinder address is set by Tag 1 and Bus 0 to 9. Throughout Tag 1, the Bus must be stable. Refer to Figures 4.5.10 and 4.5.11.
The drive must be On Cylinder prior to Tag 1. Head Addresses are specified as follows. (Storage capacity shown is unformatted)

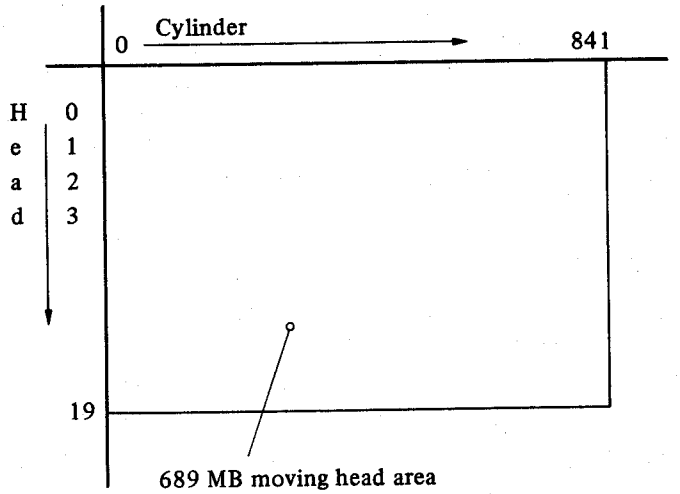


Figure 4.5.7 Mapping

Detection of Over Cylinder;
The M2361A issues both Seek End and Seek Error when illegal cylinder address (i.e., greater than 841) is issued from the controller.

(4) Head Address (Tag 2)

The head address is set by Tag 2 and Bus 0 to 4. Throughout Tag 2, Bus 0 to 4 must be stable. Refer to Figures 4.5.13 to 4.5.14.
If the Head Address transferred from the controller is equal to or more than 20, no response is generated in the drive.

(5) Control Select (Tag 3)

Bus 0 to 9 gated by Tag 3 have a different meaning in each bit. All signals are defined as control signals.

a. Write Gate (Bus 0)

Enables the write operation on the specified track. It is validated under the following conditions;

Unit Ready ..... True
On Cylinder ..... True
Seek Error ..... False
Fault ..... False
Open Cable Detect ..... True
File Protected ..... False
Servo Offset ..... False
Read Gate ..... False

If Write Gate is turned on in cases other than the above mentioned conditions, Fault occurs and the Write operation is inhibited immediately. See Figures 4.5.12, 4.5.14, 4.5.26, 4.5.27 and 4.5.28.

b. Read Gate (Bus 1)

Enables the Read operation on the specified track. It is validated under the following conditions;

Unit Ready ..... True
On Cylinder ..... True
Seek Error ..... False
Fault ..... False
Open Cable Detect ..... True
Write Gate ..... False

See the Read Gate timing chart in Figures 4.5.12, 4.5.14, 4.5.27 and 4.5.28.

c. Servo Offset Plus (Bus 2)

When this signal is true, the head is offset 100 micro-inches away from nominal On Cylinder position in the outer direction with the responses of Seek End and On Cylinder after 4.5 ms. Data cannot be written in the offset mode.
See Figure 4.5.15.
When Servo Offset Plus and Minus are sent simultaneously, Servo Offset Plus will be effective.

d. Servo Offset Minus (Bus 3)

When this signal is true, the head is offset 100 micro-inches away from nominal On Cylinder position in the inner direction with the responses of Seek End and On Cylinder after 4.5 ms. Data shall not be written while in the offset mode.
See Figure 4.5.15.

e. Fault Clear (Bus 4)

This signal clears the fault status i.e., Write/Read Check Status, however, if the cause of the Fault condition still exists, the status will not be cleared.
See Figure 4.5.16.

f. AM Enable (Bus 5)

AM Enable, in conjunction with Write Gate or Read Gate, is used in a Variable Sector Format. When AM Enable is true while Write Gate is true, an AM of three bytes (DC erase) is written on the track.
Refer to Figure 4.5.17.
When AM Enable is true while Read Gate is true, the read circuit searches for an AM of three bytes. When the AM is found, the drive will issue Address Mark Found to the controller.
See Figure 4.5.18.

g. RTZ (Bus 6)

Wherever the heads are located, they return to cylinder zero and head zero when the RTZ signal is received. This signal clears the Seek Error.
Refer to Figure 4.5.19.

h. Release (Bus 9); Dual Channel only

After the drive is reserved by Unit Select or Priority Select, Release command becomes valid at Tag 3 and Bus 9. Enabling this signal will release the reserved status in the drive, making alternate channel access possible after selection by the other channel. (Refer to Figures 4.5.29 and 4.5.30.)
If the drive has been reserved by Unit Select and the Release Timer Switch on the display panel PCB (B17B-0270-0010A#U) is set to RLTM side, the drive will automatically release the reserved condition approximately 500 ms after the Unit Select command is issued.

(6) Priority Select (Bus 9 with Unit Select Tag and Unit Select 1, 2, 4)

By sending Priority Select (Bus 9) along with Unit Select Tag, Unit Select 1, 2, 4, a controller can select the drive even if it has been selected or reserved by the other channel, except when its own channel is disabled by the Disable switch or the drive is priority selected by the other channel. With this command, the drive is set in the unconditionally reserved state with respect to that channel. Once it is unconditionally reserved, the control becomes exclusive, i.e., the other channel cannot access the drive until the drive is released from the controller which has reserved the drive. If the drive is unconditionally reserved, all the signals including Unit Selected, and Busy signals are inhibited with respect to the other channel. (Refer to Figure 4.5.30).

(7) Open Cable Detect

This signal is used to prevent damage of data caused by interface disturbances when the power to the controller is lost. Therefore, this signal must be stable when the controller is available, and must be disabled before logic levels decay on the interface when a power failure occurs in the controller.
Refer to Figure 4.5.20.

(8) Tag 4 and 5

Unit Status, Sector Status, Write/Read Check Status and Access Status can be sensed throughout Status 0 ∿ 7 lines with a combination of those two coded signals. Status 0 to 4 for Unit Status are always displayed by 5 LEDs and Status 0 to 7 for DE Sequence State, Write/Read Check State and Access State are also displayed by 7-segment LEDs on the PCB (B17B-0270-0010A#U) for maintenance aid.
See Table 4.5.2 for information about these Tags.
Note that Unit Status can always be on the interface by shorting a circuit on the Logic PCB (C16B-5327-0290#U) with a shorting plug. See Figure 4.5.21 for time specifications.

(9) Power Sequence Pick/Hold

Power Sequence is required when the Remote/Local switch on the display panel PCB (B17B-0270-0010A#U) is set to Remote. In this mode, when the controller sets the Pick and Hold lines to ground, the first drive's spindle starts rotating if the start switch has been pressed. Approximately five seconds later the Pick signal is sequenced up. When both signals go false, the spindle stops rotating. If the mode switch on the display panel PCB is set to Local, each Start Switch must be pressed manually to start the spindle rotating. Refer to Figure 4.5.22.

4.5.4 A-cable output signals

(1) Status 0 to 7

The Status 0 to 7 lines indicate status information determined by combinations of Tag 4 and Tag 5 signals. Information available is specified in Table 4.5.2.

Table 4.5.2 Status

Tag 4	False	True	False	True
Tag 5	False	False	True	True
Status	Unit Status	Sector Status	Write/Red Check Status	Access Status
0	Unit Ready	Sector 1	Index Check	DE Sequence Check
1	On Cylinder	Sector 2	Control Check	Access Time-Out Check
2	Seek Error	Sector 4	Multi Head Check	Over Shoot Check
3	Fault	Sector 8	Head Short Check	Rezero Mode Latch
4	Write Protected	Sector 16	Write Current on Read Check	Servo Latch
5	Address Mark Found	Sector 32	Write Transition Check	Linear Mode Latch
6	Index	Sector 64	Delta I Write Check	Control Latch
7	Sector	Sector 128	Servo Off-Track	Wait Latch

(2) Unit Status

When both Tag 4 and 5 are False, Status 0 ∿ 7 indicate the basic information required for the Seek, Read and Write operations.

a. Unit Ready (Status 0)

When this signal is true and the drive is selected, this signal indicates that the drive has reached the rated speed. Note that when the drive is in fault condition, Unit Ready may or may not be issued depends on the position of a jumper plug as described in Table 3.5.1.

b. On Cylinder (Status 1)

Indicates that the heads are located on the specified track. This signal goes false for approximately 4.5 ms at the beginning and at the end of the offset operation. For a zero Track Seek, On Cylinder will go false for max. 10 μs.
Refer to Figures 4.5.11 and 4.5.15.

c. Seek Error (Status 2)

Indicates that a Seek Error has occurred. In this case, On Cylinder does not go true. The Seek Error is cleared when a RTZ (Tag 3 and Bus 6) is received or by pushing the Fault Clear Switch on the operator panel or maintenance-aid MRTZ Switch on the PCB (B17B-0270-0010A#U). The Seek Error status is defined as follows;

1. Seek or RTZ operation is not completed within the specified time.
2. Heads travel to a position outside the recording area.
3. An illegal cylinder address is issued to the drive.
4. Head overshoots to an unspecified cylinder address.
5. Seek command is received by the drive during the not On Cylinder status, when the heads are in motion, or during a Write/Read operation.

d. Fault (Status 3)

Indicates that a fault condition for Write/Read operation exists in the drive. Fault conditions are described in the Write/Read Check status in detail.
If one of the Fault conditions occurs, writing is immediately inhibited and the Fault signal is issued to the controller. The Fault status can be cleared by one of the following operations;

1. Fault Clear on Tag 3 and Bus 4
2. Fault Clear switch on the operator panel
3. Pushing on the maintenance-aid MRTZ Switch on the PCB (B17B-0270-0010A#U).
4. Switching off the power to the drive
5. Stopping rotation of the spindle motor

Fault Status turns on the fault lamp on the operator panel.

e. Write Protected (Status 4)

Indicates that the drive is in the write-protected mode. The write-protect function is enabled by the File Protect Switch on the operator panel, and becomes active while the drive is not selected. If the drive is selected and the write-protect-function is desired, the drive must be momentarily deselected.

f. Address Mark Found (Status 5)

Address Mark Found is 8-Byte pulse which is sent to the controller at least 2 Bytes after the recognition of a 3-Byte DC-erased area.

g. Index (Status 6)

Index mark is derived from the servo information. It occurs once per revolution and is used for reference in Write/Read operation.
Refer to Figure 4.5.23 for the timing of Index and Sector.

h. Sector (Status 7)

The Sector mark is also derived from the servo information. The number of sectors per revolution is selectable by 16-Bit DIP switches and is determined by counting Byte Clock. The DIP switches are located on the PCB B17B-0270-0010A#U. Each switch represents a binary number minus 1 of Byte Clock to be counted in each sector.

(3) Sector Status (Status 0 ∿ 7)

Indicates the current sector address from 1 to 255 in the drive. Refer to Figure 4.5.23 for timing of Sector Address.

(4) Write/Read Check Status

Indicates the fault status while in the Write or Read operation. When one of these conditions occurs in the drive, the Fault signal in the Unit Status is issued as a summary to the controller. It can be cleared by Fault Clear Signal from the controller.

a. Index Check (Status 0)

Indicates that the Index signal is not detected where it should be or was detected where it should not have been while performing Write/Read operations.

b. Control Check (Status 1)

The following fault conditions cause Control Check.

1. Write and Read Gate are issued at the same time.
2. Write operation during offset mode.
3. Write Gate is issued in the write protect mode.

c. Multi-Head Check (Status 2)

Indicates that two or more head ICs are selected simultaneously.

d. Head Short Check (Status 3)

Indicates that abnormal current was sensed in the Write Select line during write operation.

e. Write Current on Read Check (Status 4)

Indicates that write current was sensed during a read operation.

f. Write Transition Check (Status 5)

Indicates that write current has not been switched for writing data. The detection is continued from byte-8 after Write Gate is true until the end of the Write operation.

g. Delta I Write Check (Status 5)

Indicates that an abnormal write current was sensed in the inner head or outer head.

h. Servo Off-Track (Status 7)

Indicates the following fault conditions.

1. The head is ±100 micro-inches off the desired track during the Write/Read operation.
2. Write/Read Gate is received by the drive during not On Cylinder status, heads in motion or seek error.

(5) Access Status

Indicates access status of the head in Seek and RTZ operation. It also indicates start and stop sequence of the spindle motor.

a. DE Sequence Check (Status 0)

Indicates that an abnormal start/stop sequence of the DE occurred in the drive. Latch 4, Latch 2, and Latch 1 of DE SEQ represent the various DE sequence status as shown in the Table 4.5.3.

One of the following errors occurred as DE Sequence State advanced:

1. Initial State Good (Motor At Speed and Hall Alarm not present) does not result in State 1.
2. Run State Good (not Hall Alarm and Motor At Speed are sent out) cannot be obtained for approximately 40 seconds in State 3.
3. Run State Good goes off during State 6.

It cannot be cleared by the Fault Clear Switch on the operator panel or Fault Clear signal on the interface but only by stopping rotation of the spindle.

Table 4.5.3 Contents of DE Sequence Latches

State No.	Latch 4	Latch 2	Latch 1	Status
0	0	0	0	Wait status
1	0	0	1	The START/STOP switch on the operator panel is set to START.
3	0	1	1	The spindle motor starts rotating.
2	0	1	0	Sequence Rezero starts approximately 40 seconds after State 3.
6	1	1	0	Sequence Rezero is completed and seek operation is possible.
7	1	1	1	DE Stop Sequence State results and the head begins to return to the home position. (Go Home)
5	1	0	1	Go Home operation is completed and the spindle motor stops rotating.
4	1	0	0	Approximately 40 seconds have passed since State 5. (Returns to State 0.)

b. Access Time-Out Check (Status 1)

During an RTZ or Seek operation, On Cylinder failed to appear within 250 ms ±30% after Access Start. It can be cleared by RTZ operation.

c. Over-Shoot Check (Status 2)

Indicates the heads go past the desired track during Seek or RTZ operation or go into the Guard Band or ID Position during a Seek operation.
It also indicates that the heads are moving at abnormal speed during RTZ operation.
Over-Shoot Check can be cleared by RTZ operation.

d. Rezero Mode Latch (Status 3)
Servo Latch (Status 4)
Linear Mode Latch (Status 5)
Control Latch (Status 6)
Wait Latch (Status 7)

The five latches observe the sequence of seek and RTZ operations. Whenever an error occurs during seek or RTZ, the content of these latches are frozen at that time, so that they are beneficial for error analysis. They can be cleared by RTZ operation. The relationship between access state and the contents of latches is shown in Table 4.5.4.

Table 4.5.4 Access states

Rezero Mode Latch	Servo Latch	Linear Mode Latch	Control Latch	Wait Latch	State	Mode
0	0	0	0	1	Wait State	Reset
0	0	0	0	0	State RTZ	RTZ
1	0	0	0	0	Move In	
1	0	0	1	0	Turn Around	
1	0	1	1	0	Move Out	
0	0	1	1	0	RTZ Linear Mode	
0	1	1	1	0	On Track	
0	1	0	1	0	Accelerate	Seek
0	1	0	0	0	Decelerate	
0	1	1	0	0	Seek Linear Mode	
0	1	1	1	0	On Track	

(6) Busy (Dual Channel only)

If the drive has been already reserved and/or selected, a Busy signal will be issued together with Unit Selected to the other channel attempting the select. Busy signal will remain true until Unit Select Tag is dropped or the Busy condition in the drive is released.
It is necessary to gate Busy signal by Unit Selected signal at the controller.

4.5.5 B-cable input signals

(1) Write Data

Carries NRZ data which is to be written on the disk surface and must be synchronized with Write Clock. Refer to Figure 4.5.24.

(2) Write Clock

Write Clock is a return signal of the IF Write Clock issued from the drive as shown in Figure 4.5.8, and must be synchronized with the NRZ Write Data.
Refer to Figure 4.5.24.

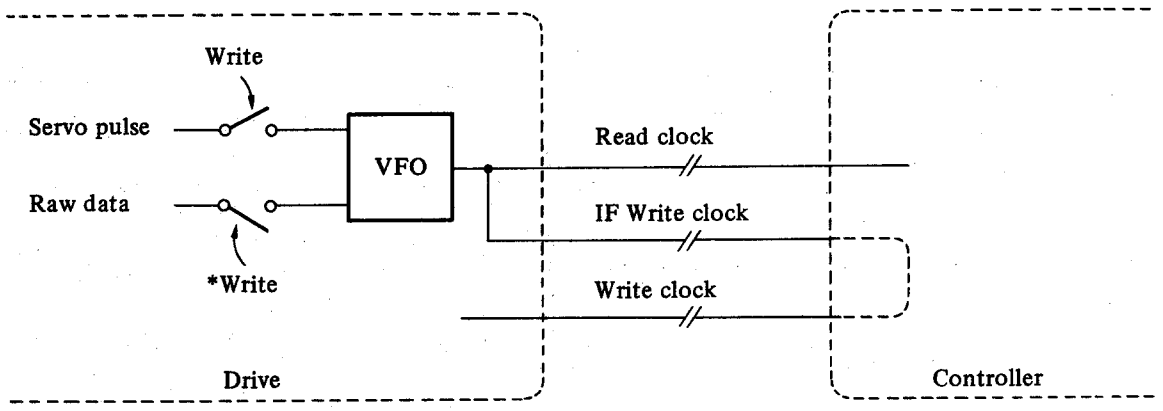


Figure 4.5.8 Generation of write/read clock

4.5.6 B-cable output signals

(1) If Write Clock

Used by the controller to synchronize Write Data and Write Clock. It is synchronized to the Servo Pulse while in the Write operation and to the Raw Data during a Read operation. Refer to item (1) of Section 4.5.5 and Figure 4.5.24.

(2) Read Data

Transmits the recovered data in the form of NRZ data synchronized with the Read Clock. Refer to Figure 4.5.25.

(3) Read Clock

Transmits Read Clock which defines the beginning of a bit cell. The Read Data is synchronized with the Read Clock. Refer to Figure 4.5.25.

(4) Unit Selected

When three Unit Select lines match with the logical address of the drive, and the leading edge of Unit Select Tag is received, the Unit Selected goes true and is issued to the controller. This signal activates all signals in the A-cable. Refer to Figure 4.5.9.

(5) Seek End

In a combination with On Cylinder or Seek Error, Seek End goes true after a Seek or RTZ, indicating that a Seek or RTZ operation has terminated. Seek End goes false for 4.5 ms at the beginning and end of an Offset operation in default mode. In the other mode, Seek End never goes false at resetting offset as described in Table 3.5.1.
For Zero Track Seek, it will go false for max. 10 μs. Note that Seek End and On Cylinder do not change when a fixed head is selected. Refer to Figures 4.5.10, 4.5.11, 4.5.13, 4.5.15 and 4.5.19.

In case of dual channel sub-system, Seek End is always true to the other channel (unselected channel). Suppose that channel-A attempts to select the drive which has already been selected by channel-B. When channel-B releases Selected and Reserve Condition, Seek End goes false for approximately 30 μs for channel-A which has been waiting.

(6) Index

Same as Index signal in the A-Cable which is described in item (2)-g. of Section 4.5.4. This signal is available with or without the dual channel feature.

(7) Sector

Same as Sector signal in the A-Cable which is described in item (2)-h. of Section 4.5.4. This signal is available with or without the dual channel feature.

4.5.7 Time specifications

Timings are specified at the connector position of the drive. It is necessary for signal timings to consider both the delay time of the interface cable and the circuit of the controller.

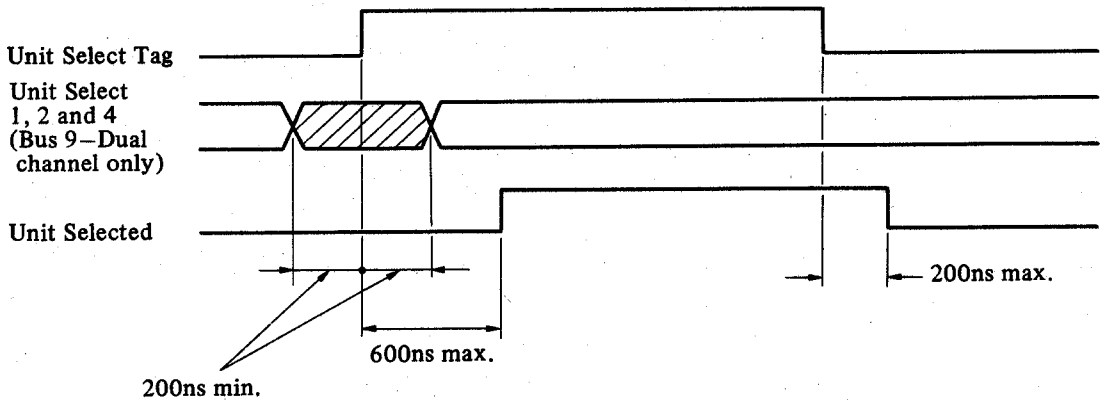
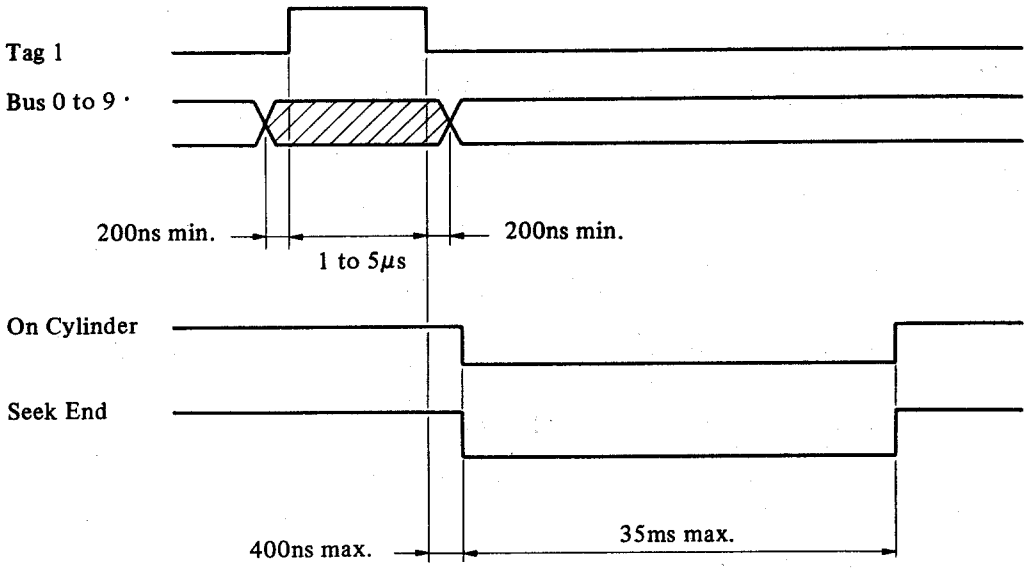


Figure 4.5.9 Unit Select timing



Note: The cylinder address must be less than 841 to select a movable head.

Figure 4.5.10 Seek timing

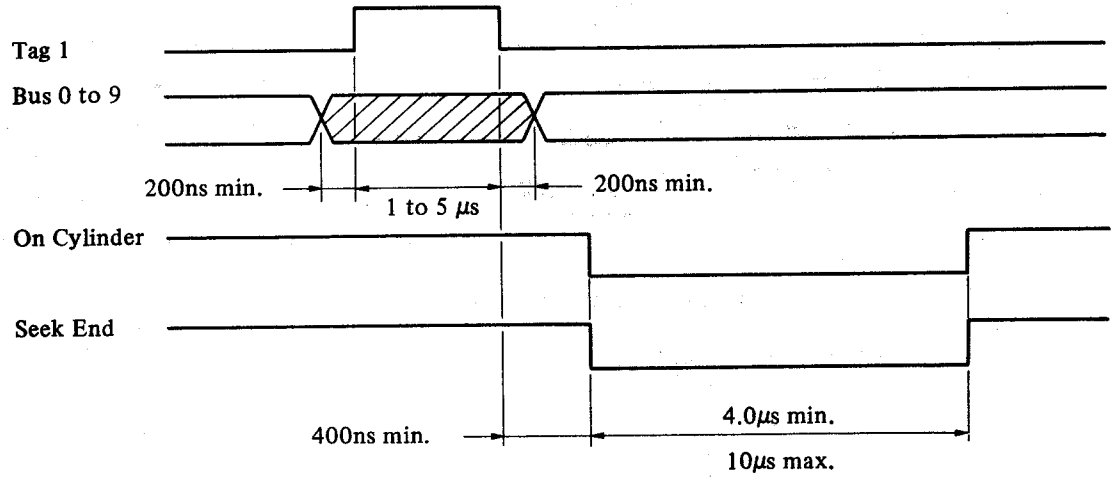


Figure 4.5.11 Zero Track Seek timing

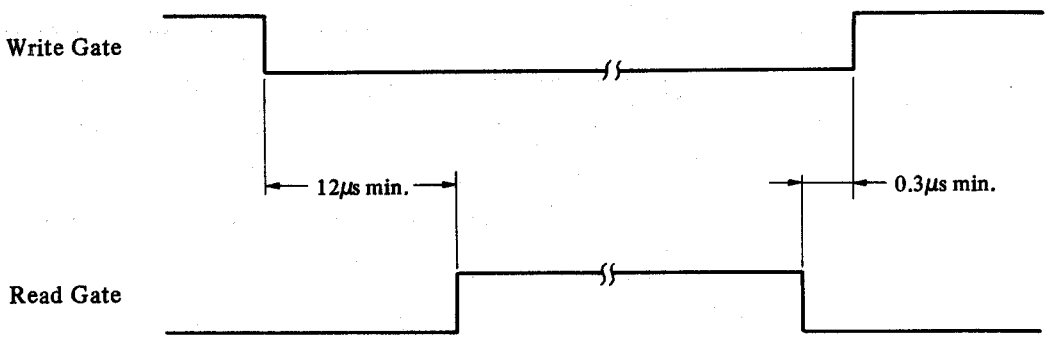
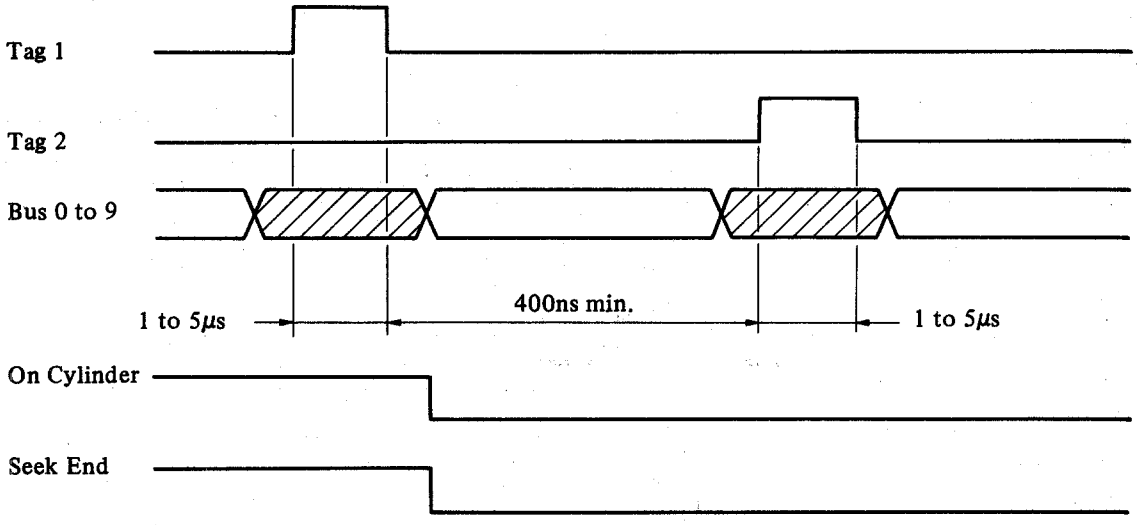


Figure 4.5.12 Read after Write and Write after Read timing



Note: Tag 2 can be set during seek operation.

Figure 4.5.13 Addressing for movable head

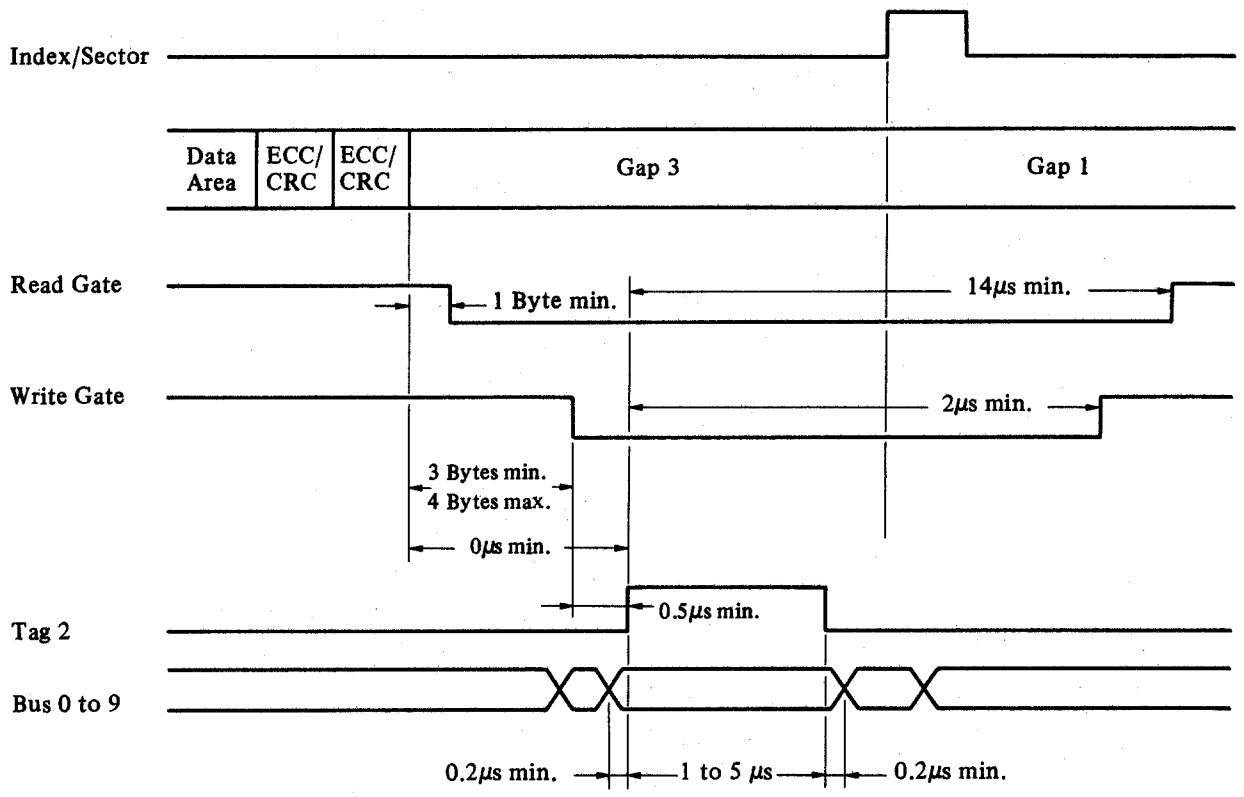
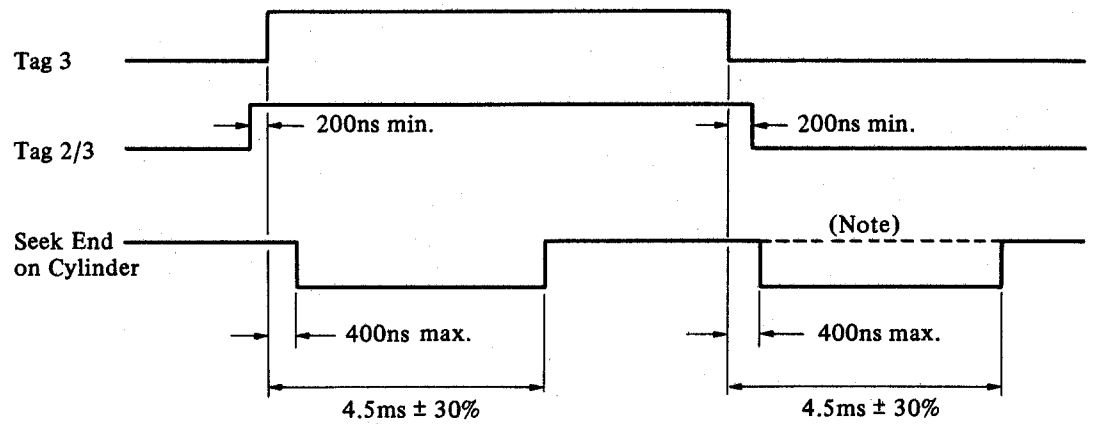


Figure 4.5.14 Head address change at the last gap



Note that Seek End does not go false at offset-reset operation depending on the position of a jumper plug as described in Table 3.5.1.

Figure 4.5.15 Offset timing

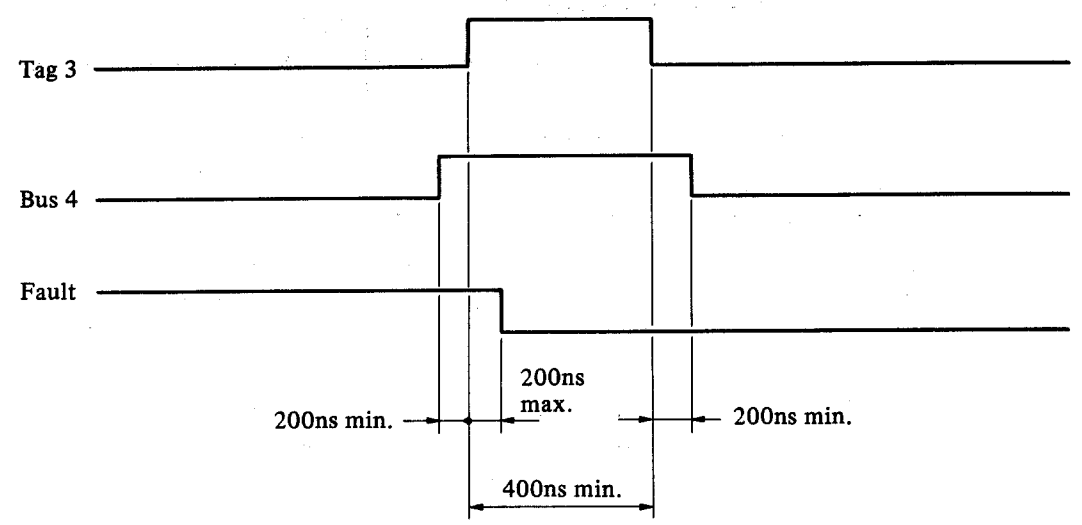


Figure 4.5.16 Fault Clear timing

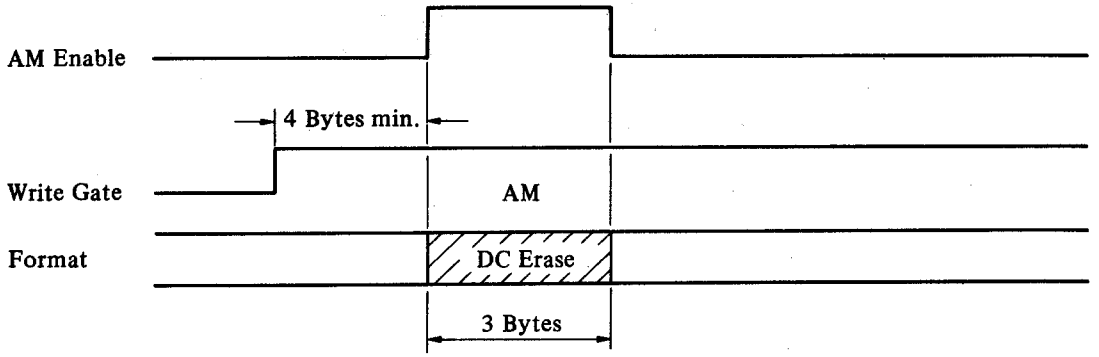


Figure 4.5.17 AM Write

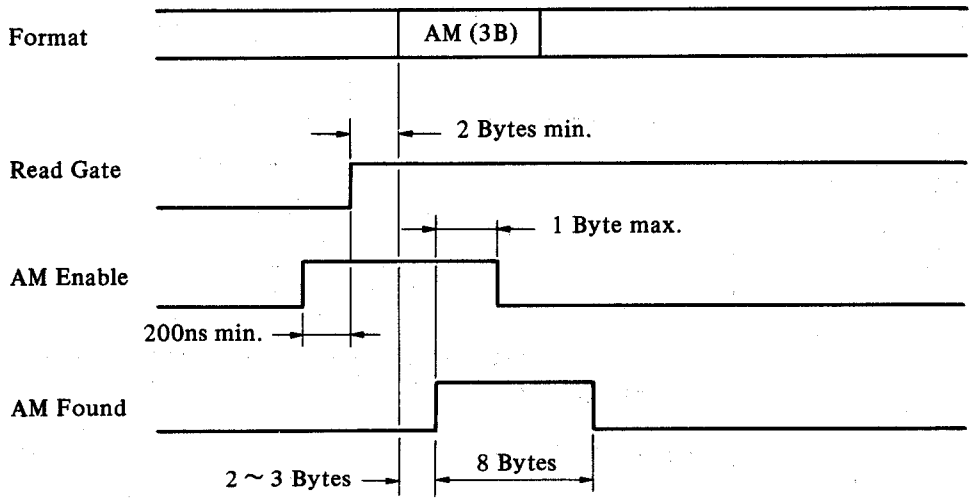
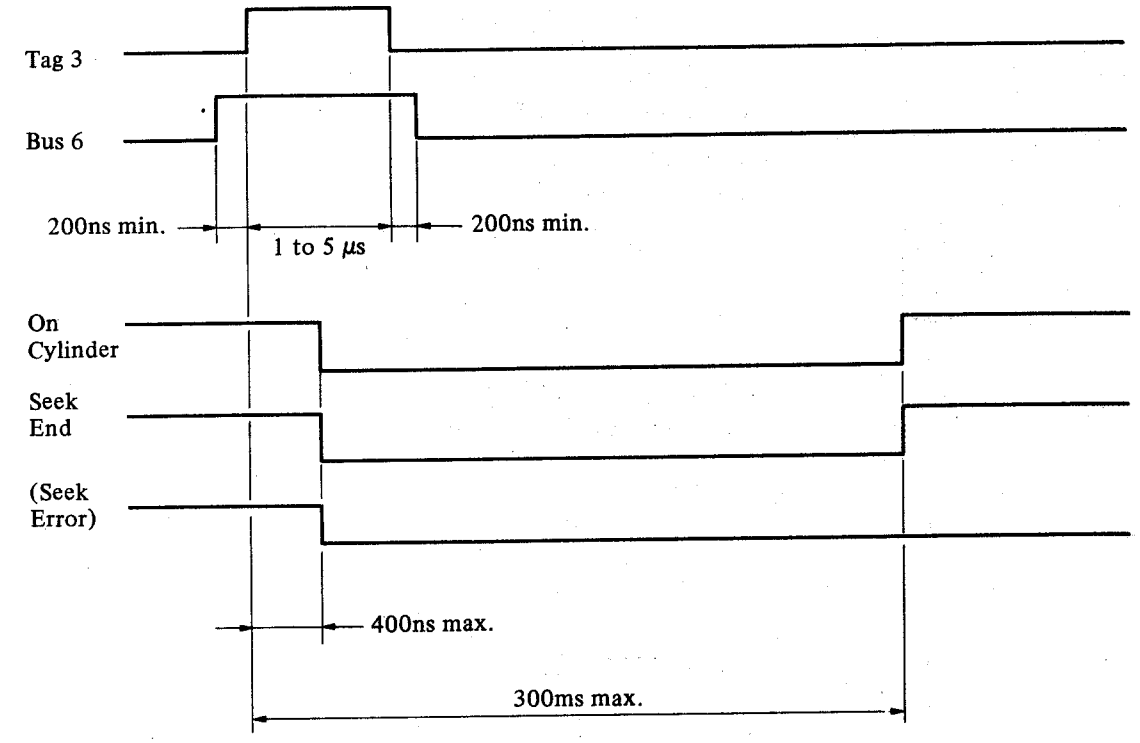
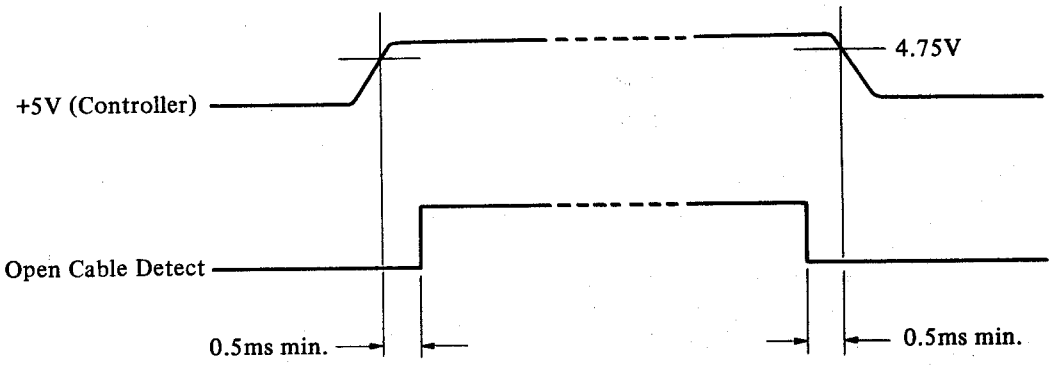


Figure 4.5.18 AM Detection



Note: On Cylinder is not always set if Seek Error occurs.

Figure 4.5.19 RTZ timing



Note: Two Drivers of SN75110 would be required in parallel without termination to increase the drive current in the interface cable.

Figure 4.5.20 Open Cable Detect timing

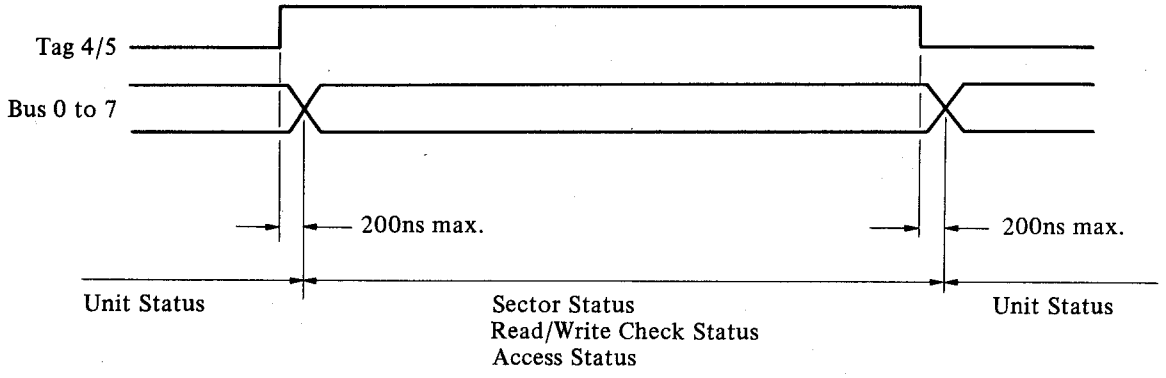


Figure 4.5.21 Tag 4/5 timing

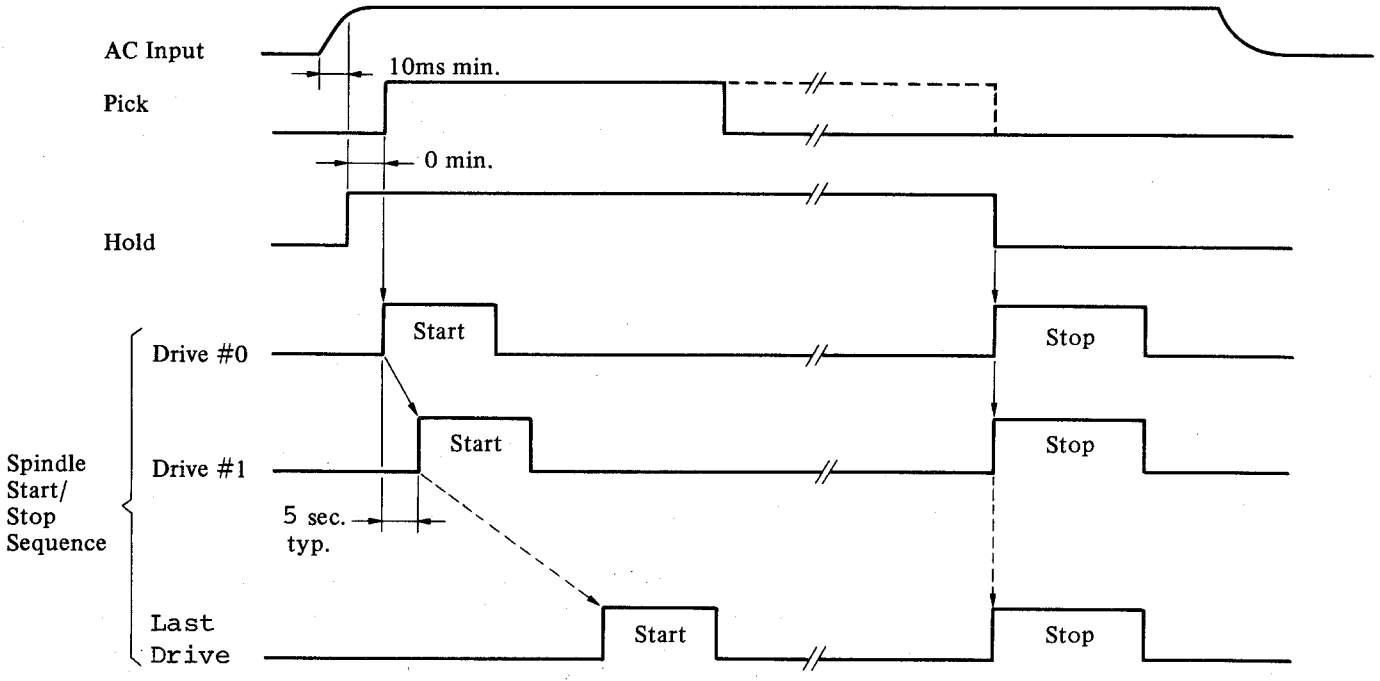


Figure 4.5.22 Power sequence Pick/Hold timing

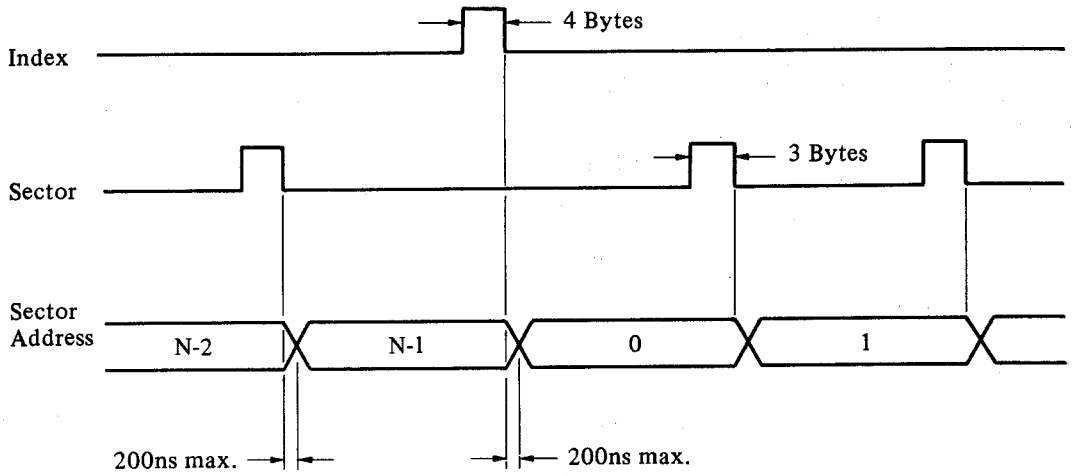
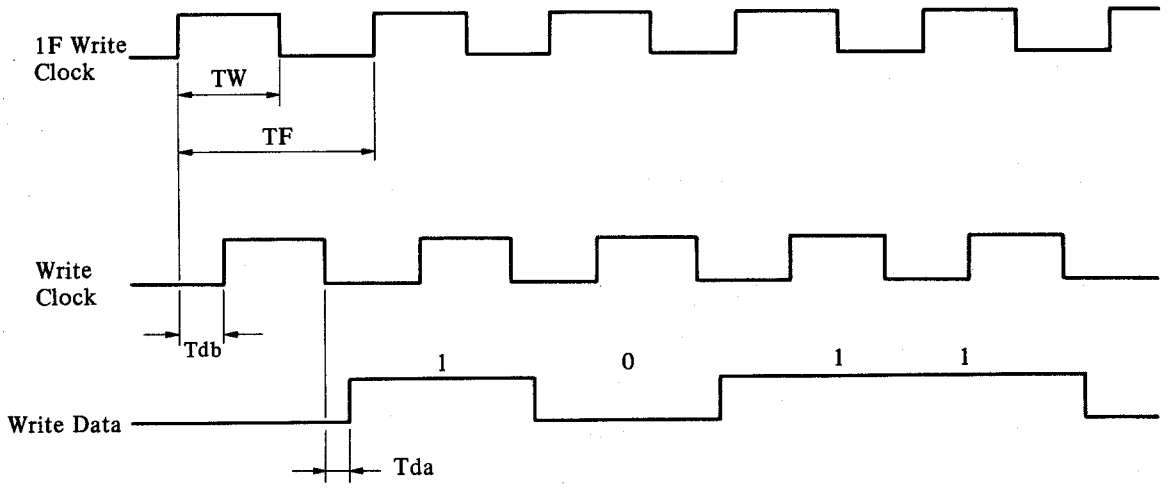


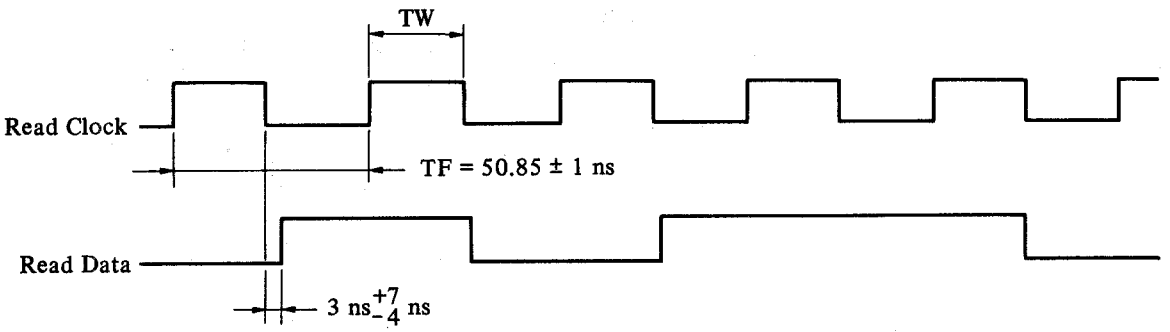
Figure 4.5.23 Index and Sector timing



TW = TF/2 = 25.43 ±2 ns
TF = 50.85 ±2 ns
Tdb = Continuous delay within 2 bits
Tda = 0 ±10 ns

Note: (1) Write Data and Write Clock timing shall be specified at the output connector of the controller.
(2) The tolerance of TF includes the rotational speed tolerance and the jitter of servo signal.
(3) NRZ Write Data issued from the controller is put in to the RLL-Encoder and then written on the disk surface with write-compensation.

Figure 4.5.24 Write Clock and Write Data timing



TW = TF/2 = 25.43 ±5 ns

Note: (1) Read Clock and Read Data timing shall be specified at the output connector of the drive.

(2) Read Data signal should be clocked at the positive-going edge of Read Clock in the controller. The high speed IC (ex. shottky type) should be used for the clocking circuit (ex. ser/des circuit ECC/CRC circuit) in the control unit.

Figure 4.5.25 Read Clock and Read Data timing

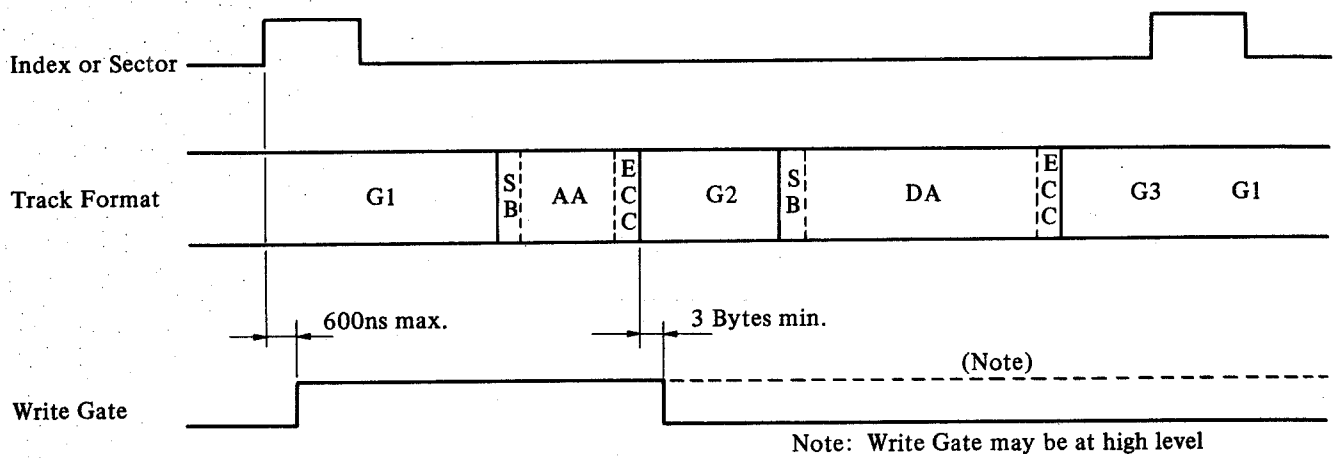
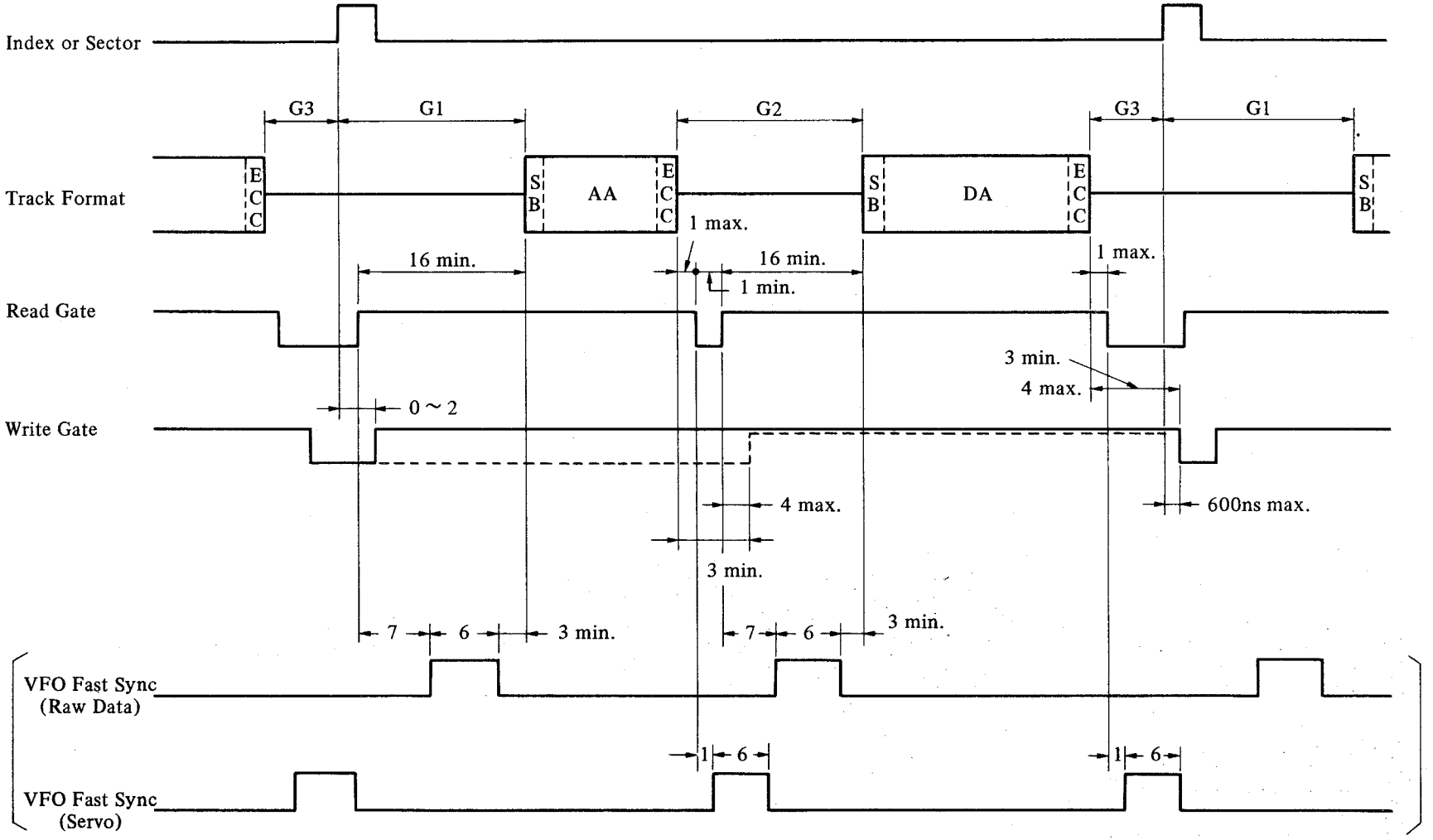
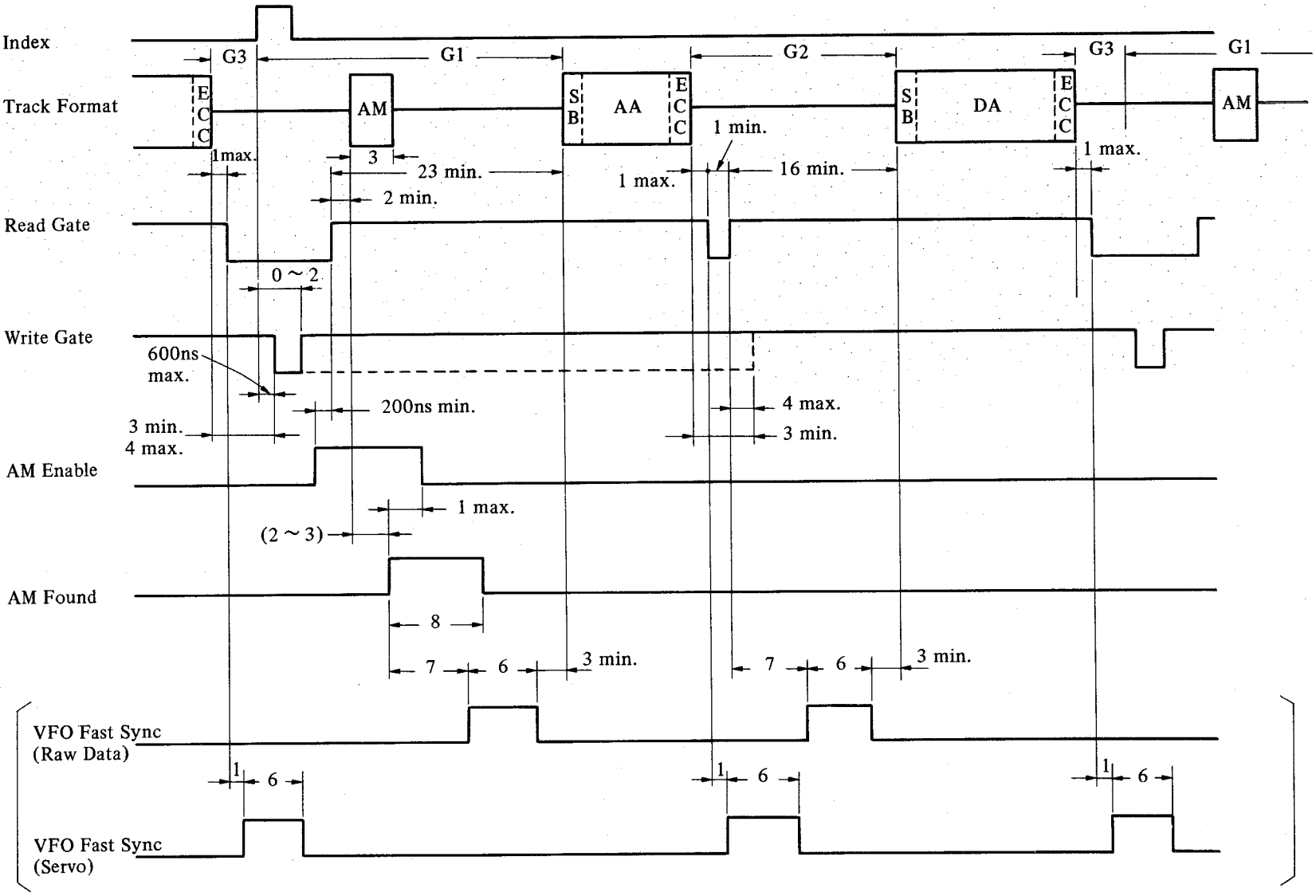


Figure 4.5.26 Format Write timing



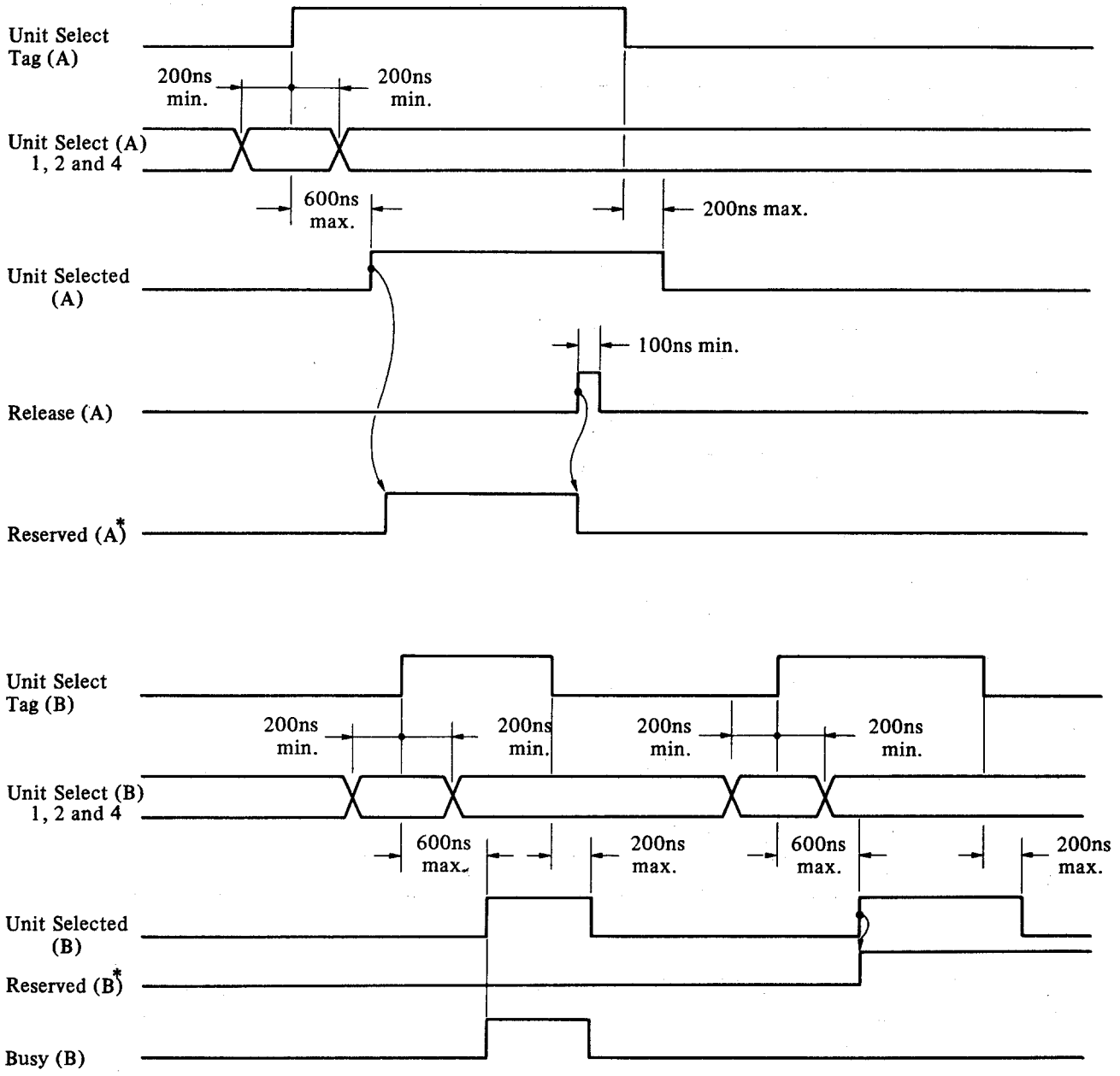
* Unit: Byte
* Not including head switching time, read-after-write and write-after-read transient time.
* VFO Fast Sync (Raw Data and Servo) are signals in the drive.

Figure 4.5.27 Fixed Sector Format timing



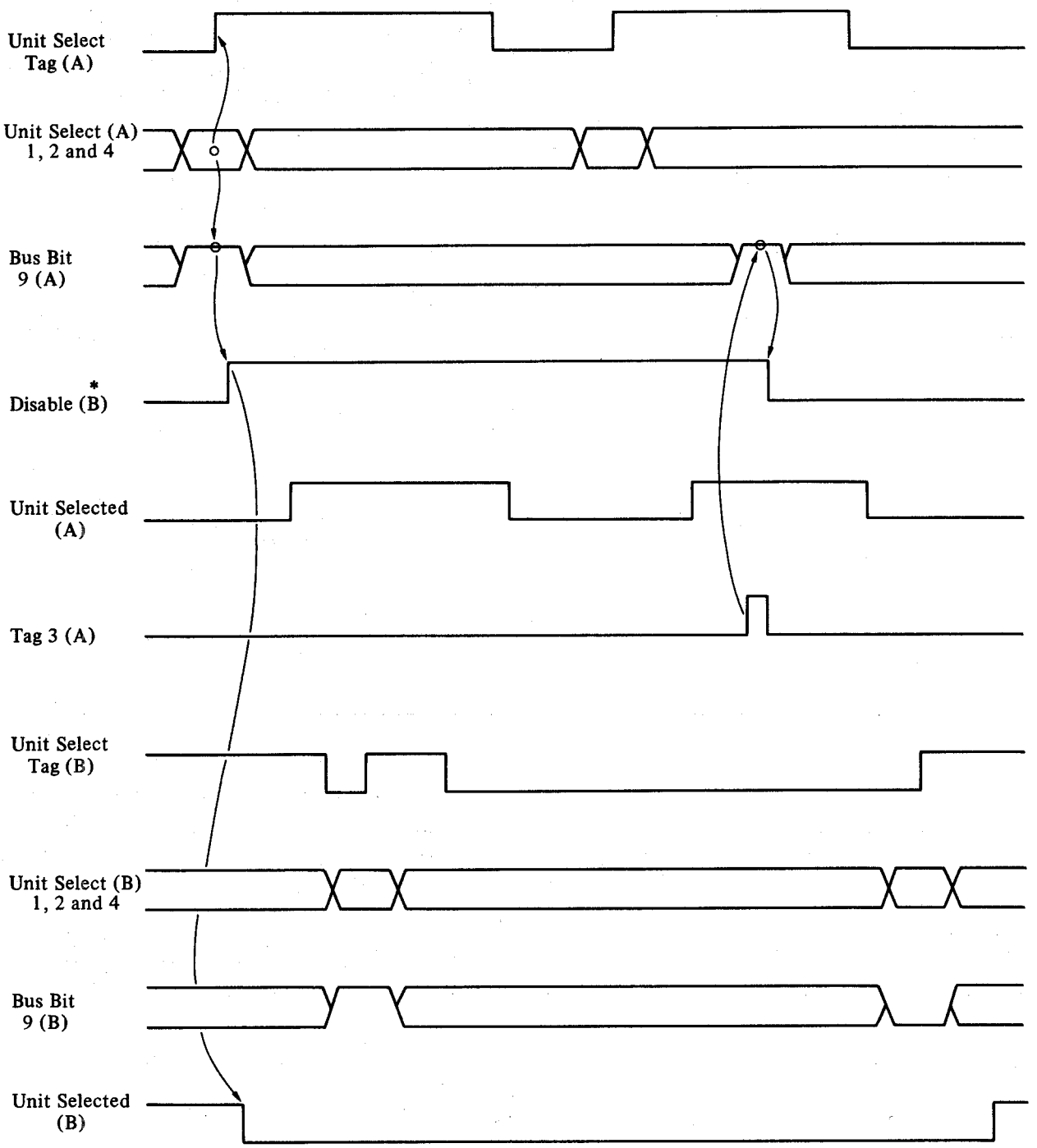
* Unit: Byte
* Not including head switching time, read-after-write and write-after-read transient time.
* VFO Fast Sync (Raw Data and Servo) are signals in the drive.

Figure 4.5.28 Variable Sector Format timing



Note: Reserved (*) is a signal within the drive.

Figure 4.5.29 Unit Select timing (Dual channel only)



Note: (1) Disable (*) is a signal within the drive.
(2) A sequence example of the above is as follows:
Channel B Select → Channel A Priority Select
→ Channel B Priority Select Try → Channel A Release
→ Channel B Select

Figure 4.5.30 Priority Select sequence (Dual channel only)

4.6 Electrical Circuit Function

4.6.1 Introduction

This section describes electrical circuit functions of the Logic Circuit, Servo Circuit and R/W Circuit.

Figure 4.6.1 shows the functional block diagram.

4.6.2 Logic circuit

(1) DE Sequence Control

The drive can execute instructions (TAG1, TAG2, TAG3) sent from the controller after the START switch on the operator panel is set to ON, the disk comes up to the rated speed, the head is moved from the CSS area to cylinder 00 (hereafter called sequence RTZ), and the drive becomes ready. The operations performed between the moment the START switch is set to ON and the moment the drive becomes ready is called the DE Start Sequence. When the START switch is set to OFF, the drive stops the rotation of the disk after the head is moved to the CSS area. The operations performed between the moment the START switch is set to OFF and the moment the disk stops is called the DE Stop Sequence.

Each of these sequences is divided into several states (five states for the DE Start Sequence, and three states for the DE Stop Sequence), which are determined by decoding DE sequence latches 1, 2, and 4 (hereafter called DESQL1, DESQL2, and DESQL4) and are named states 0 to 7 (hereafter called ST0 ∿ ST7). Figure 4.6.2 shows the states of a drive.

These DE sequences can be monitored by the LEDs on the panel.

a. DE Start Sequence States

(a) State 0

When power is turned on, DESQL1, DESQL2, and DESQL4 are reset by the Initial Reset signal (PWRST).

(b) State 1

When the START switch on the operator panel is set on ON in state 0 (STARTS is set high), the start latch (STARTL) is set and DESQL1 is set. At this time, if the Initial Good signal is low (INSTG = Hall Alarm signal is low (*HALRM) and Motor Speed signal is low (*MTRSP)), the DE sequence check latch (DESQCKL) is set, DESQL1 is reset, and the operation returns to state 0. When the START switch is set to ON again (OFF → ON), DESQCKL is reset and the operation enters state 1.

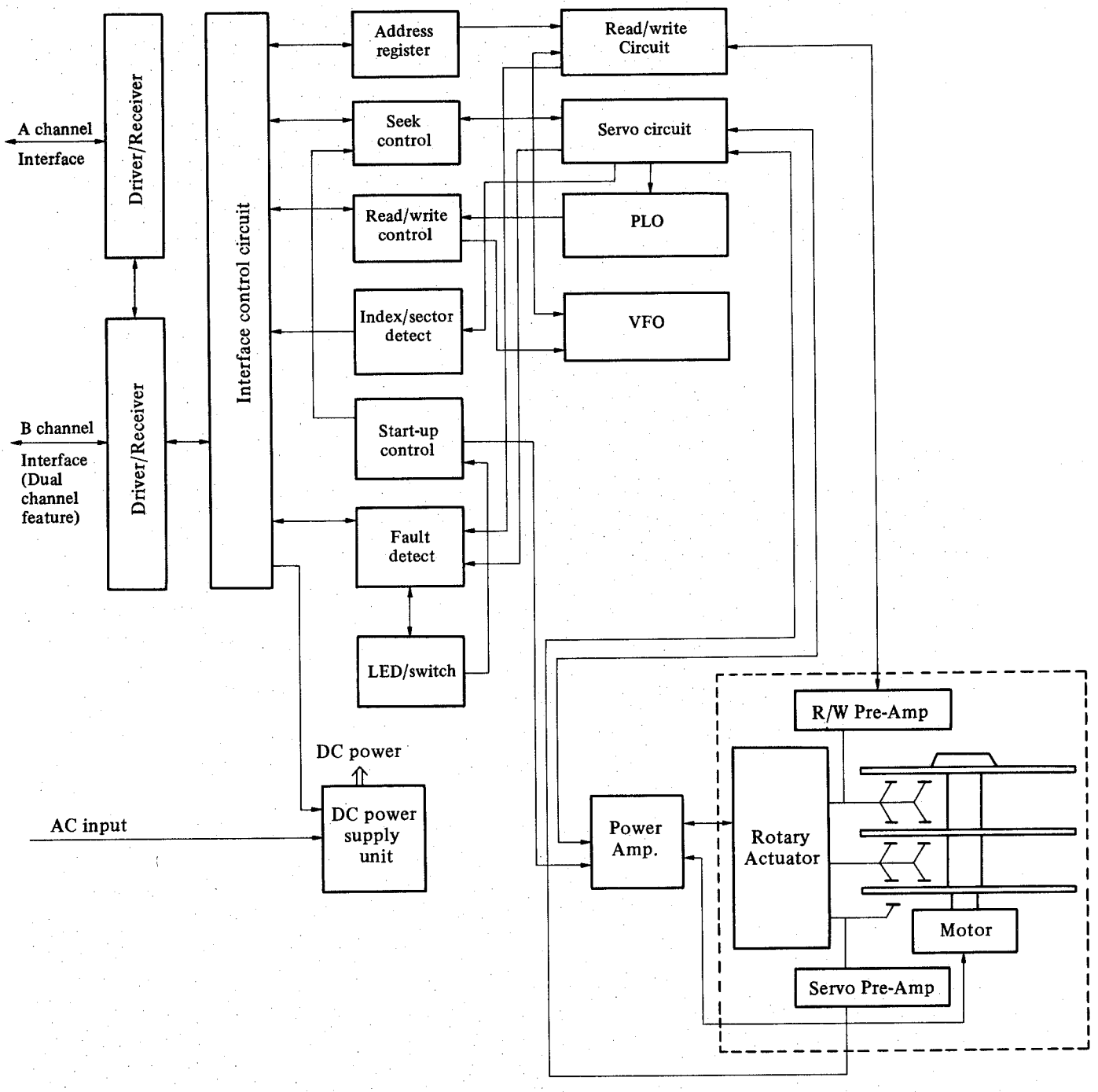


Figure 4.6.1 Functional block diagram

(c) State 3

When the INSTG state occurs, DESQL1 and DESQL2 are set in this order and the operation enters state 3. When DESQL2 is set, the disk starts rotation. When the state 3 signal (ST3) goes high, the Start Timer signal (STTMR) is set high, causing the timer to be started. If the Run State Good signal (RNSTG = *HALRM* MTRSP) remains low about 60 seconds after it has started (EN60S), DESQCKL and DESQL4 are set and the operation enters state 7.

(d) State 2

If RNSTG is high when EN25S is high in state 3, DESQL1 is reset and the operation enters state 2.

The state 2 signal (ST2) goes high, causing the sequence RTZ (SQRTZ) operation to be started.

(e) State 6

The interrupt signal (ACCMP) generated upon completion of the SQRTZ operation sets DESQL4 and the operation enters state 6. In this state, the Unit Ready signal may be sent to the controller.

If one of the following conditions occur during state 6, DESQL1 is set and the operation enters state 7:

1 The START switch on the operator panel is set to OFF.
2 The MTRSP signal goes low.
3 The HALRM signal goes high.

b. DE Stop Sequence States

(a) State 7

When the state 7 signal goes high, the ANGHM signal is set high, causing the head to start moving to the CSS area (GO HOME).

(b) State 5

The interrupt signal (GHCMP) generated upon completion of the Go Home operation resets DESQL2, and the operation enters state 5. The state 5 signal (ST5) causes the timer to be started.

(c) State 4

The EN11S signal generated upon completion of the timer operation resets DESQL1, and the operation enters state 4.

(d) State 0

The state 4 signal (ST4) resets DESQL4, and the operation enters state 0 to indicate the end of the DE Stop Sequence.

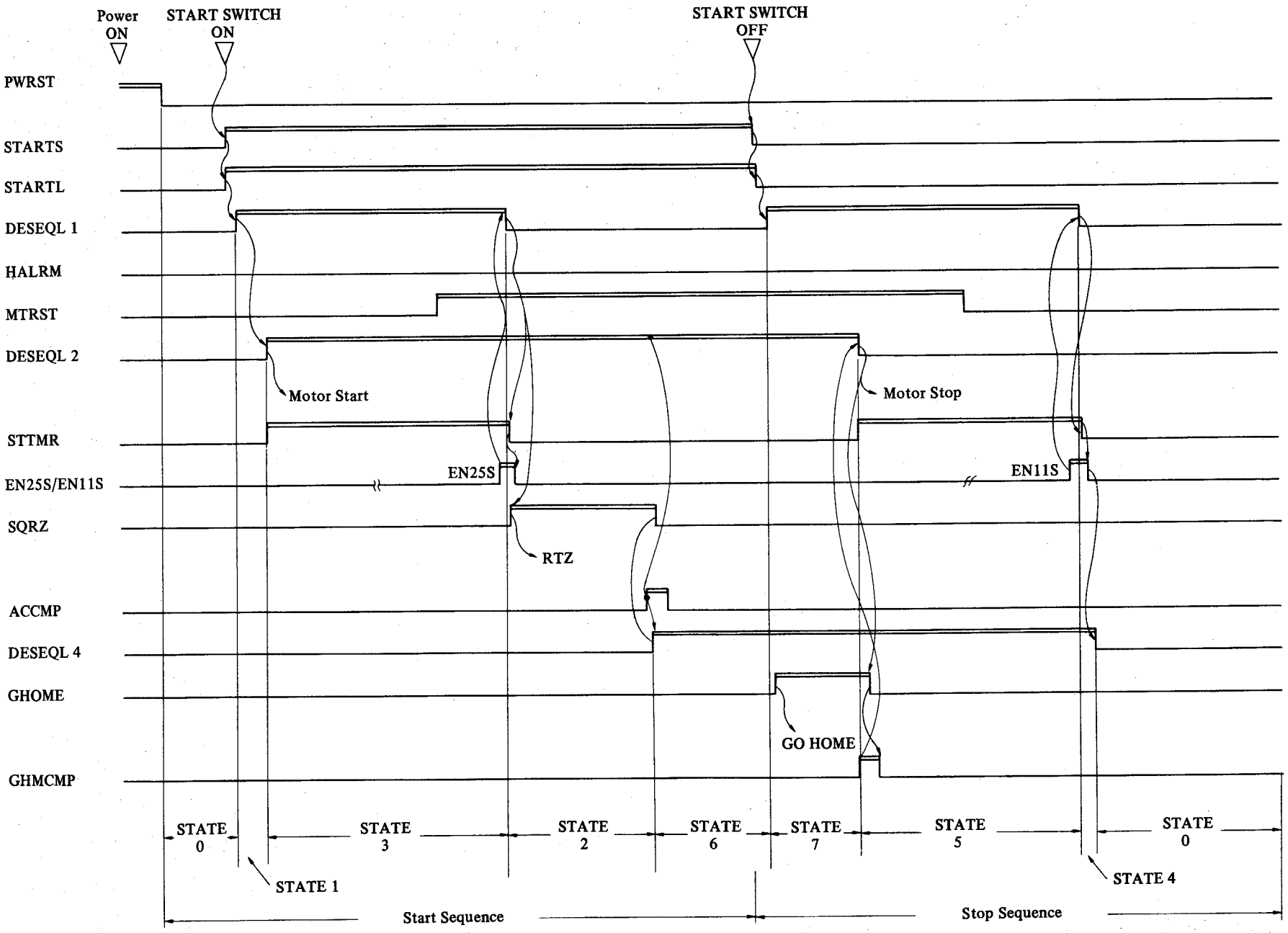


Figure 4.6.2 DE Start/Stop sequence

(2) Selection

Unit selection must be performed before instructions such as Seek and Read/Write can be sent from the controller.

When a drive receives Unit Select Tag (USLTG) and Unit Select 1, 2, 4 (USLCT1, USLCT2, and USLCT4), the drive compares it with its own address. The drive address is set by DIP switches on the display panel. If the address sent from the controller matches the address of the drive when the Open Cable Detector (OCDTR) and Power Ready (PWRDY) signals are high, Select Latch (SLCTL) is set, Enable signal (ENABL) is generated, Unit Selected (SLCTD) is sent to the B-cable, and, at the same time, the driver/receivers for the A-cable are enabled for transmission.

While the drive is selected, instructions (Seek, RTZ, Read/Write, and others) may be received. The drive is released when one of USLTG, OCDTR, PWRDY goes low.

Figure 4.6.3 shows the unit selection sequence timing diagram.

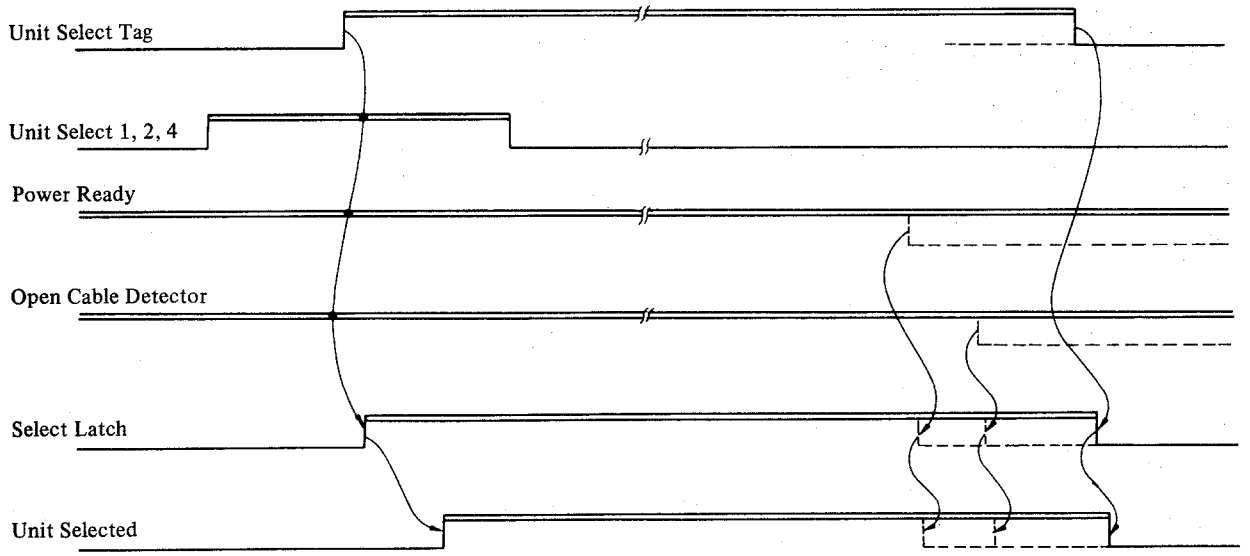


Figure 4.6.3 Unit selection

(3) Outline of access control

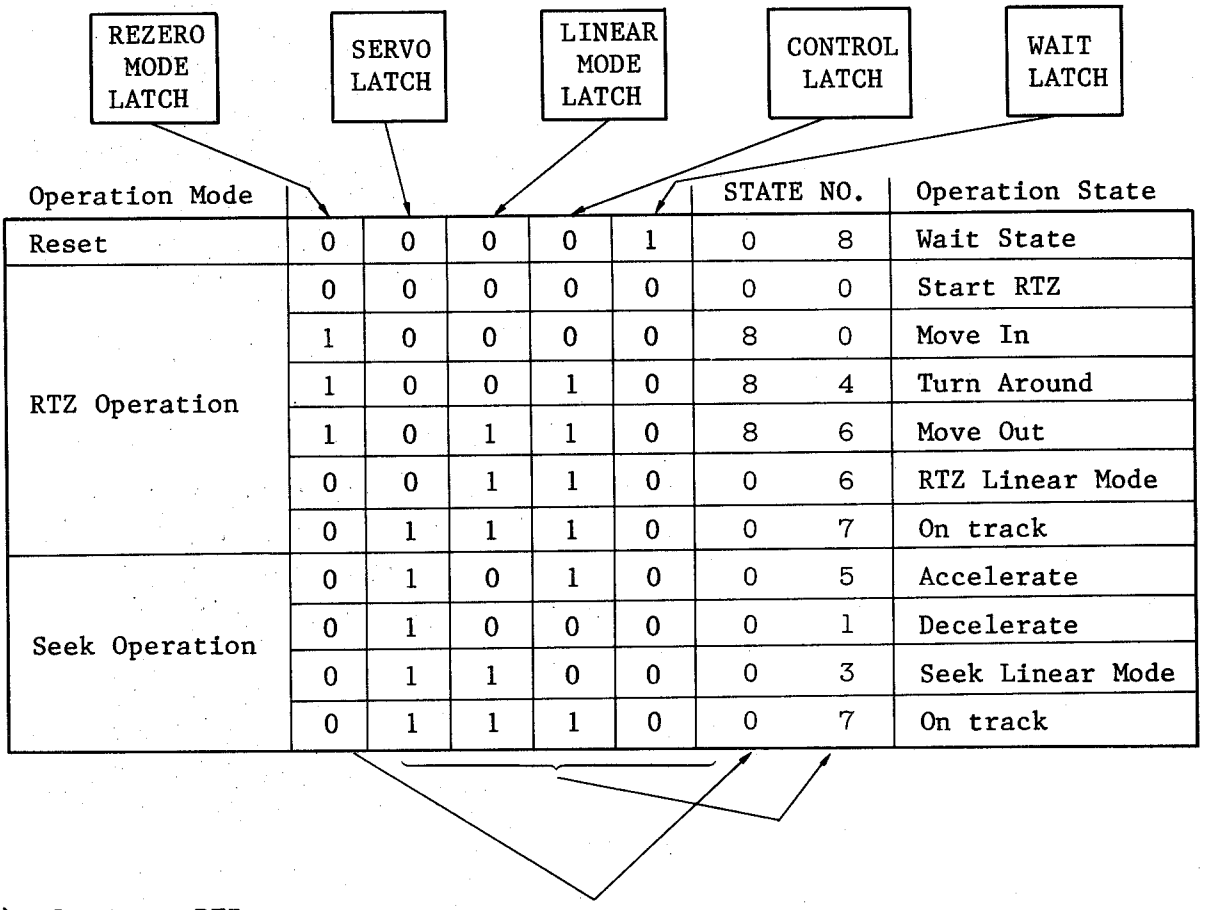
The access control circuit has five latches for controlling access operation.

The operation modes and the outputs of the latches are as follows:

1. Sequence RTZ
2. System RTZ
3. Manual RTZ
4. Direct seek
5. Fine control

The following access mode latches (Table 4.6.1) can be monitored on the 7 segment display on the display panel PCB.

Table 4.6.1 Access mode latches



Operation Mode	REZERO MODE LATCH	SERVO LATCH	LINEAR MODE LATCH	CONTROL LATCH	WAIT LATCH	STATE NO.		Operation State
Reset	0	0	0	0	1	0	8	Wait State
RTZ Operation	0	0	0	0	0	0	0	Start RTZ
	1	0	0	0	0	8	0	Move In
	1	0	0	1	0	8	4	Turn Around
	1	0	1	1	0	8	6	Move Out
	0	0	1	1	0	0	6	RTZ Linear Mode
	0	1	1	1	0	0	7	On track
Seek Operation	0	1	0	1	0	0	5	Accelerate
	0	1	0	0	0	0	1	Decelerate
	0	1	1	0	0	0	3	Seek Linear Mode
	0	1	1	1	0	0	7	On track

(4) Sequence RTZ

In this mode, the head is moved from the CSS zone to cylinder 00 during the DE Start Sequence. Figure 4.6.4 shows the timing diagram.

a. State 08 (Wait State)

When Power On Reset goes high, Wait Latch (WAITL) is set high. Control Latch (CNTL), Linear Mode Latch (LNML), Servo Latch (SRVL), and Rezero Mode Latch (RZML) are low.

b. State 00 (Start RTZ)

When the state 2 (ST2) signal goes high in the DE Start Sequence, Sequence Rezero (SQRZ) and Any Rezero (ANYRZ) are set high and WAITL is set low.

c. State 80 (Move In)

When ANYRZ goes high, Start Rezero (STRZ) and Rezero Mode Latch (RZML) are set high. STRZ initializes the head address register and the cylinder address register. When RZML is set high, Rezero Mode (RZMOD) is set high and is sent to the servo control circuit.

At this time, the servo head is located at the innermost position of the CSS zone.

d. State 84 (Turn Around)

When guard band pattern 2 (GBP2) in the CSS zone is detected, Control Latch (CNTL) is set high and, at the same time, High Velocity Set (HVLST) and Move Out Gate (MVOTG) are set high and are sent to the servo control circuit. Upon receipt of these signals, the servo control circuit moves the head from Guard Band Pattern 2 (GBP2) to Guard Band Pattern 1 (GBP1) at the Rezero High Speed.

e. State 86 (Move Out)

As the head is moved through the GBP2 zone in the outer direction, GBP1 is detected. Upon detection of GBP1, Linear Mode Latch (LNML) is set high and, at the same time, HVLST is set low.

From this moment, the head movement speed is reduced to the REZERO Low Speed, and the head is moved in the direction of cylinder 00 (outer direction).

When the end of the GBP1 zone is reached, Guard Band Latch (GRDBL) is set low and, after that, the head speed is controlled by the Position Curve generated from the Position signal.

f. State 06 (RTZ Linear Mode)

When the head speed reaches the speed determined by the Position Curve, the servo control circuit sets End Decelerate (ENDDC) high and, then, RZML is set low.

When RZML goes low, the head is controlled in the Position Error Mode. If the head reaches within a specified distance from the center of cylinder 00 (On Track is high), the monostable multivibrator is activated. If On Track is high again at the end of the monostable multivibrator operation, Track Following Timer (TFTMR) is set high.

The operation mode controlled by Position Error is called Fine Control.

g. State 07 (On Track)

If Valid Index (VLIX) goes high while TFTMR is high, Servo Latch (SRVL) is set high and Unit Ready, Seek End (SKEND), and On Cylinder (ONCYL) are sent to the controller.

If the sequence RTZ is unsuccessful, that is, if Overshoot Check (OVSCK) or Time Out Check (TMOCK) is detected, Access Check (ACCCK) is set high and the carriage is released. At this time, Unit Ready (UNRDY), Seek End (SKEND), and Seek Error are sent to the controller.

Over Shoot Check (OVSCK) is set high when the head is moved at an abnormal speed during the RTZ operation (VG20I is set high if the speed exceeds 20 inches/second), or when Guard Band Pattern (Inner Guard Band Pattern (GBP2 and GBP1) or the Outer Guard Band Pattern (OGB)) is detected during the fine control, or when the head is not on the track and Track Crossing Pulse (TRXGP) is set high three or more times. Time Out Check (TMOCK) is set high if the operation is set high and the operation is not terminated within 250 ms.

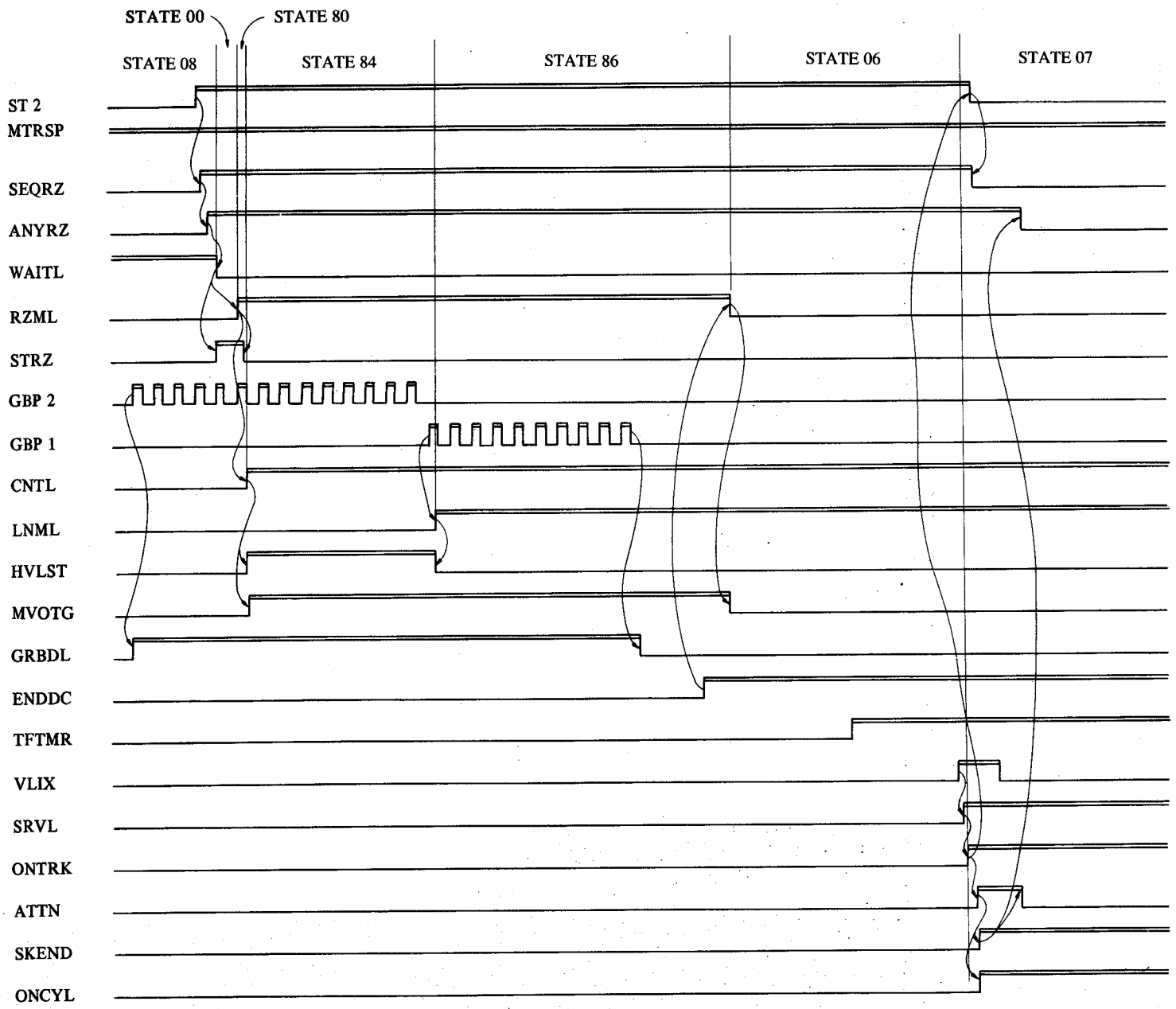


Figure 4.6.4 Sequence RTZ

(5) System RTZ/Manual RTZ

In the System RTZ (SYSRZ) and Manual RTZ (MRTZL) modes, the head is moved to cylinder 00 regardless of the position at which the head is currently located. The System RTZ operation (SYSRZ) is started upon receipt of Tag 3/Bit 6 (RTZ) from the controller when the drive is selected and is not performing a seek or RTZ operation or when a seek error occurs. The Manual RTZ operation (MRTZL) is started by the MRTZ switch on the display panel when the drive is not performing the seek, RTZ, offset, or read/write operation.
Figures 4.6.5 and 4.6.6 show how SYSRZ and MRTZL are started, respectively. Figure 4.6.7 shows the sequence that is performed after RZML is set high.

a. State 08 (Wait State)

When the SYSRZ or the MRTZL operation is performed, ANYRZ is set high.

Then, WAITL is set high, and the access mode latches (RZML, SRVL, LNML, CNTL) and Seek Error (Access Check: ACCCK) are set low.

b. State 00 (Start RTZ)

When the SYSRZ operation is performed, the access mode latches are set low and, then, WAITL is set low.

When the MRTZL operation is performed, WAITL is set high while SW2 is high. When SW2 goes low, WAITL is set low.

c. State 80 (Move In)

When WAITL is set low, STRZ and RZML are set high.

Before the head detects Guard Band Patterns 1 and 2 (GBP1 and GBP2), the carriage is moved in the inner direction at the RTZ High Speed. When the carriage passes cylinder 00 and GBP1 is detected, Guard Band Latch 1 is set high and the speed is reduced to the low speed.

If the head is on GBP1 at the start of this state, the carriage is moved at the low speed from the beginning.

d. State 84 (Turn Around)

When the head passes GBP1 and detects GBP2, CNTL is set high and, at the same time, HVLST and MVOTG are set high. In this case, the head is moved at the high speed in the outer direction.

e. State 86 (Move Out)

Same as that of sequence RTZ.

f. State 06 (Rezero Linear Mode)

Same as that of sequence RTZ.

g. State 07 (On Track)

Same as that of sequence RTZ.

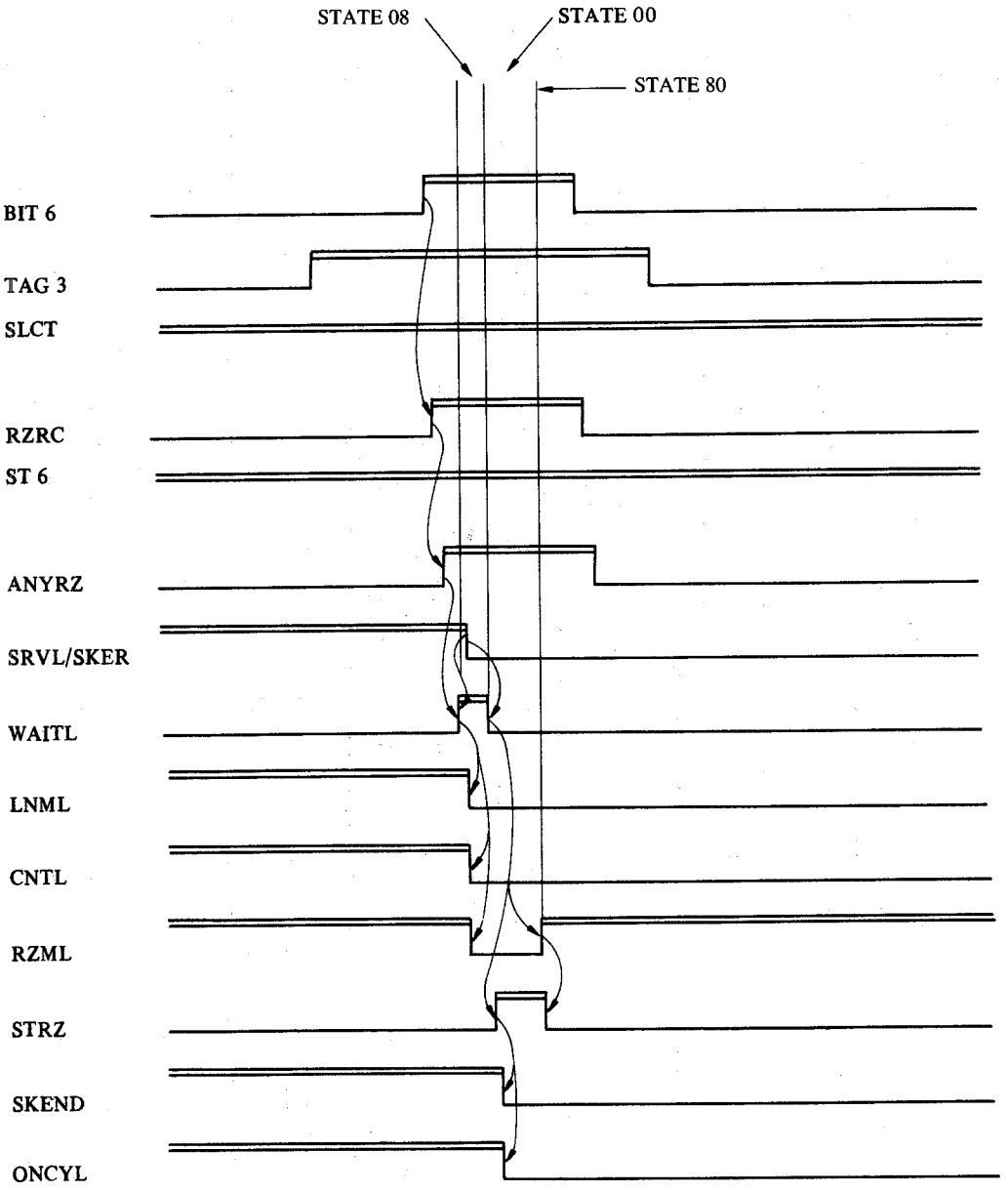


Figure 4.6.5 System RTZ sequence

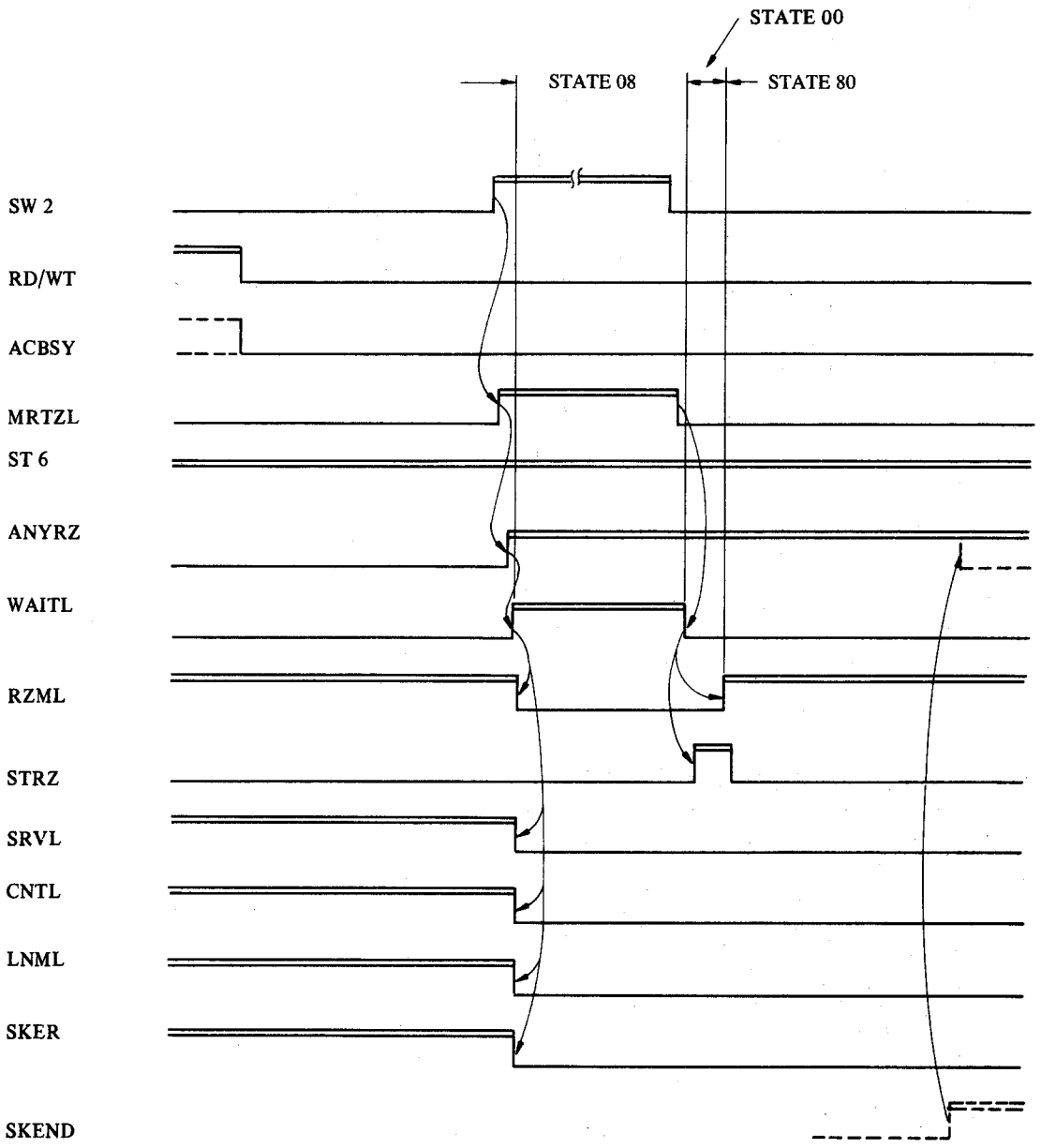


Figure 4.6.6 Manual RTZ sequence

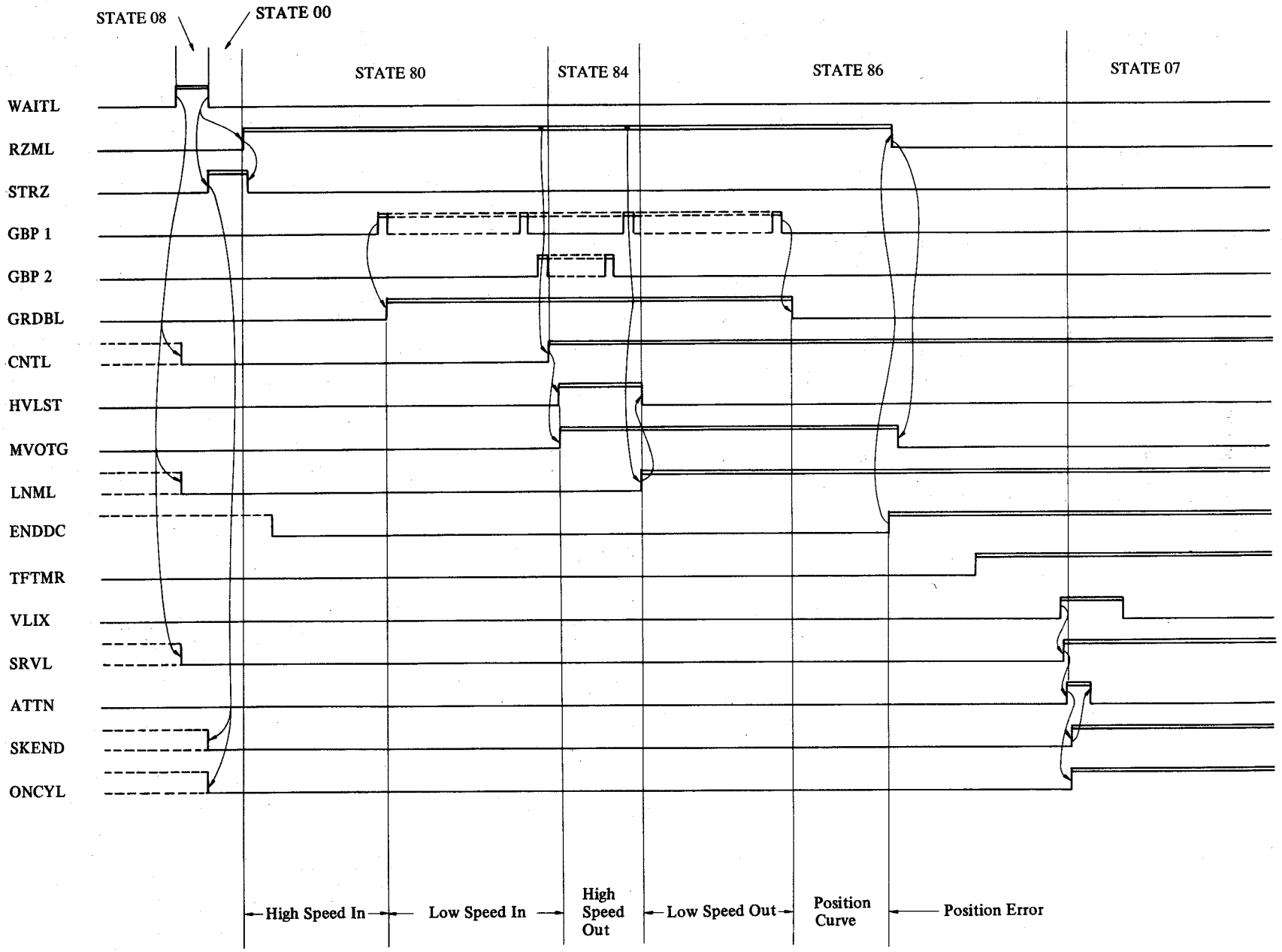


Figure 4.6.7 System/Manual RTZ sequence

(6) Seek

The head is moved to the cylinder specified by Tag 1/Bits 0 - 9 sent from the controller. Figure 4.6.8 shows the timing diagram.

a. State 05 (Accelerate)

When TAG1 goes high, the contents of Bits 0 to 9 are set in the New Cylinder Address Register (NCAR). The address of the cylinder on which the head is currently located is stored in the Present Cylinder Address Register (PCAR). The difference between the address stored in the NCAR and that in the PCAR is calculated and is output in the binary code (D1 - D128). If the difference is 144 or greater (NCAR - PCAR > 144), D1 - D128 is set to a value of all 1 bits and is sent to the servo control circuit. The servo control circuit forms the desired speed curve according to the value indicated by D1 - D128.

If the value indicated by the NCAR is greater than that indicated by the PCAR, Move Out Gate (MVOTG) is set high to cause the head to be moved in the outer direction; conversely, if the value indicated by the NCAR is smaller than that indicated by the PCAR, MVOTG is set low to cause the head to be moved in the inner direction.

Then, when TAG1 goes low, Set CAR Off Pulse (SCAROFP) is set high, SKEND, ONCYL, TFTMR, and LNML are set low, and Access Mode (ACCMD) is set high.

The servo control circuit moves the head according to the desired speed curve and generates Track Crossing Pulse (TRXGP) whenever the head crosses a cylinder. TRXGP is sent to the PCAR to increment the register when the head is moved in the outer direction, or to decrement the register when the head is moved in the inner direction. Thus, the output of the difference counter (D1 - D128) is decremented by one at a time.

b. State 01 (Decelerate)

If the head is moved at a speed higher than that indicated by the desired speed curve, the servo control circuit generates End Accelerate (ENDAC) and sets CNTL low. The speed of the head is then reduced so that the head is moved according to the desired speed curve.

c. State 03 (Seek Linear Mode)

When the head detects On Cylinder at the desired cylinder (NCAR=PCAR), the servo control circuit generates End Decelerate (ENDDC) and, at the same time, starts the 2.5 ms-timer and sets LNML high. Then, the operation mode of the head is changed from the position curve control mode to the position error control mode.

d. State 07 (On Track)

If the head is on the desired track when the operation of the 2.5 ms-timer is ended, TFTMR is set high. CNTL is set high and, at the same time, SKEND and ONCYL are set high. This means that the seek operation is terminated. When a no-motion seek command is issued from the controller, the 5 µs-timer is activated and, at the completion of the timer, SKEND and ONCYL are set high.

If an illegal cylinder address is sent (a value greater than 841), SKER and SKEND are set high after about 5 µs. If the seek operation is not terminated normally, that is, if the seek operation is not terminated within 250 ms (TMOCK), or if the Inner or Outer Guard Band are detected during the seek operation, or if TRXGP is detected three times or more after the head reaches the desired cylinder (OVSCK), SKER and SKEND are set high.

When SKER is set high, the carriage is released.

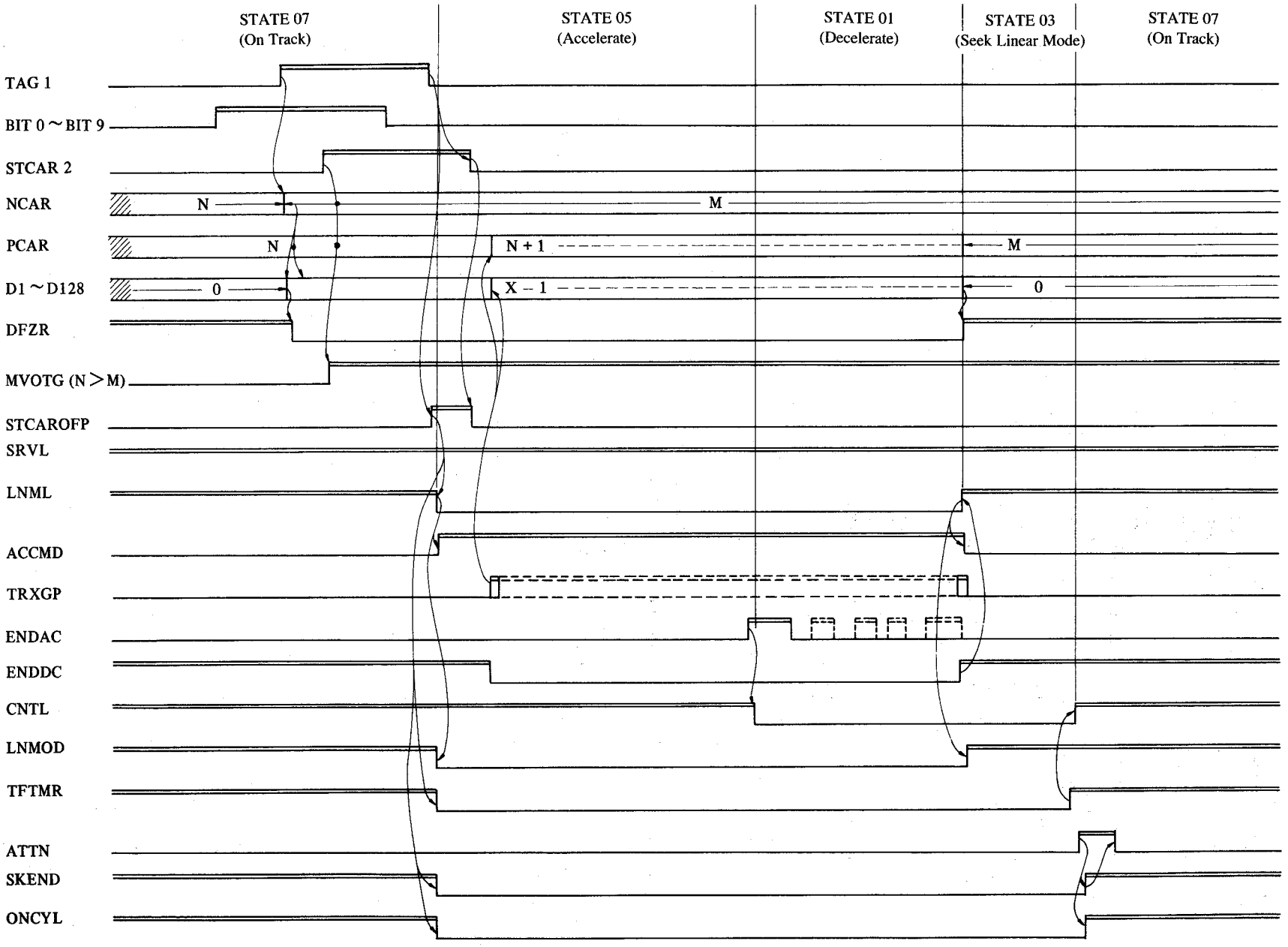


Figure 4.6.8 Seek sequence

(7) Offset

The head, being at the center of a track (On Track), is moved 100μ inches in the direction specified by Bit 2 or 3 when TAG3 is sent from the controller. The fine control method is used in this operation mode. Figure 4.6.9 shows the timing diagram.

While the drive is selected (SLCT), Offset Plus (OFSTP) is set high when Bit 2 of TAG3 is set to 1 by the controller and, at the same time, Offset Out (OFSOT) is set high. If the drive is not in the abnormal condition (ABN) at this time, Offset Active (OFACT) is set high and, at the same time, Difference 16 (GD16) is set high. Then, the servo control circuit moves the head in the outer direction; i.e., the servo control circuit starts the offset operation and moves the head to the location 100μ inches outward of the on-track position. This operation is terminated within 5 ms.

When OFACT goes high, Offset Active Pulse (OFACP) is set high and the 5 ms-timer is started (M5MS). At the same time, Seek End (SKEND) and On Cylinder (ONCYL) are set low. SKEND and ONCYL are set high when the timer operation is terminated.

When Bit 3 of TAG3 is set to 1, Offset Minus (OFSTM) is set high and, by holding OFSOT low, the head is moved in the inner direction.

When Bit 2 or Bit 3 of TAG3 is set to 0 and OFSTP, OFSTM, OFSTA, and GD16 are set low, the head is returned to the on-track position. This operation is terminated within 5 ms.

When OFACT goes low, OFACP is set high, the 5 ms-timer (M5MS) is started and, at the same time, SKEND and ONCYL are set low. When M5MS goes low, SKEND is set high and, if the head is at the on-track position, ONCYL is set high.

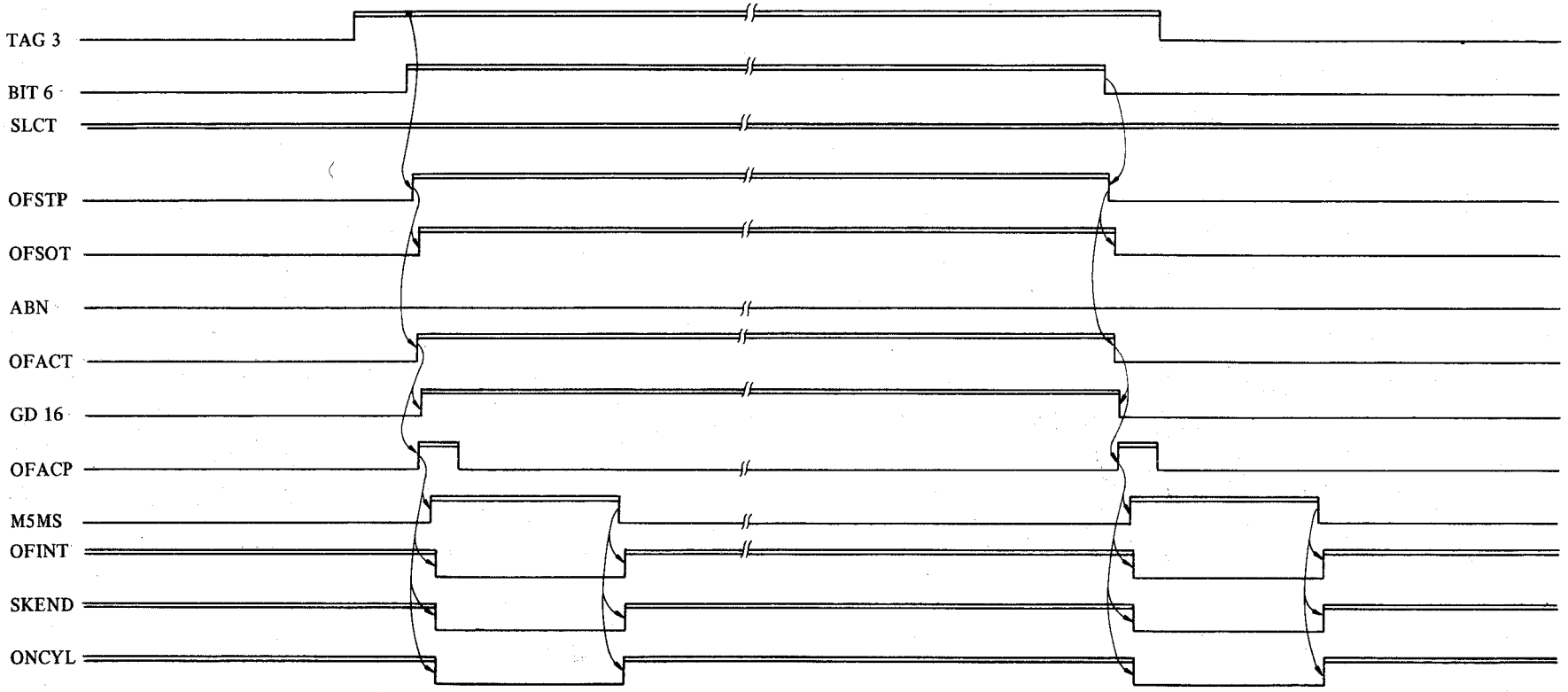


Figure 4.6.9 Offset sequence

(8) Fault and Error Detection

Faults and errors detected in the drive are displayed by the maintenance – aid LEDs on the display panel and reported to the controller through the interface lines.

a. Fault Register

If the following errors occur, the Fault register will be set and Fault line will be enabled.

Table 4.6.2 Write/Read check conditions

No.	Write/Read Check State	Conditions	LED	Rotary SW
1	Index Check	(RG + WG).IDXCK	Bit 0	R/W
2	Control Check	RG.DSKER RG.WG OFACT.WG RONLY.WG	Bit 1	
3	Not Sync Check	RG.NSC	Bit 2	
4	Head Short Check	(RG + WG).HDSHT	Bit 3	
5	Write Current On Read Check	RG.MUSFV	Bit 4	
6	Write Transition Check	WG.MUSFV	Bit 5	
7	Delta I Write Check	WG.DIECK	Bit 6	
8	Servo Off-Track	WG.$\overline{\text{RWCAP}}$.($\overline{\text{URDY}}$+$\overline{\text{TFTMR}}$+ACCK) RG.$\overline{\text{EQUAL}}$	Bit 7	
9	Deskew Error	RG.DSKER	Bit 0	CTLC
10	R/W Gate Check	RG.WG	Bit 1	
11	Offset Active Check	OFACT.WG	Bit 2	
12	Read Only Mode Check	RONLY.WG	Bit 3	

These faults can be cleared by one of the following:

① Depressing the Fault Clear switch on the operator panel
② Fault Clear signal sent from the controller
③ Depressing the MRTZ switch on the display panel

b. Seek Check Latch

If seek error occurs in the drive, the error will set Seek Check Latch, enabling Seek Error to the controller, and light the maintenance-aid LED.

Table 4.6.3 Seek error fault conditions

No.	Access State	Conditions	LED	Rotary SW
1	Access Timeout Check	Timeout in direct or RTZ seek	Bit 1	ACC
2	Over Shoot Check	Any Guard Band in direct seek, or Over track-crossing pulse in settling	Bit 2	

4.6.3 Servo circuit

(1) Seek control operation

The seek control operation is classified roughly into the coarse control operation and fine control operation.

a. Coarse control operation

The coarse control operation is performed to move the head to the desired cylinder position. That is, the head is moved with a speed feedback loop at a high speed by comparing the target speed, derived from the position difference between the desired position sent from the logic circuit and the actual position, with the actual speed derived from the position signal read from the servo surface with the servo head.

The speed is decreased as the position difference is reduced and, when the head approaches the desired cylinder, the speed becomes very slow.

b. Fine control operation

When the head nears the desired cylinder and the difference between the desired position and the current position is within the specified range (on track), the coarse control operation is switched to the fine control operation. During the fine control operation, the position signal is fed back to ensure that the head is always on the desired cylinder notwithstanding mechanical vibration and temperature change.

The speed signal is used as the damping factor. The signal generated by integrating the position signal is also used to increase stiffness.

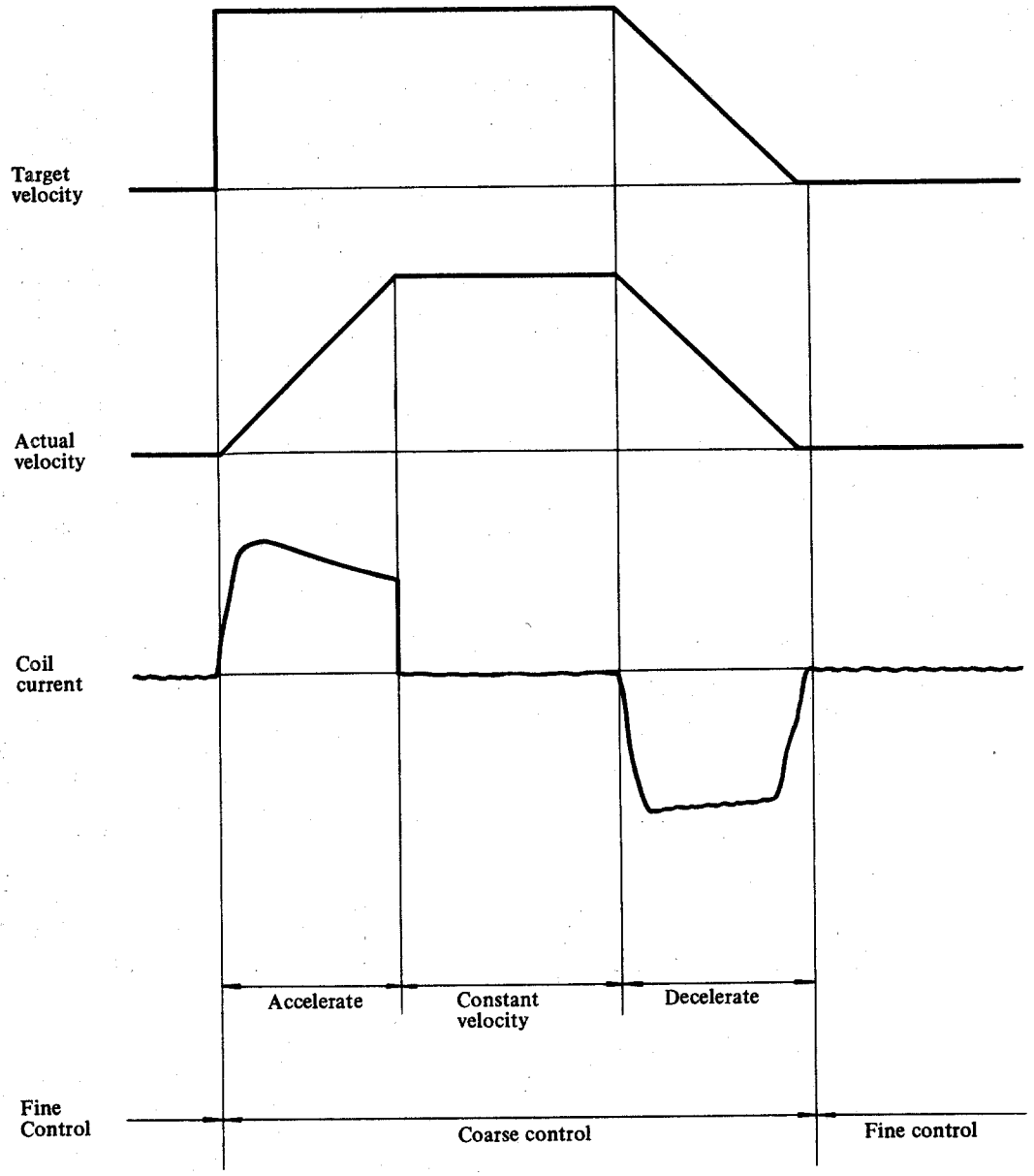


Figure 4.6.10 Seek control

(2) Rezero control operation

The head is returned to the reference cylinder (cylinder 0). The rezero seek operation is classified into the coarse control operation and the fine control operation as with the seek control operation; however, unlike the seek control operation, the target speed is determined by the signal generated by the reference voltage. The following explains how the rezero seek operation is performed, assuming that the head is not in the Inner Guard Band.

a. High Speed In (HSPIN)

The head is moved in the inner direction at 8 inches per second until Inner Guard Band 1 (IGB1) is detected.

b. Low Speed In (LSPIN)

The head is moved in the inner direction at about 2.5 inches per second between the moment when IGB1 is detected in the neighborhood of cylinder-2 (minus 2) and the moment when Inner Guard Band 2 (IGB2) is detected.

c. High Speed Out (HSPOT)

The direction in which the head is to be moved is reversed, and the head is moved in the outer direction at about 3.5 inches per second between the moment when IGB2 is detected in the neighborhood of cylinder-18 (minus 18) and the moment when IGB1 is detected.

d. Low Speed Out (LSPOT)

The head is moved in the outer direction at about 0.8 inches per second after detecting IGB1.

e. Rezero Out (RZOUT)

When the head enters the servo zone from IGB1 after it travels in the neighborhood of cylinder-2 (minus 2), the head is moved to cylinder 0 with the target speed signal generated from the position signal.

f. Fine control

After On Track is detected when the head is in the neighborhood of cylinder 0, the Position control is performed in the same manner as the seek control operation.

The rezero operation is performed from b. if the head is to be returned from IGB1, or from c. if the head is to be returned from IGB2; after that, the same control method is performed until the head is positioned on cylinder 0.

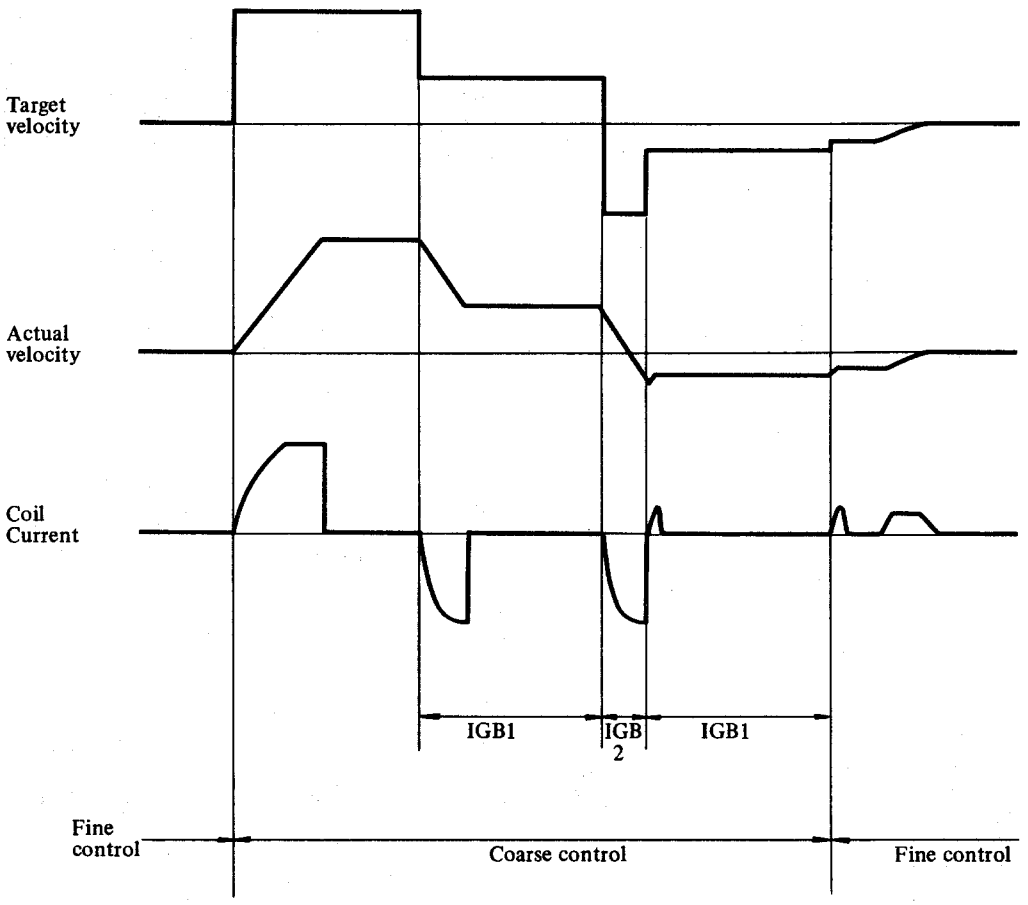


Figure 4.6.11 Rezero control

(3) Servo blockdiagram

a. AGC amplifier

The AGC amplifier amplifies the output signal from the servo head (SVPRE and *SVPRE) to generate the carrier amplifier signal (CRAMP). The amplifier gain is controlled by the output (SAGC) of the AGC voltage generating circuit to compensate for level fluctuation on the servo surface.

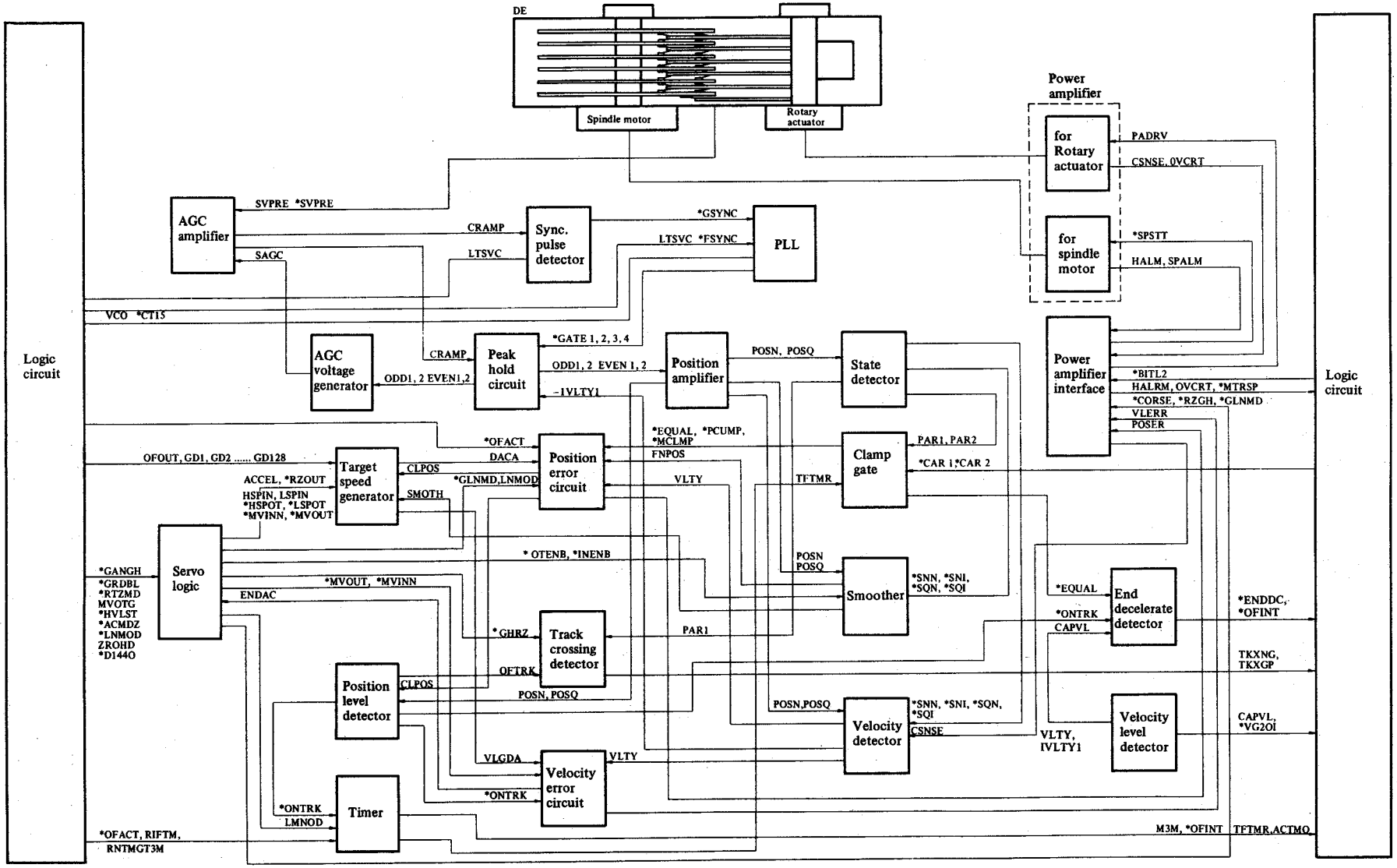


Figure 4.6.12 Servo block diagram

b. Peak hold circuit

The peak hold circuit receives gate signals (*GATE1 - 4) from PLL to sample ODD1, EVEN1, ODD2, and EVEN2 pulses from the output of an AGC amplifier (CRAMP).

This circuit uses the output (- VLTY) from the speed detect circuit in order to vary the discharge time constant of the sampling circuit according to the head travelling speed.

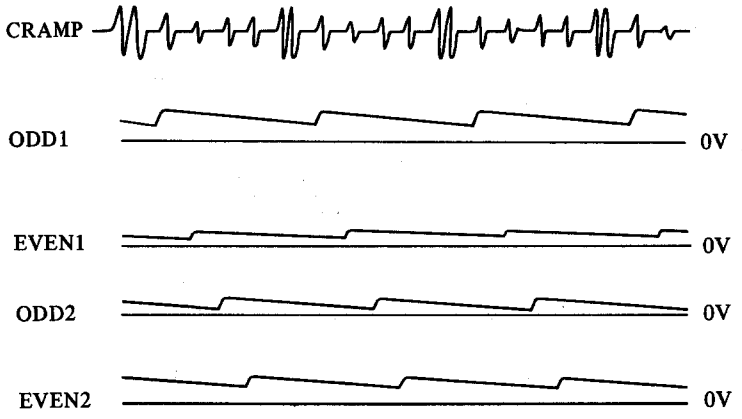


Figure 4.6.13 Peak hold circuit

c. AGC voltage generator

This circuit generates the AGC amplifier gain control signal SAGC by means of ODD1, EVEN1, ODD2, and EVEN2 which are generated by the peak hold circuit. If the output voltage of the servo head falls due to variations in the level of the signal read from the media, the amplitude of the carrier amplifier output decreases and the output voltage of the peak hold circuit falls, lowering the SAGC voltage. When the control voltage SAGC of the AGC amplifier falls, the gain is increased to compensate for the drop in the output voltage level of the servo head. Conversely, when the output voltage rises, it is compensated for in the same manner.

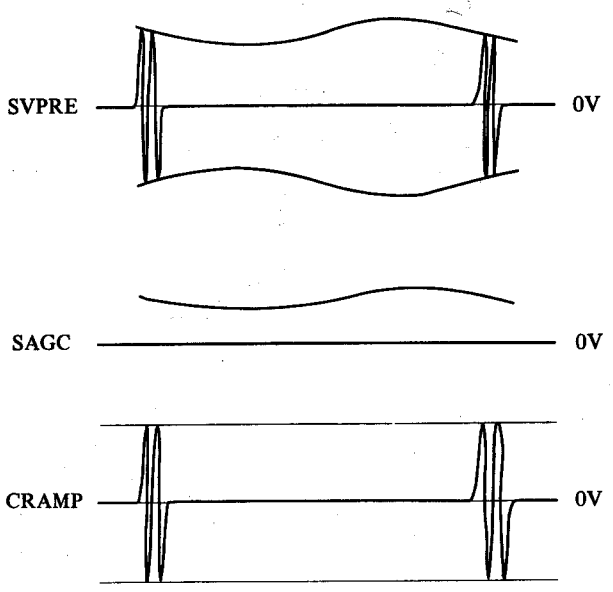


Figure 4.6.14 Function of AGC

d. Sync pulse detector

The Gated Sync Pulse signal (*GSYNC) is generated using the signal generated by slicing the Carrier Amplifier signal (CRAMP). *GSYNC is absent at the locations where the index pulses in the valid Index pattern and the Guard Band patterns are written. This signal is used for the VCO and logic circuits to detect patterns.

*GSYNC is generated by ANDing TP4 and the LTSVC signal generated by the logic circuit.

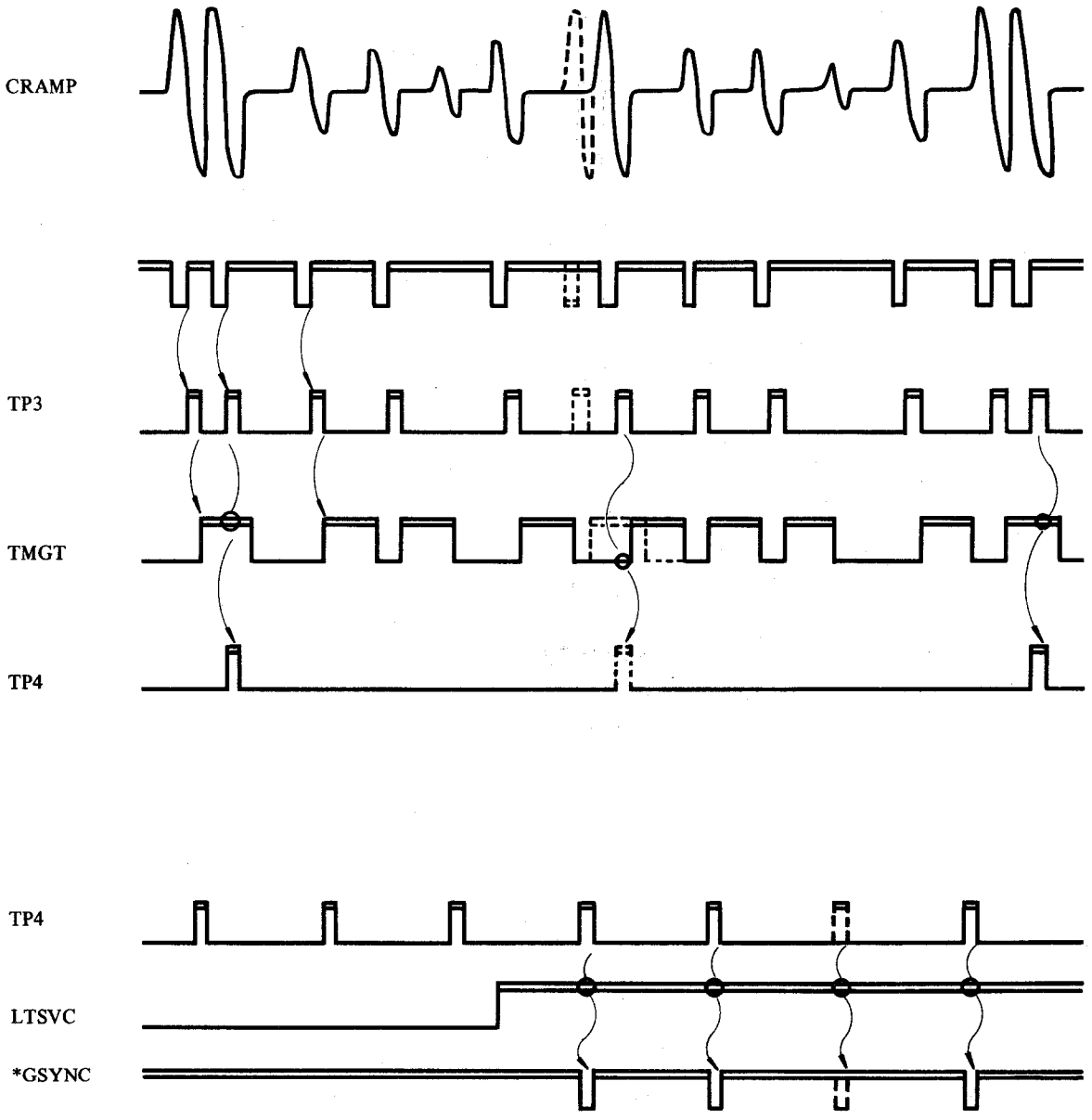


Figure 4.6.15 Detection of Sync pulse

e. PLL

The PLL circuit, consisting of the phase detector, charge pump, VCO, counter, and decoder, generates gate signals used to sample ODD1, ODD2, EVEN1, and EVEN2 of the carrier amplifier. Even in the area where the index pulse is absent, the circuit generates gate signals.

- Phase detector

  This circuit detects the difference in phase between *CT7, generated by VCO which divides *GSYNC by 16, and *GSYNC. It outputs *INC or *DEC according to a shift in phase.

- Charge pump

  The charge pump raises or lowers the PLO Analog (PLOAN) voltage depending on the signal from the phase detector (*INC/*DEC). The output voltage of PLOAN is 0 when the disk is rotating at the specified constant speed.

- VCO, counter, and decoder

  The VCO converts DC voltage to an oscillation frequency. The PLOAN voltage is proportional to the oscillation frequency. When the disk is rotation at the specified speed, the oscillating frequency of the VCO is 9.83 MHz, 32 times as high as the frequency of *GSYNC. The output of the VCO is sent to the logic circuit and counted by the four-bit binary counter. The output of the counter is decoded and *CT7 is sent to the phase detector and *GATE1 - *GATE4 to the peak hold circuit. *CT15 is sent to the logic circuit to detect the valid Index pattern and Guard Band Patterns.

f. Position amplifier

The position amplifier generates POSN by the difference between ODD1 and EVEN1, and POSQ by the difference between ODD2 and EVEN2. These two position signals are 90 degrees out of phase with each other.

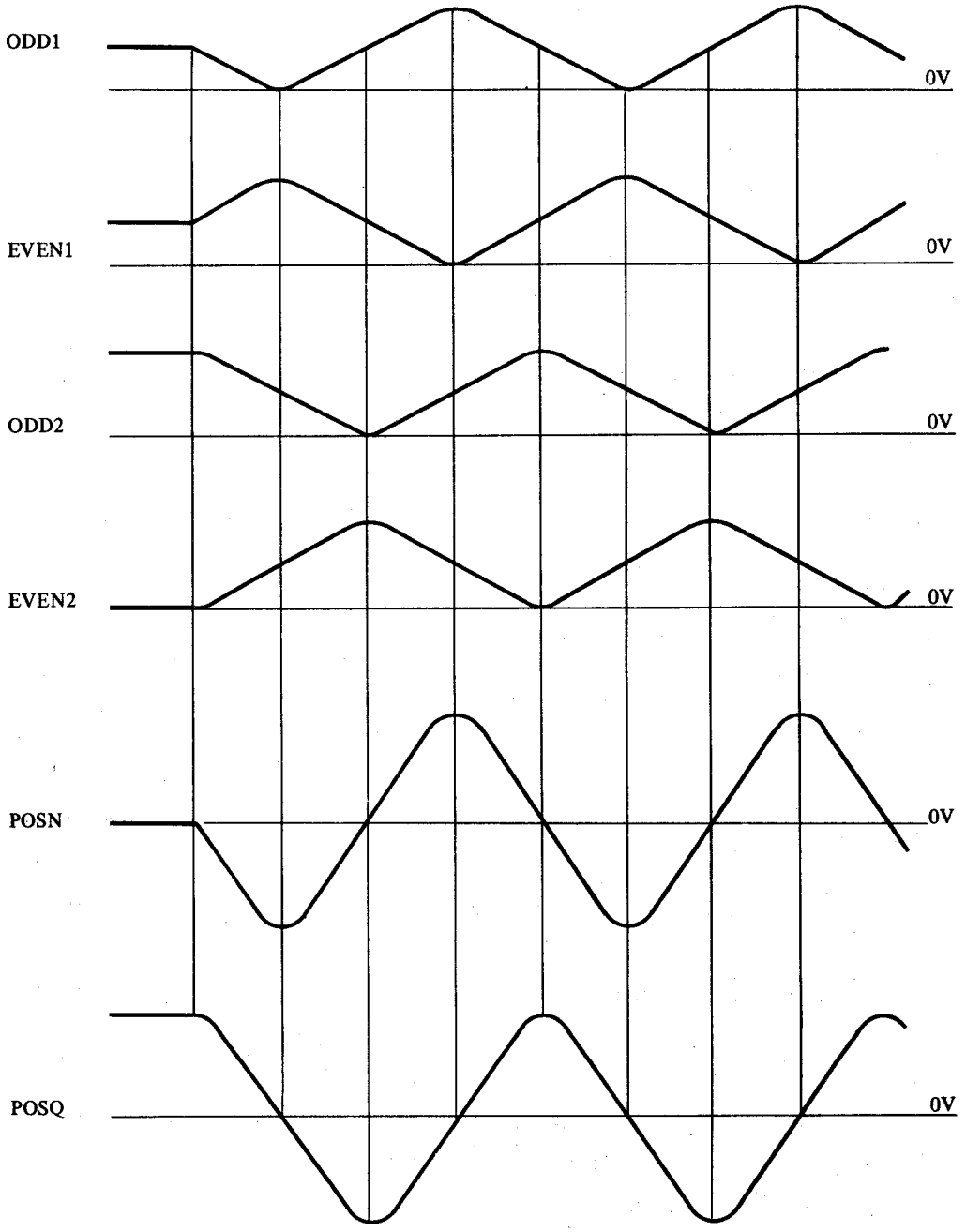


Figure 4.6.16 Position signals

g. State detector

The state detect circuit detects the low-order two bits of the present head position by two position signals, POSN and POSQ.

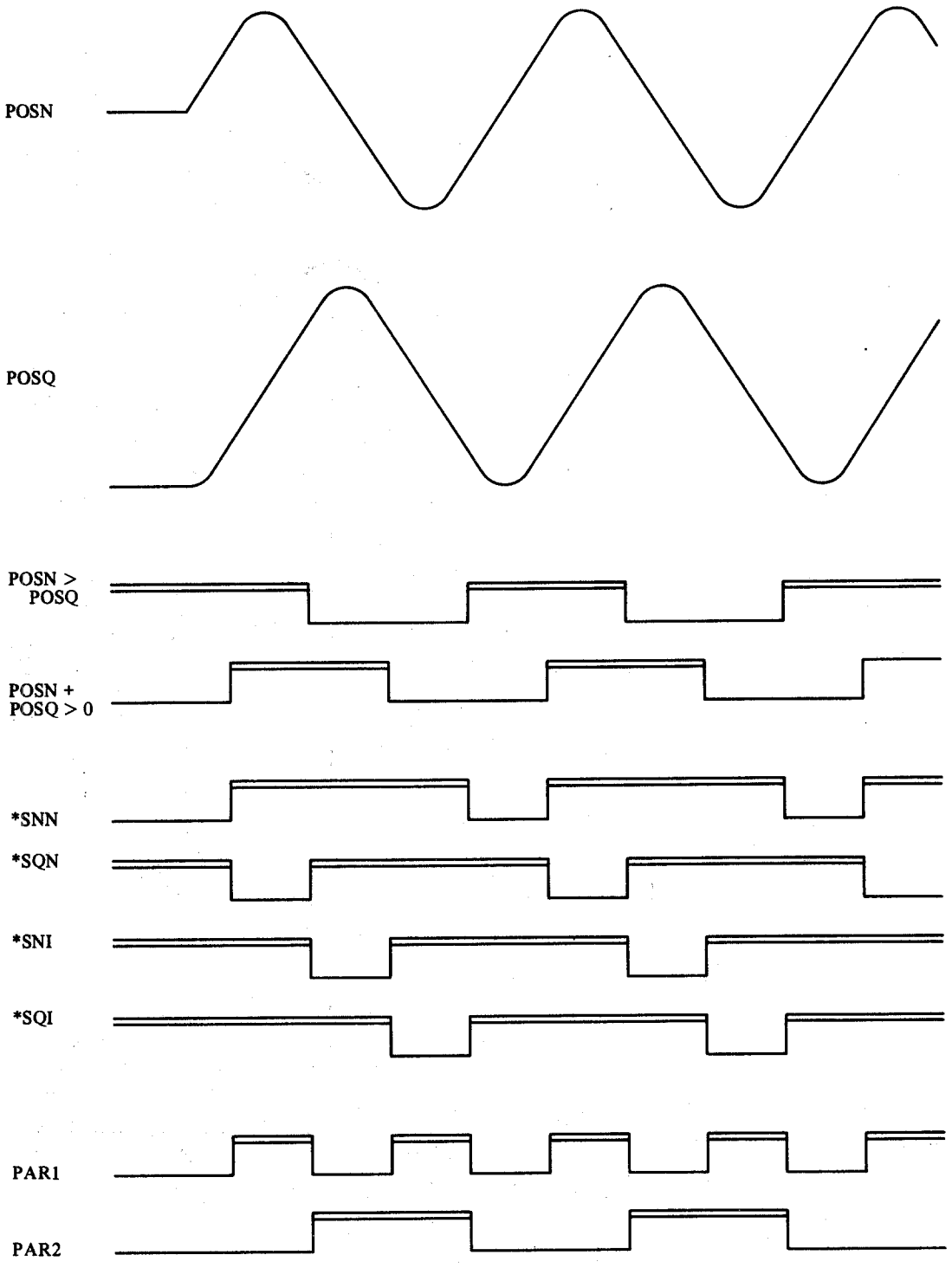


Figure 4.6.17 State of Position signals

h. Smoother

The position signal (FNPOS) for fine control is generated by selecting POSN or POSQ by means of *SNN, *SNI, *SQN, and *SQI generated from the state detect circuit.

Switching the polarity of FNPOS according to the carriage movement direction, the interpolation signal (SMOTH) is generated for smoothing the stair step signal from the DA converter.

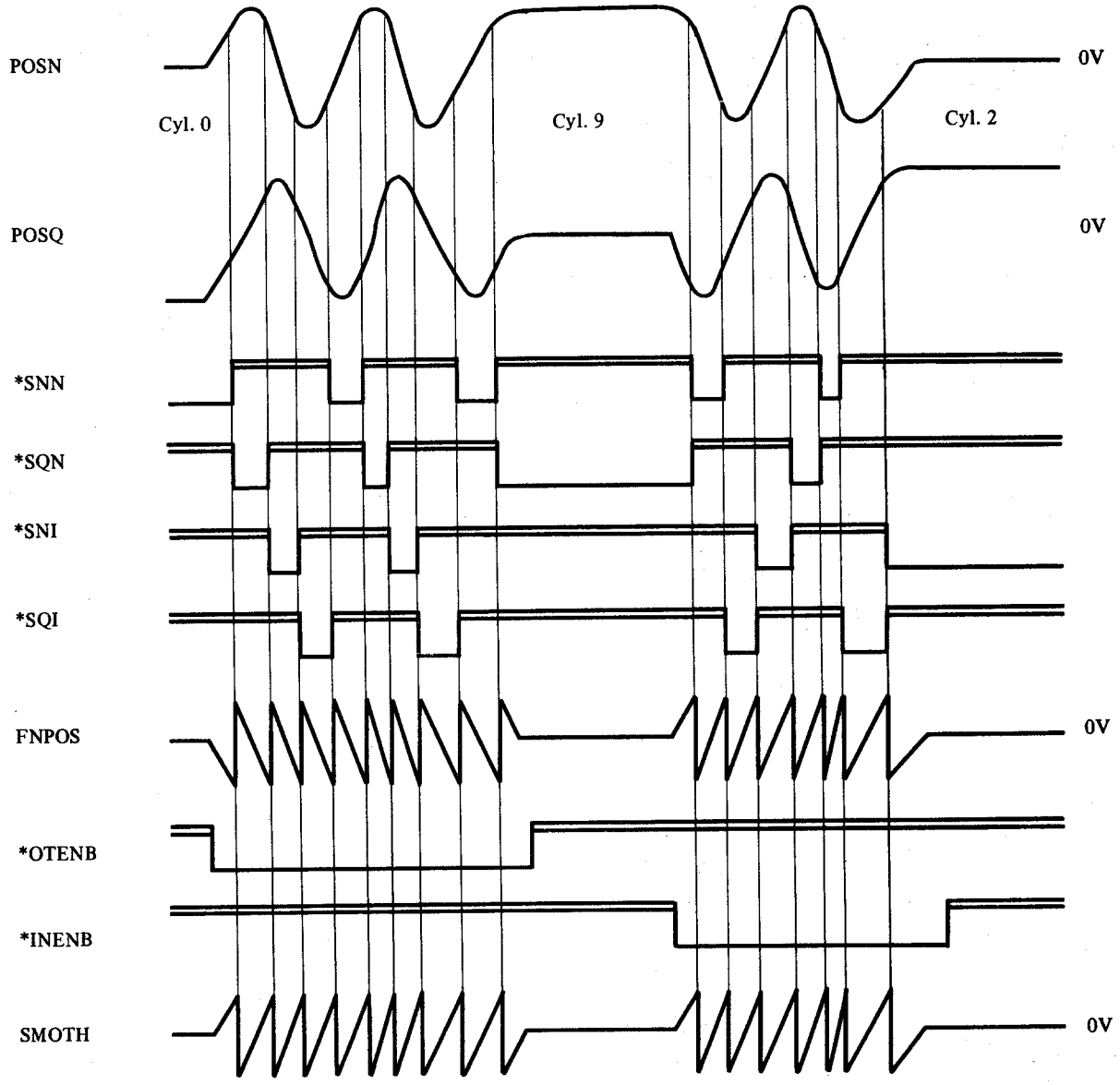


Figure 4.6.18 Output signal of smoother

i. Clamp gate

The clamp gate holds the position signal at the specified level when the signal voltage is higher or lower than the specified level in order to extend the distance over which the head can be controlled. It generates *EQUAL, *PCLMP, and *MCLMP by comparing the low-order two bits of the desired position sent from the logic circuit with the low-order two bits of the present head position sent from the state detect circuit.

j. Position error circuit

The position error circuit generates the position signal (CLPOS) for position control by means of FNPOS generated from the smoother circuit and *EQUAL, *PCLMP, and *MCLMP signals sent from the clamp gate circuit. It then combines CLPOS and the velocity signal (VLTY) to generate the position error signal (POSER), the error signal for fine control. During offset operation, this circuit combines the output (DACA) from the DA converter with the position signal. Figure 4.6-19 shows how the clamp circuit works when the head is moved from cylinder 0 to cylinder 9 (*CAR1=0, *CAR2-1).

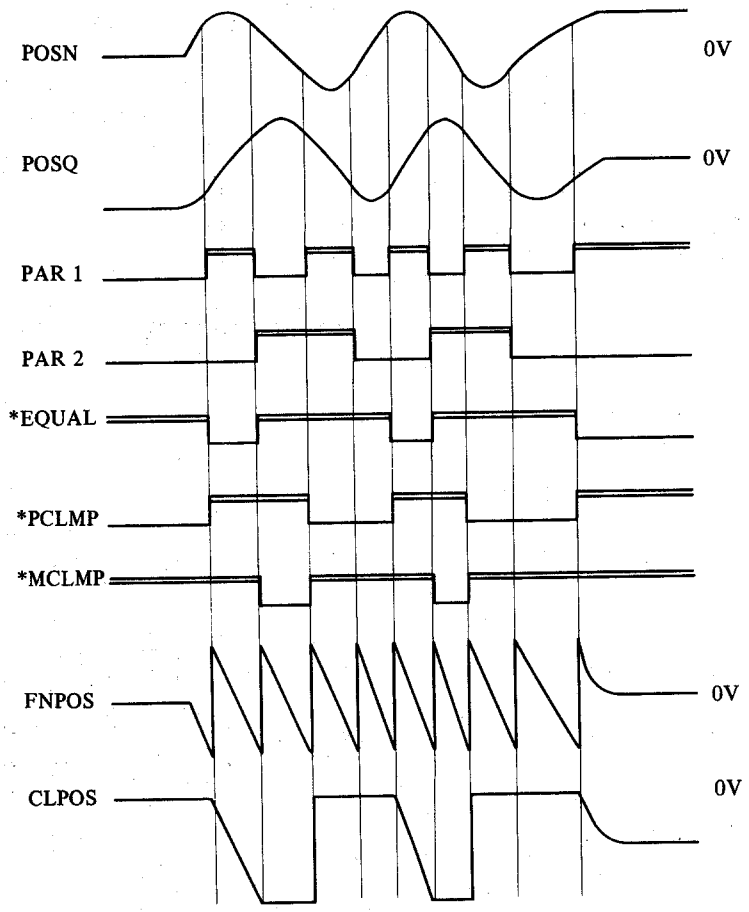


Figure 4.6.19 Clamped Position signal

k. Track crossing detector

The track crossing detect circuit generates the Track Crossing signal (TKXNG) by means of PAR1 sent from the state detect circuit and OFTRK sent from the position level detect circuit. The Track Crossing Pulse (TKXGP) used to decrement the difference counter is generated on the rising edge of TKXGP. At rezero operation, *GHRZ is activated to prevent TDXGP from being generated.

l. Position level detector

The position level detect circuit generates the Off-Track signal (OFTRK) by slicing the position signal (POSN, POSQ) and also generates the On-Track signal (*ONTRK) by slicing Clamped Position signal (CLPOS) output from the position error circuit.

OFTRK is used in the circuit which generates the track crossing pulse for decrementing the difference counter in the logic circuit. *ONTRK is used to generate switching signal (*ENDDC) which changes the control method from the coarse control to the fine control, the signal (ENDAC) which indicates the end of carriage acceleration, and the signal (TFTMR) which indicates, after the control is switched to the fine control, that the head is positioned properly.

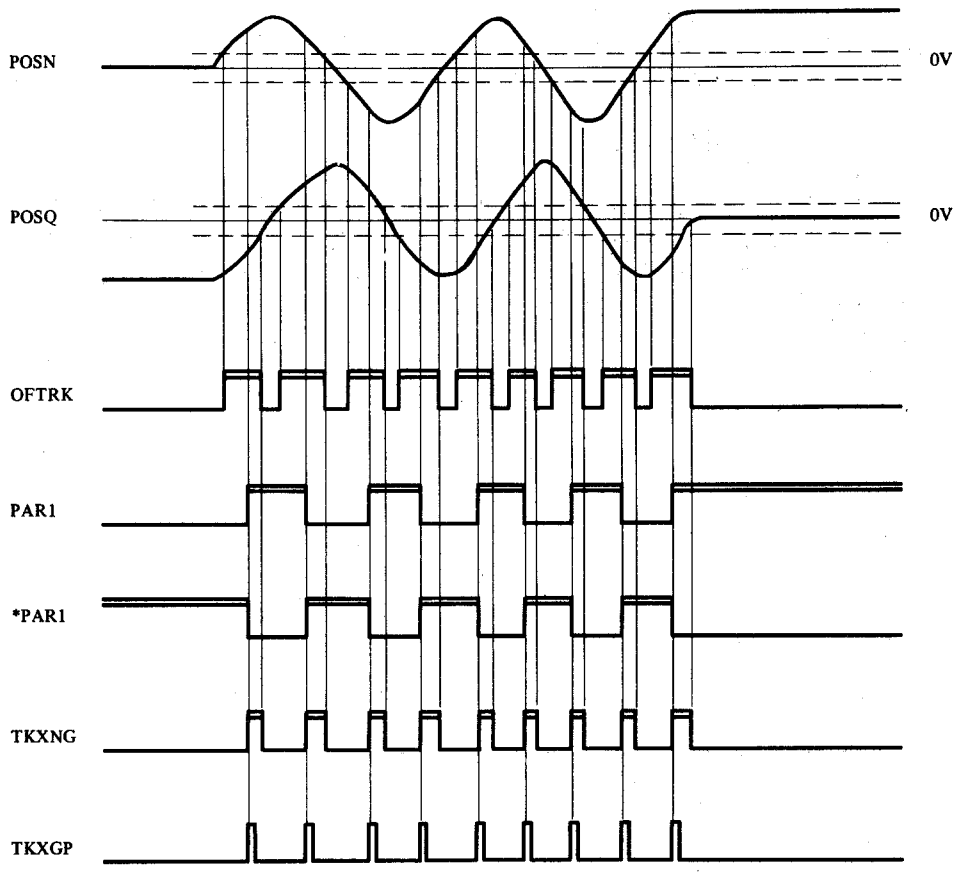


Figure 4.6.20 Position Level detector

m. Target speed generator

The target speed generator, consisting of the DA converter, non-linear circuit, and switching circuit, determines the carriage traveling speed during seek or rezero operations.

(a) DA converter

The DA converter converts the digital positional difference (held to 144 when the number of remaining cylinders is not less than 144) stored in the difference register. The number of cylinders over which the carriage is to be moved is set and is decremented whenever the track crossing pulse is detected, decreasing the analog stair step waveform as the carriage approaches the desired cylinder.

The DA converter is also used in converting the offset amount (3-bit digital amount) to the corresponding analog voltage at offset operation.

(b) Non-linear circuit

The non-linear circuit combines the stair step signal sent from the DA converter with the signal sent from the smoother to smooth the waveform and, at the same time, generates the deceleration curve which is optimum from viewpoints of decelerating current and the access time. In addition, it applies the output from the charge-discharge circuit, which is controlled by the Acceleration signal (ACCEL), to prevent excessive accelerating force from being applied to the carriage.

(c) Switching circuit

The switching circuit selects the target velocity for seek, and rezero operations based on the reference voltage generated by means of various logic signals derived from the servo logic circuit.

Figure 4.6.22 is the timing chart of the signals during the rezero operation.

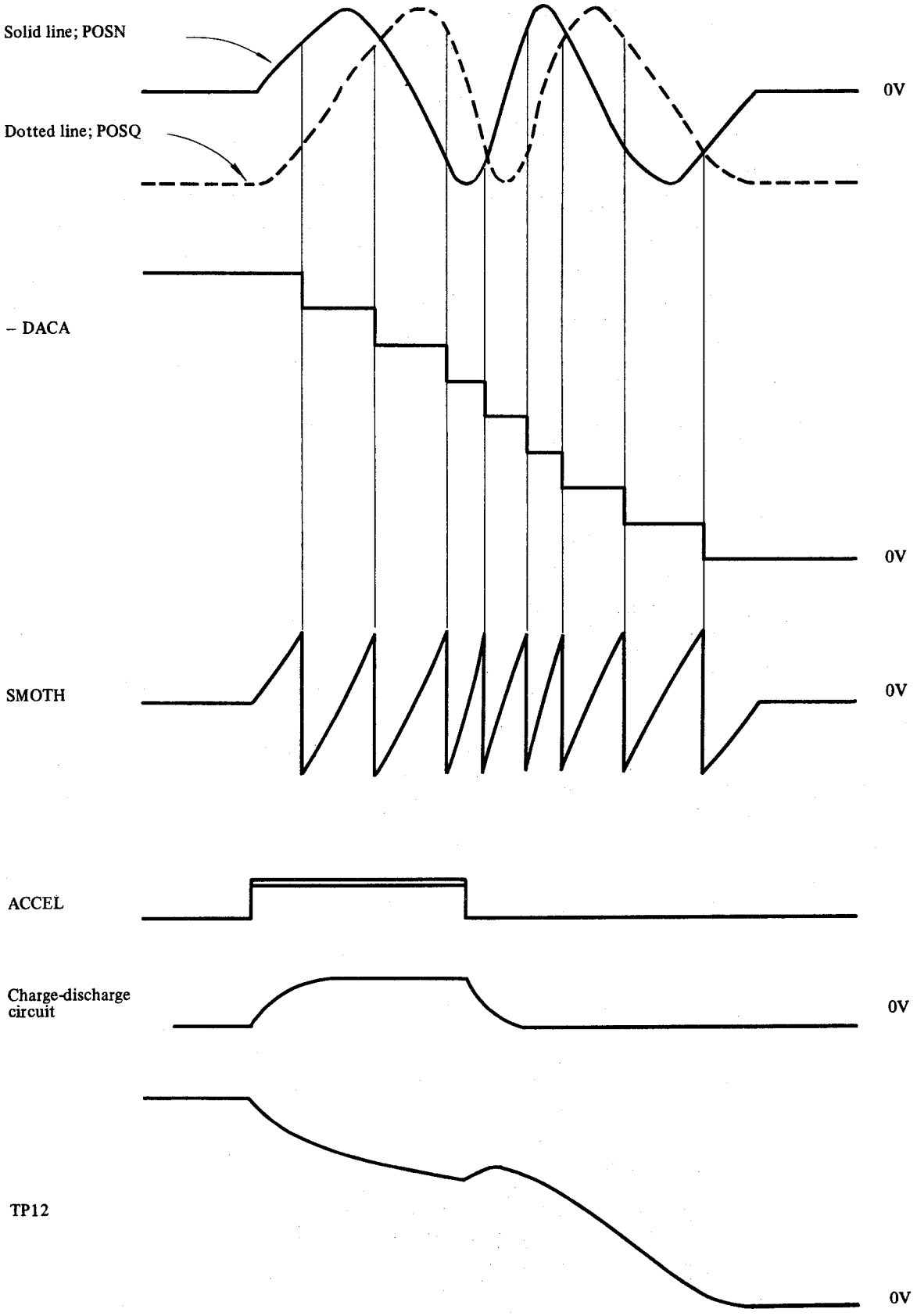


Figure 4.6.21 Target speed

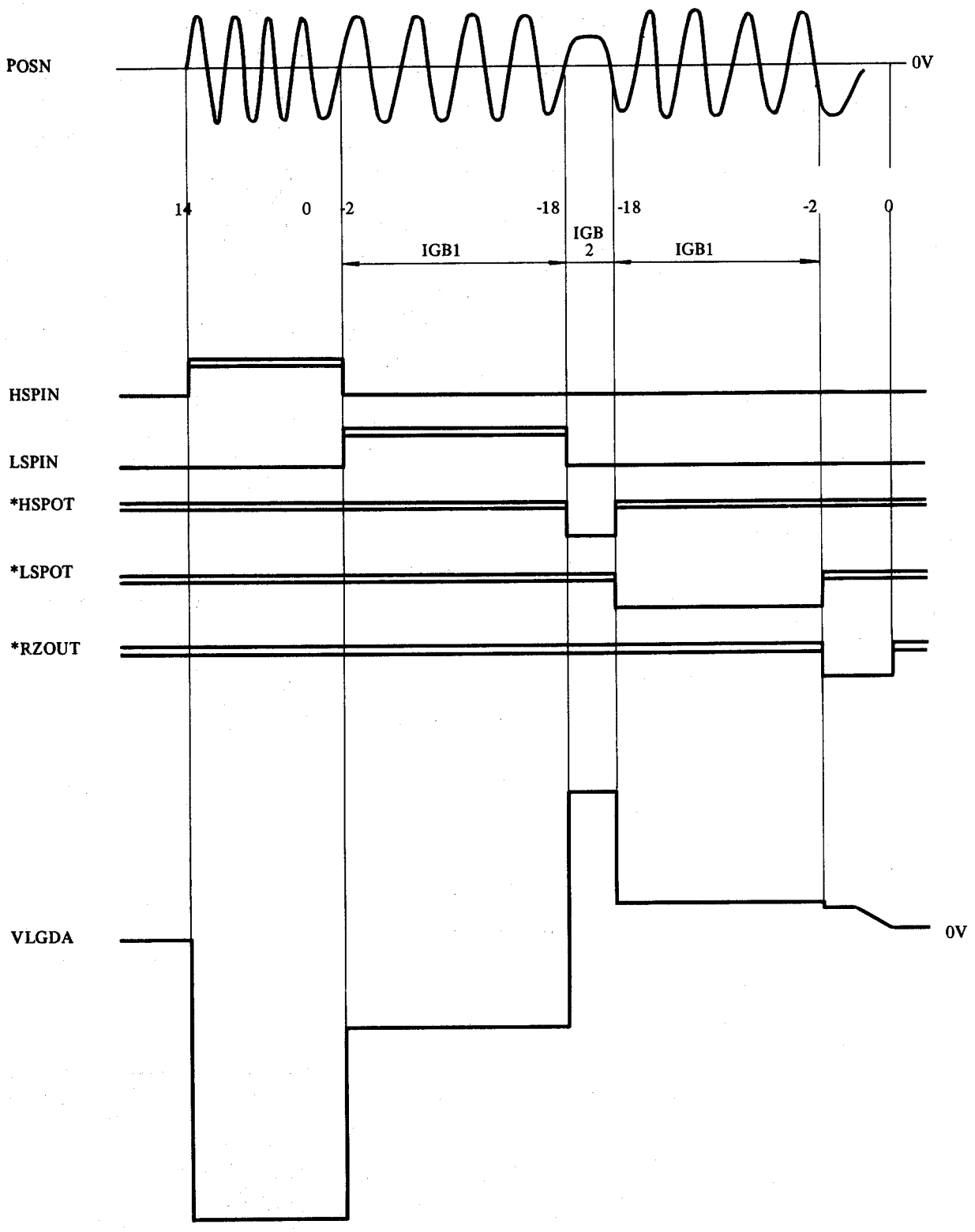


Figure 4.6.22 Signals in rezero operation

n. Velocity detector

The velocity detect circuit generates the velocity signal by composing the differentiated value of the position signal (POSN and POSQ) for the linear portion with the integrated value of the coil current (CSNSE) in the rotary actuator. The output of the state detect circuit is used to select the linear portion of the position signal.

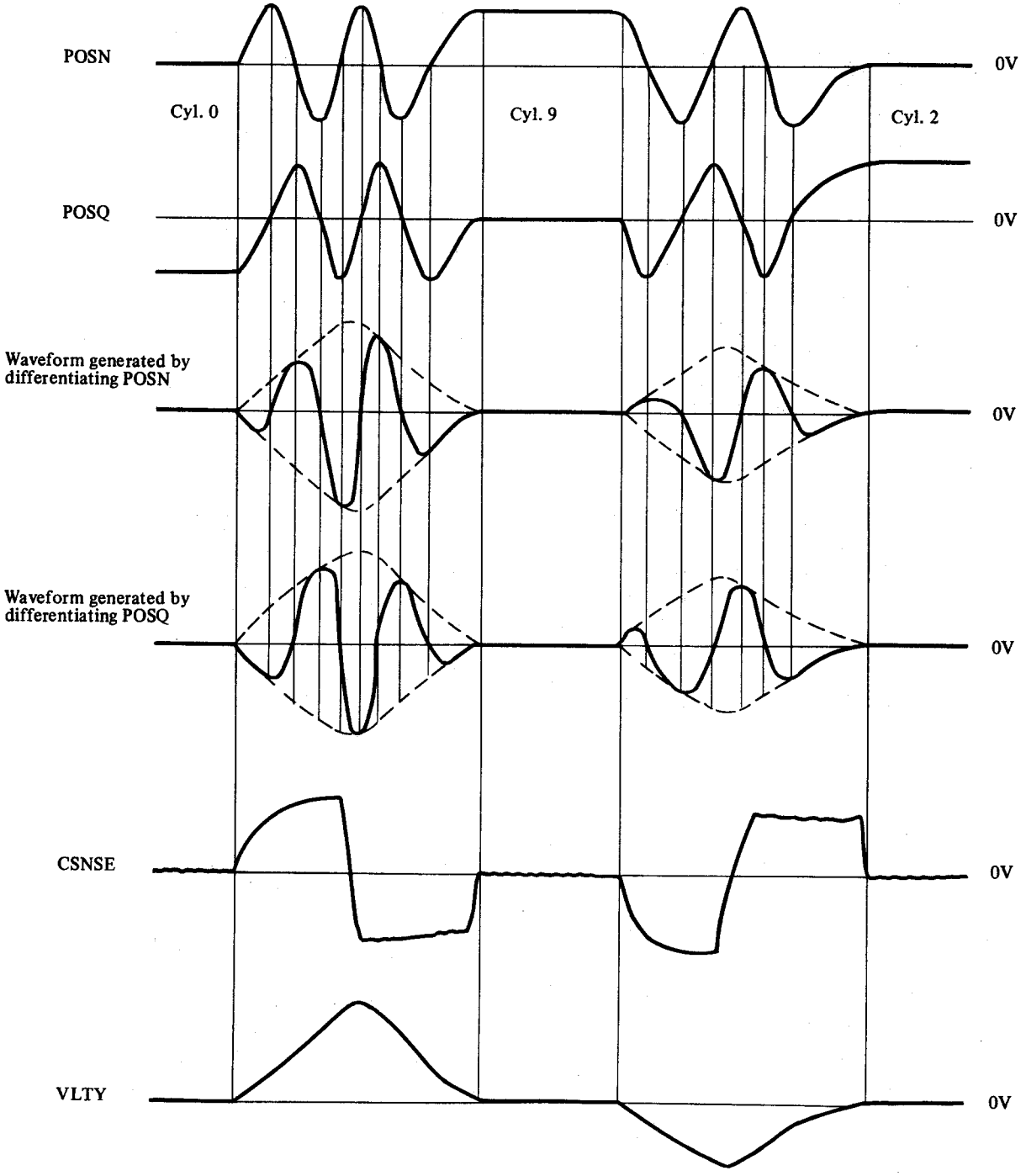


Figure 4.6.23 Velocity

o. Velocity level detector

The velocity level detect circuit slices the velocity signal (VLTY) and sends CAPVL and *VG20I signals to the logic circuit. CAPVL, which indicates the carriage Velocity is lower than the specified value, is used to prevent the rezero operation from being started while the carriage is being moved at high speed, and also used to provide switching moment from coarse control to fine control. *VG20I, which indicates the carriage velocity is too high during the rezero operation, is used to monitor the access mechanism.

p. Velocity error circuit

The velocity error circuit generates the velocity error signal (VLERR) which indicates a difference between the target velocity signal VLGDA and the actual velocity signal VLTY. It also generates, by slicing VLERR, the end accelerate signal (ENDAC) which indicates the end of acceleration.

q. End decelerate detector

The end decelerate detect circuit generates the End Decelerate signal (*ENDDC) which indicates switching of the control mode from the coarse control to the fine control. That is, the circuit generates *ENDDC after the specified time has elapsed from the moment *ONTRK goes low and *EQUAL is low. At this time, CAPVL is used to indicate that the velocity is lower than the specified velocity.

r. Timer

The timer is used to generate the Track Following Timer signal (TFTMR) which informs the logic circuit that the access operation has been completed normally after the specified time period from the moment the control mode had been switched to the fine control or, it sends the Access Timeout signal (ACTMO), which indicates that the operation has not been completed within the specified time period after the start of movement. It also provides the time setting signal (M3M, *OFINT) to be used during an offset operation.

s. Reference voltage generator

The reference voltage generator generates -4V and +6V reference DC voltages to be supplied to the head IC on the servo head assembly. They are also used as reference voltages for various level detect circuits and the desired velocity level during a rezero operation.

t. Servo logic

The servo logic generates various signals used in coarse control and fine control based on the control logic signals sent from the logic circuit.

u. Power amplifier interface

This is the interface between the power amplifier for driving the rotary actuator and spindle motor and the servo circuit. When the coarse control operation is performed, the interface selects VLERR by means of *CORSE. When the fine control is performed, the interface selects POSER by means of *GLNMD. One of these signals is sent to the power amplifier as the power amplifier drive signal (PADRV). When the rezero operation is performed, the amplifier gain of PADRV is reduced to prevent excessive acceleration force from being applied to the carriage and the head. In addition, a DC bias circuit is provided to prevent the head from moving away from the CSS area when the spindle motor rotation is lower than the specified rotational speed (3,600 rpm -2%). The interface for the power amplifier of the rotary actuator includes the Current Sense signal (CSNSE) which is proportional to the current in the drive coil and the Overcurrent signal (OVCRT) which indicates excessive current flow. The interface for the power amplifier of the spindle motor includes the Spindle Start signal (*SPSTT) which indicates the start/stop of the motor, the Speed Alarm signal (SPALM) which indicates that the rotational speed is not in the range of 3,600 rpm $\pm$2%, and the Hall alarm signal (HALM) which indicates an abnormal condition of the hall-effect element used for monitoring the spindle motor rotation.

v. Power amplifier for rotary actuator

This amplifier provides drive coil current proportional to PADRV sent through the power amplifier interface and sends CSNSE to the servo circuit upon detection of coil current. In addition, it sets OVCRT high to indicate an abnormal condition when current of 5A or more flows for 0.7 seconds or longer.

w. Power amplifier for spindle motor

This amplifier controls the spindle motor so that it rotates at the specified speed (3,600 rpm) when the Spindle Start signal (*SPSTT) is "0". The rotational speed is checked by the output of three hall-effect elements which are contained in the motor. The rotational speed is compared with the specified speed each time the disk rotates; if the speed is lower than 3,600 rpm, the amplifier provides current and, if the speed is higher than 3,600 rpm, current does not flow, allowing the disks to be rotated by the force of inertia. The Speed Alarm signal (SPALM) is changed from "1" to "0" when the rotational speed comes up to 3,600 rpm, and changed to "1" again when the rotational speed is not within the specified range.

The rotational speed monitor circuit is reset when the disk is restarted.

The following diagram shows the outputs of the hall-effect elements.

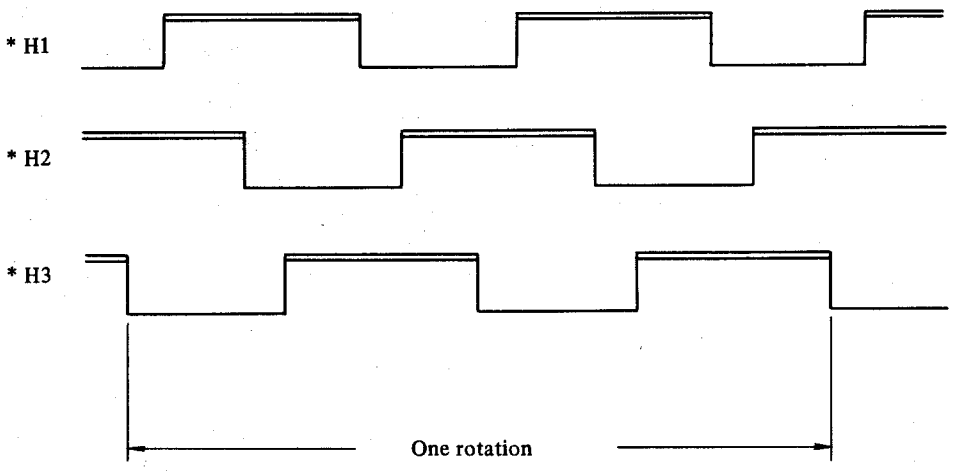


Figure 4.6.24 Outputs of hall-effect elements

4.6.4 Read/Write function

(1) Read/Write basic principles

When the disk is rotating at a nominal 3,600 rpm, a read or write may be performed. The basic principles of the read/write function are as follows:

a. Data Write

During a write instruction, a 0 or 1 is recorded by reversing the direction of the current flowing in the data head coil. When the direction of the current flowing in the head coil is reversed, the magnetic poles of the head are reversed and the direction of magnetic flux at the gap is revered. The direction of magnetization of the surface of the disk is then reversed. Each flux reversal means that a "1" or "0" has been recorded on the disk.

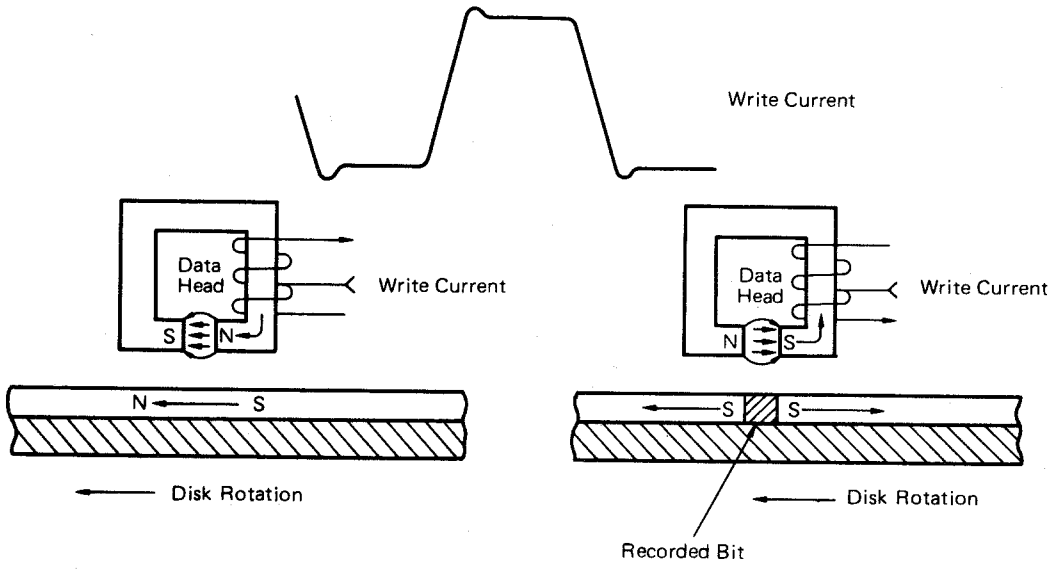
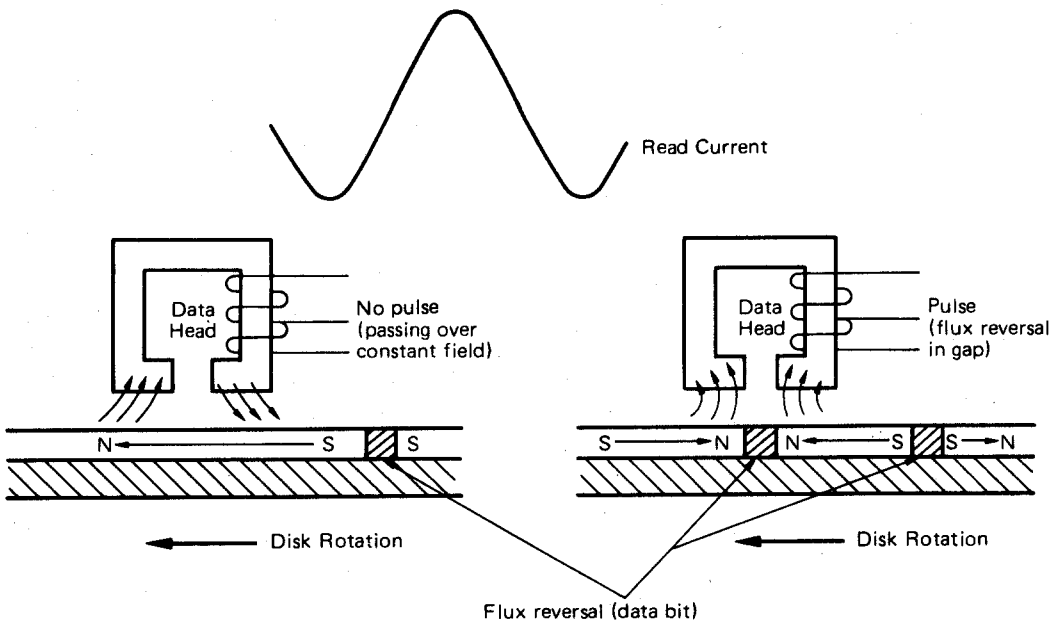


Figure 4.6.25 Data Write

b. Data Read

During a read instruction, the transitions recorded on the surface of the disk are detected by the head gap. When magnetized in the same direction continuously, no output is produced. However, when a recorded bit (180-degree flux reversal in the horizontal direction) passes under the head gap, the mangetic flux flowing in the ring and coil is reversed and an output pulse is obtained.



Figue 4.6.26 Data Read

(2) 2-7 coding

The M2361A uses the 2-7 recoridng method. Since data is transferred between the controller and the disk drive unit by NRZ transmission, the NRZ data is converted to 2-7 data by an encoder in the drive, then recorded on the magnetic disk. In read operation, the recorded data in 2-7 code is read and converted to NRZ data by a decoder, then transferred to the controller.

The 2-7 code is a code of 4 to 8 bits in length converted from NRZ data of 2 to 8 bits in length according to the specified rule shown in Table 4.6.4. The 2-7 code contains continuous 0s from 2 to 7 between two 1s.

In the 2-7 code, the minimum code bit period is more than 1.5T (T indicates the data bit period) for any input data combination.

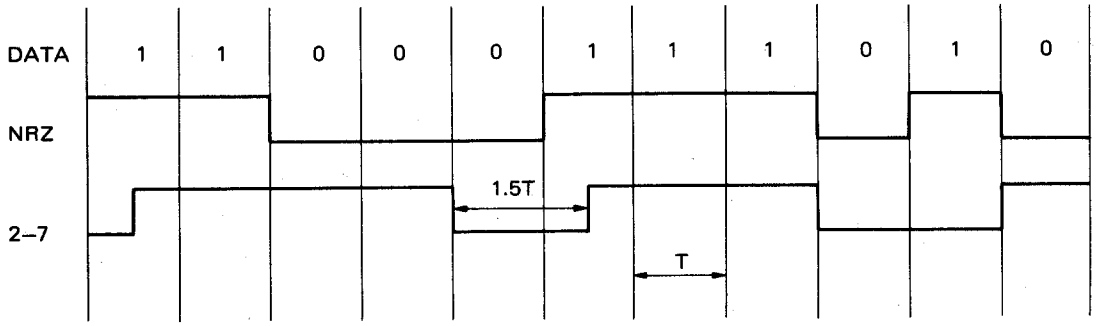


Figure 4.6.27 2-7 coding

Table 4.6.4 Translation Between NRZ and 2-7 Codes

NRZ Code words	2-7 Code words
1 0	0 1 0 0
0 1 0	1 0 0 1 0 0
0 0 1 0	0 0 1 0 0 1 0 0
1 1	1 0 0 0
0 1 1	0 0 1 0 0 0
0 0 1 1	0 0 0 0 1 0 0 0
0 0 0	0 0 0 1 0 0

(3) Write operation

The Write circuit block diagram is shown in Figure 4.6.28. The servo data written on the disk are read by the servo head, and the PLO circuit generates 2 bit cell FCO1 signal. The VCO1 signal is applied to the VFO (variable frequency oscillator).

The VFO is synchronized with the VCO1 signal and generates four times the frequency o the VCO1; VFO2F signal. VFO2F signal is applied to the ENCODER circuit; VFO1F is also sent to the control unit as the Read Write Clock signal. The control unit must use this Read Write Clock signal in the case of Write Clock (WTCL) and Write Data (WTDT) generation.

When a write command is issued from the control unit after head selection, the WTDT and WTCL signals are sent to the disk drive, and the WTDT signal is clocked by the positive-going edge of WTCL signal.

The clocked WTDT signal is applied to Encoder circuit, WTDT of NRZ code is converted into Encode Write Data (ENCWD) of 2-7 code, (refer to Table 4.5.2), and circuit is converted into Write Data Pulse (WDTA).

When the Write Gate signal goes true, the WDTA signal is toggled by a flip-flop and passes throught he Read/Write Bus Switch IC. It is then applied to the Head IC (HIC) chips as Data X (DX) and Data Y (DY) signals. The write current is supplied to the selected HIC chip through a Write Current (WTCR) line.

The block diagram of write operation is shown in Figure. 4.6.28.

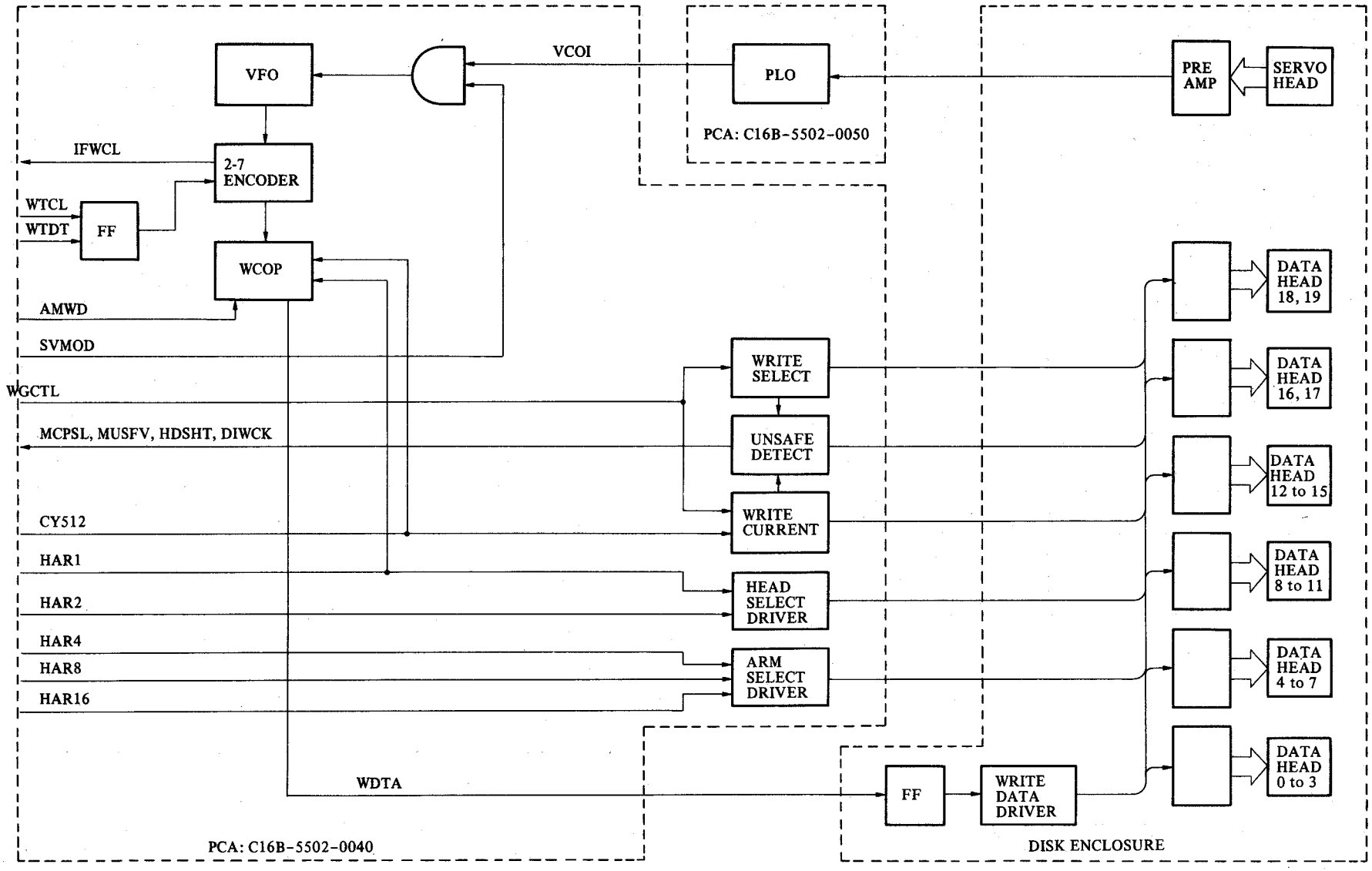


Figure 4.6.28 Write Operation Block Diagram

(4) Write compensation

When the bit density (BPI) is high on a disk surface, and a read operation is performed, a peak shift phenomenon appears, which tends to widen the narrow part of the bit spacing because of mutual magnetic interference of the bits. When such a phenomenon appears, reading of the data will deviate from the correct bit spacing, causing errors. The write compensation circuit measures this peak shift beforehand so the data is written by shifting the peak in the opposite direction of the peak shift appearing during the read operation.

The NRZ write data (WTDT) sent from the control unit is clocked by the positive-going edge of the WTCL signal. It is then synchronized with the internal one-bit cell clock (CLKA) which is issued from the sync decision window circuit, comparing the phase difference between WTCL and VFO2F by enabling the Write Gate Control (WGCTL) signal.

The NRZ data synchronized with the internal clock is applied to 2-7 encoder circuit. The output of the 2-7 encoder circuit is applied to six-bit shift register. Each output of the six-bit shift register is applied to write compensation circuit and then converted into 2-7 data pulse train with write compensation according to the truth table (as shown in Table 4.6.5). The preshift timing of write compensation is defined by Early (EY), on-Time (OT) and Late (LT) signals.

The block diagram and timing chart are given in Figure 4.6.29 and Figure 4.6.30.

Table 4.6.5 Write Compensation Truth Table

REGISTER STATUS			WRITE COMP			2-7
ENCWD	ESR2	ESR5	EY	OT	LT	DT
1	1	1	0	1	0	1
0	1	1	1	0	0	1
0	1	0	0	1	0	1
1	1	0	0	0	1	1
*	0	*	*	*	*	0

Note: EY: Early Pulse
OT: On-Time Pulse
LT: Late Pulse
DT: Data Pulse

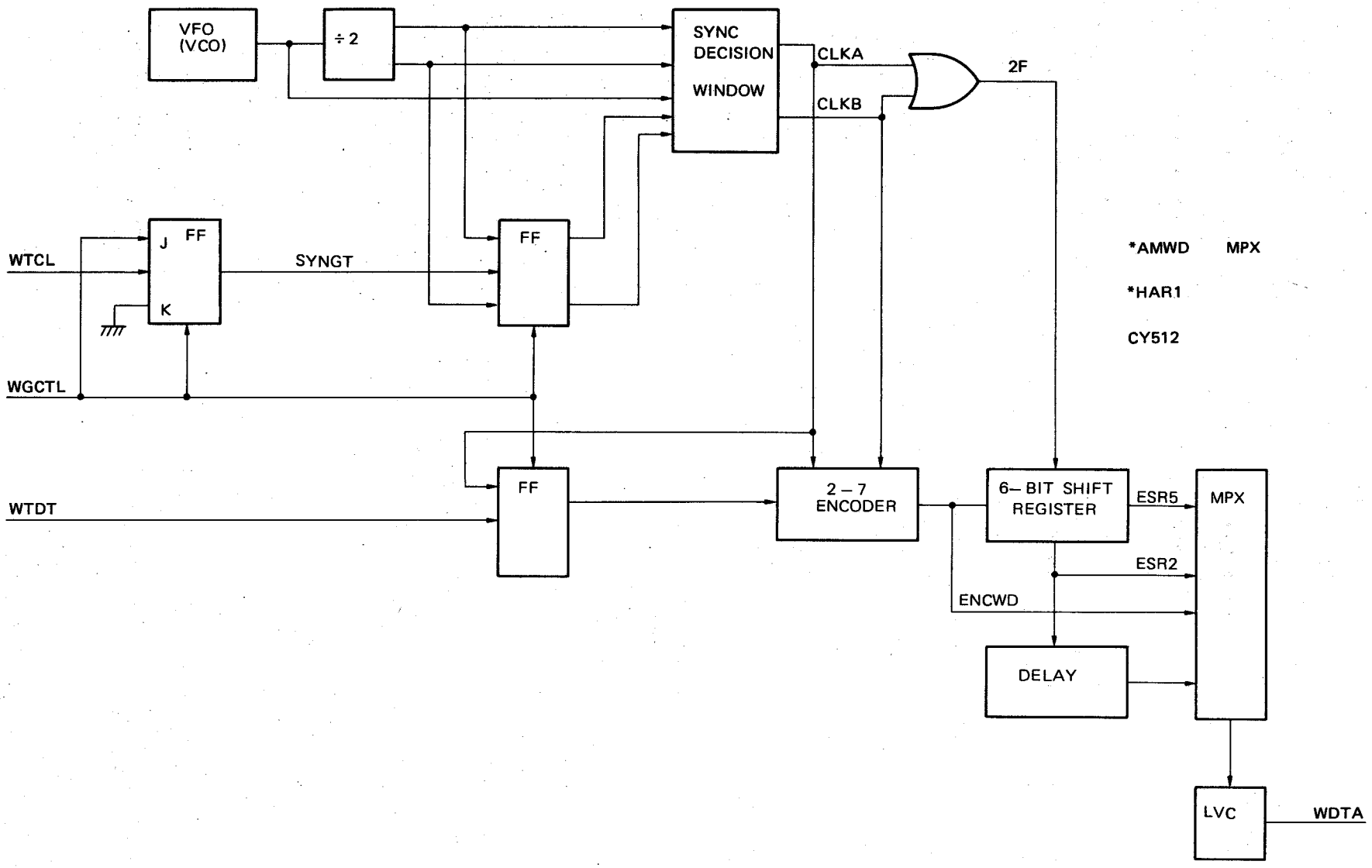


Figure 4.6.29 2-7 Coding, AM Write and Write Compensation Block Diagram

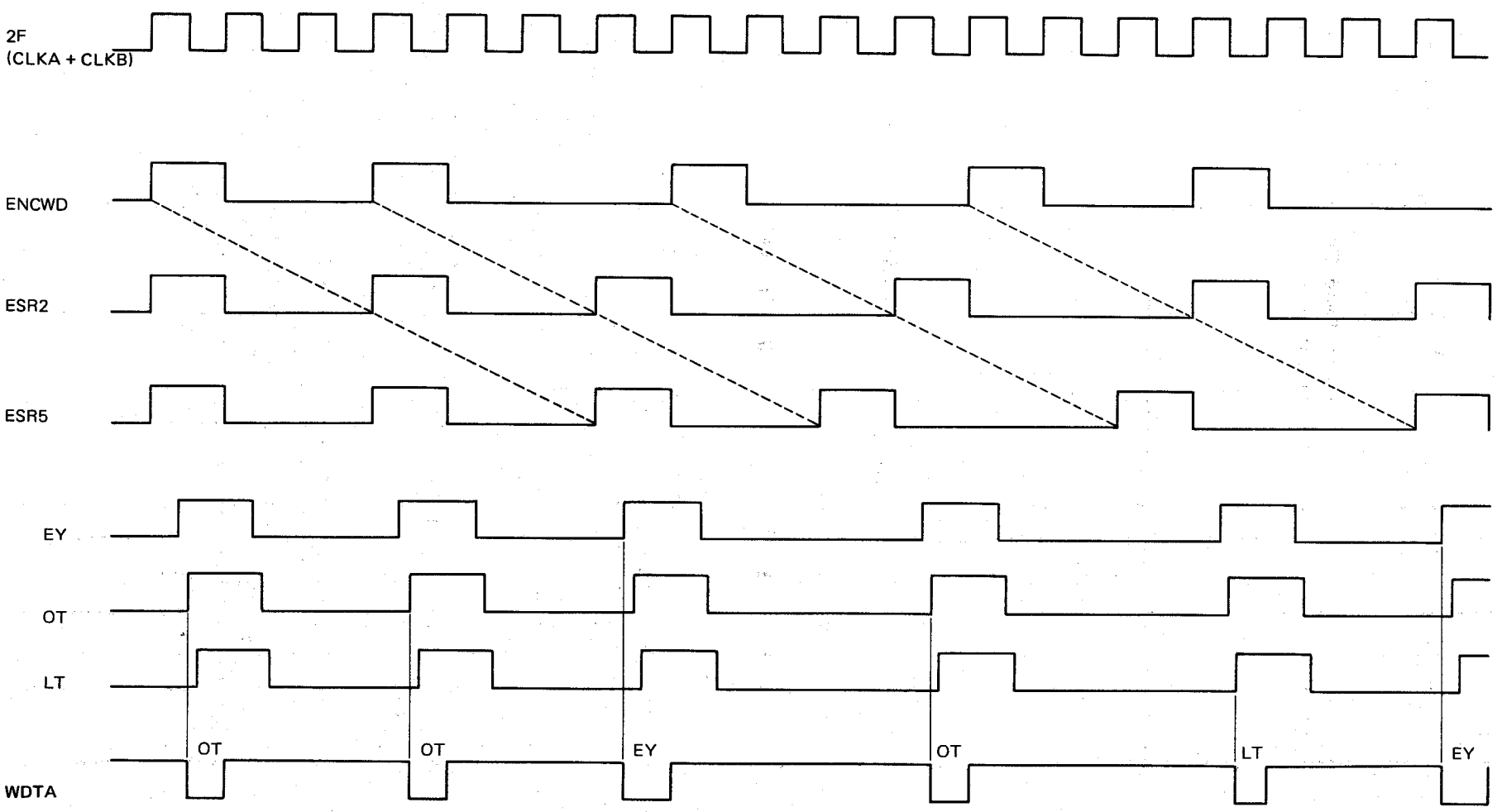


Figure 4.6.30 Write Compensation Timing Chart

(5) Read operation

A read operation is initiated by enabling Read gate (Set read/write command, Bus out bit 3). The analog read/write circuit is always in read condition so long as the WENB signal is disabled.

The HIC outputs (DX, DY) are applied to the Read/Write Bus Switch IC (MB4316), amplified, and then sent to Receiver (RB) circuit as shown in Figure 4.6.31.

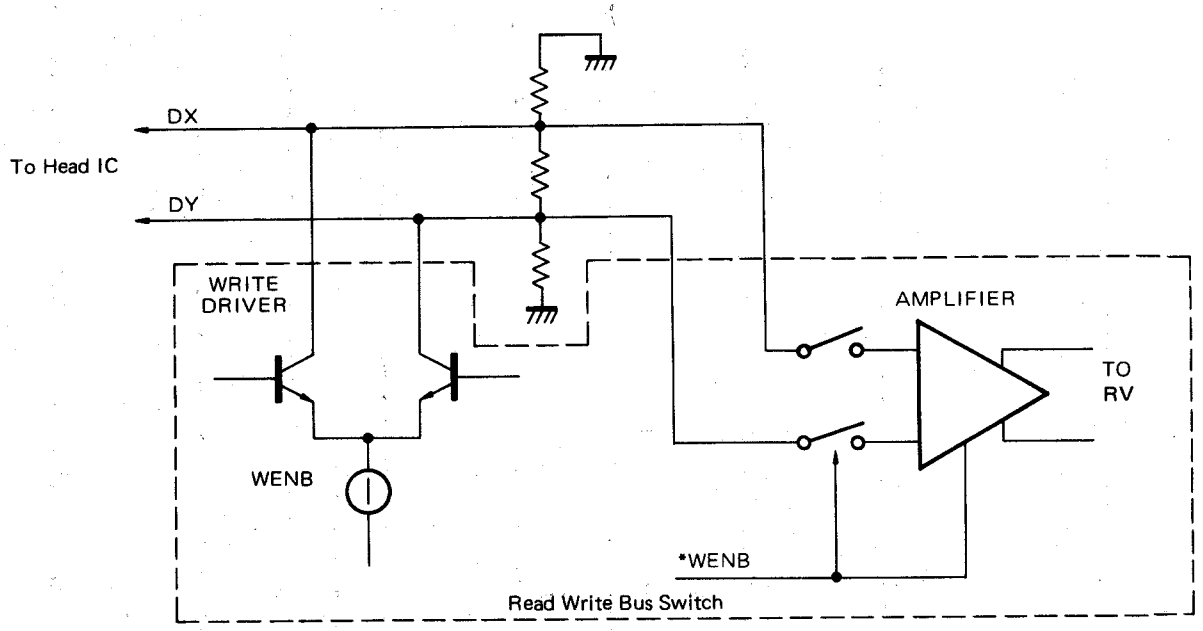


Figure 4.6.31 Read Write Bus Switch

The Receiver circuit output signal is then applied to the Automatic Gain Control (AGC) circuit.

The AGC circuit consists of an AGC amplifier IC (MB43303), Equalizer circuit, LPF (Low Pass Filter) circuit and Reak Detector IC (MB4311).

The AGC circuit develops the control voltage to the AGC amplifier and holds AGC output amplitude (200 mVp-p) at a constant level. The output of the AGC circuit is amplified to 2.0 Vp-p, and sent to the Pulse Shaper circuit.

After going false of WGCTL, the read circuit is activated, however, a read-transient which is caused by the DC unbalance of the read pre-amplifier will occur. Therefore, Not Squelch Gate signal (NSQHG) is enabled about 2μsec after the Write Gate Control signal (*WGCTL) goes high. The NAQHG signal suppresses this read transient. The profile of read after write transient wave form is shown in Figure 4.6.32.

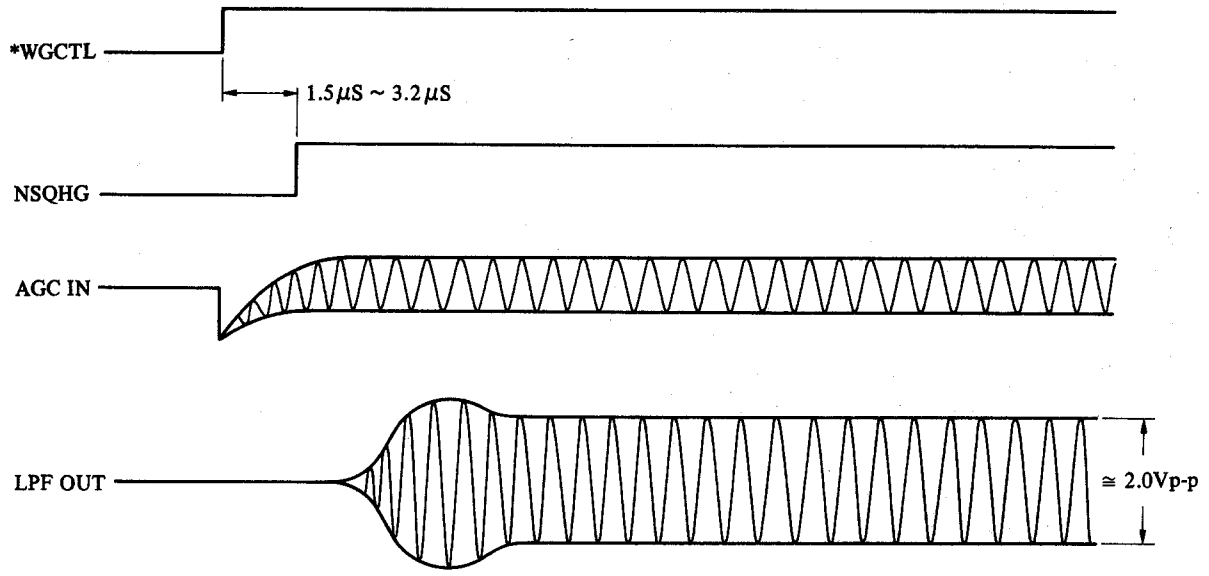


Figure 4.6.32 AGC Squelch Function

The Address Mark (AM) which is four-bytes area is used for indicating the beginning of record. (Refer to Figure 4.6.33).

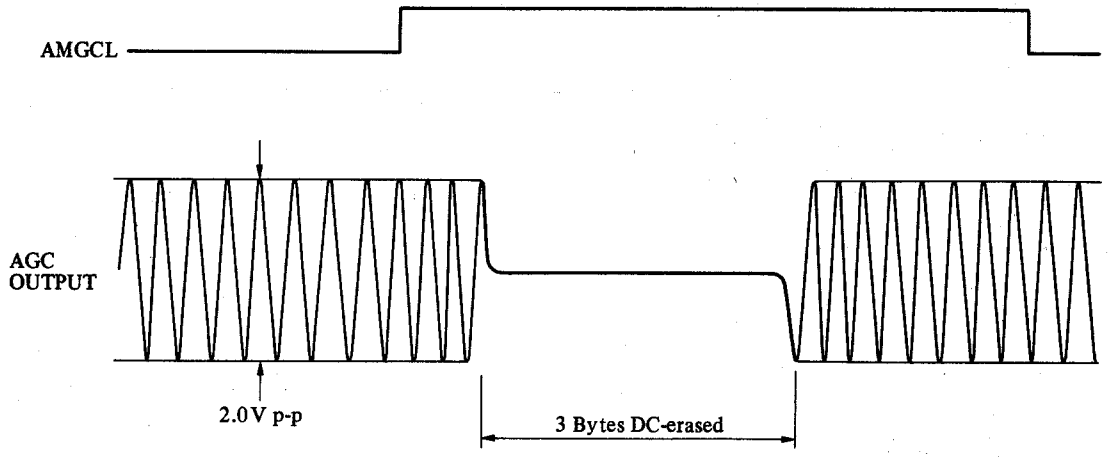


Figure 4.6.33 AM Enable on Read Signal

The AGC output signal is applied to Pulses Shaper which is the analog-to-digital convertor circuit.
The block diagram is shown in Figure 4.6.34.
The output of Pulse Shapter which is Raw Data (RAWD), is sent to the VFO circuit.

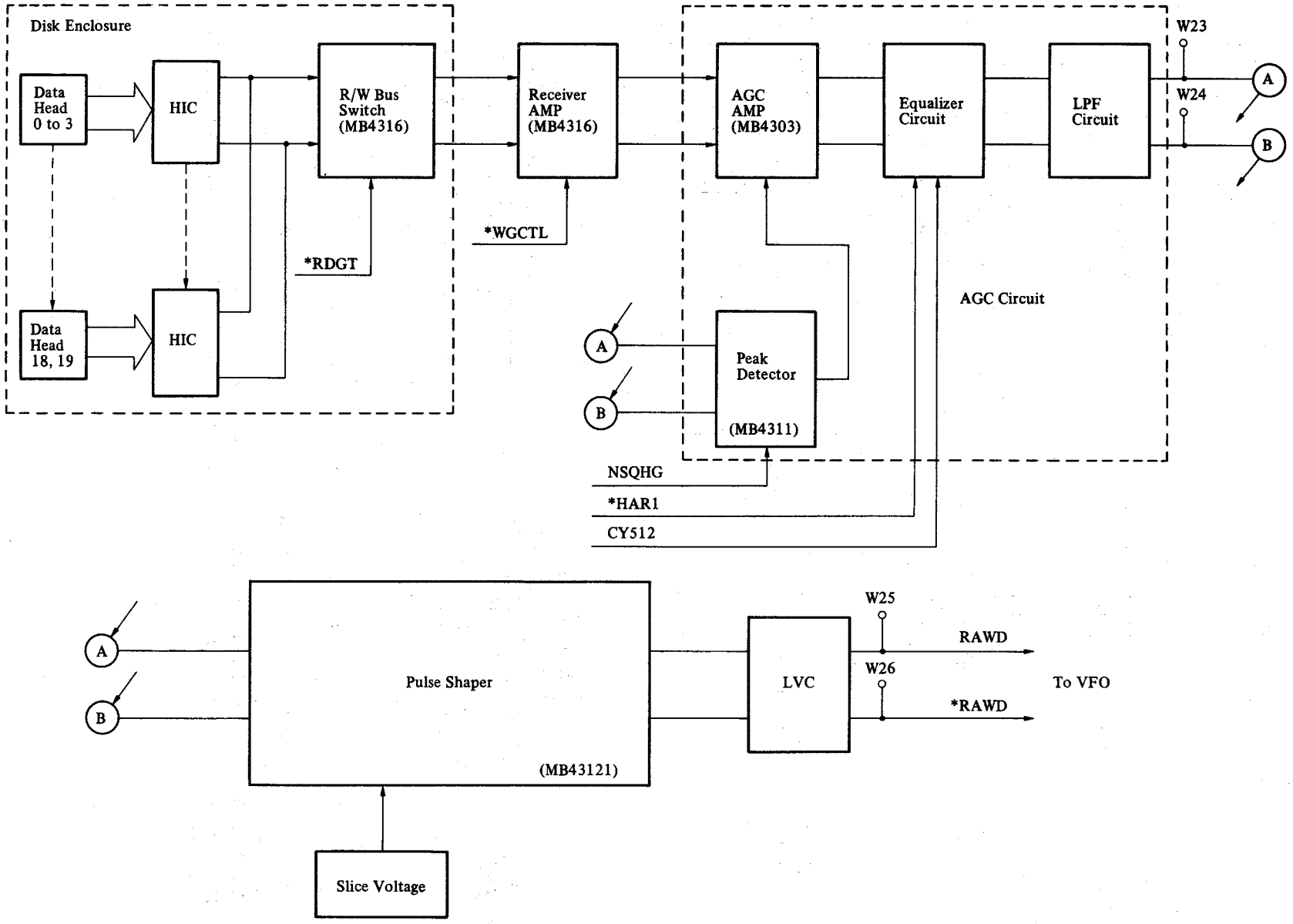


Figure 4.6.34 Read Operation Block Diagram

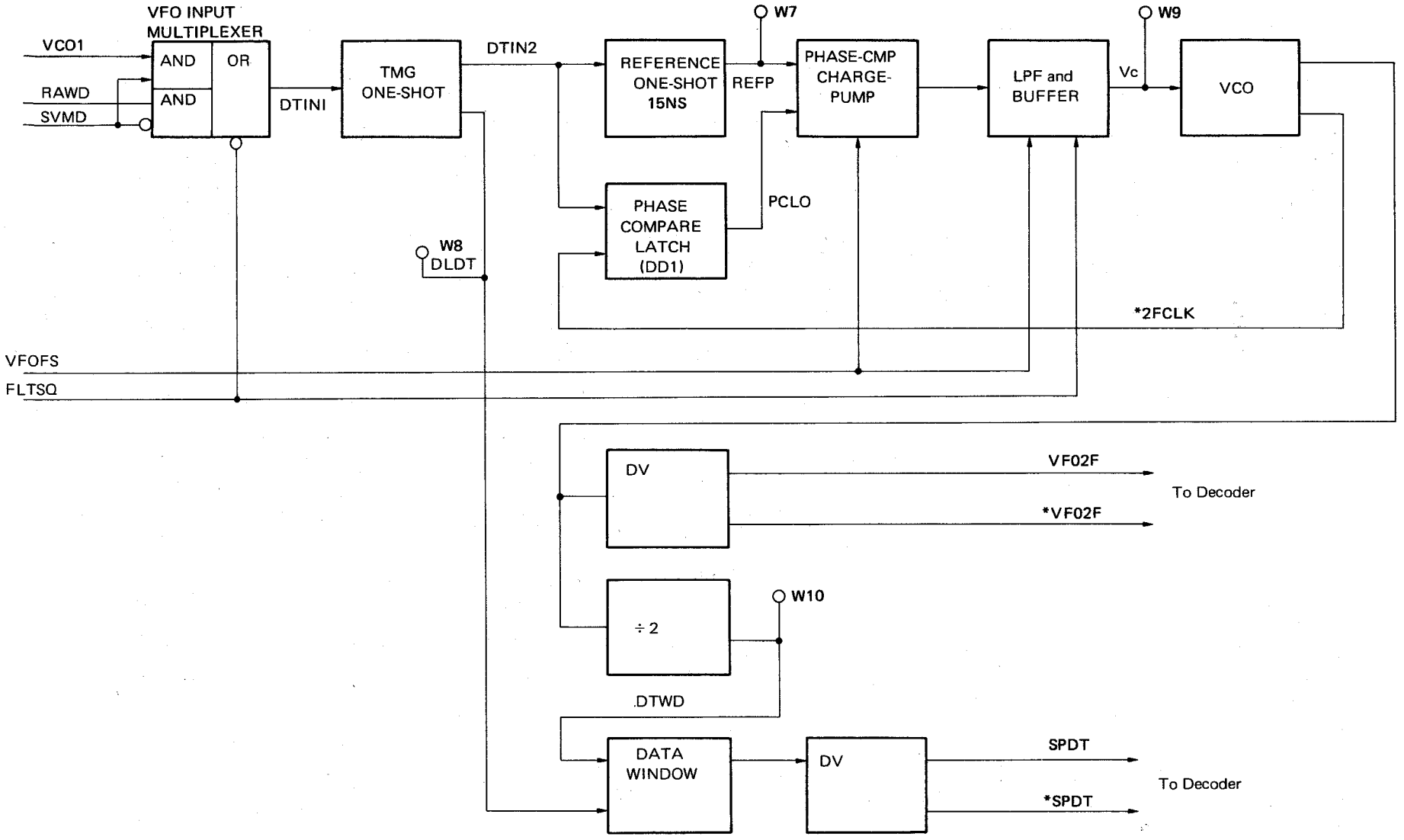


Figure 4.6.35 VFO Block Diagram

(6) VFO

The Variable Frequency Oscillator (VFO) output is synchronized with VCO1 signal from the servo information during non-read operation, and with the Raw Data (RAWD) signal from the data track during a read operation. The block diagram of the VFO circuits is shown in Figure 4.6.35.
The VFO are composed of the following circuit.

. VFO Input Multiplexer
. Time-Margin Measurement (TMG) One-Short
. Reference One-Shot
. Phase compare Latch
. Phase Comparator and Charge Pump
. Low Pass Filter and Buffer
. Voltage Controlled Oscillator (VCO)

a. VFO Input Multiplexer

The VFO input multiplexer controls the VFO input. During an initial seek operation or a RTZ operation, this circuit inhibits an input of data into the VFO circuit by enabling the Filter Squelch (FLTSQ) signal. This causes the VCO to oscillate at a free-running frequency. After an initial seek operation or a RTZ operation, the VFO Input multiplexer controls the transmission of the VCO1 or RAWD signals into the VFO circuit.

During a non-read operation, the signal is applied to the VFO circuits by the enabling of the Servo Mode (SVMD) signal. During a read operation, the RAWDT signal is applied to the VFO circuits by disabling the SVMD signal. The VFO input multiplexer output, Data Input 1 (DTIN1), is applied to the TMG One-shot circuit.

b. TMG One-shot

The TMG One-shot circuit issues a Data Input 2 (DTIN2) signal to the Phase Comparator, and Reference One Shot circuit. It also issues Delayed Data (DLDT) signal to the Data Window circuit. The timing relation between DTIN2 and DLDT signals adjusted by potentiometer RV4 determines the read margin. (Refer to Figure 4.6.37)

c. Reference One-shot

The leading edge of the DTIN2 signal triggers the Reference One-shot, which issues a 16 ns Reference Pulse (REFP) signal to the Phase Comparator Charge Pump circuit.

d. Phase-Compare Latch

The leading edge of the DTIN2 signal sets the Phase-Compare Latch and the negative-going edge of *2F clock (*2F CLK) resets it. The Phase-Compare Latch issues a Phase-Compare Latch Output (PCLO) signal to the Phase Comparator Charge Pump circuit.

e. Phase Comparator and Charge Pump

The Phase Comparator Charge Pump circuit issues a Decreas frequency (DEC) signal when the VFO input phase is lagging, and an Increase frequency (INC) signal when the VFO input phase is leading, comparing the phases between DTIN2 signal and PCLO signal.

The INC or DEC signal drive the constant-current circuit to change or discharge the filter circuit (LPF and Buffer).

f. LPF and Buffer

The charge pump output is applied to a Low Pass Filter (LPF) and converted into DC voltage to control the VCO. During an initial seek operation or RTZ operation, the FLTSQ signal clamps the charge gump output to 0V to recalibrate the VFO function.

During an initial data read operation, a VFO Fast-Sync (VFOFS) signal is issued to the VFO circuit which increases the loop gain of the VFO circuit to widen the pull-in range, and to shorten the pull-in time for synchronization to the RAWD signal. At termination of the data read operation, the same function is activated for synchronization with the VCO1 signal.

The LPF and Buffer output is applied to two stages of an emitter-follower circuit. It controls the VCO frequency as a Control Voltage (Vc) signal.

g. Voltage Controlled Oscillator

The VCO issues ECL level output.

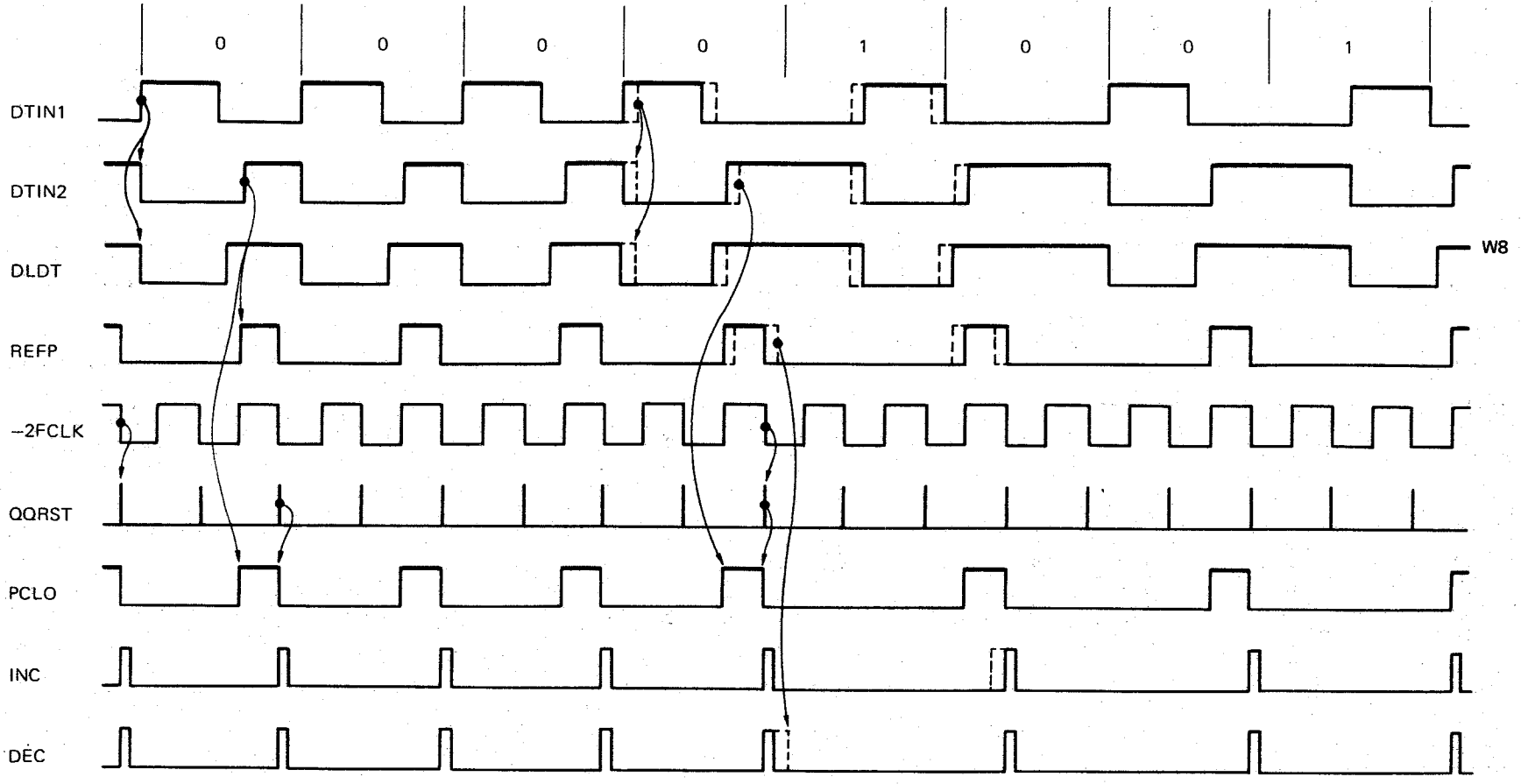


Figure 4.6.36 VFO Timing Chart

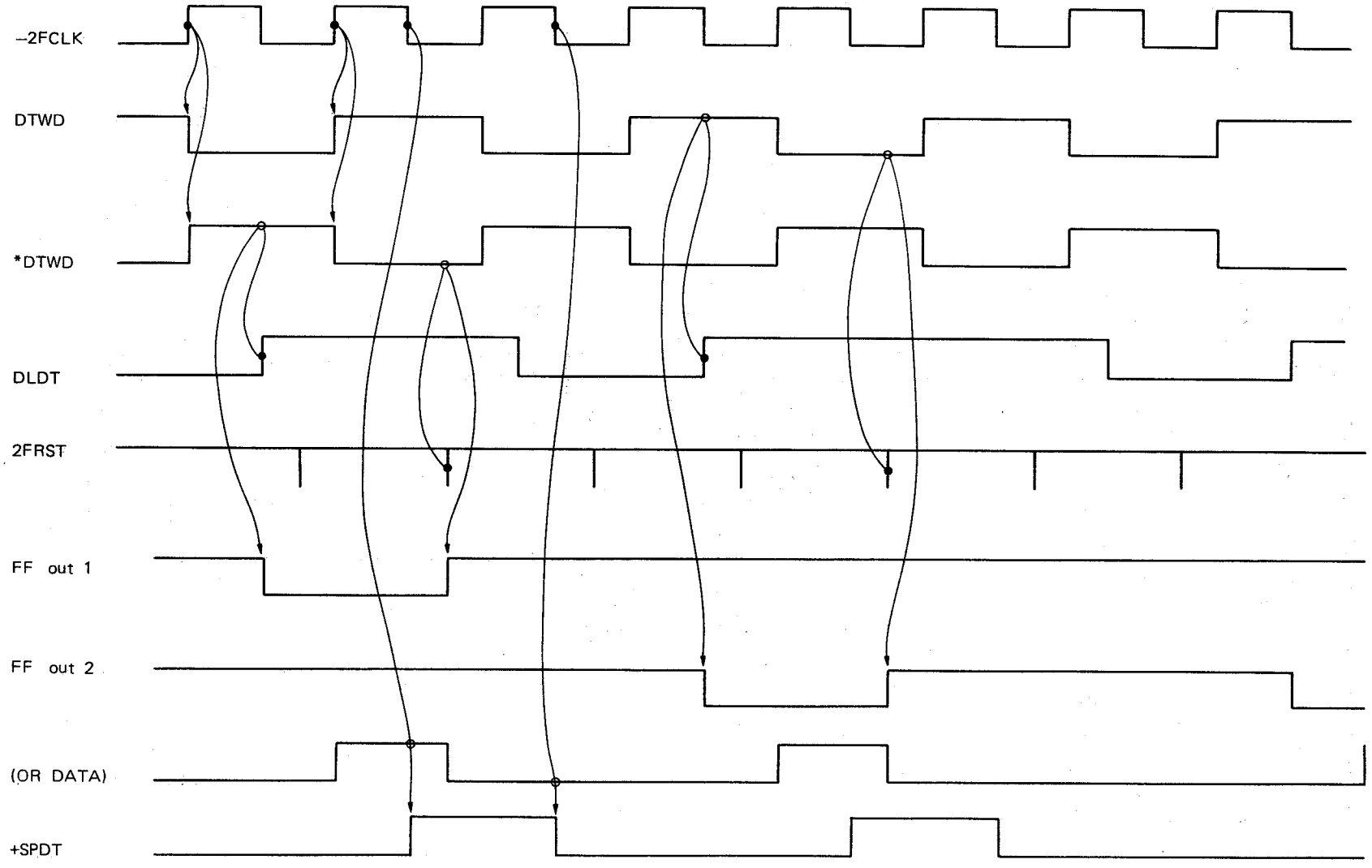


Figure 4.6.37 Data Window Timing Chart

(7) 2-7 decoder

The 2-7 decoder converts the 2-7 data into NRZ data.

The 2-7 data synchronized with 2F clock sent from VFO circuit is input to an eight-bit shift register, then sent to a decoder in which the 2-7 data is converted to NRZ data according to the conversion table listed in Table 4.6.4.

A read command starts the decoder detecting all 1 gap data. When this data is detected, the 2F clock is toggled to VFO clock (VFOCLK) to transfer the data. The 2-7 data is converted to NRZ data by gating VFOCLK. The NRZ data synchronized with VFOCLK is sent to the controller.

Figure 4.6.4.37 shows the abbreviated block diagram of the 2-7 decoder.

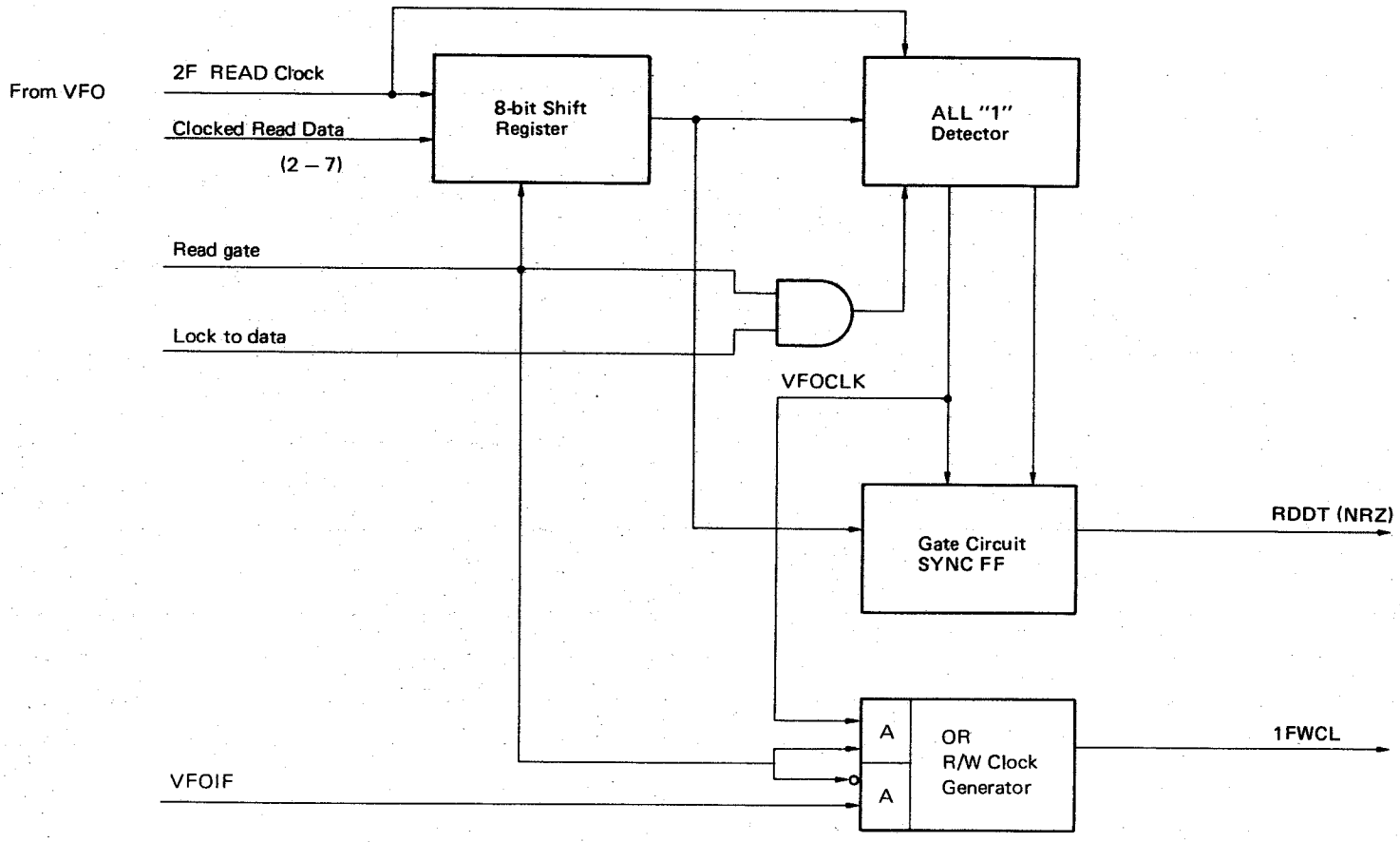


Figure 4.6.38 2-7 Decoder Block Diagram

CHAPTER 5 TROUBLESHOOTING GUIDE

5.1 Introduction

This chapter contains troubleshooting flow charts according to the error status on the drive and controller.

Note: Before any operation is attempted, maintenance personnel should read carefully Chapter 6 and fully understand the details of the procedures and tools required.

Check the following items before applying power to the drive after installation.

(1) Ensure that the AC line conditions satisfy the power supply requirements.

(2) Inspect the interface cables to ensure pin 1 on the cable goes to pin 1 of the connector at both the drive and the controller.

(3) If the drive is in a daisy chain mode with one or more drives, make sure that only the last drive has a line terminator installed.

(4) Ensure that the desired logical unit number (LUN) of the drive is set on the display panel and that each LUN in the system is unique. See Sub-section 3.4.8.

(5) Ensure that the correct sector count is set on the display panel. See Sub-section 3.4.9.

(6) Ensure that the other switches on the display panel are set correctly. See Sub-sections 3.4.2 to 3.4.4.

(7) Ensure that the File Protect switch is on the proper position to meet the system requirement. See Section 3.3.

(8) Ensure that all PCBs and cables are firmly seated.

5.2 Error State

The drive and the controller will issue the follwoing statuses.

Table 5.2.1 Error status

NOT READY	Not Ready status indicates drive is not ready.
FAULT	Fault status indicates a fault conditions has occurred in the drive.
SEEK ERROR	Seek Error status indicates a seek error has occurred in seek operation.
READ ERROR	Read Error status indicates a data error has occurred in read oeration.
AM MISSING	AM Missing status indicates that AM (Address Mark) has not found in read operation.

Maintenance Personnel can see the drive status and error state on the display panel and the operator panel. Refer to Sections 3.3 and 3.4 for detailed drive status and error state, and how to know the error state by drive state indicators (colored LEDs), state indicators (7-segment LEDs) and state switch (Toggle Switch) mounted on the display panel.

The trouble shooting guide is provided with the error state which is defined by indicators on the display panel and the operator panel.

The error state is shown in Table 5.2.1.

Table 5.2.2 Error state

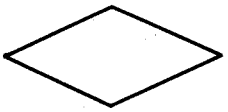
Error Status	Indicator Unit (HGAMU)						Indicators on the Operator Panel			Error State	Figure
	Unit State Indicator (LEDs)			State Indicator Lamp							
				State Switch	Lamp 1	Lamp 2					
	URDY	ACCK	FALT		Bit 1 2 4 8	Bit 1 2 4 8	Fault	Power on	Ready		
Not Ready	Off	-	-	-	- - - -	- - - -	-	Off	Off	Power Alarm } Not Ready	
	Off	-	-	2	- - - 1	- - - -	-	-	Off	Hall Alarm } Not Ready	
	Off	-	-	1	- - - -	1 - - -	-	-	Off	DE Sequence Check } Not Ready	
Fault	-	-	On	0	1 - - -	- - - -	On	-	-	Index Check	5.4.2
	-	-	On	0	- 1 - -	- - - -	On	-	-	Control Check	
	-	-	On	0	- - 1 -	- - - -	On	-	-	Multi Head Check	
	-	-	On	0	- - - 1	- - - -	On	-	-	Head Short Check	
	-	-	On	0	- - - -	1 - - -	On	-	-	Write Current On Read Check	
	-	-	On	0	- - - -	- 1 - -	On	-	-	Write Transition Check	
	-	-	On	0	- - - -	- - 1 -	On	-	-	Delta I Write Check	
	-	-	On	0	- - - -	- - - 1	On	-	-	Servo Off-Track	
Seek Error	-	On	-	1	- 1 - -	- - - -	-	-	-	Access Timeout Check	
	-	On	-	1	- - 1 -	- - - -	-	-	-	Over Shoot Check	
Read error	-	-	-	-	- - - -	- - - -	-	-	-	Read Error	
AM Missing	-	-	-	-	- - - -	- - - -	-	-	-	AM Missing	

5.3 Troubleshooting Symbol

The troubleshooting flow charts contain the procedures to pursue trouble causes starting from error status information.

The following conventions are provided to aid understanding the symbols used in the trouble shooting flow charts as shown in Table 5.3.1.

Table 5.3.1 Symbol of flow chart

Symbol	Description
	Terminal. Starting point of the trouble.
 ( )	Decision, go ahead according with YES or NO. (Reference test point.)
	Connector, go ahead same-numbered symbol in the same sheet.
	Connector, go ahead same-numbered symbol in another sheet.
	Process.

5.4 Troubleshooting Flow Chart

In this paragraph, the following charts are provided.

Figure 5.4.1 Not Ready
Figure 5.4.2 Fault
Figure 5.4.3 Seek Error
Figure 5.4.4 Read Error
Figure 5.4.5 AM Missing (for only Soft Sector Mode)

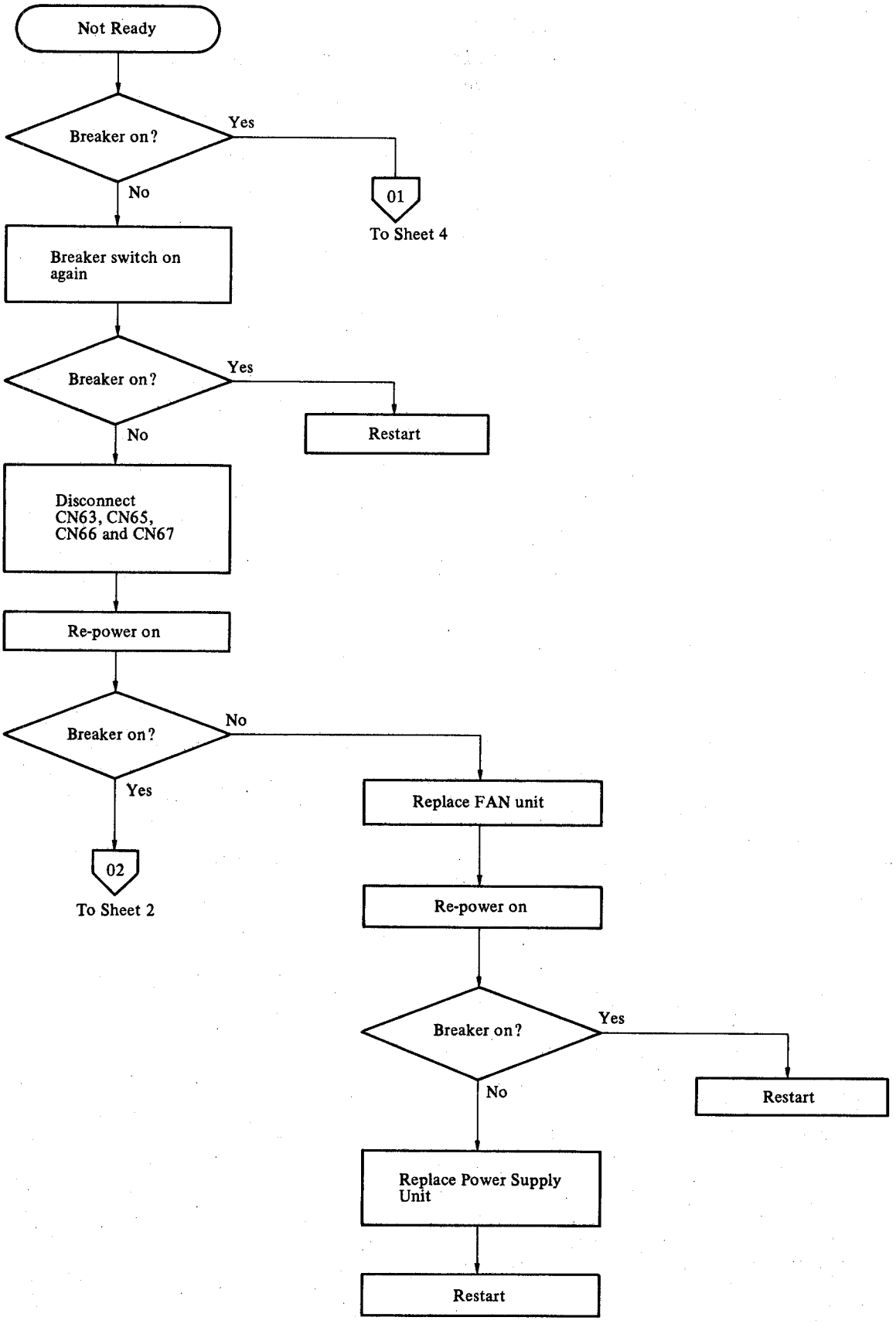


Figure 5.4.1 Not Ready flow chart (Sheet 1 of 5)

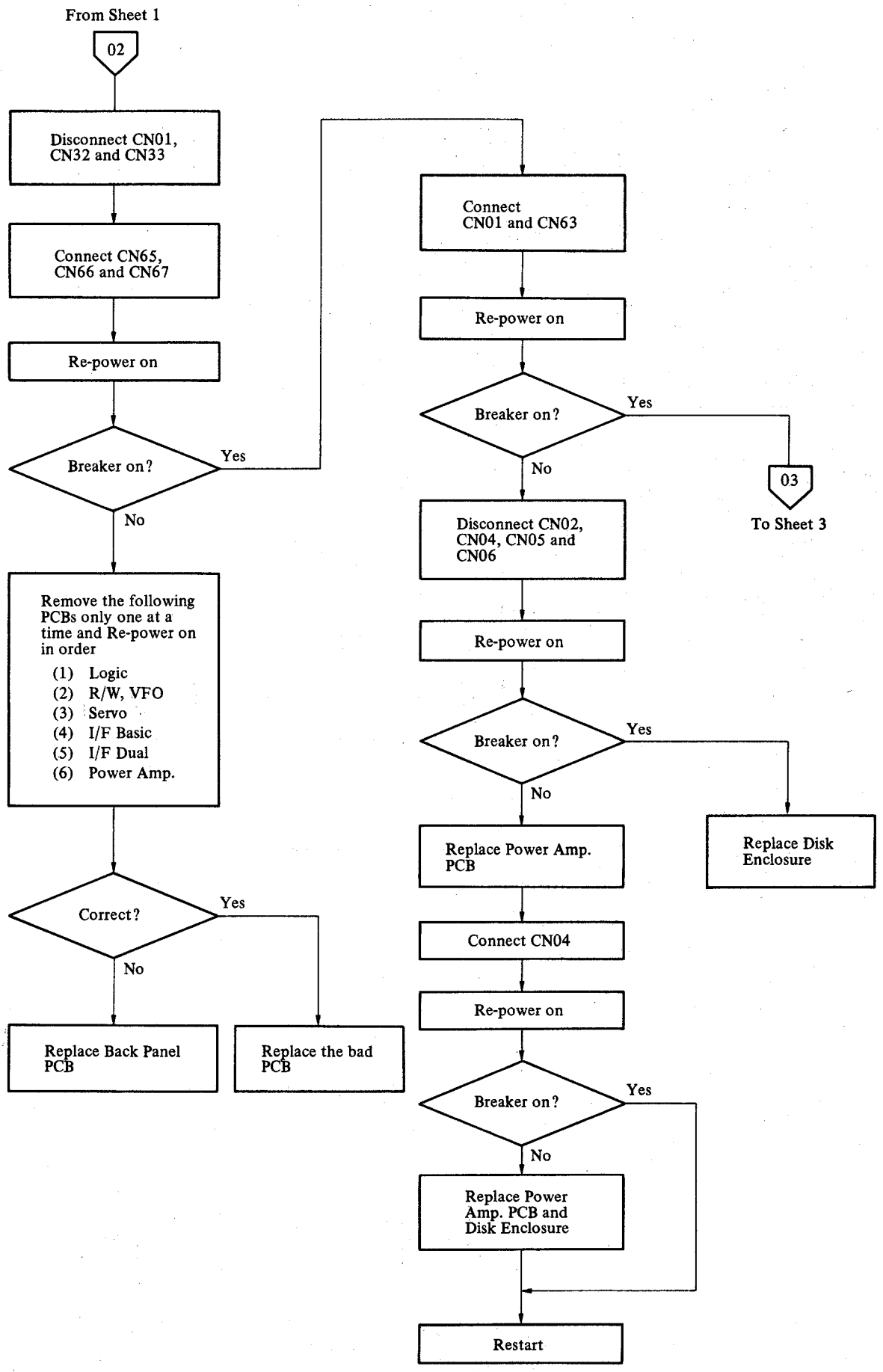


Figure 5.4.1 Not Ready flow chart (Sheet 2 of 5)

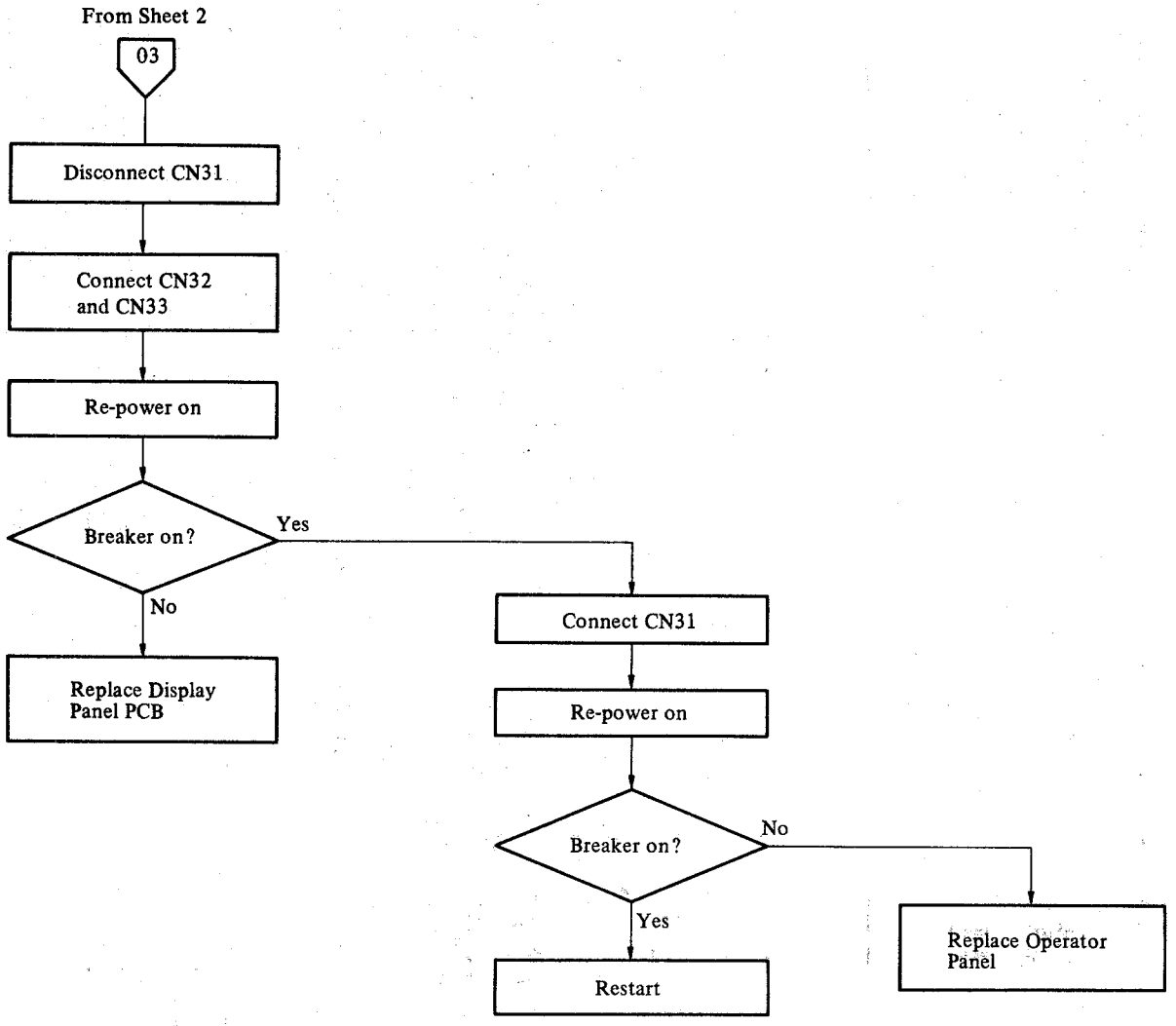


Figure 5.4.1 Not Ready flow chart (Sheet 3 of 5)

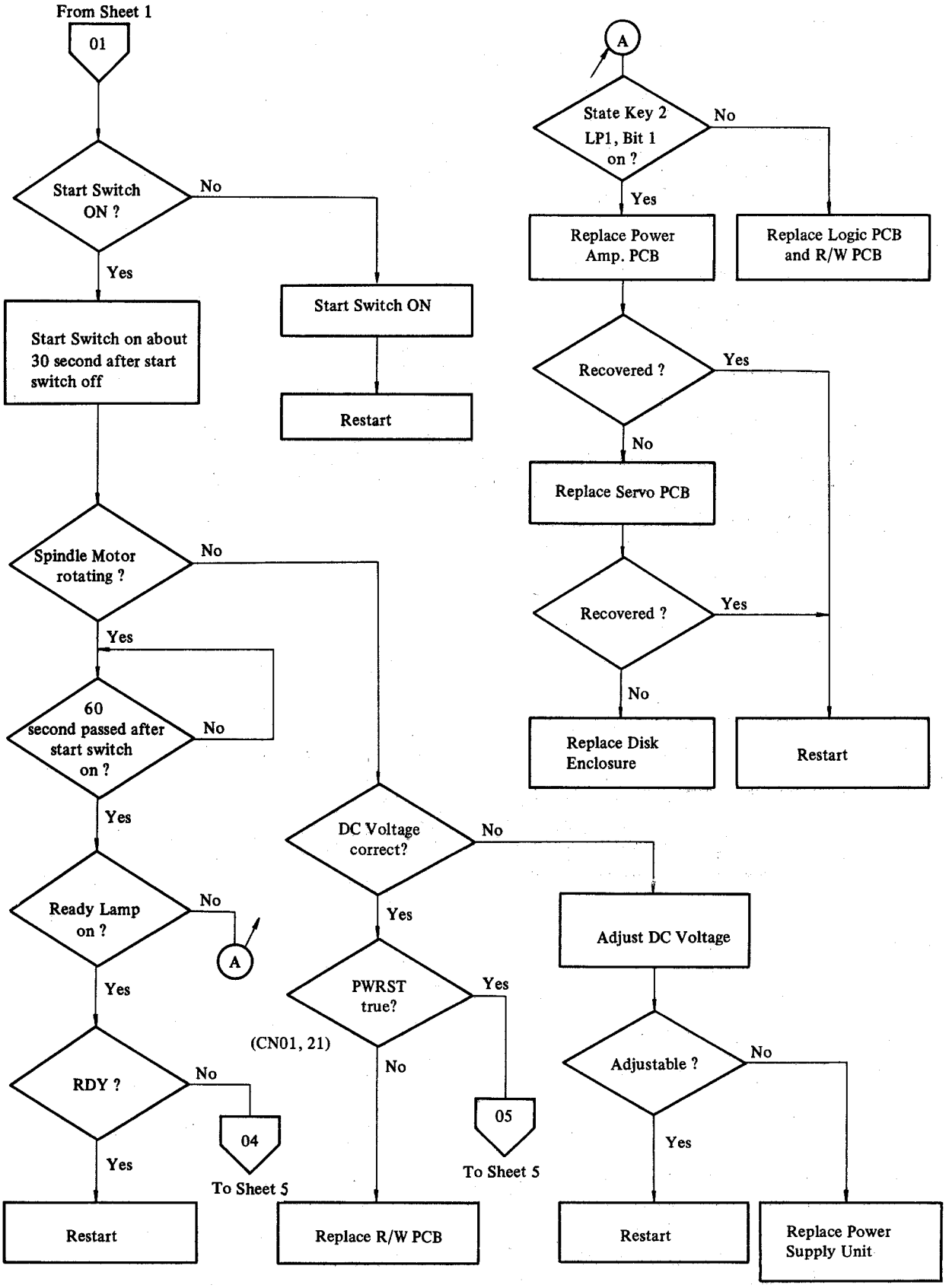


Figure 5.4.1 Not Ready flow chart (Sheet 4 of 5)

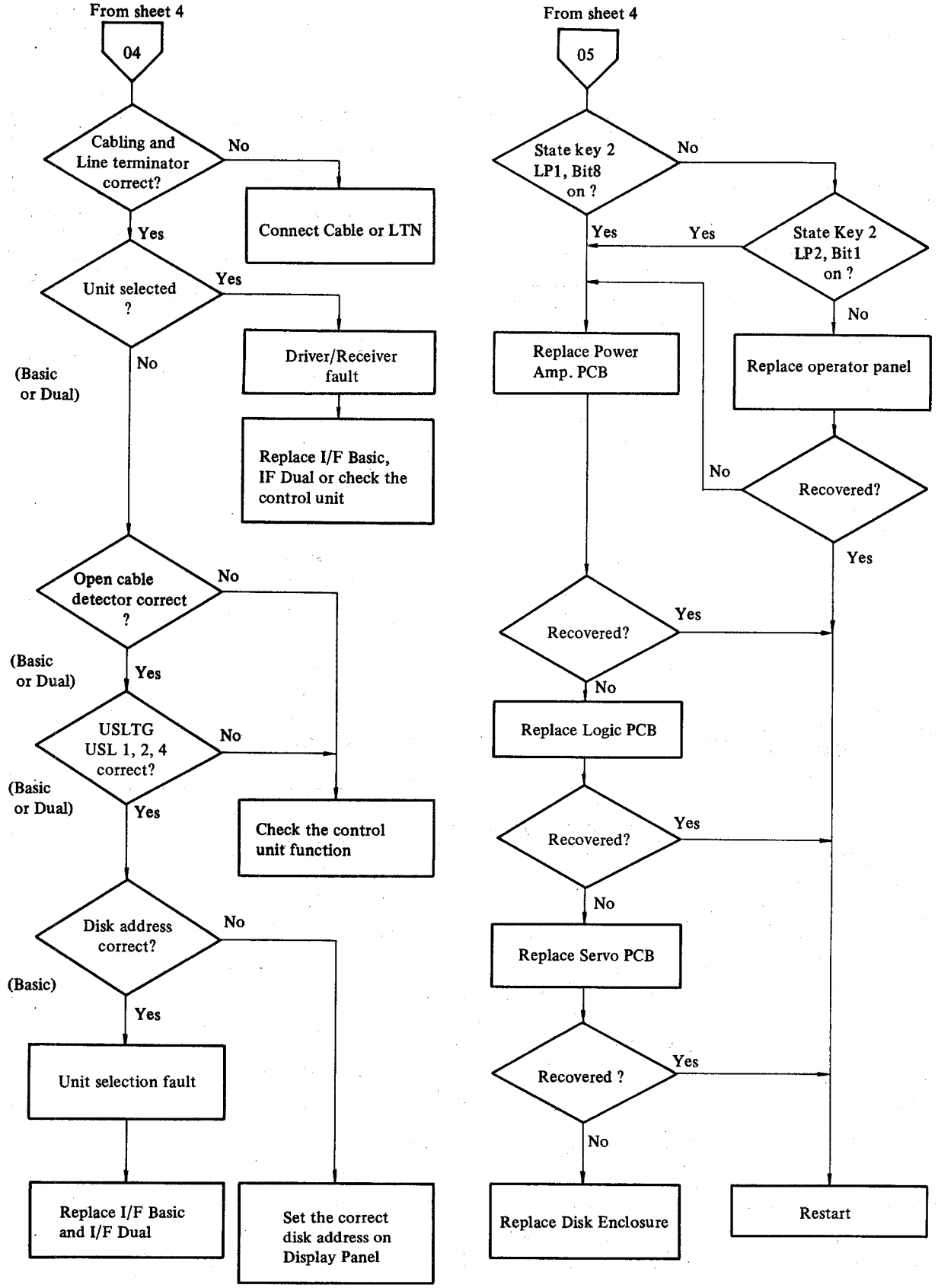


Figure 5.4.1 Not Ready flow chart (Sheet 5 of 5)

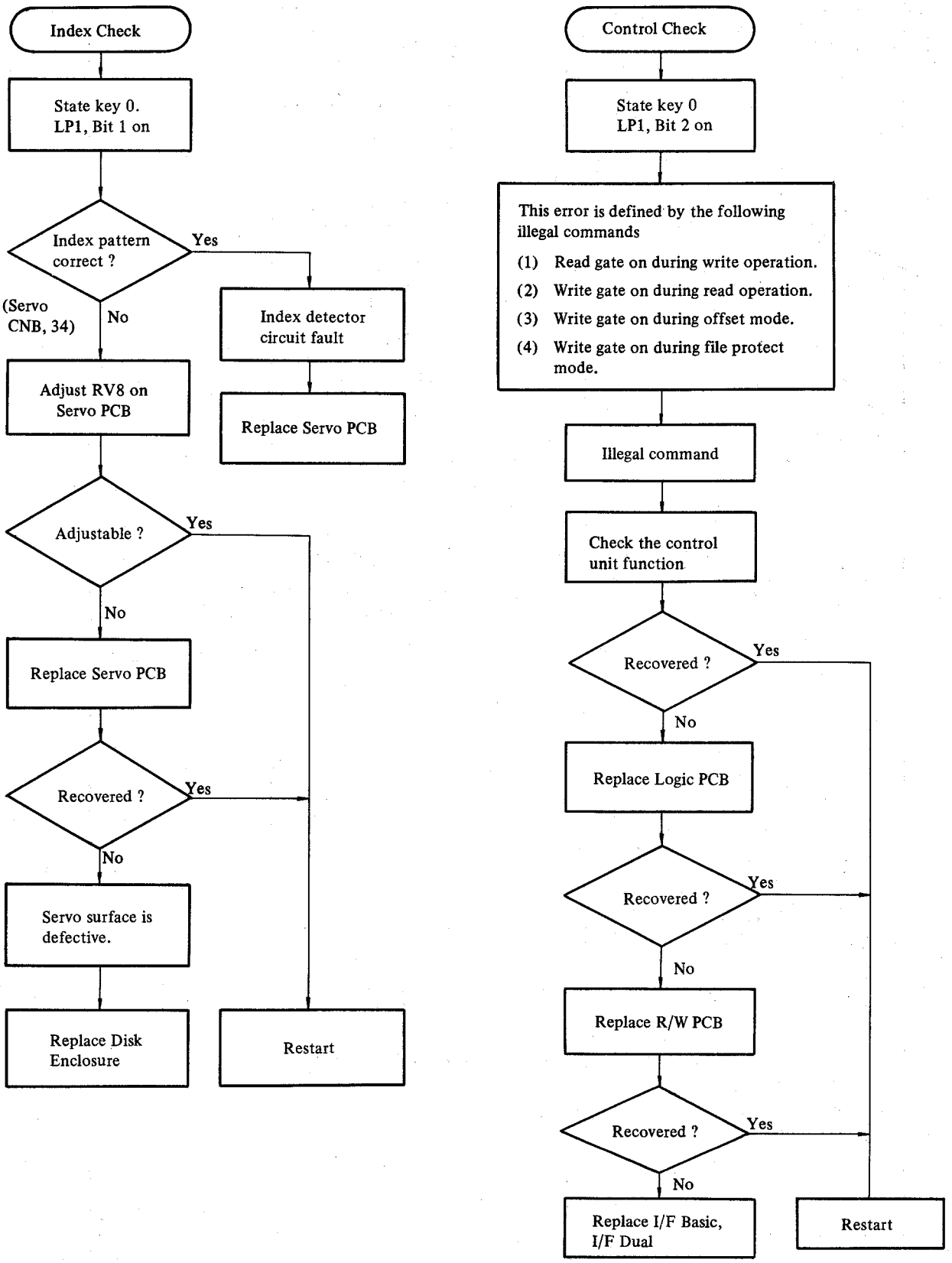


Figure 5.4.2 Fault flow chart (Sheet 1 of 4)

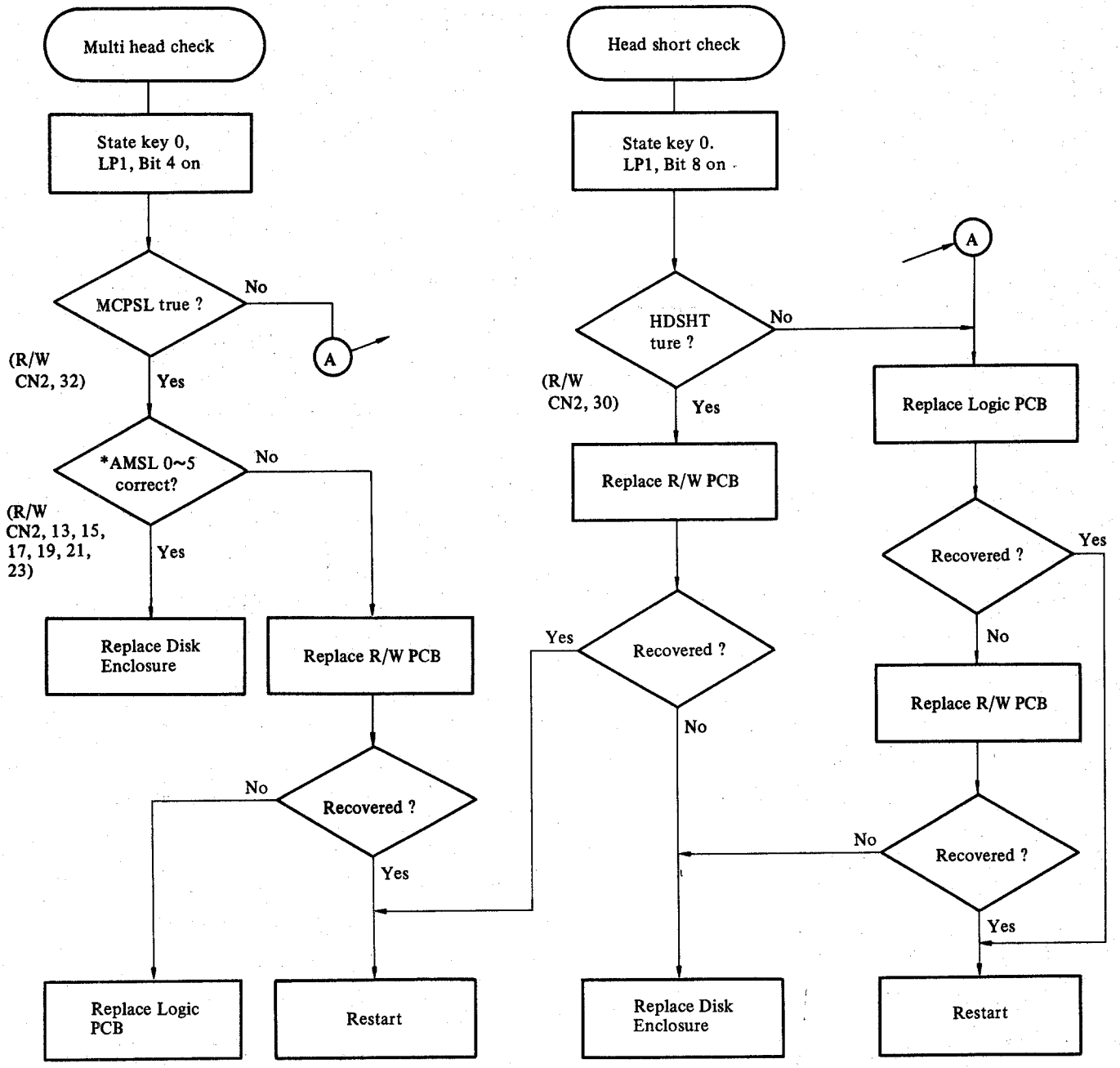


Figure 5.4.2 Fault flow chart (Sheet 2 of 4)

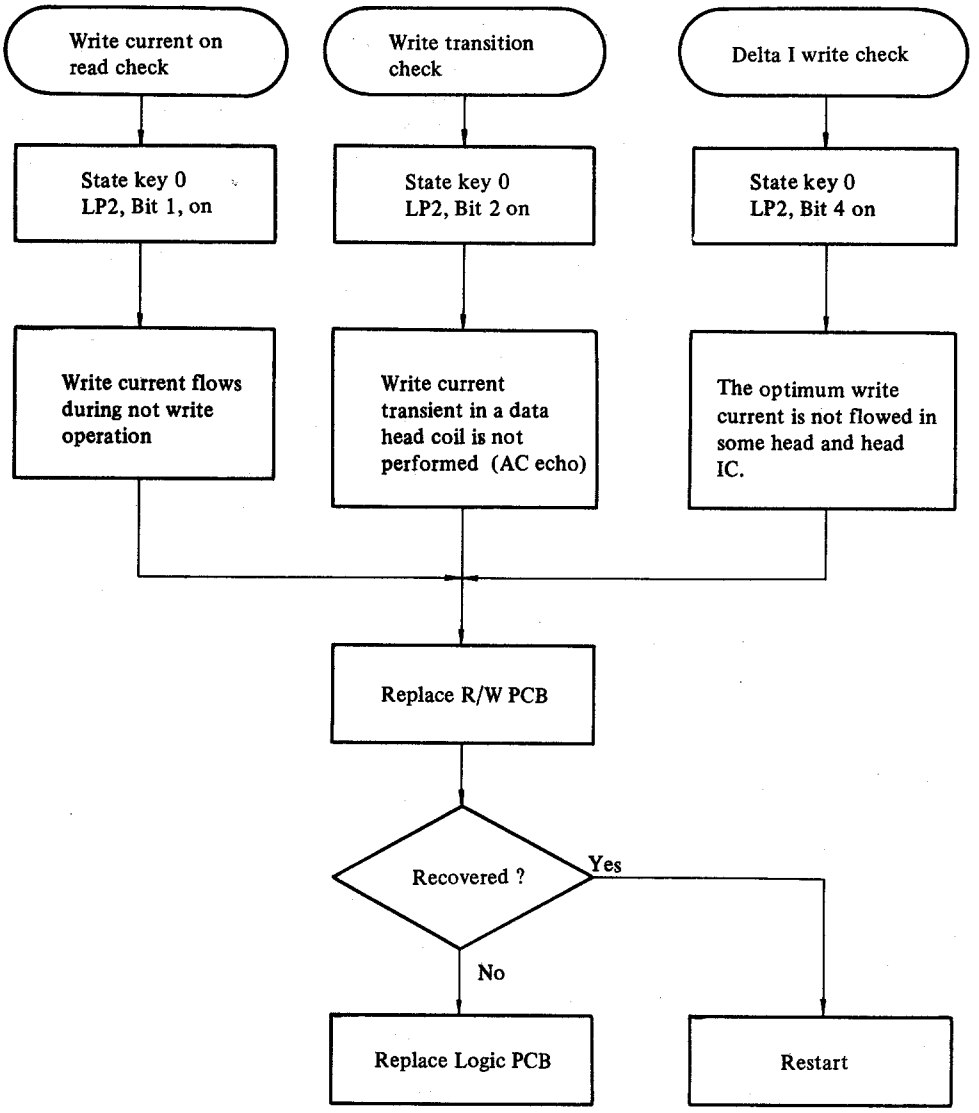


Figure 5.4.2 Fault flow chart (Sheet 3 of 4)

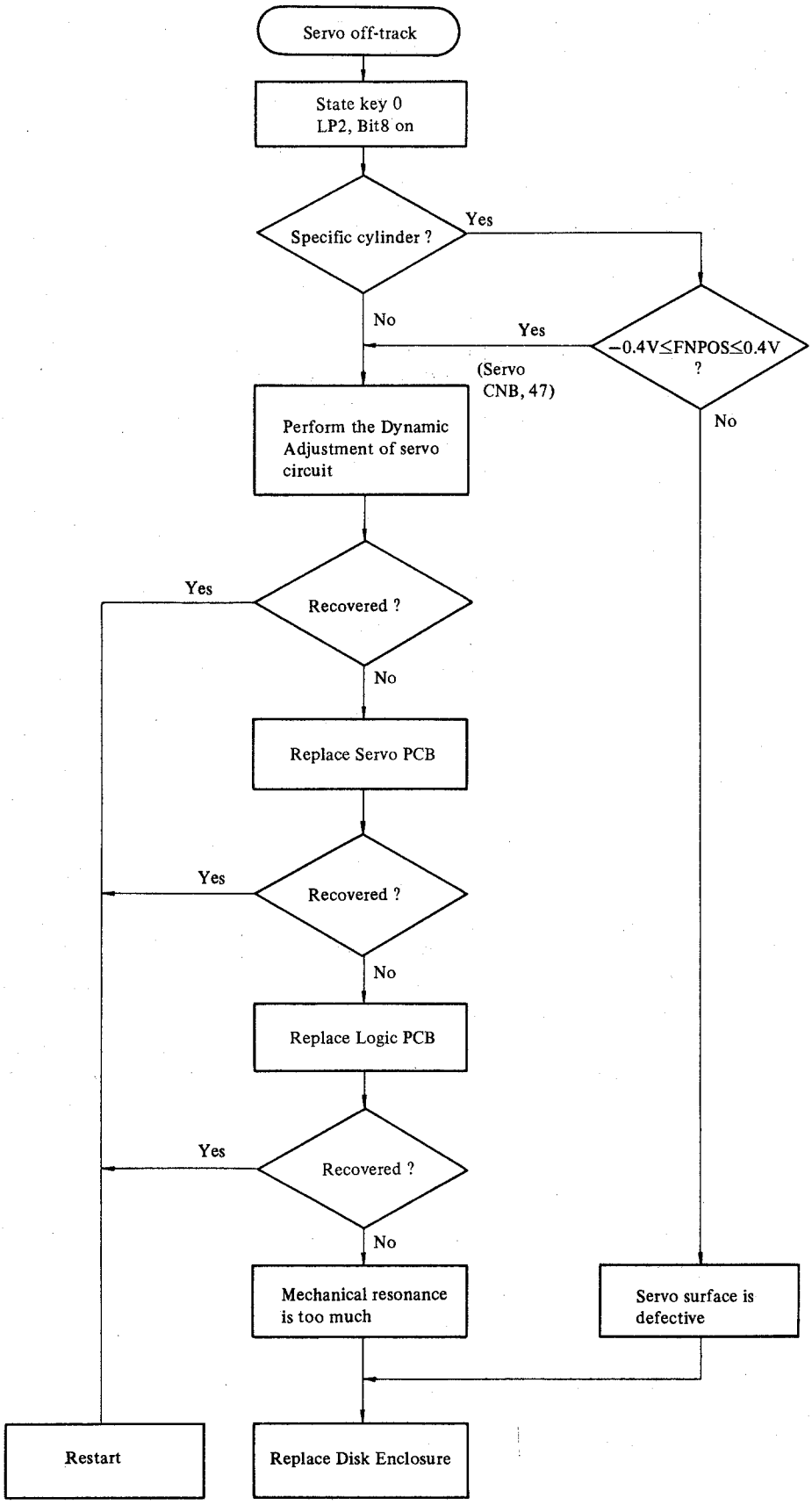


Figure 5.4.2 Fault flow chart (Sheet 4 of 4)

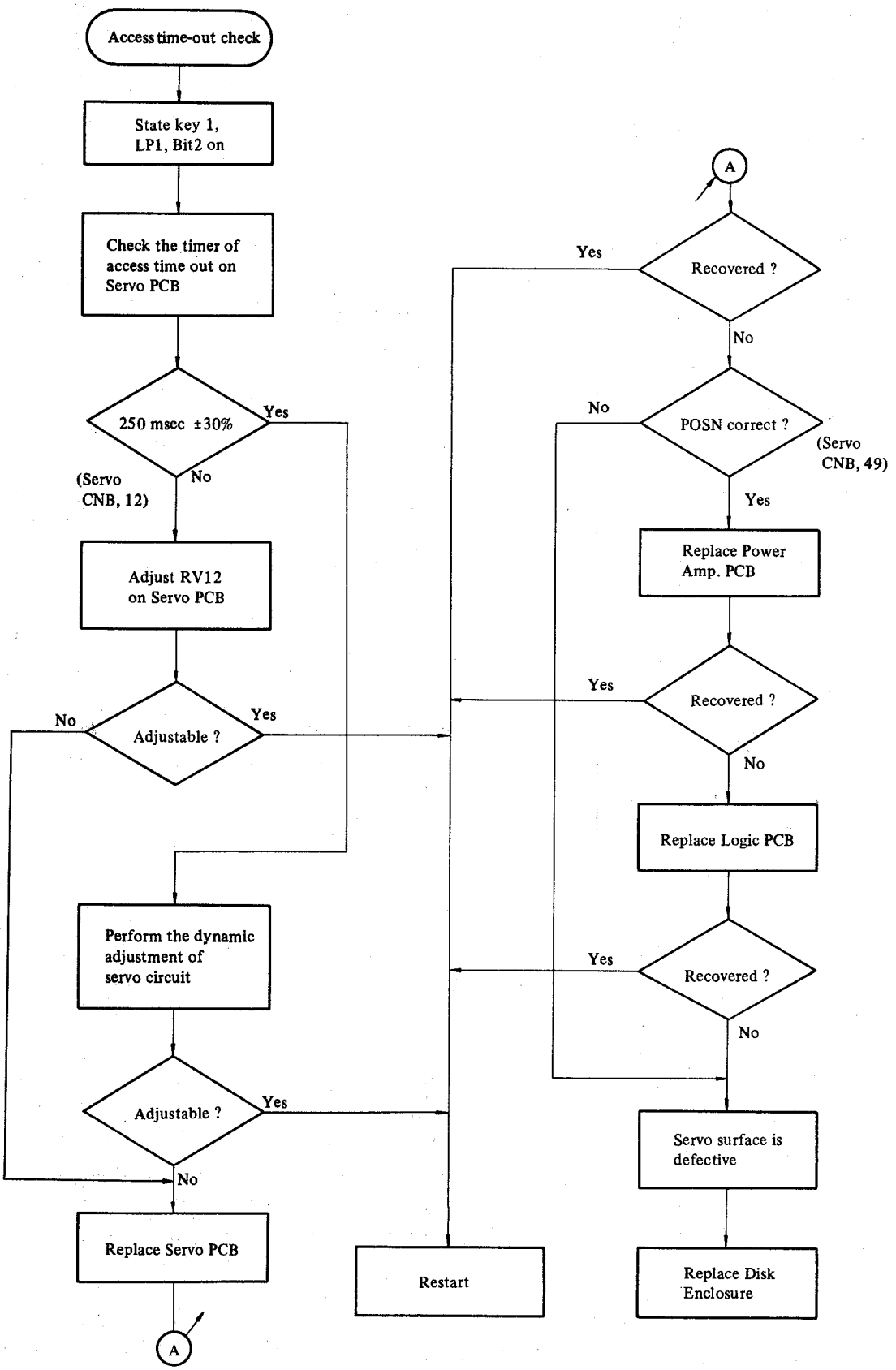


Figure 5.4.3 Seek Error flow chart (Sheet 1 of 2)

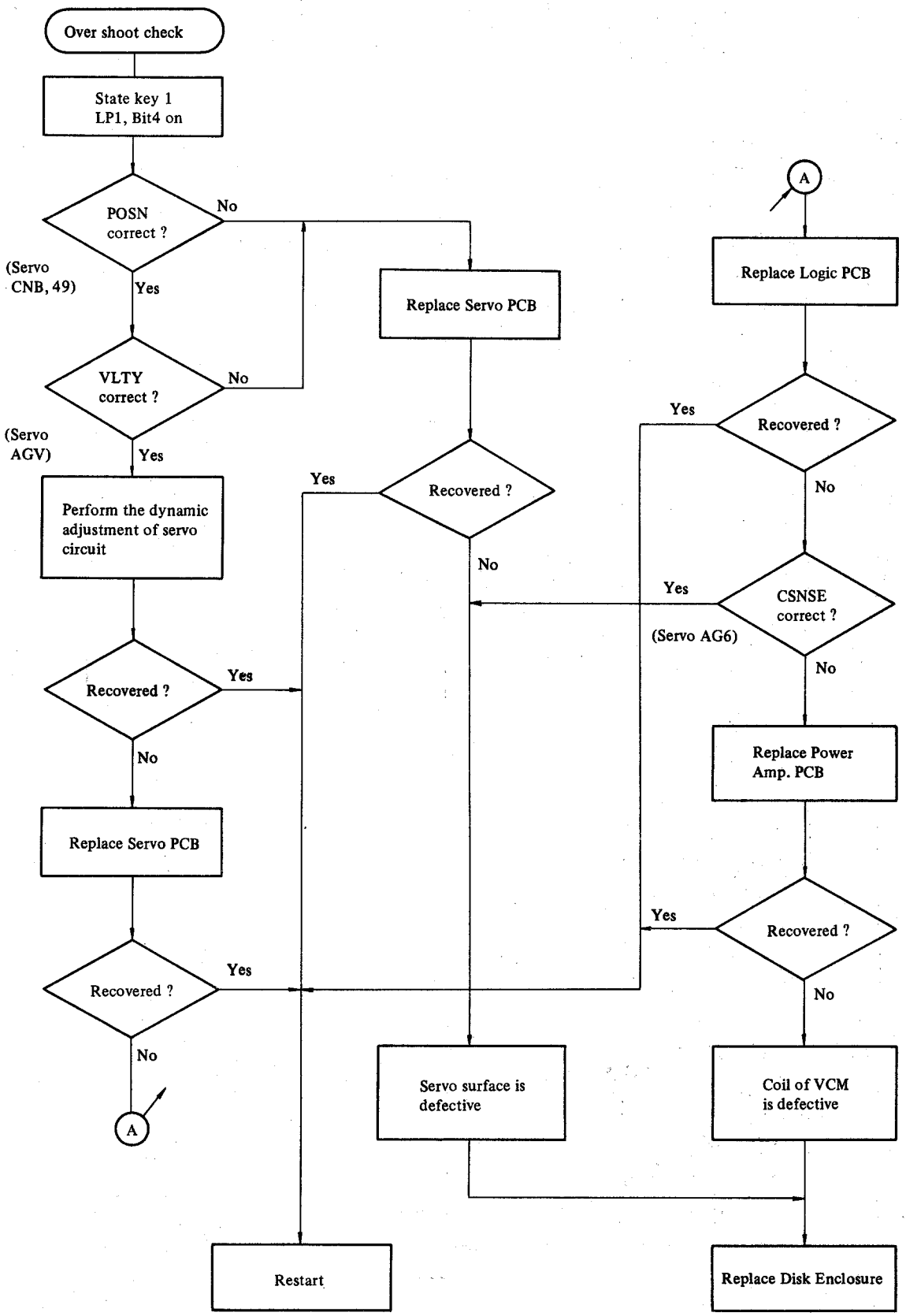


Figure 5.4.3 Seek Error flow chart (Sheet 2 of 2)

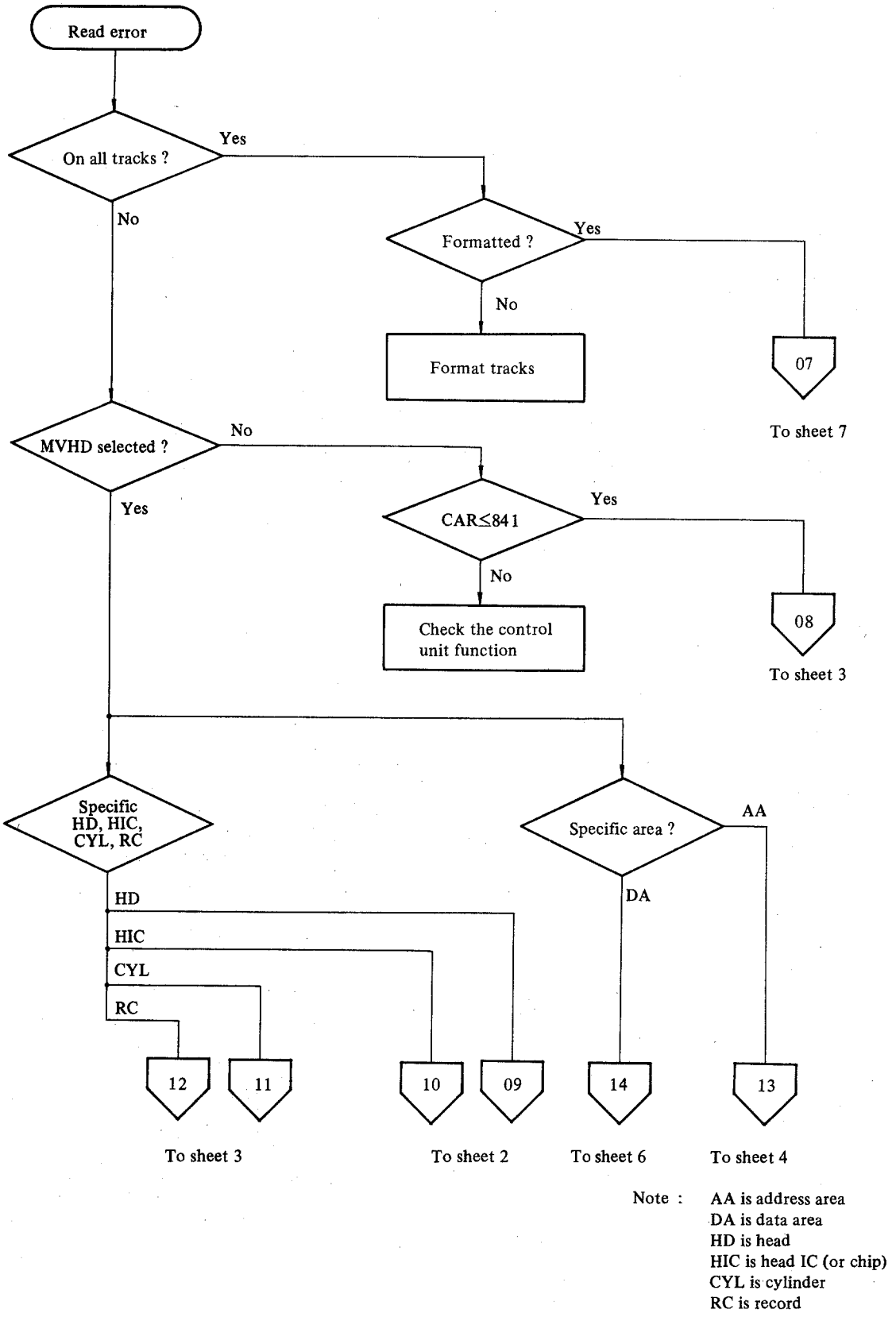


Figure 5.4.4 Read Error flow chart (Sheet 1 of 7)

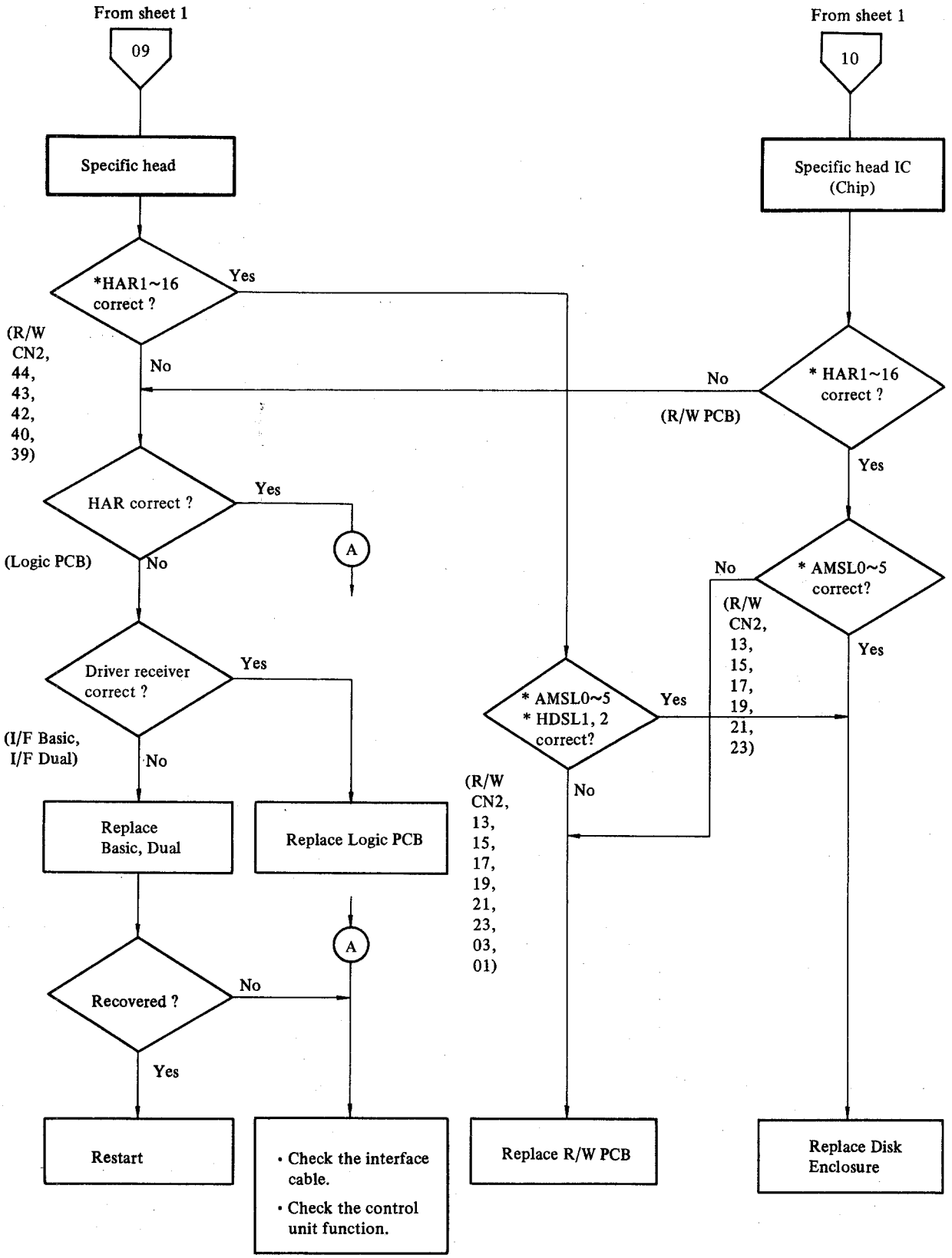


Figure 5.4.4 Read Error flow chart (Sheet 2 of 7)

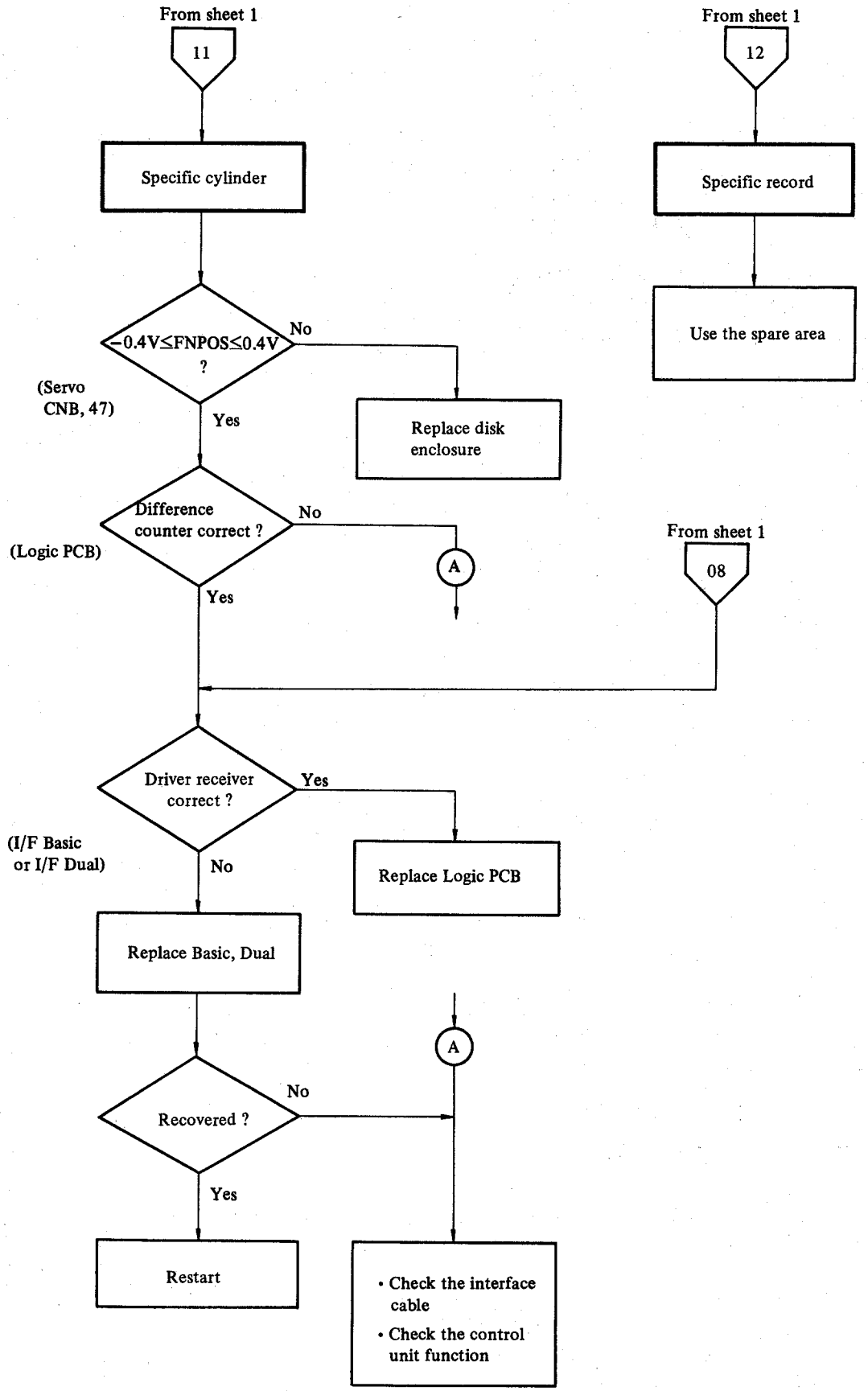


Figure 5.4.4 Read Error flow chart (Sheet 3 of 7)

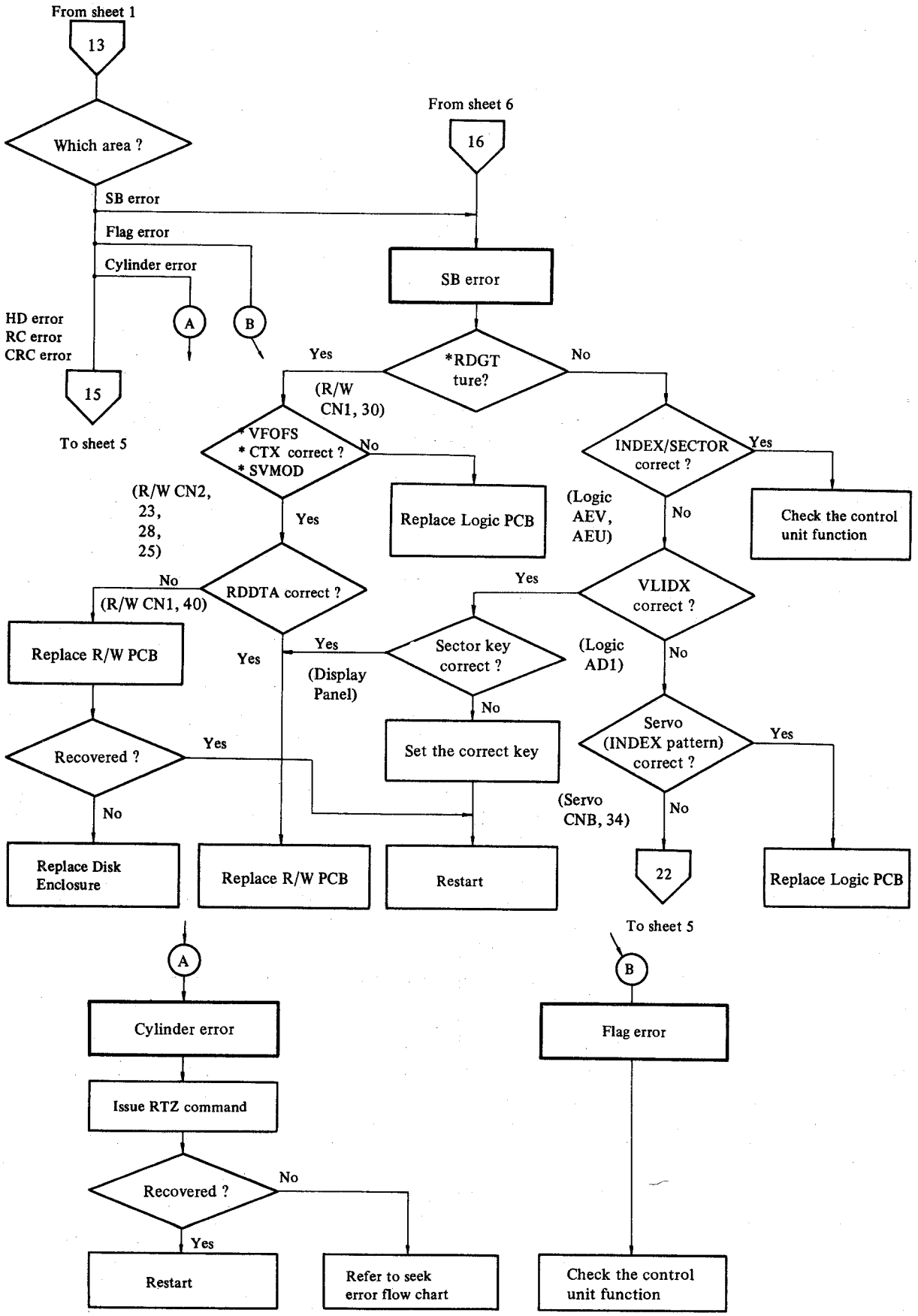


Figure 5.4.4 Read Error flow chart (Sheet 4 of 7)

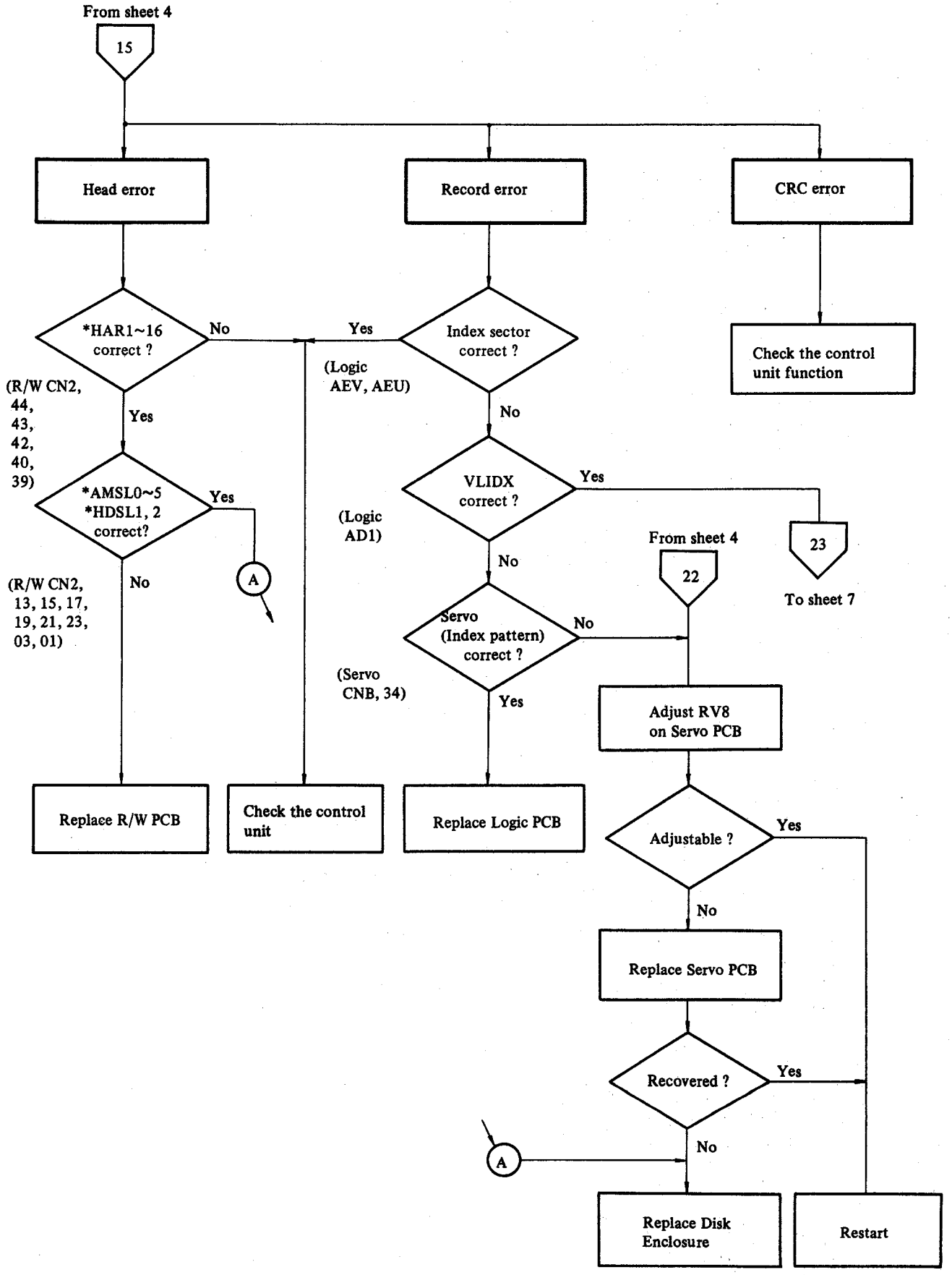


Figure 5.4.4 Read Error flow chart (Sheet 5 of 7)

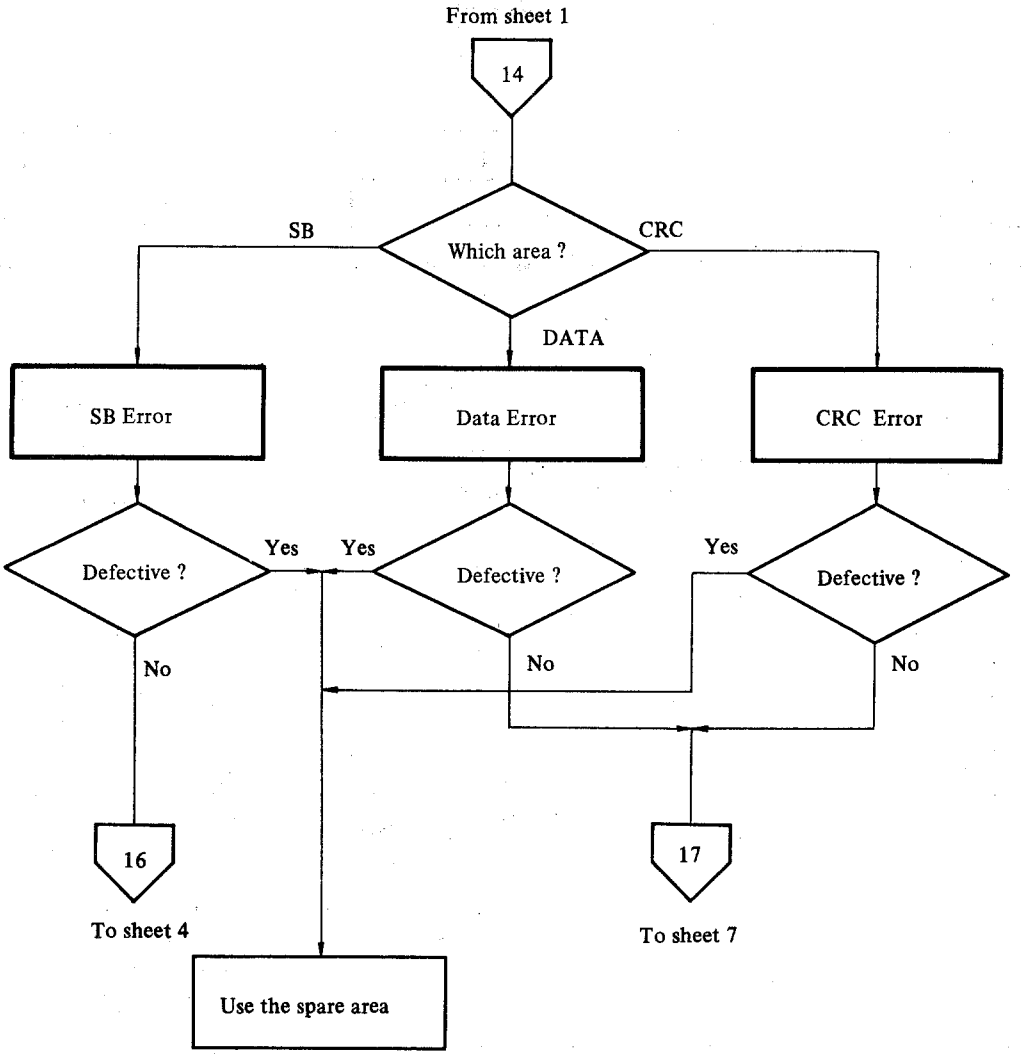


Figure 5.4.4 Read Error flow chart (Sheet 6 of 7)

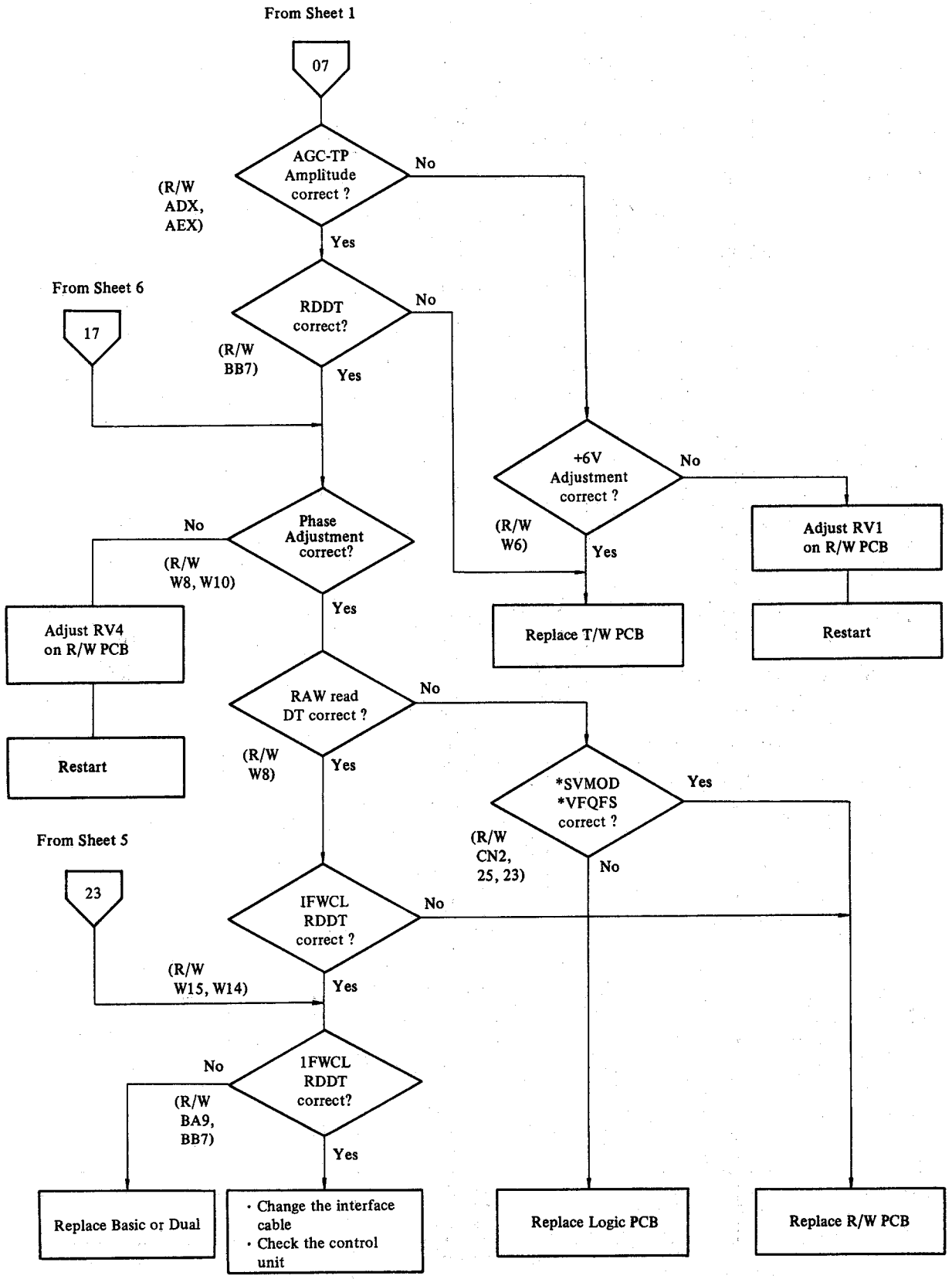


Figure 5.4.4 Read Error flow chart (Sheet 7 of 7)

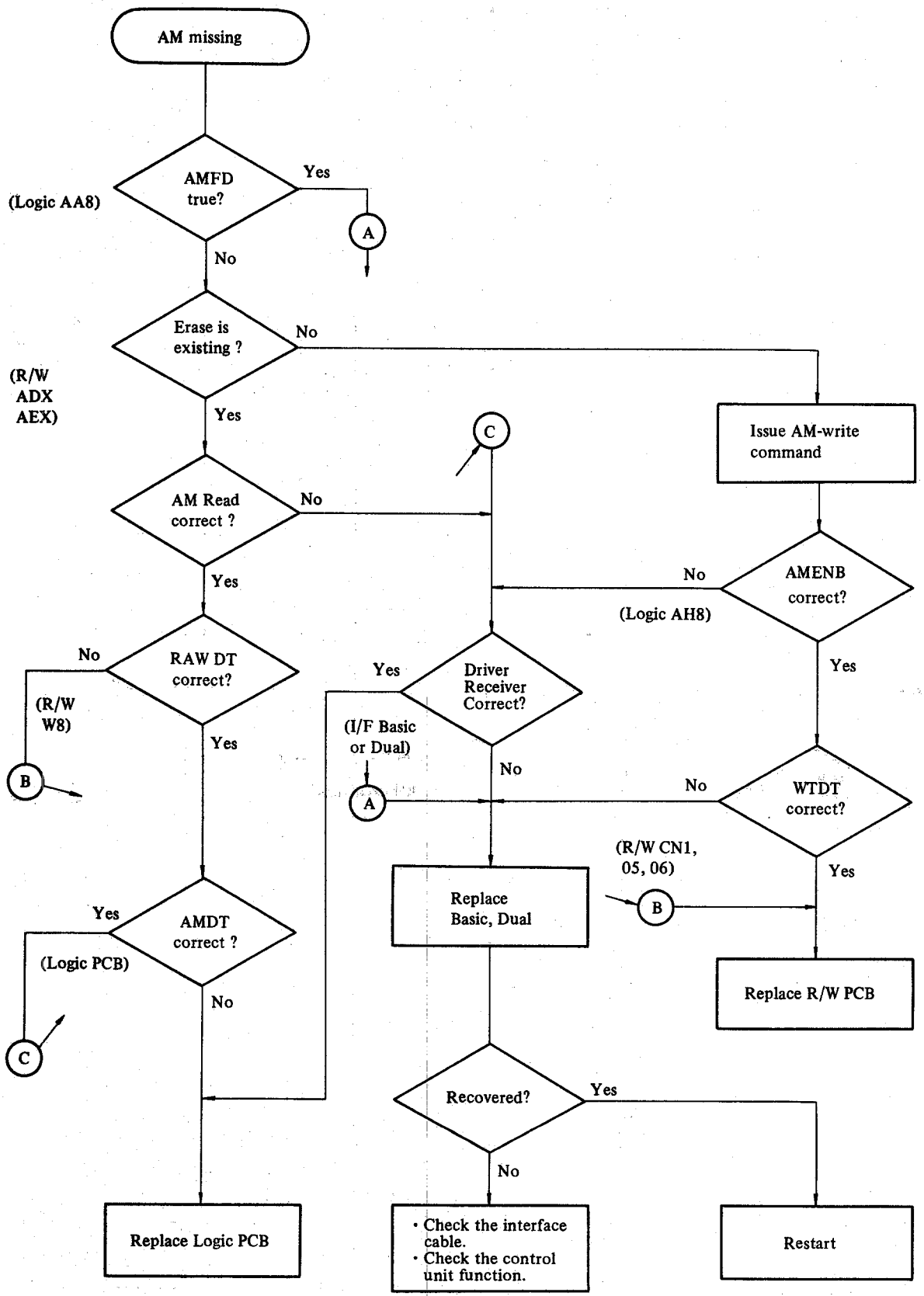


Figure 5.4.5 AM Missing flow chart (Sheet 1 of 1)

CHAPTER 6 MAINTENANCE

6.1 Introduction

This section covers maintenance of the unit, and is divided into General Precautions, Spare Parts List, Maintenance Tools and Equipment, Preventive Maintenance, Spare parts Replacement, and PCB Check/Adjustment.

6.2 General Precautions

6.2.1 Power on/off

(1) Visually check the condition of the drive before turning the power on or off.

(2) Always turn the power off before removing or inserting printed circuit boards or connectors.

(3) After maintenance, before turning the power on, ensure that all printed circuit boards and connectors are seated and installed in the correct position.

6.2.2 Replacement

(1) Use screwdrivers and other tools suitable for the screws and bolts to be installed or removed.

(2) Do not leave removed screws in the drive.

Caution: Never loosen the retaining screws for the DE alminum cover. The DE must not be opened in the field.

6.2.3 Others

(1) Use test equipment that has been correctly calibrated.

(2) Always record failure symptoms and remedies employed for later reference.

6.3 Spare Parts List

Table 6.3.1 Recommended spare parts list

No.	Name	Specification	Quantity	RM	Remark
1	DE Assembly	B030-4825-T001A	1	R	
2	DC Power Supply	B14L-5105-0182A	1	R	
3	Line Blower	C90L-1370-0900	1	-	
4	Operator Panel Assembly	N860-3346-T001	1	R	
5	PCB	C16B-5327-0290#U	1	R	Logic Circuit
6	PCB	C16B-5502-0040#U	1	R	Read Amplifier
7	PCB	C16B-5502-0050#U	1	R	Servo Circuit
8	PCB	B17B-0230-0010A#U	1	R	Interface Circuit
9	PCB	B17B-0240-0010A#U	(1)	R	Interface Circuit (Dual Ch. Option)
10	PCB	B17B-0250-0010A#U	1	R	Power Amplifier
11	PCB	B17B-0270-0010A#U	1	R	Display Panel Assembly
12	PCB	B03B-4825-E010A#U	1	R	Back Panel
13	Air Filter	B90L-1570-0001A	1	-	
14	Fan Sensor	C90L-1350-0001	1	-	
15	Fan	B03B-4825-D030A	1	-	

Notes: RM; Repairable Mark (R; Repairable)

6.4 Maintenance Tools and Equipments

Table 6.4.1 Maintenance tools and equipments

No.	Tools and Equipment	Specification	Remark
1	Extension Cable	B660-1060-T072A#L510R0	20 pins
2	Extension Cable	B660-1060-T074A#L510R0	50 pins Two required
3	Extension Unit	C960-0030-T029	
4	Extractor	C960-0300-T001	One required
5	Oscilloscope	TEKTRONIX 475, or equivalent	
6	Oscilloscope Probe (X10)	TEKTRONIX P6053B or equivalent	
7	Digital Multimeter		
8	Screwdriver	#2 Straight Blade #2 Philips	
9	Hexagonal Wrenches		Metric system
10	Extension Cable	B660-1950-T646A#L510R0	40 pins
11			
12			
13			

6.5 Preventive Maintenance

The air filter should be cleaned or replaced at one year intervals or as required. Any other preventive maintenance is not required.

6.6 Spare Parts Replacement

6.6.1 Pre-procedure for replacement

Prior to the replacement of spare parts, fully extend the drive and remove the top and rear covers. See Figure 6.6.1.

(1) Extension of the drive

① Remove the 4 screws holding the bracket to the rack (each side).

② Slide out the drive fully from the rack.

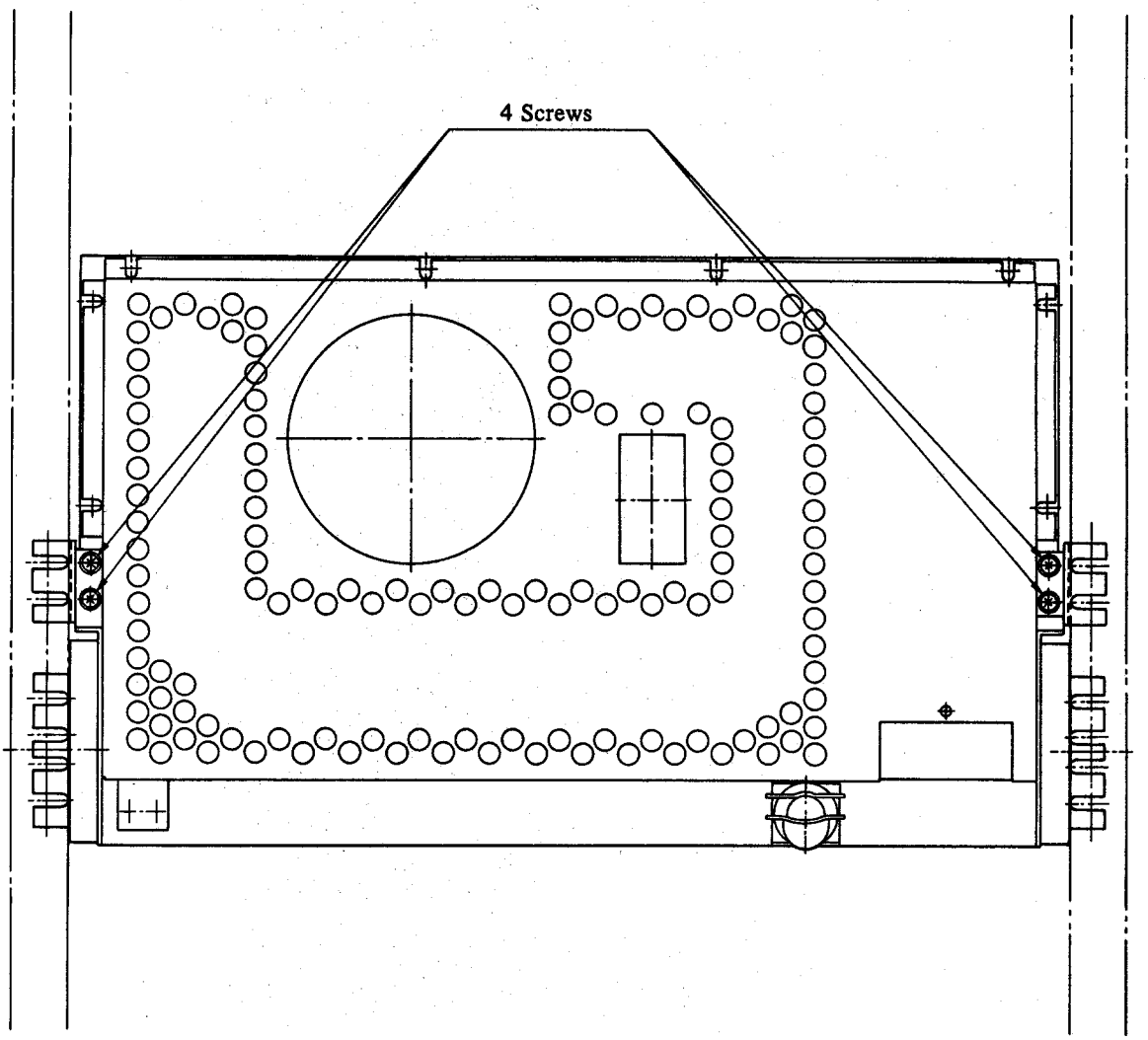


Figure 6.6.1 Extension of the drive

(2) Top cover removal

① Remove the 2 screw "A" holding the front side top cover.

② Loosen then 4 screws "B" holding the middle and rear side of the top cover.

③ Remove the top cover upward.

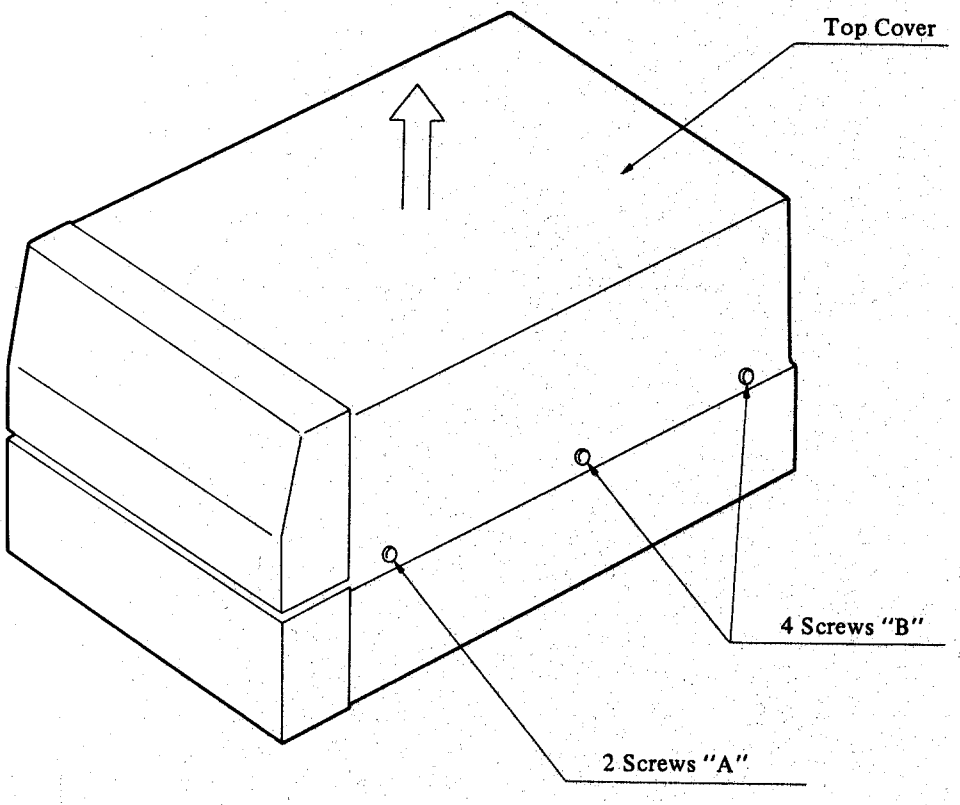


Figure 6.6.2 Top cover removal

(3) Rear cover removal

① Remove the 11 screws "A" holding the rear cover.

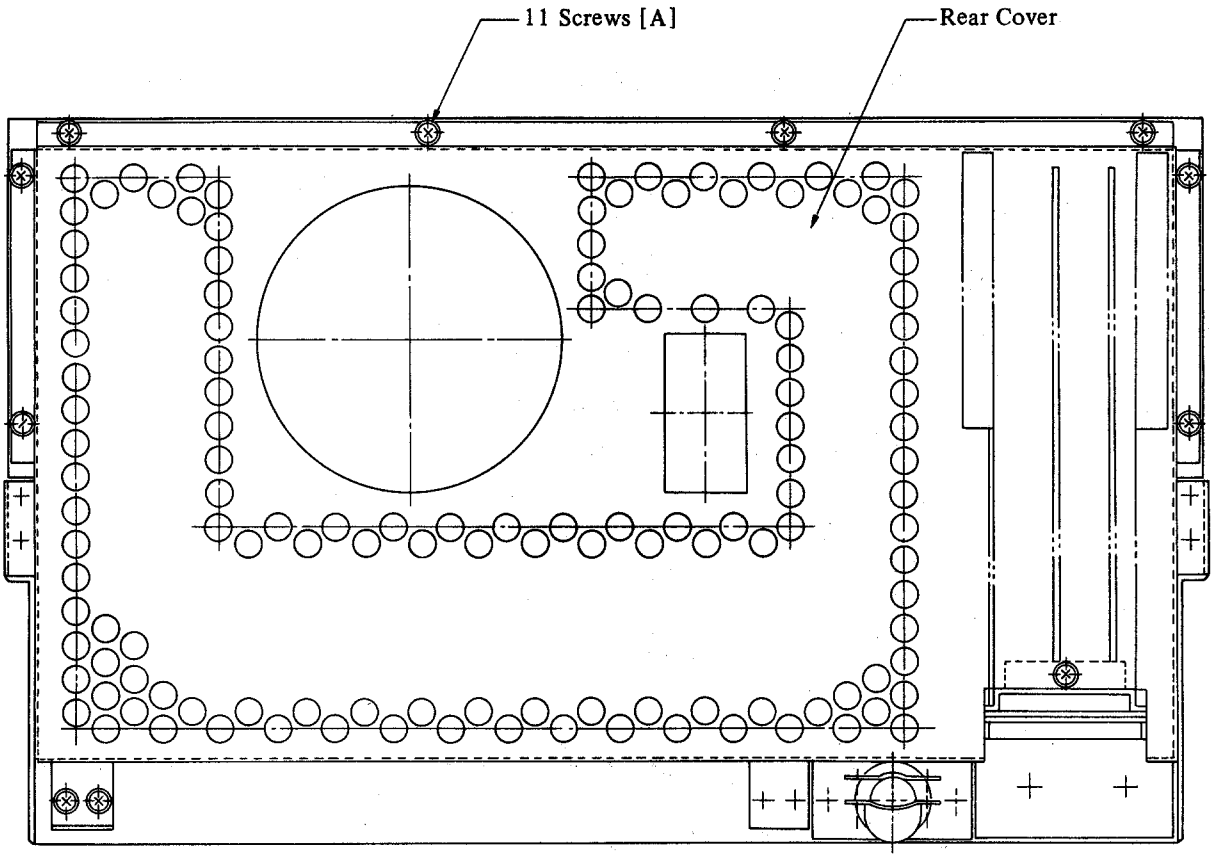


Figure 6.6.3 Rear cover removal

6.6.2 DE replacement

(1) Removal

① Remove connectors (CN02, 04, 05, 06) that go out from the power amplifier.

② Remove connector (CN21) and SG wire "A" that go out from the DE.

③ Loosen the 4 screws "B" holding the DE.

④ Lift out the DE carefully from the drive.

Caution: Take care, because the DE weighs approx. 58 lbs (25 kg).

(2) Installation

① Before installing the DE, ensure that the cables are connected correctly.

② Lower the DE gently on the shock mounts taking care to watch the area all around the DE so cables are not pinched.

③ Follow, in reverse order, the procedures for removal.

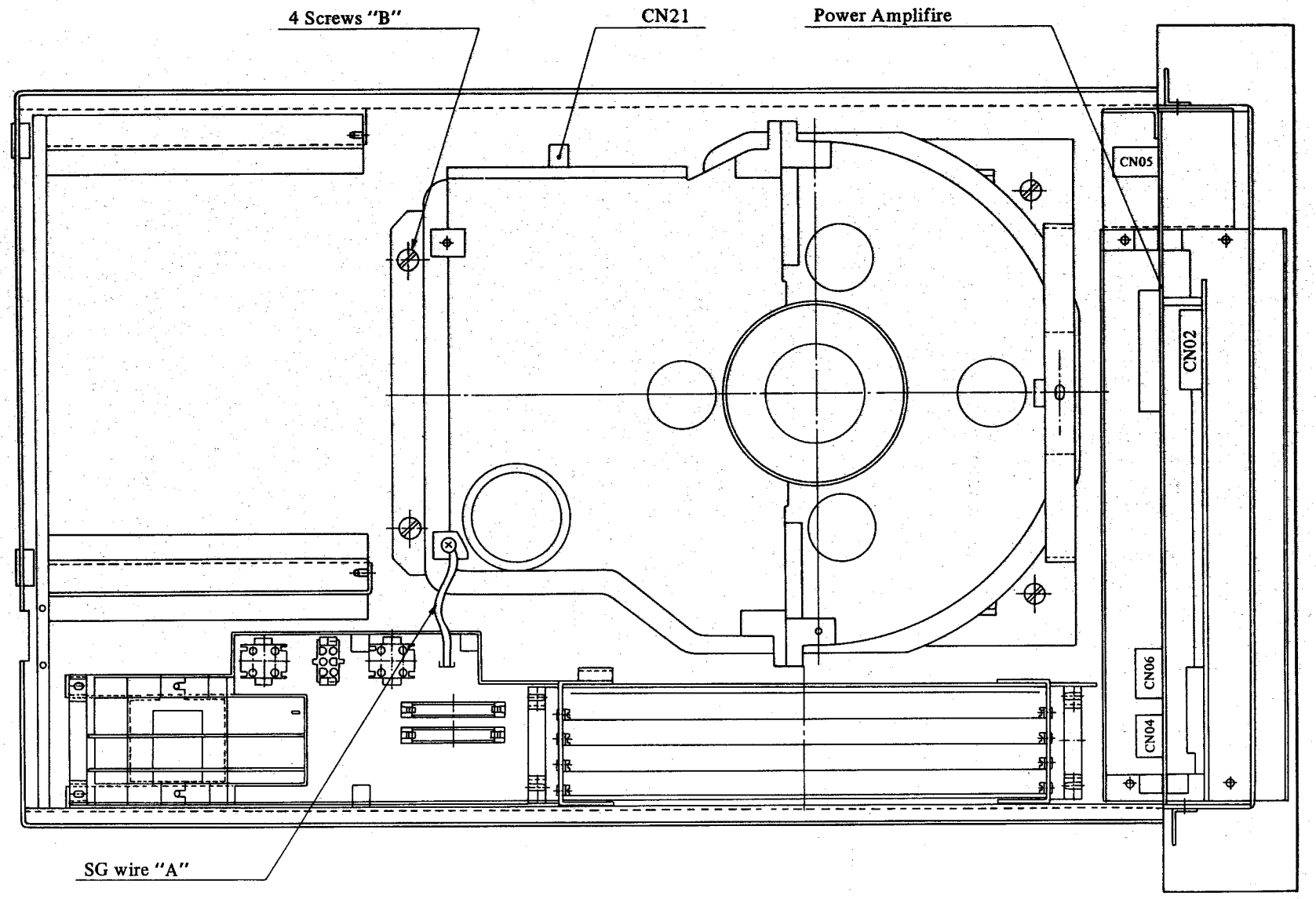


Figure 6.6.4 DE replacement

6.6.3 DC power supply unit replacement

(1) Removal

① Remove connectors (CN61, 63, 65 - 67) that go out from the power supply unit.

② Remove the input AC power cable.

③ Remove the 6 screws and the 2 brackets holding the power supply unit.

④ Slide out and remove the power supply unit.

(2) Installation

Follow, in reverse order, the procedures for removal.

(3) DC voltage adjustment

Check the DC voltages at the check terminals (W1-W6) on the back panel PCB using digital multimeter. The check terminals' configuration is shown in Figure 2.6.3. If a DC voltage is out of the permitted range listed in Table 6.6.1 readjust the corresponding variable resistor shown in Figure 6.6.5.

Table 6.6.1 Permitted range of DC voltage

DC Voltage	Permitted Range	Check Terminal
+12 V	11.4 ∿ 12.6 V	W3
+5 V	4.75 ∿ 5.25 V	W2
-4 V	-3.8 ∿ -4.2 V	W6
-5.2 V	-4.94 ∿ 5.46 V	W4
-12 V	-11.4 ∿ -12.6 V	W5
GND	-	W1

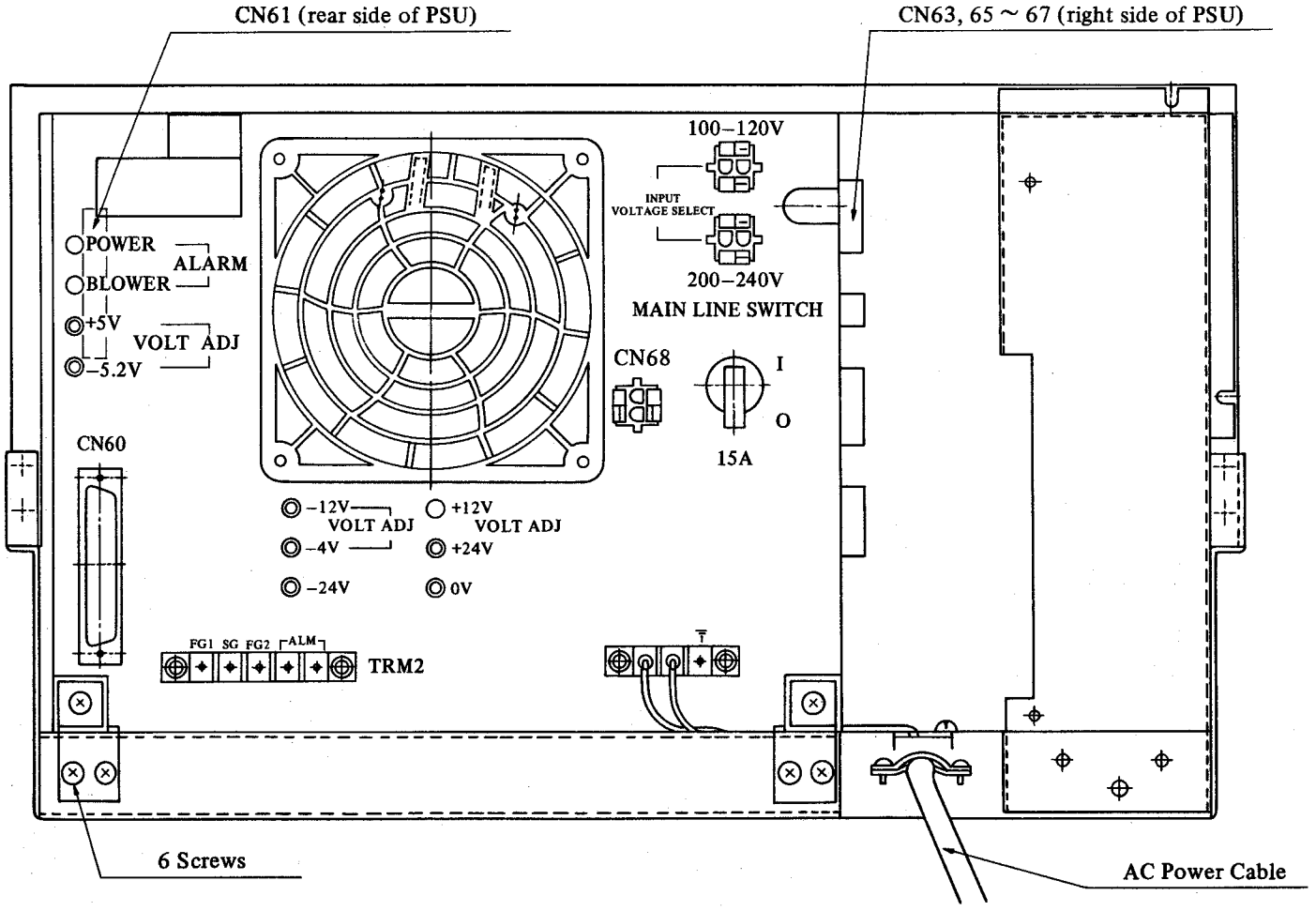


Figure 6.6.5 Rear view of DC power supply unit

6.6.4 Fan replacement

(1) Removal

① Remove the connector (CN68) that go out from fan.

② Remove the 4 screws "A" holding the fan.

(2) Installation

Follow, in reverse order, the procedures for removal.

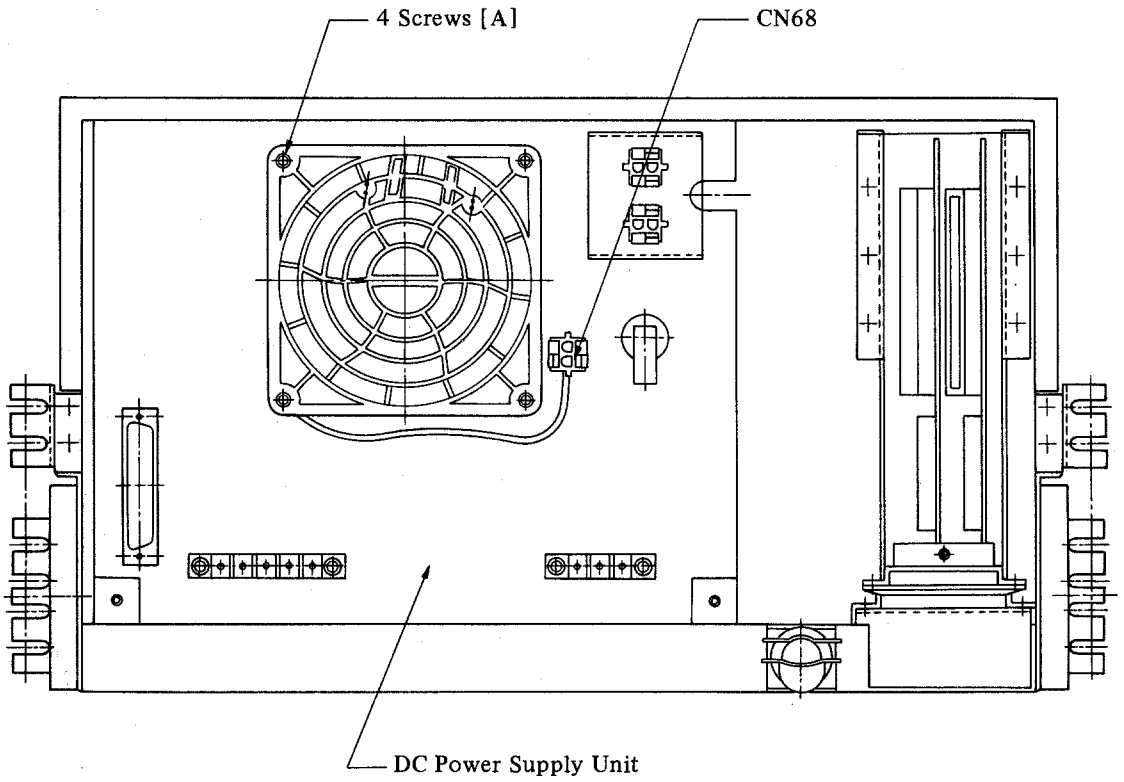


Figure 6.6.6 Fan replacement

6.6.5 Operator panel replacement

Refer to Figure 6.6.7.

(1) Removal

① Remove the 4 screws "A" holding the front panel, and then remove it.

② Remove the connector (CN83) that goes out from the operator panel.

③ Remove the 4 screws "B" holding the operator panel, and then remove it.

(2) Installation

Follow, in reverse order, the procedures for removal.

6.6.6 Display panel replacement

Refer to Figure 6.6.7.

(1) Removal

① Remove the 4 screws "A" holding the front panel and then remove it.

② Remove the connectors (CN31-33) that go out from the display panel.

③ Remove the 6 screws "C" holding the display panel and then remove the PCB.

(2) Installation

Follow, in reverse order, the procedures for removal.

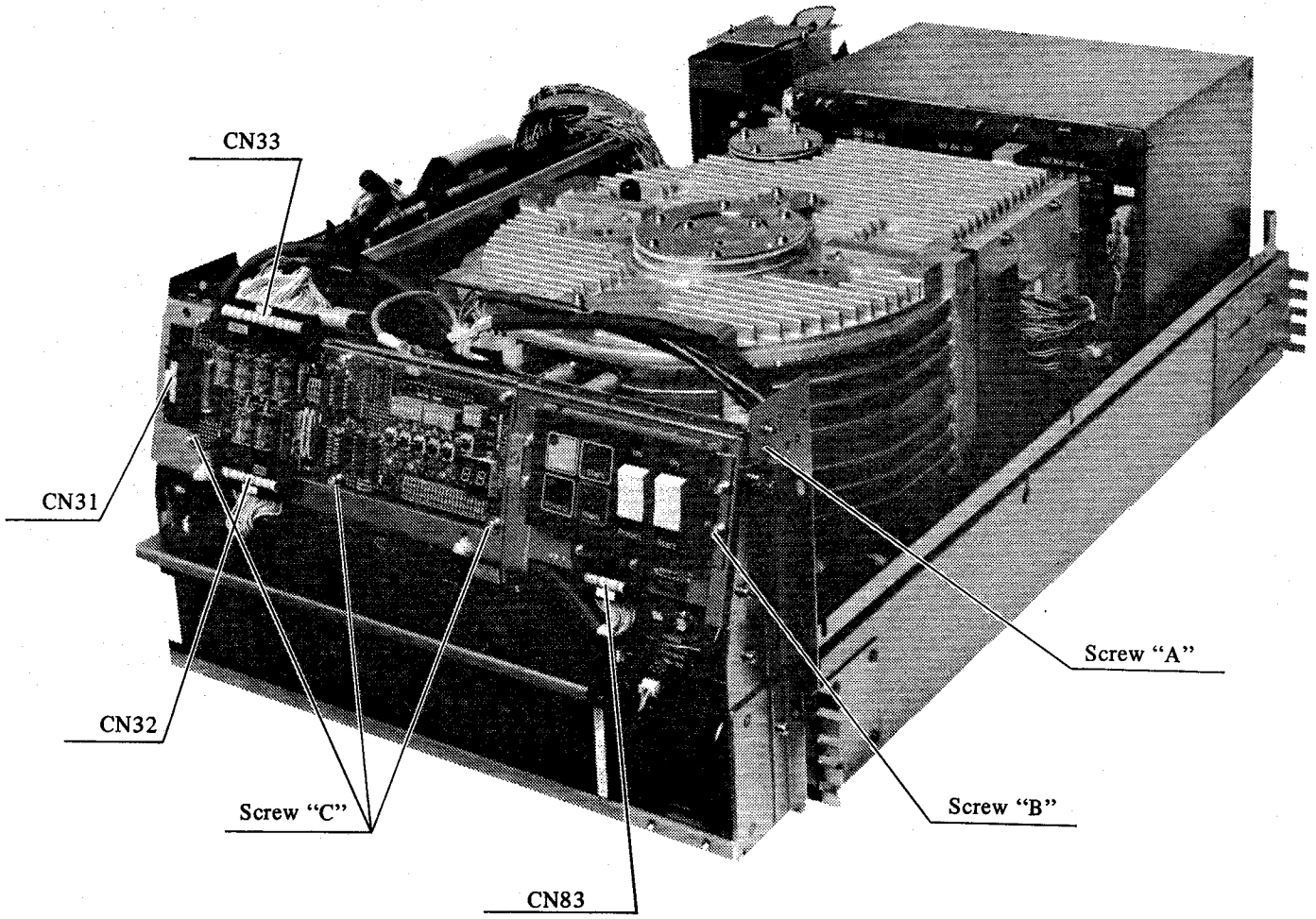


Figure 6.6.7 Operator panel and display panel replacement

6.6.7 Interface PCB replacement

Interface PCBs (basic and dual port) are installed in the interface card cage. Refer to Figure 6.6.8.

(1) Removal

① Remove the interface cables connected to the interface PCB.

② Remove the 2 screws holding the card fixture and then remove it.

③ Pull up the interface PCB.

(2) Installation

Follow, in reverse order, the procedures for removal.

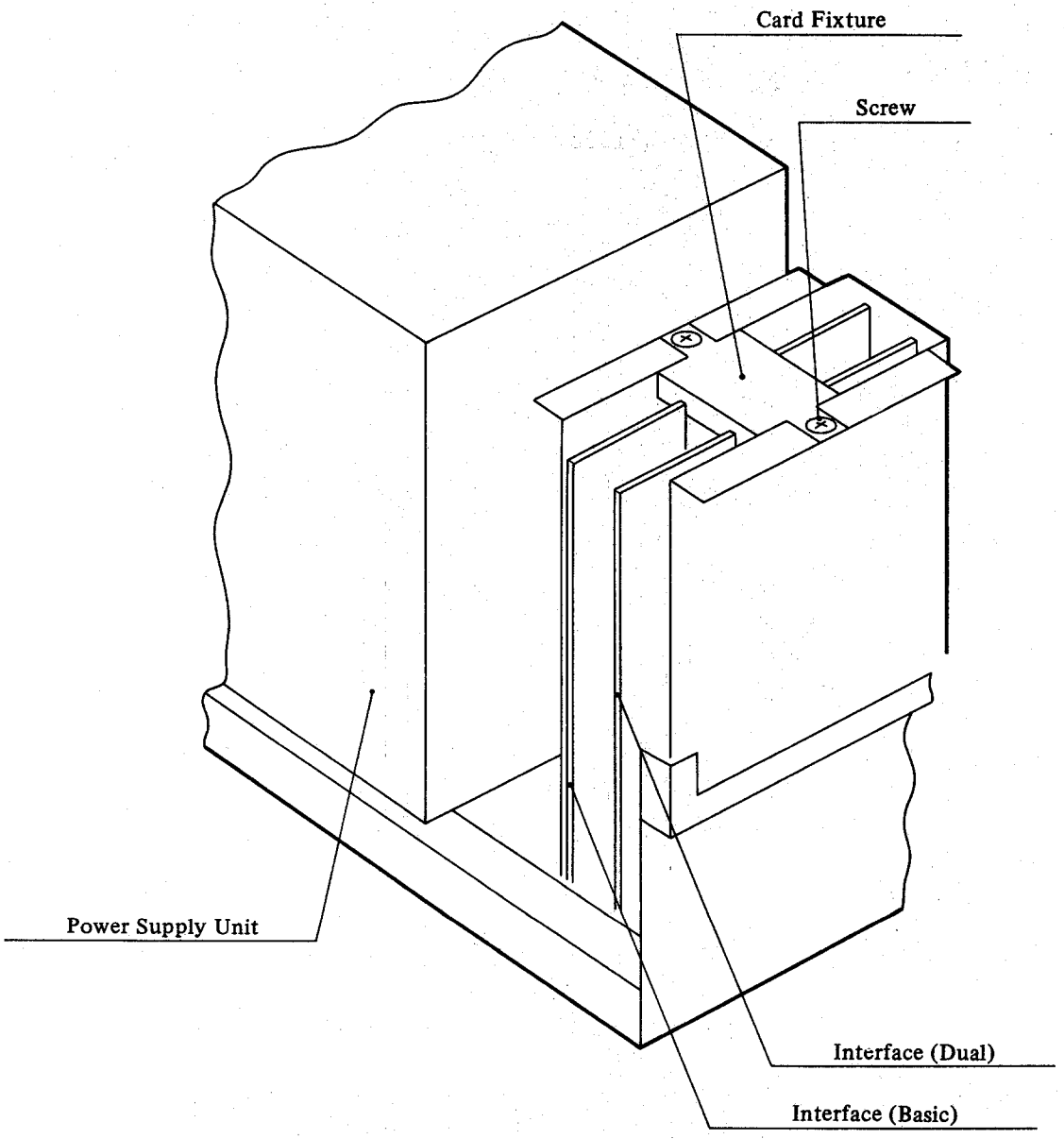


Figure 6.6.8 Interface PCB replacement

6.6.8 Power amplifier replacement

(1) Removal

① Remove the 4 screws "A" holding the front panel and then remove it.

② Remove the connectors (CN01-06) and FG wire that go out from the power amplifier PCB.

③ Remove the 2 screws "B" holding the right side bracket and then remove it.

④ Remove the connectors (CN31, 33) that go out from the display panel PCB.

⑤ Pull out the 2 nylon latches and remove the power amplifier.

(2) Installation

① Follow, in reverse order, the procedures for removal.

② Ensure that the power amplifier is correctly seated in the PCB guides.

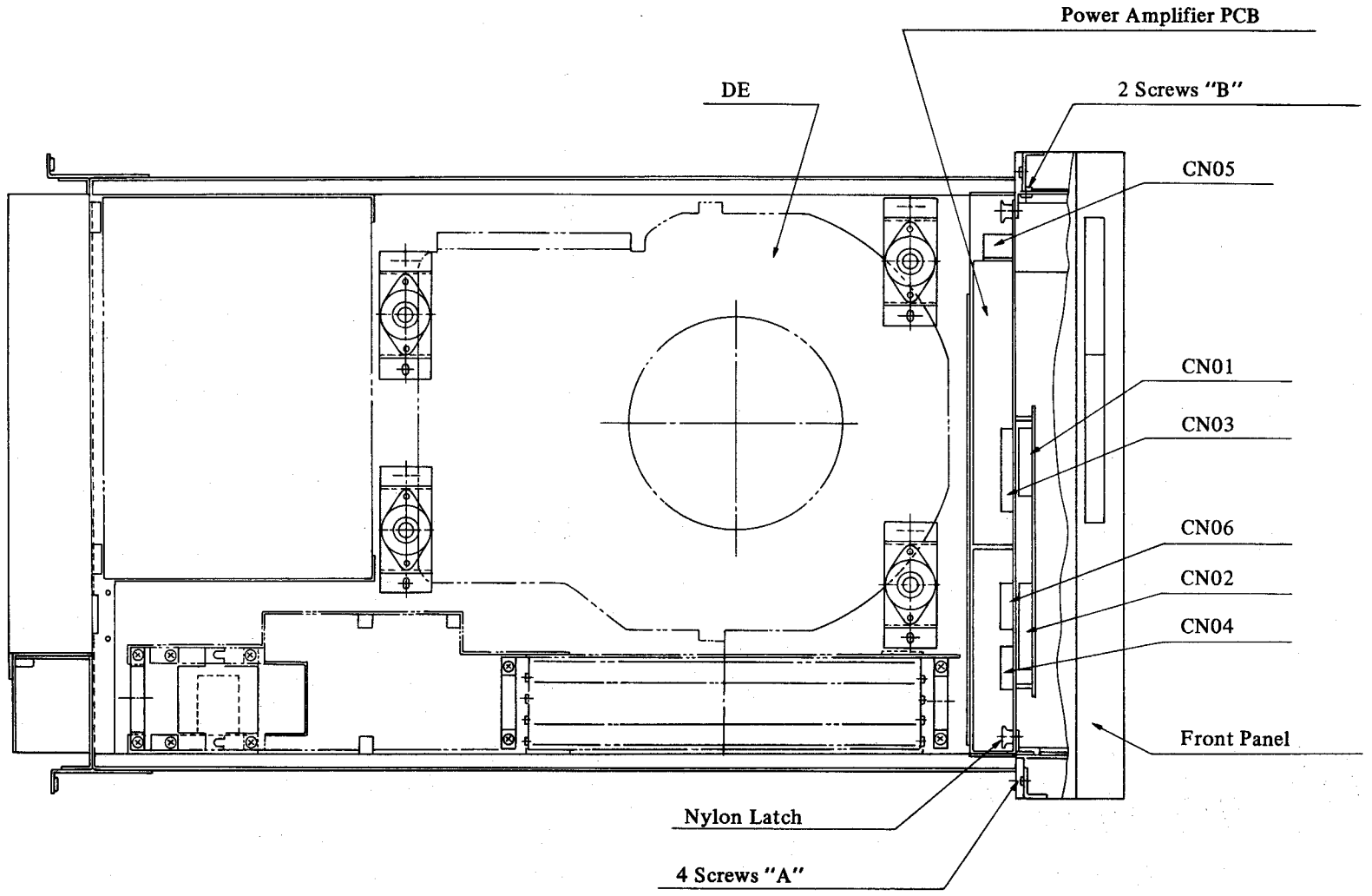


Figure 6.6.9 Power amplifier replacement

6.6.9 Air filter replacement

Refer to Figure 6.6.10.

(1) Removal

① Remove the 4 screws "A" holding the front panel and then remove it.

② Remove the 2 screws "B" holding the air filter and then remove it.

(2) Installation

Follow in reverse order, the procedures for removal.

6.6.10 Line blower replacement

Refer to Figure 6.6.10.

(1) Removal

① Remove the power amplifier PCB. (Refer to item (1) of subsection 6.6.8.)

② Remove the 4 screws "C" holding the blower bracket.

③ Remove the 4 screws "D" holding the upper side of the line blower.

Caution: Take care not to drop the screws.

④ Remove the air filter. (Refer to item (1) of subsection 6.6.9.)

⑤ Remove the connector (CN71) that goes out from the fan sensor, and remove the blower assembly.

⑥ Remove the connector (CN91) that goes out from the line blower.

⑦ Pull and remove the fan sensor.

(2) Installation

Follow in reverse order, the procedure for removal.

6.6.11 Fan sensor replacement

Refer to Figure 6.6.10.

(1) Removal

① Remove the power amplifier PCB. (Refer to item (1) of subsection 6.6.8.)

② Remove the 4 screws "C" holding the blower bracket.

③ Remove the 4 screws "D" holding the upper side of the line blower.

Caution: Take care not to drop the screws.

④ Remove the connector (CN71) that goes out from the fan sensor, and remove the blower assembly.

⑤ Remove the connector (CN91) that goes out from the line blower.

⑥ Pull and remove the fan sensor.

(2) Installation

Follow in reverse order the procedure for removal.

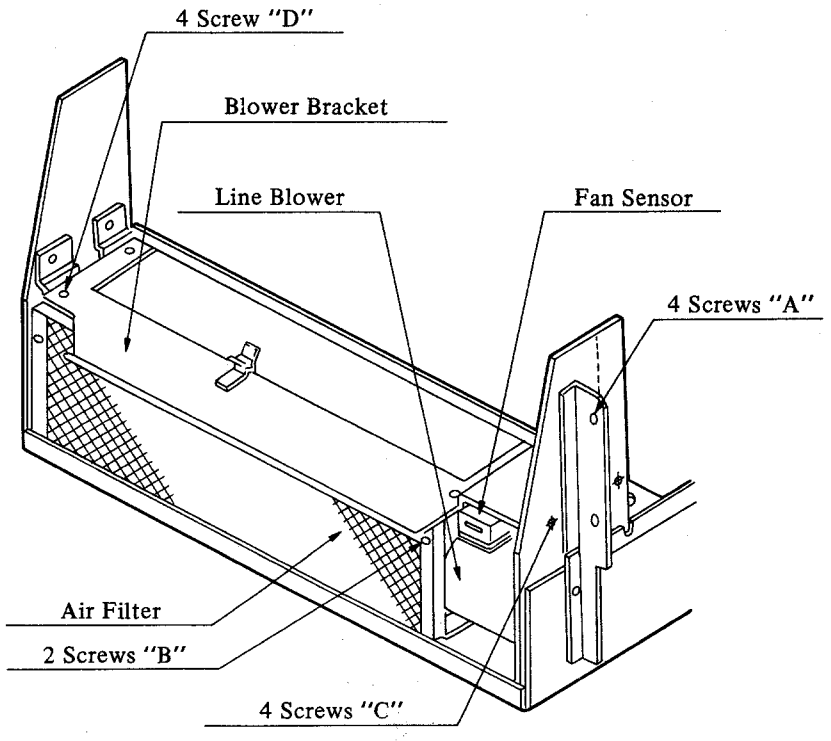


Figure 6.6.10 Blower assembly replacement

6.6.12 Card-caged PCB replacement

(1) Removal

① Remove the connectors that go out from the PCB to be replaced.

② Insert pin of the extractor tool provided with the drive into the hole of the PCB and turn it as shown below.

(2) Installation

Follow, in reverse order, the procedures for removal.

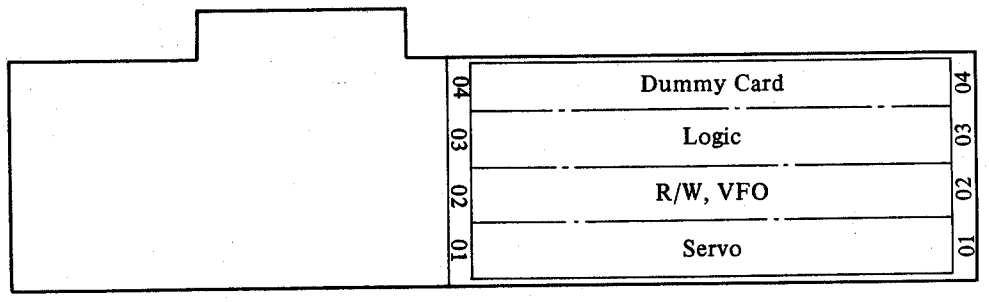


Figure 6.6.11 Card-cage PCB allocation

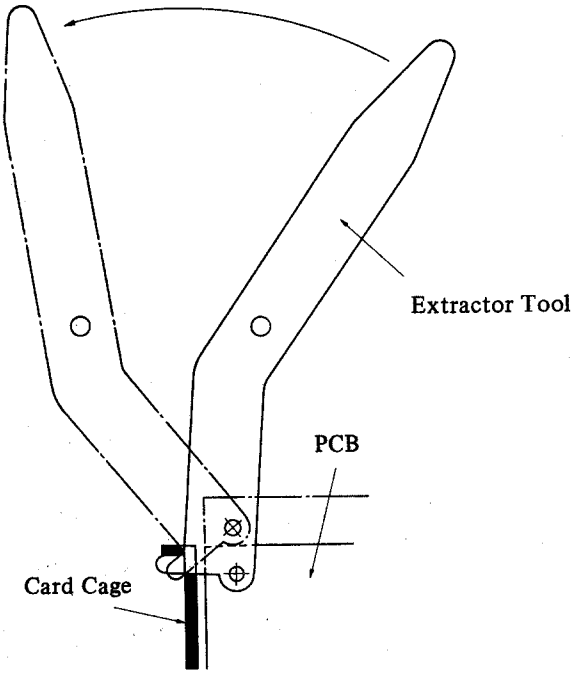


Figure 6.6.12 PCB removal

6.6.13 Back panel replacement

(1) Removal

① Remove all the PCBs in the card cage.

② Remove the connectors (CN11, 12, 15 ∿ 17) and SG wire on the back panel PCB (BRAMU).

③ Remove the interface PCBs. (Refer to subsection 6.6.7.)

④ Remove the 4 screws "A" fixing the card cage for interface PCBs.

⑤ Remove the 2 screws "B" holding the back panel PCB.

⑥ Remove the 4 screws "C" fixing the card cage and the PCB to the base plate of the drive.

⑦ Pull up the back panel assembly from the drive base.

⑧ Remove the 8 screws "D" fixing the PCB to the card cage, and pull apart the PCB.

(2) Installation

Follow, in reverse order, the procedures for removal.

6.6.14 Line terminator replacement

Refer to Figure 2.6.1.

(1) Removal

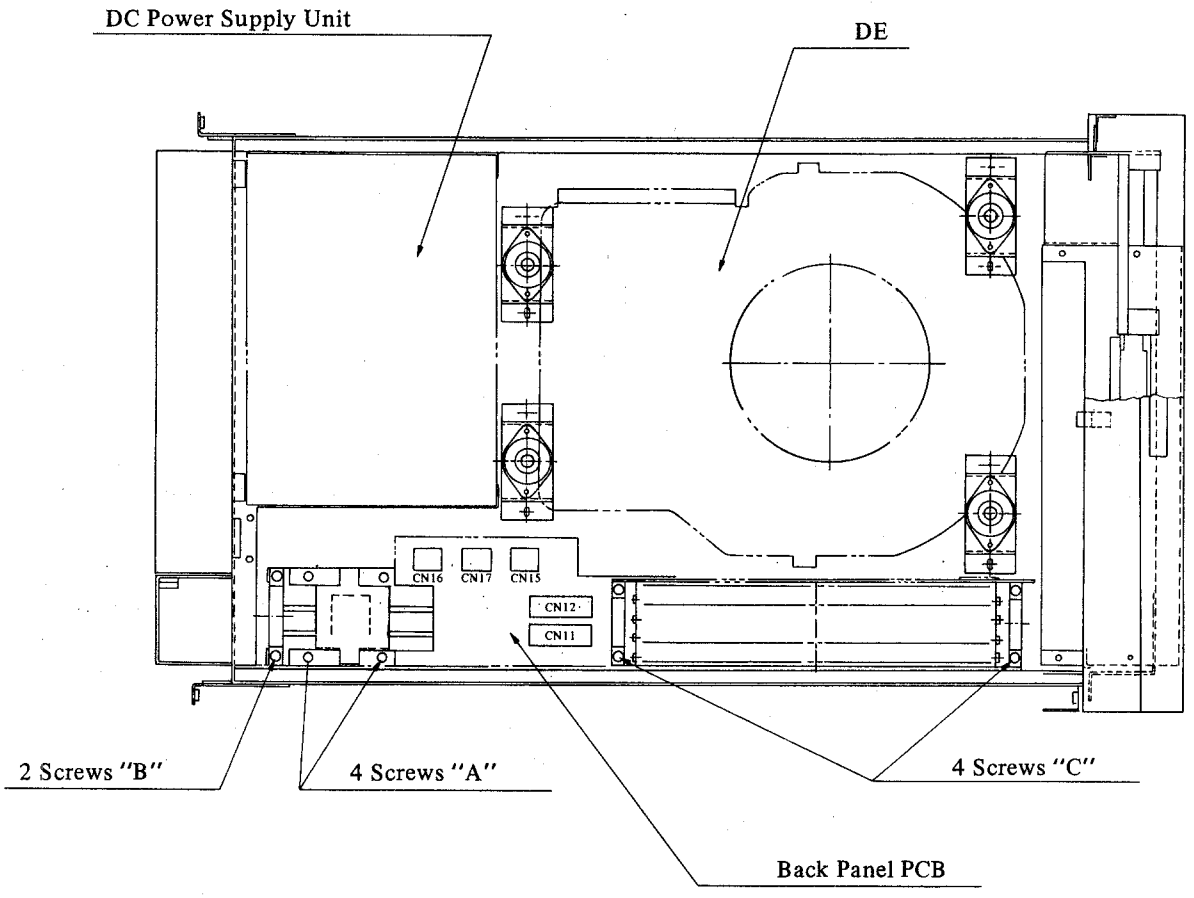
① Remove the screw holding the GND cable of the line terminator PCB to the GND terminal on a interface PCB.

② Pull and remove the line terminator PCB.

(2) Installation

Follow, in reverse order, the procedures for removal.

Caution: The line terminator PCB must be inserted with care to the "Out" connector for the A-cable.



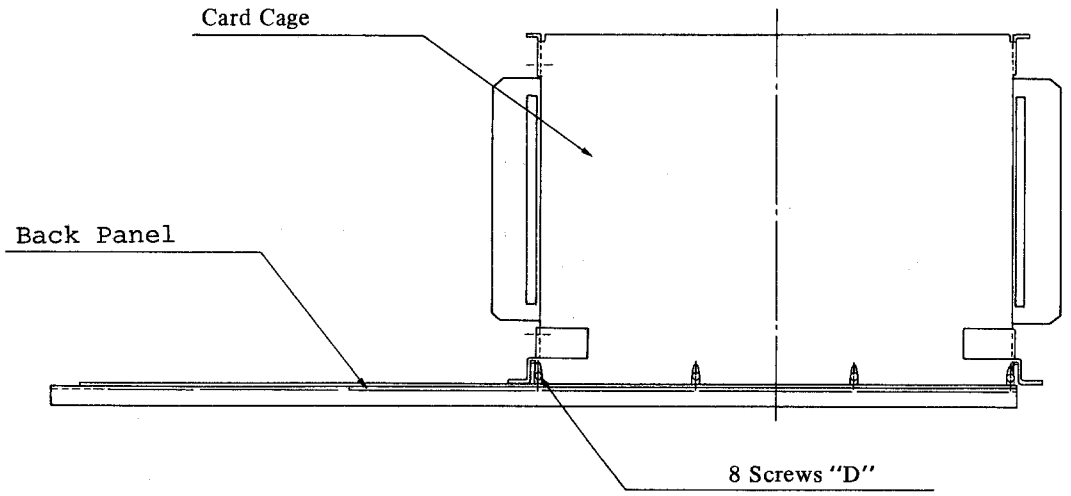


Figure 6.6.13 Back panel removal

6.7 PCB check and adjustment

6.7.1 Guide to PCBs and logic diagrams

Circuit diagrams contain input and output signal names (mnemonics), coordinate locations of ICs, input origines, destination coordinates of output signals, IC pin numbers and IC types. Figure 6.7.1 shows how to read circuit diagrams.

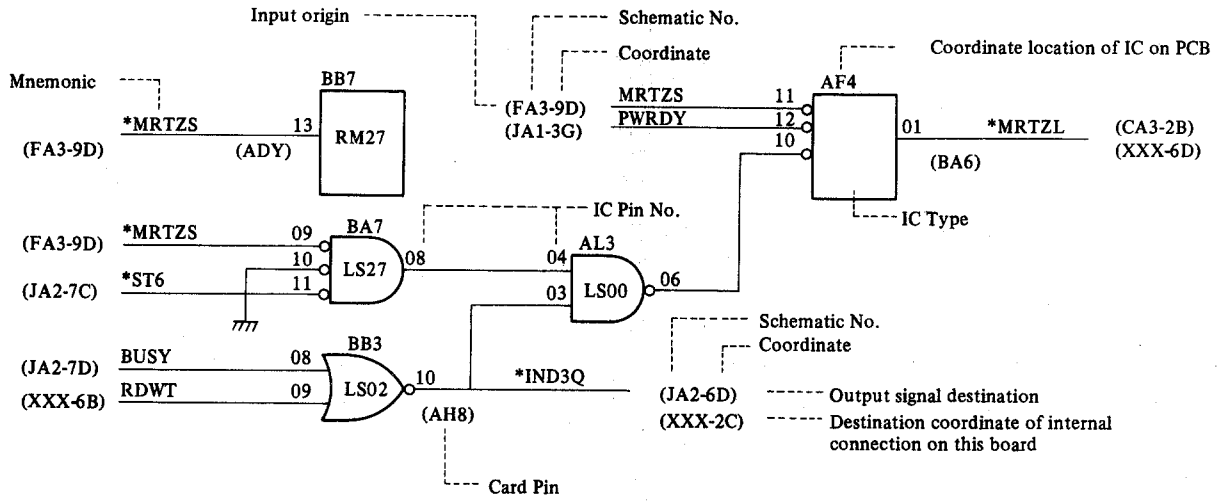


Figure 6.7.1 Logic Symbols

Figure 6.7.2 shows the IC location of logic PCB 532729U.
Figure 6.7.3 shows the pin numbering of a PCB.
Figure 6.7.4 shows the pin numbering of the back panel PCB.

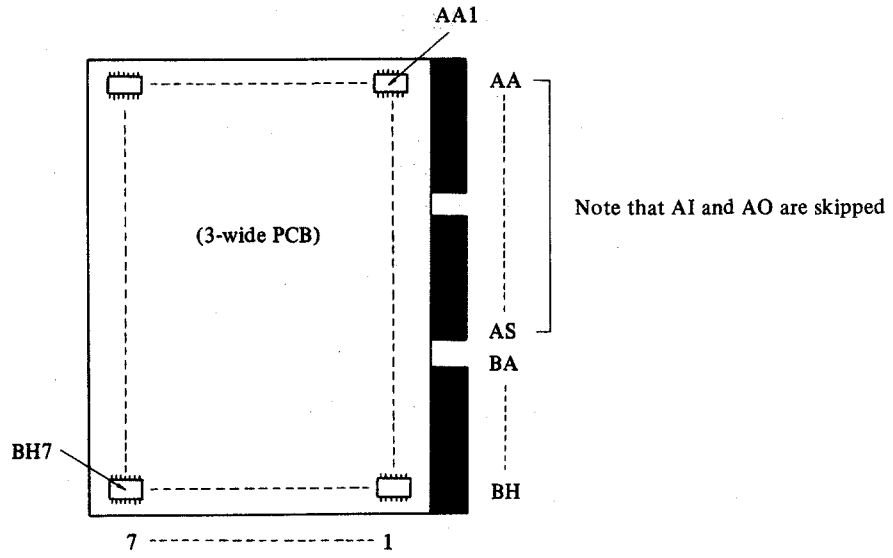


Figure 6.7.2 IC Location

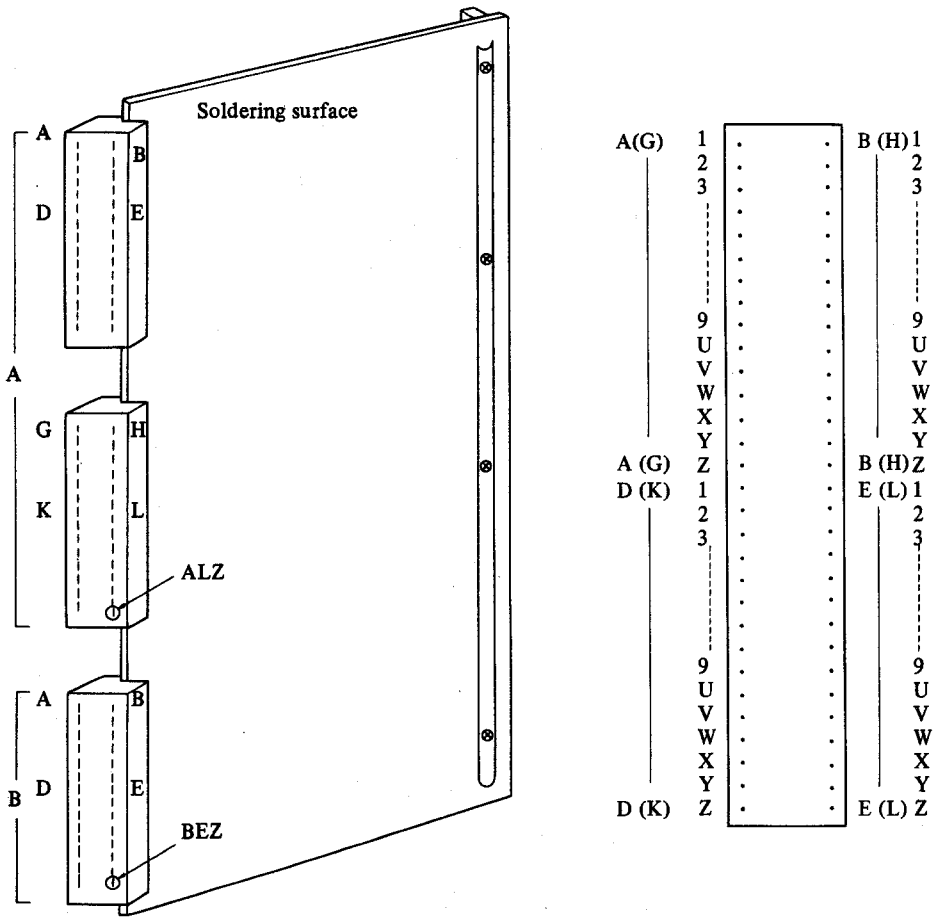


Figure 6.7.3 PCB Pin Numbering

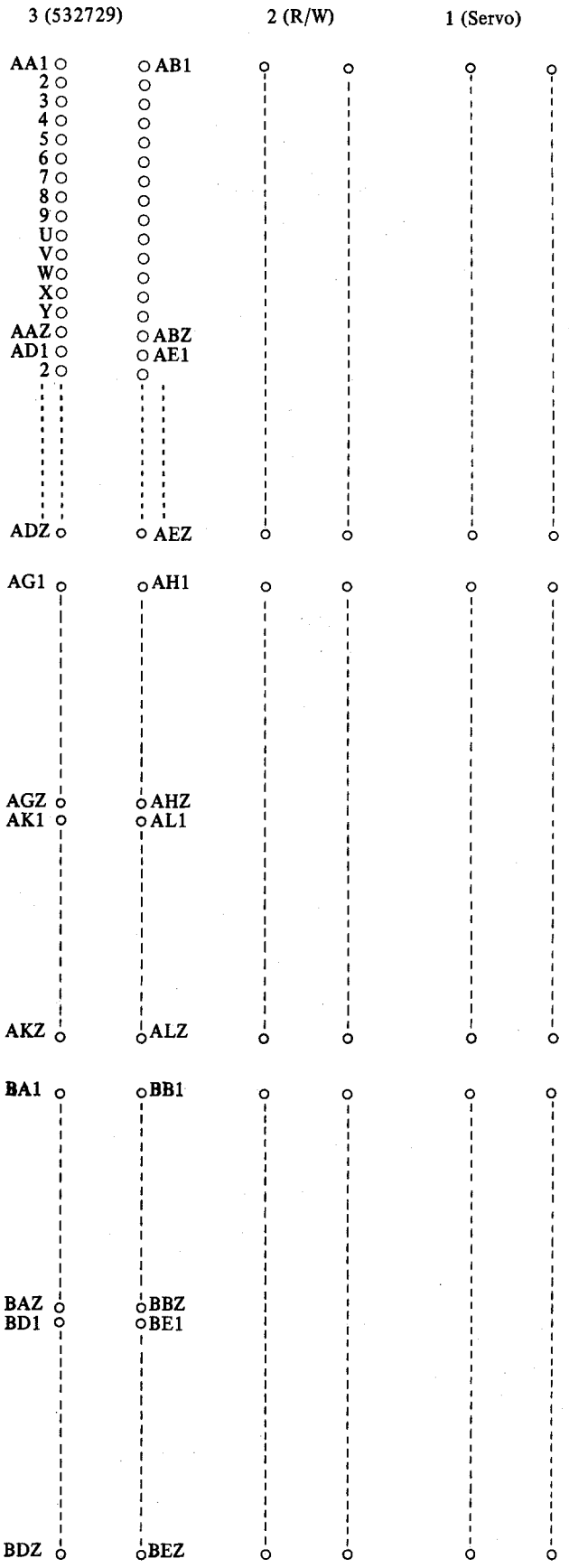


Figure 6.7.4 Back Panel Pin Numbering (Bottom View)

6.7.2 Adjustment of servo circuit

(1) Introduction

The following shows how to adjust and test the servo circuit.

If none of variable resistors have been adjusted, both "Static Adjustment" and "Dynamic Adjustment" are necessary. After changing the DE or Servo Circuit PCB, only "Dynamic Adjustment" is required, that is, only RVs 1, 2, 3, 4 and 5 may need to be adjusted.

Prior to the "Static Adjustment", stop the spindle, power off and pull out the connector CN04 which is the output cable of power amplifier to the coil of rotary actuator.

Refer to Table 6.7.1 for the function of potentiometers on the Servo Circuit PCB.

The test points and potentiometers located on the PCB Servo Circuit are shown in Figure 6.7.5.

Table 6.7.1 Function of Potentiometers

RV No.	Function	Sealed*
1	Position Signal Gain Adjustment	No
2	Transient Adjustment	No
3	Access time Adjustment	No
4	Velocity Offset Adjustemnt	No
5	Fine Control Settling Adjustment	No
6	Offset Adjustment of Desired Velocity Curve	Yes
7	VCO Free-Run Frequency Adjustment	Yes
8	Timer Gate Adjustment	Yes
9	Sync Gate Timing Adjustment	Yes
10	DAC Output Adjustment	Yes
11	Track Following Timer Adjustment	Yes
12	Access Timer Adjustment	Yes

* Do not touch the sealed RVs unless adjustments are required.

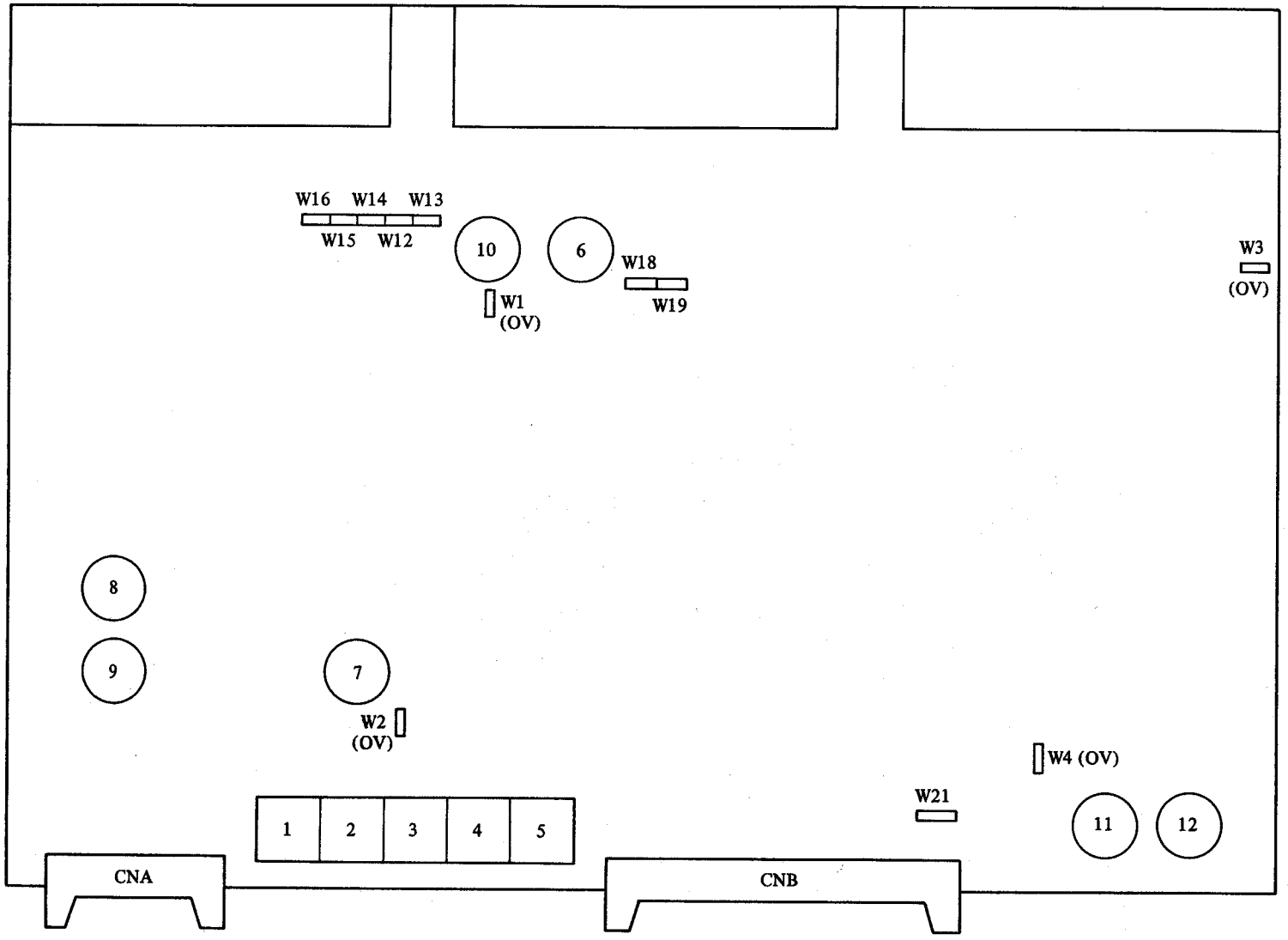


Figure 6.7.5 RVs and TPs (W No.) on PCB SVIAU
(OV pins of CNB are -06, -10, -16, -20, -26, -30, -36, -40 and -46.)

(2) Static Adjustment

a. VCO free-run frequency adjustment (RV7)

① Trigger by itself at the positive-going edge.

② Adjust the potentiometer RV6 so that the following Tvco is 102 ns±5 ns.

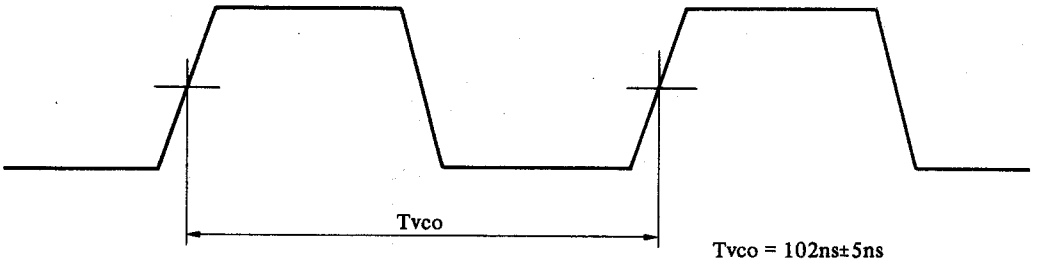


Figure 6.7.6 VCO Free-Run Frequency Adjustment

b. Pre-Adjustment of Servo Signal

① Connect the CNB-34 to an oscilloscope.

② Trigger by itself and adjust the potentiometer RV1 coarsely so that the signal amplitude is 7.0V±0.5V (peak-to-peak). Refer to Figure 6.7.7.

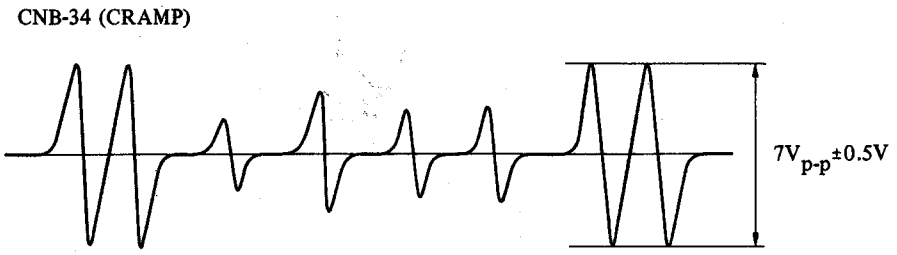


Figure 6.7.7 Pre-Adjustment of Servo Signal

c. Timer Gate Adjustment (RV8)

① Connect the CNB-32 to an oscilloscope.

② Trigger by itself at the negative-going edge.

③ Adjust the potentiometer RV8 so that the following T_{TG} is 320nx±10ns.

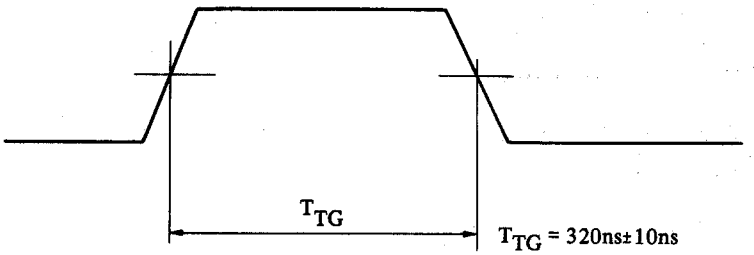


Figure 6.7.8 Timer Gate Adjustment

d. Sync Gate Timing Adjustment (RV9)

① Connect the CNB-24 of the Servo Circuit PCB to an oscilloscope and trigger with positive-going edge of this signal.

② Connect the CNB-28 of the Servo Circuit PCB to the other channel of the oscilloscope.

③ Adjust the potentiometer RV9 so that $T_1 = T_2 - 60ns \pm 10ns$ as shown in Figure 6.7-9.

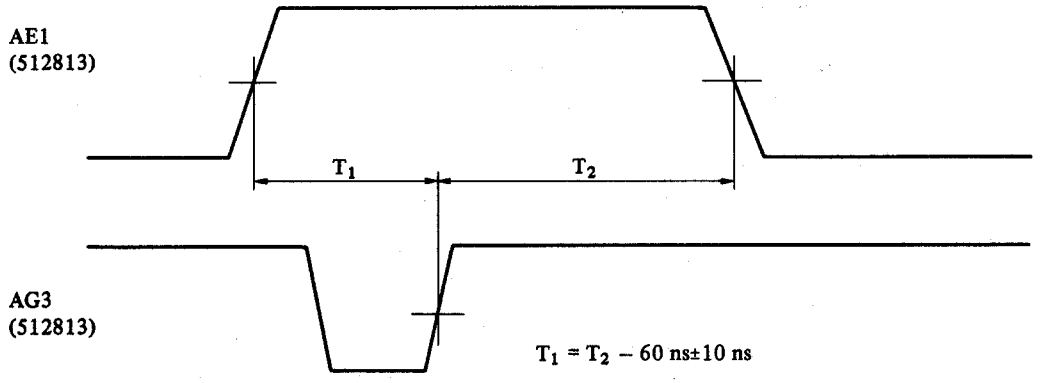


Figure 6.7.9 Sync Gate Timing Adjustment

e. Access Timer Adjustment (RV12)

① Connect the CNB-12 to an oscilloscope and trigger with positive-going edge of this signal.

② Toggle the MRZ switch on the CE panel and adjust the potensiometer RV12 so that T_{AT} is 250ms±10ms as shown in Figure 6.7.10.

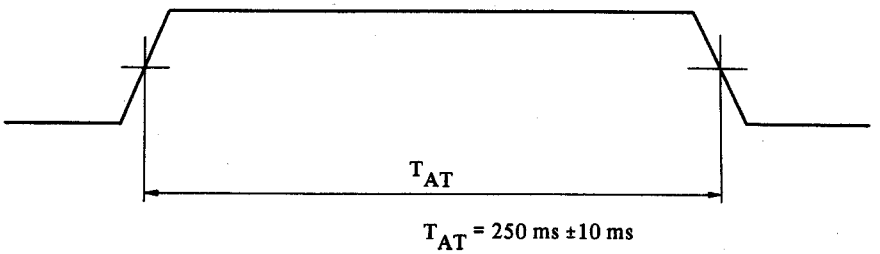


Figure 6.7.10 Access Timer Adjustment

f. Offset Adjustment of Desired Velocity Curve (RV6)

① Connect the test points W18 and W19 to a digital voltmeter.

② Adjust the potentiometer R6 so that $|Vw_{18} - Vw_{19}|$ is 0.5mV, Vw_{18} and Vw_{19} are Voltages of w_{18} and w_{19} respectively.

g. Track Following Timer Adjustment (RV11)

① Turn power off.

② Connect CN04 which is the output cable of the power amplifier to the coil of rotary actuator.

③ Turn power on.

④ Turn on the start switch on the operator panel and wait for one minute. If the ready lamp does not light after one minute, adjust coarsely the potentiometer RV3 toggling the MRZ switch on the CE panel so as to get READY.

⑤ Connect the CNB-11 to an oscilloscope and trigger with negative-going edge of this signal.

⑥ Toggle the MRZ switch repeatedly and adjust the potentiometer RV11 so that T_{TF} is 2.5ms±0.1ms as shown in Figure 6.7.11.

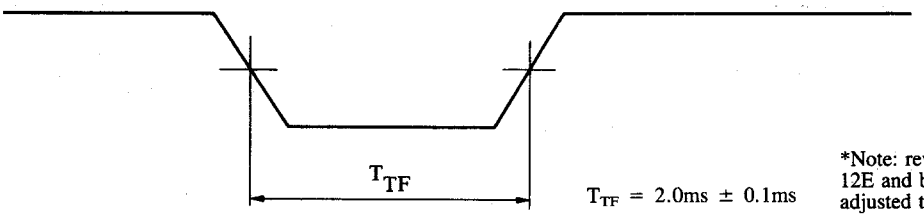
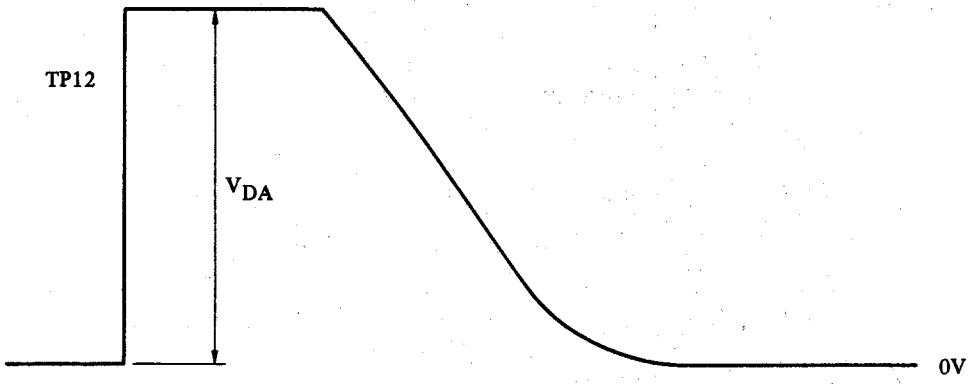


Figure 6.7.11 Track Following Timer Adjustment

h. DAC Output Adjustment (RV10)

① Connect the test point W18 to an oscilloscope.

② Execute the diagnostic routine mode 02, which issues repetitive seek command between cyl.384 and cyl.640, and adjust the potentiometer RV10 so that V_{DA} is 6.0V±0.1V as shown in Figure 6.7.12.



V_{DA} = 6V ±0.1V

Figure 6.7.12 DAC Output Adjustment

(3) Dynamic Adjustment

a. Position signal Gain Adjustment (RV1)

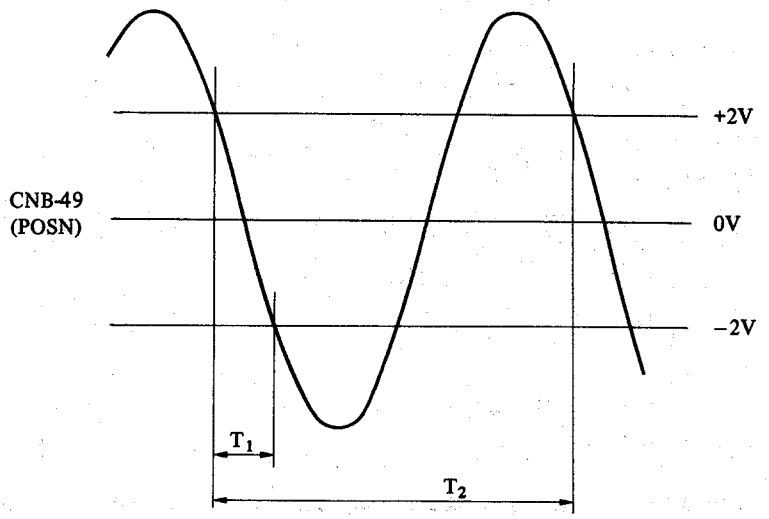
① Confirm that the drive has a normal status.

② Connect the CNB-49 to an oscilloscope.

③ Execute the diagnostic routine mode 03, which issues repetitive RTZ command from cyl.841.

④ Trigger the oscilloscope with the negative-going edge of the CNB-49 signal.

⑤ Adjust potentiometer RV1 so that the following $T_2 = 5.8 \times T_1 \pm 2\%$ as shown in figure 6.7.13.



$$\frac{T_1}{T_2} = \frac{1}{5.8} \pm 2\% \fallingdotseq \frac{1.7}{10}$$

Figure 6.7.13 Position Signal Gain Adjustment

b. Velocity Offset Adjustment (RV4)

① Connect the CNB-43 to one vertical input channel of an oscilloscope and trigger with the negative-going edge of this signal.

② Connect the CNB-49 to the other vertical channel of the oscilloscope.

③ Execute the diagnostic routine mode 01 which issues repetitive seek command between cyl.000 and cyl.006.

④ Adjust the potentiometer RV4 so as to get the following figure.

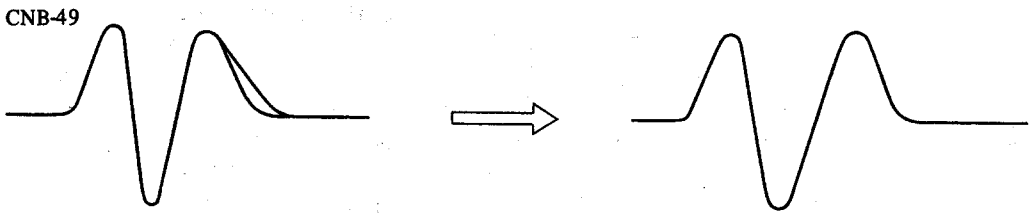


Figure 6.7.14 Velocity Offset Adjustment

c. Fine Control Settling Adjustment (RV5)

① Do the same procedures ① ∿ ③ in RV4 adjustment.

② Adjust the potentiometer RV5 so as to get the following figure.

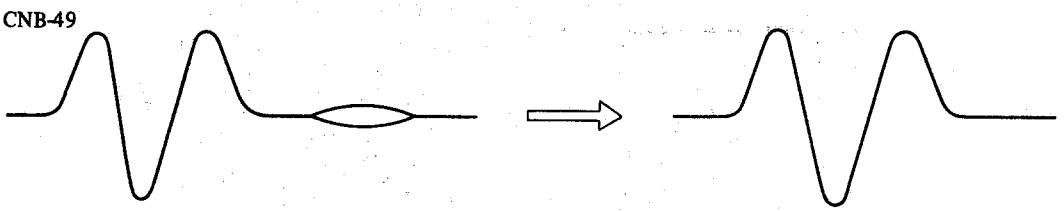


Figure 6.7.15 Fine Control Settling Adjustment

d. Access Time and Transient Adjustment (RV2, RV3)

① Connect the CNB-43 to one vertical input channel of an oscilloscope and trigger with the negative-going edge of this signal.

② Connect the CNB-49 to the other vertical channel of the oscilloscope.

③ Execute the diagnostic routine mode 02 which issues repetitive seek command between cyl. 384 and cyl.640.

④ Adjust the potentiometers RV2 and RV3 so as to realize following figures.

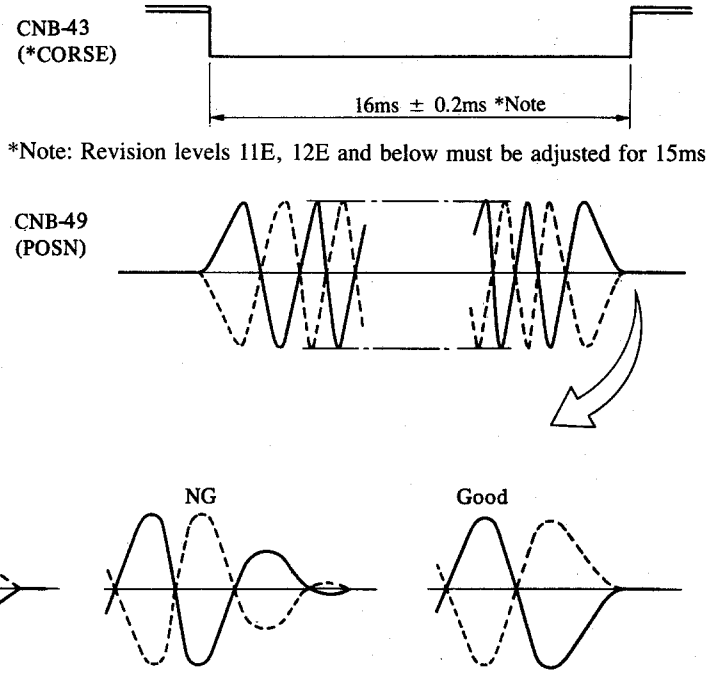


Figure 6.7.16 Access Time and Transient Adjustment

6.7.3 Adjustment of Read/Write circuit

The following describes how to adjust and test the Read/Write circuit in case none of variable resistors have been adjusted.
PCB 550204U must be inserted in Extender Unit.
Refer to Table 6.7.2 and Figure 6.7.17 for monitor point and location.

Table 6.7.2 Variable Resistors in Read/Write Circuit

Item	RV No.	Test Point	Specification
+6V (DC Voltage)	RV 1	W6	+6V ± 0.01V
Write Current	RV 2	Refer to (1)	
Floating Slice Level	RV 6	W4	Refer to (2)
Fixed Slice Level	RV 7	W5	+4.2V ± 0.01V
Balance of Read Signal	RV 8	(ADX, AEX) W23, W24	Refer to (3)
Floating Slice Level at AM Mode	RV 9	W4	Refer to (2)

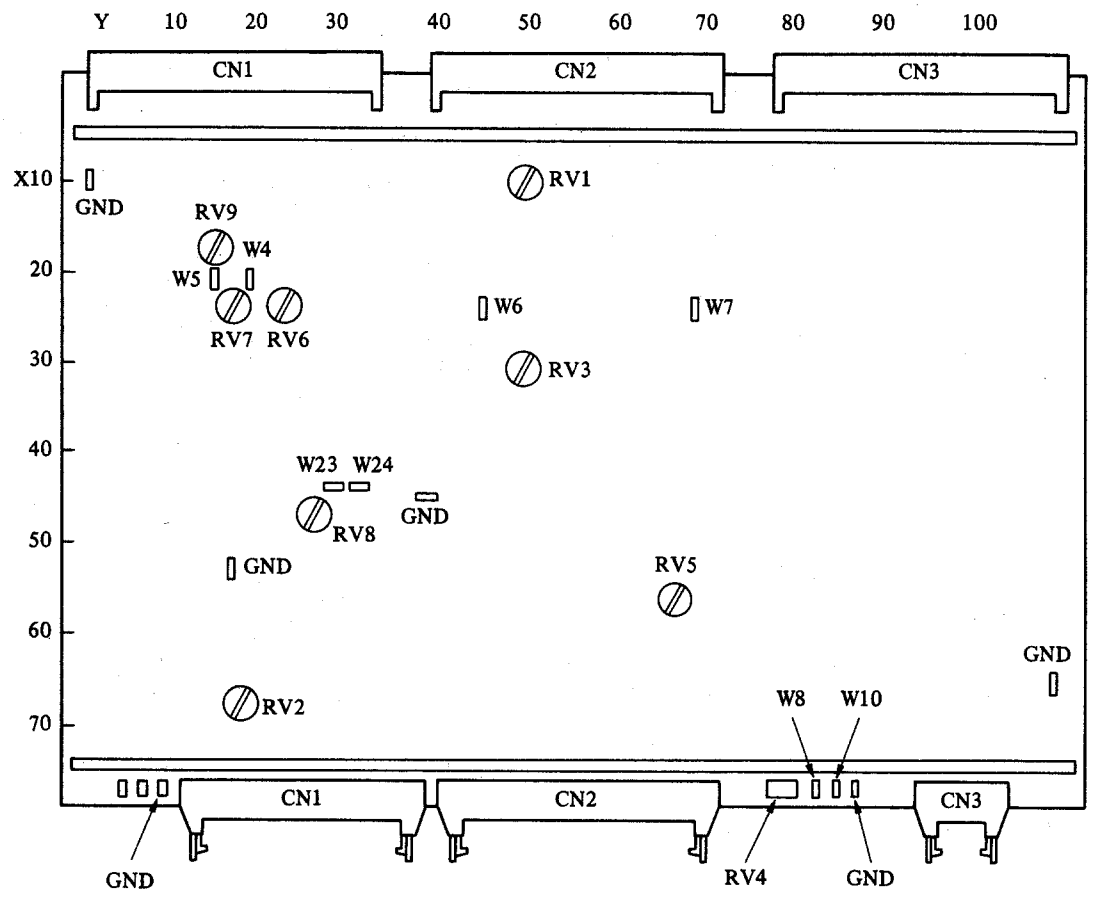


Figure 6.7.17 Variable Resistors on PCB 550204

(1) Write Current Adjustment (RV2)

The connector in Figure 14.3-2 must be inserted into the Connector CN1 in Figure 6.7.18.

Connect CN2-44 (Connector 2, Pin 44) and CN2-49 (Connector 2, Pin 49) to ground, and adjust RV2 so that the differential output voltage V1 in Figure 6.7.18 is -1.020V±0.03V.

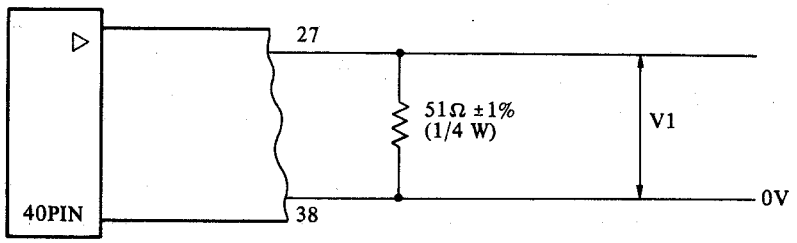


Figure 6.7.18 The Connector to Adjust the write current

(2) Floating Slice Level Adjustment

1 AM Mode

Table 6.7.3 RV9 Adjustment

RV No.	Test Point	Specification
RV. 9	W4	+4.8V±0.01V

2 Normal Mode

Connect CN2-46 (Connector 2, Pin 46) to ground, and adjust RB6 according to the following table.

Table 6.7.4 RV6 Adjustment

RV No.	Test Point	Specification
RV. 6	W4	+3.0V±0.01V

(3) Balance of Read Signal (RV8)

Read the data recorded in Variable Sector Format on Cylinder 00 and Head 01, and adjust RV8 so that the read signal matches Figure 6.7.19.

Verify that, this balanced waveform is maintained on Cylinder 256, 512 and 841 for Head 00 and 01.

NSQHG
CN2-48

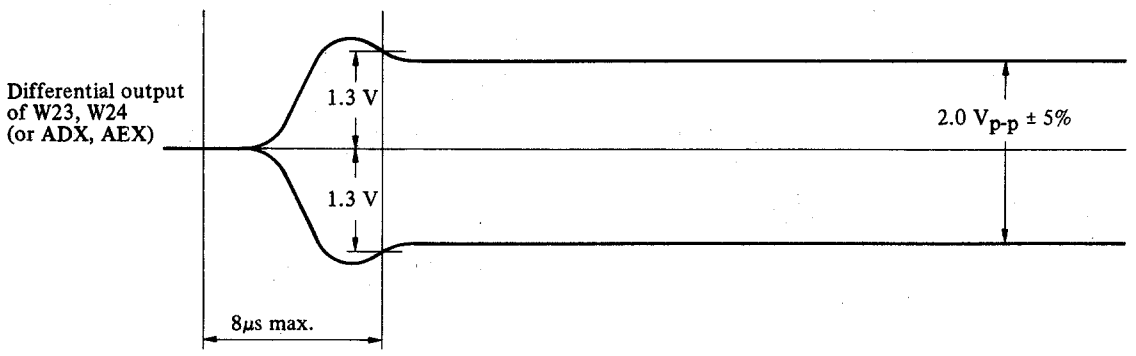


Figure 6.7.19 Balance of Read Signal

6.7.4 Adjustment of VFO circuit

The following describes how to adjust and test the VFO (Modulator and Demodulator) circuit (PCB 550204U) in case none of variable resistors have been adjusted. Refer to Table 6.7.5 and Figure 6.7.17 for monitor point and location.

Table 6.7.5 Variable Resistors in VFO Circuit

Item	RV No.	Test point	Specification
VCO Free-running Frequency	RV5	W10	Refer to (1)
Reference Pulse Width	RV3	W7	Refer to (2)
Phase Adjustment	RV4	W8 W10	Refer to (3)

(1) VCO Free-running Frequency (RV5)

Connect CN2-24 (Connector 2, Pin 24) to ground, and adjust RV5 so that the pulse period or frequency of W10 matches Figure 6.7.20.
Disconnect the cable between CN2-24 and ground after adjust or confirm the the item.

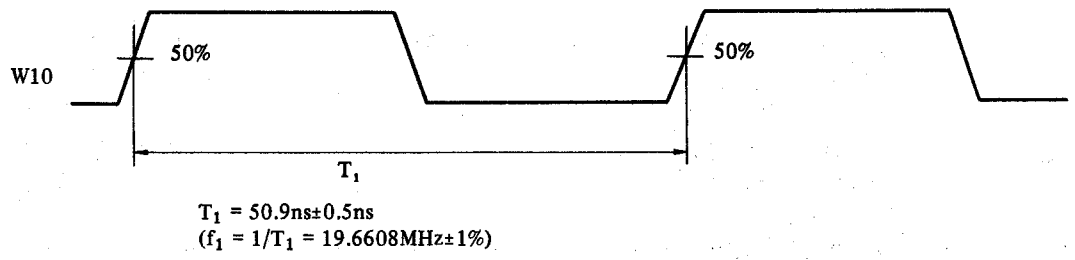


Figure 6.7.20 VCO Free-running Frequency Adjustment

(2) Reference Pulse width (RV3)

Read or write any data, and adjust RV3 so that the pulse width of W7 matches Figure 6.7.21.

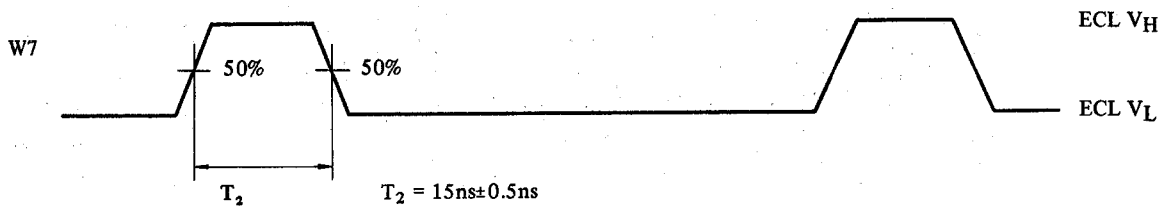


Figure 6.7.21 Reference Pulse width Adjustment

(3) Phase adjustment (RV4)

Read the data pattern of "00...00", and adjust RV4 so that the phase between W8 and W10 matches Figure 6.7.22.

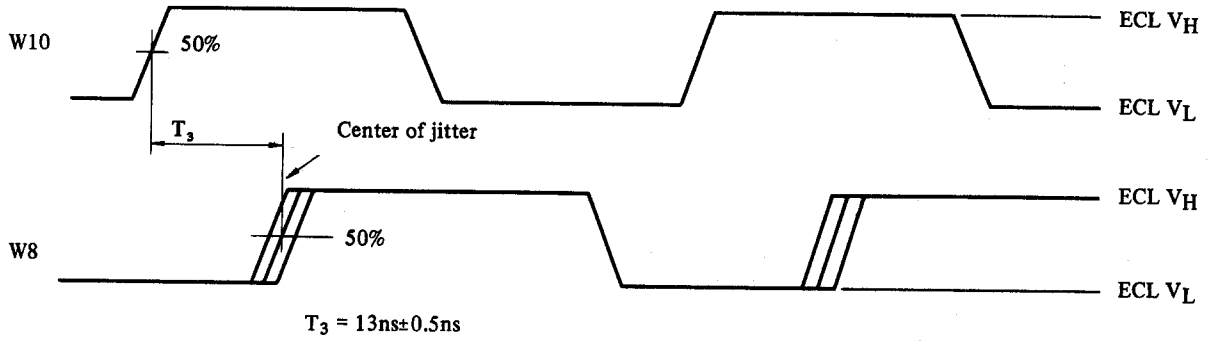


Figure 6.7.22 Phase Adjustment

7.1 Explanation

7.1.1 Illustrations

The illustration gives an exploded view of an assembly, and sparate parts and how they fit together. Each part has a number corresponding to an Index No. on the parts list.

7.1.2 Parts list

The parts list gives the index number, composition and quantity, specification, and description for each part of the assembly.

(1) INDEX NO.

The number which corresponds with a part's number in the illustration.

- When the mark "*" precedes the index number, the part is a spare part.
- When a "-" is given, the part (screw or washer) is not shown in the illustration.
- When blank, and the QUANTITY and SPECIFICATION are given, a whole of that part is not shown in the illustration or that part is illustrated for detail breakdown in the other page.

(2) COMPOSITION & QUANTITY

These columns are shown the relationship between units, assemblies, subassemblies, and parts. A unit indicated in a column is assembled the parts indicated in the next right column. The figure is the quantity needed to assemble into on higher assembled unit.

(3) SPECIFICATIONS

Part number of the units, assemblies, subassemblies, or parts.

(4) DESCRIPTION

The part name, applicable device number, and other information are given in this column.

FIGURE 1 FINAL ASSEMBLY

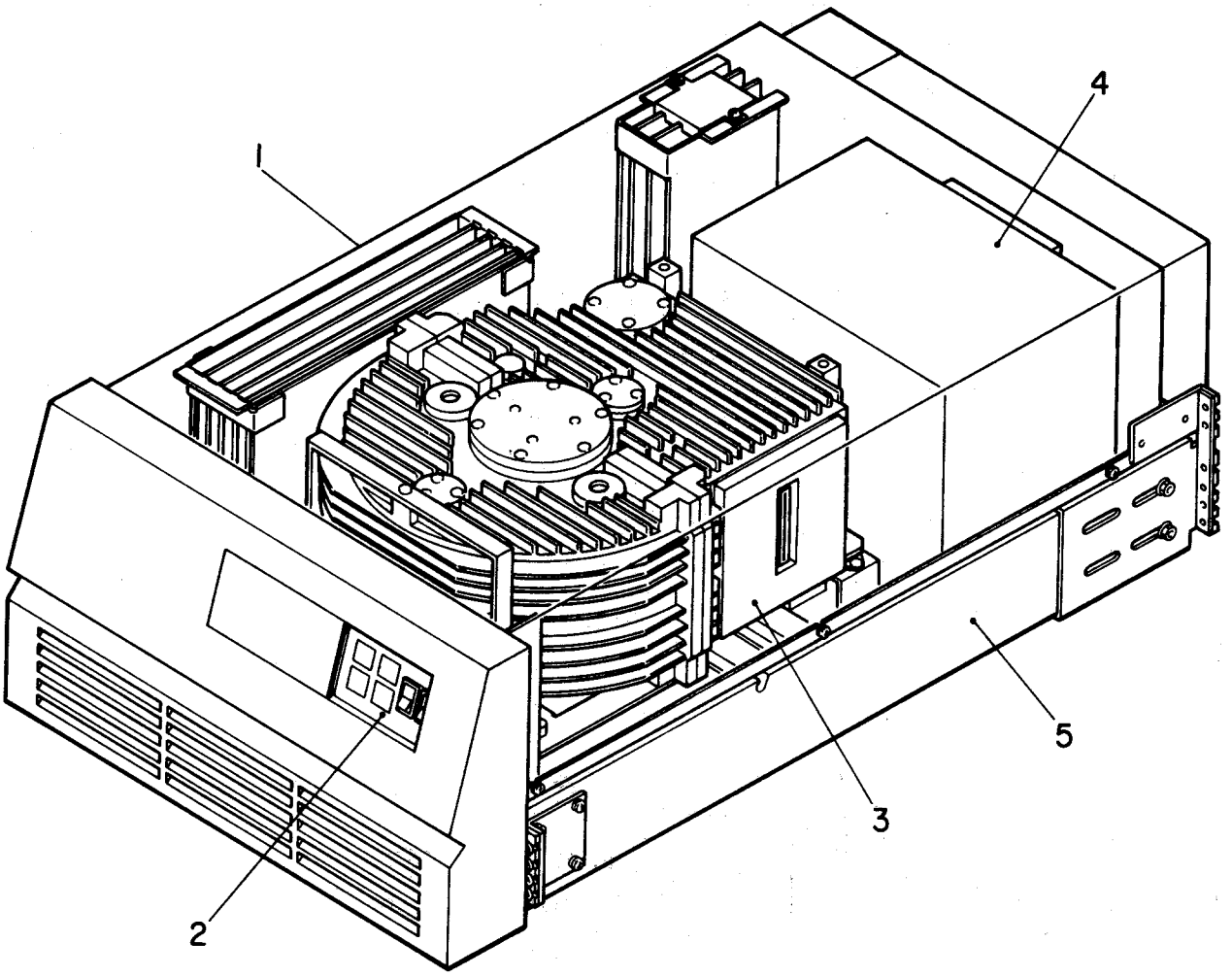


FIGURE 1 FINAL ASSEMBLY

INDEX NO.	COMPOSITION & QUANTITY	SPECIFICATIONS	DESCRIPTION
	1	B03B-4825-B001A	M2361A mini-disk drive
1	1	B210-1985-T001A	Frame assembly (FIG 2)
2	1	N860-3346-T001	Operator panel (FIG 2)
3	1	B03B-4825-T001A	DE assembly (FIG 3)
4	1	B14L-5105-0182A	DC power supply (FIG 3)
5	1	B03B-4825-D020A	Slide guide assembly (option)

FIGURE 2 MECHANICAL ASSEMBLY

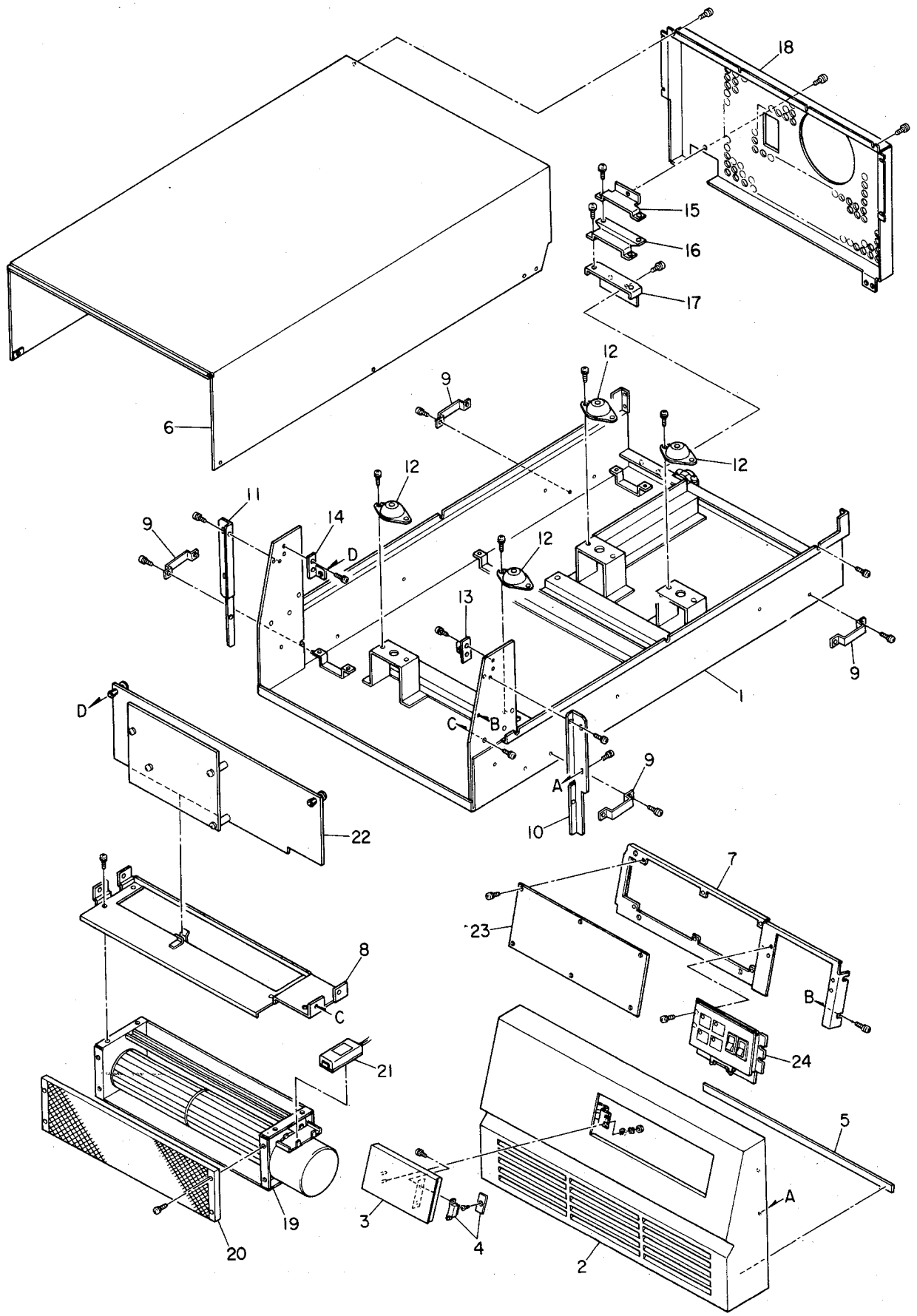


FIGURE 2 MECHANICAL ASSEMBLY

INDEX NO.	COMPOSITION & QUANTITY								SPECIFICATIONS	DESCRIPTION
										Cross-refer to FIGURE 1
	1								B210-1985-T001A	Frame assembly
1		1							B210-1985-V100A	Sub-frame assembly
		1							B210-1985-V200A	Front panel
2			1						B210-1985-W201A	Panel
3			1						B210-1985-W220A	Panel
-			2						F6-N1-3S	Nut
-			2						F6-WM-3S	Washer
-			2						F6-WB-3S	Washer
-			1						F6-SSA-2.5x6S-M-NI1A	Screw
4			1						CT-TL-98-AL-F	Magnet catch
-			2						F6-SW2NA-2x6S	Screw
5			1						B210-1820-X324A	Conductive rubber
-		4							F6-SW2NA-4x10S-M-NI1A	Screw
6		1							B210-1985-W001A	Top cover
-		6							F6-SW2NA-4x10S-M-NI1A	Screw
7		1							B210-1985-X002A	Panel
-		4							F6-SW2NA-4x10S-M-NI1A	Screw
8		1							B210-1985-W003A	Bracket
-		4							F6-SW2NA-4x10S-M-NI1A	Screw
9		4							B210-1820-X113A	Guide
-		8							F6-SW2NA-4x10S-M-NI1A	Screw
10		1							B210-1985-X007A	Plate
-		2							F6-SW2NA-4x10S-M-NI1A	Screw

FIGURE 2 MECHANICAL ASSEMBLY

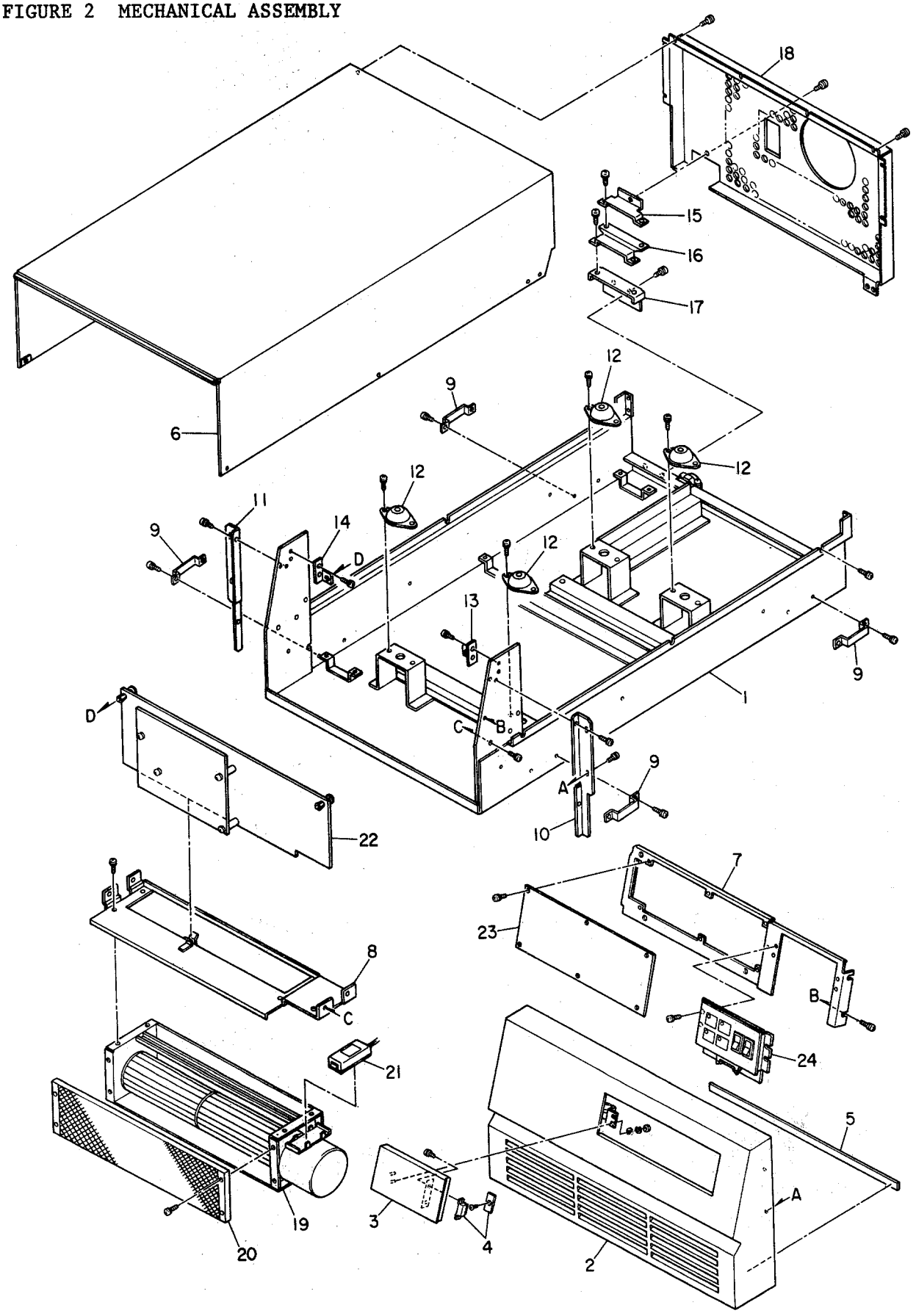


FIGURE 2 MECHANICAL ASSEMBLY - continued

INDEX NO.	COMPOSITION & QUANTITY	SPECIFICATIONS	DESCRIPTION
11	1	B210-1985-X008A	Plate
-	2	F6-SW2NA-4x10S-M-NI1A	Screw
12	4	B30L-0860-0400A	Rubber cushion
-	8	F6-SW2NA-4x10S-M-NI1A	Screw
13	1	B210-1985-X012A	Bracket
-	2	F6-SW2NA-4x10S-M-NI1A	Screw
14	1	B210-1985-X013A	Bracket
-	2	F6-SW2NA-4x10S-M-NI1A	Screw
15	1	B210-1985-X021A	Clamp base
-	2	F6-SW2NA-4x10S-M-NI1A	Screw
16	1	B210-1985-X022A	Clamp
-	2	F6-SW2NA-4x10S-M-NI1A	Screw
17	1	B210-1985-X023A	Clamp
-	2	F6-SW2NA-4x10S-M-NI1A	Screw
18	1	B210-1985-X024A	Rear cover
-	9	F6-SW2NA-4x10S-M-NI1A	Screw
*19	1	C90L-1370-0900	Line blower
-	4	F6-SW2NA-4x10S-M-NI1A	Screw
*20	1	B90L-1570-0001A	Air filter
-	2	F6-SW2NA-4x10S-M-NI1A	Screw
21	1	C90L-1350-0001	Fan sensor
*22	1	B17B-0250-0010A#U	PCB (Power amplifier)
*23	1	B17B-0270-0010A#U	PCB (Indicator)
-	6	F6-SW2NA-4x10S-M-NI1A	Screw

FIGURE 2 MECHANICAL ASSEMBLY - continued

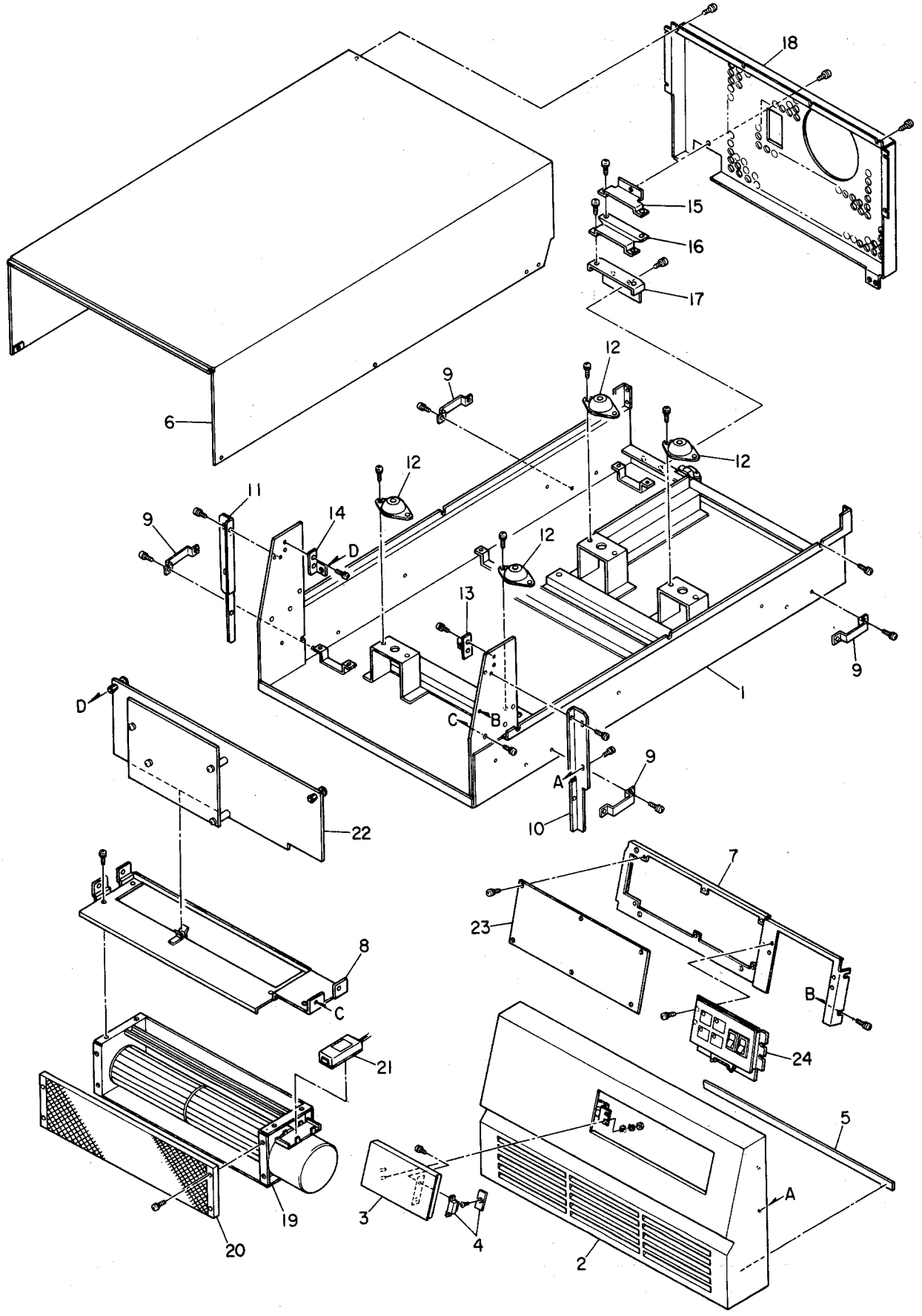


FIGURE 2 MECHANICAL ASSEMBLY - continued

INDEX NO.	COMPOSITION & QUANTITY	SPECIFICATIONS	DESCRIPTION
*24	1	N860-3346-T001	Operator panel
-	4	F6-SW2NA-4x10S-M-NI1A	Screw

FIGURE 3 DE, CARD CAGE & POWER SUPPLY

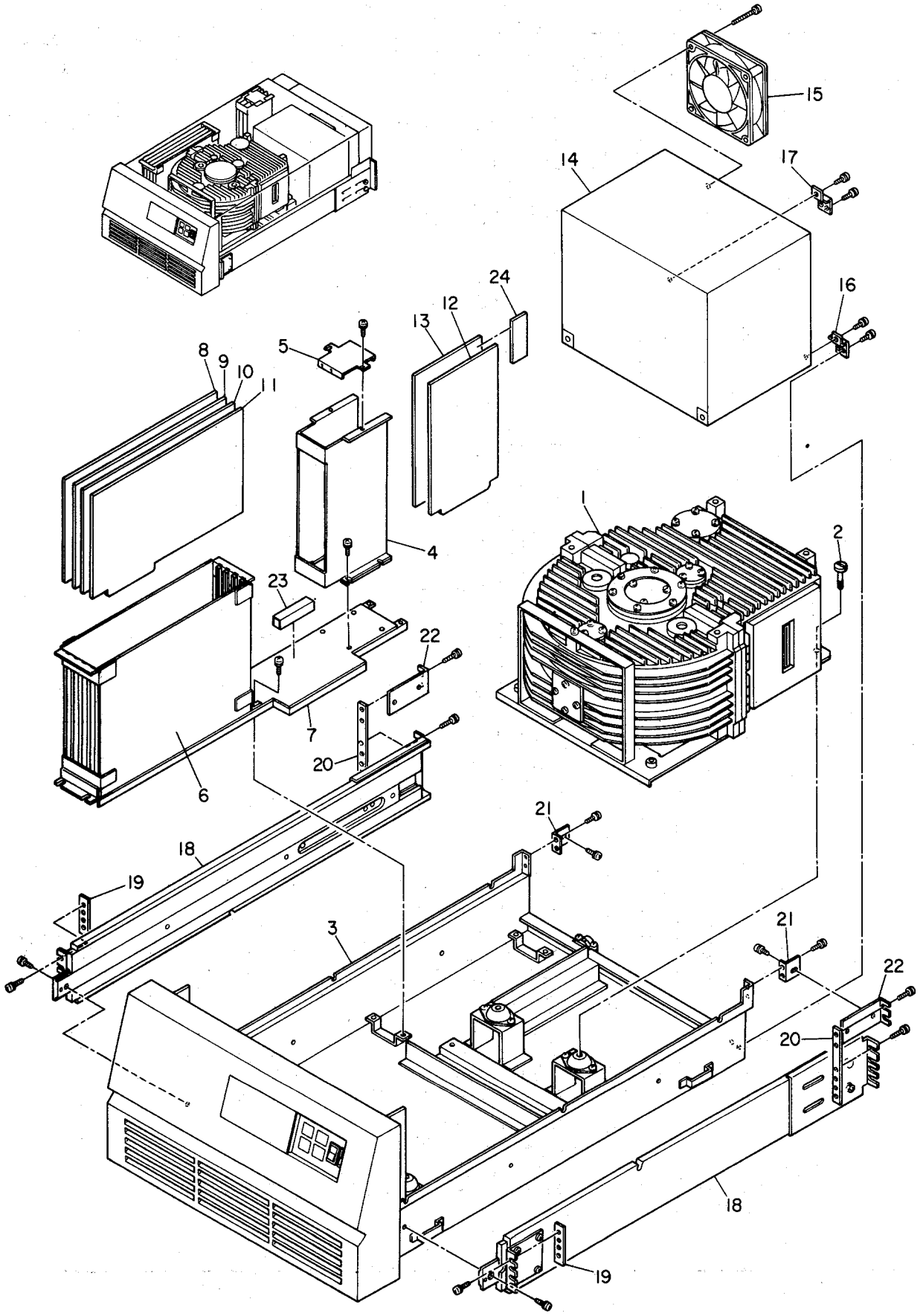


FIGURE 3 DE, CARD CAGE & POWER SUPPLY

INDEX NO.	COMPOSITION & QUANTITY	SPECIFICATIONS	DESCRIPTION
			Cross refer to FIGURE 1
*1	1	B03B-4825-T001A	DE assembly
2	4	B210-1985-X255A	Screw
3	1	B210-1985-T001A	Frame assembly
4	1	B210-1985-W004A	Frame
-	4	F6-SW2NA-4x10S-M-NI1A	Screw
5	1	B210-1985-W006A	Retaining bracket
-	2	F6-SW2NA-4x10S-M-NI1A	Screw
	1	B03B-4825-D010A	Card cage assembly
6	1	B210-1985-V050A	Card cage
*7	1	B03B-4825-E010A#U	PCB (Back panel)
-	8	F6-SW2NA-2.5x6S	Screw
*8	1	C16B-5502-0050#U	PCB (Servo)
*9	1	C16B-5502-0040#U	PCB (R/W, VFO)
*10	1	C16B-5327-0290#U	PCB (Logic)
11	1	C970-0030-X077	Dummy card
-	6	F6-SW2NA-4x10S-M-NI1A	Screw
*12	1	B17B-0230-0010A#U	PCB (Interface, Basic)
*13	1	B17B-0240-0010A#U	PCB (Interface, Dual) (option)
14	1	B14L-5105-0182A	DC power supply
-	2	F6-SW2NA-4x10S-M-NI1A	Screw
*15	1	B03B-4825-D030A	Fan
-	4	F6-SW2NA-4x35-M-NI1A	Screw

FIGURE 3 DE, CARD CAGE & POWER SUPPLY

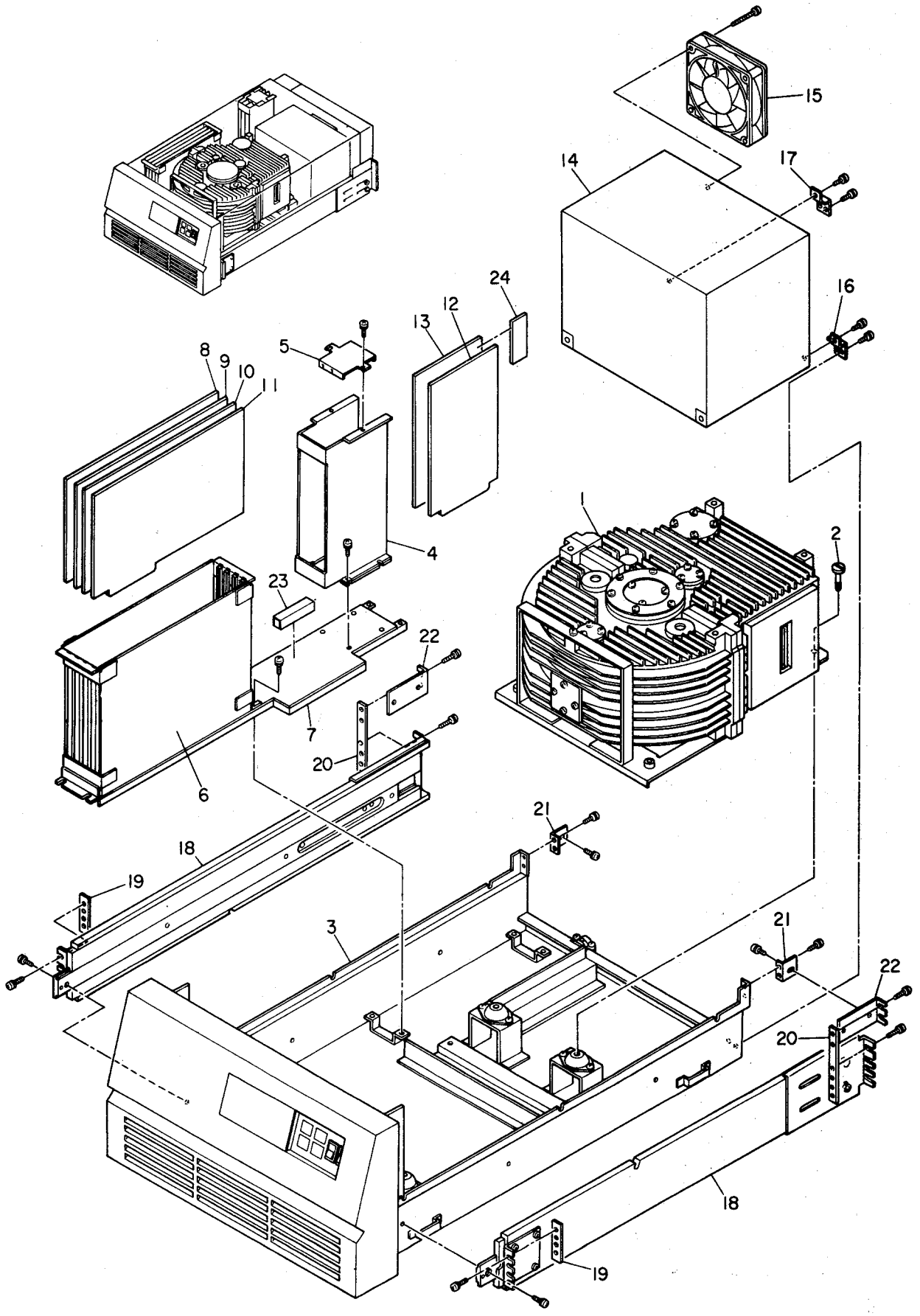


FIGURE 3 DE, CARD CAGE & POWER SUPPLY - continued

INDEX NO.	COMPOSITION & QUANTITY	SPECIFICATIONS	DESCRIPTION
16	1	B210-1985-X009A	Bracket
-	2	F6-SW2NA-4x10S-M-NI1A	Screw
17	1	B210-1985-X010A	Bracket
-	2	F6-SW2NA-4x10S-M-NI1A	Screw
	1	B03B-4825-D020A	Slide guide assembly (option)
18	1	B27L-0230-0016A	Slide guide
-	8	F6-SBD-4x6S-M-NI1A	Screw
10	2	B210-1985-X271A	Tapped plate
20	2	B210-1985-X272A	Tapped plate
-	20	F6-SW2NA-5x16S-M-NI1A	Screw
21	2	B210-1985-X273A	Bracket
22	2	B210-1985-X274A	Stopper
-	6	F6-SW2NA-4x10S-M-NI1A	Screw
23	1	B61L-0140-0011A#10000	Hour meter (option)
24	1	B03L-4790-0003A	Terminator (option)

CONTENTS

MODEL NO. & NAME: M2361A Mini-Disk Drives

TITLE

DRAW. NO B03Q — 4825 — 0010A | DIST. 6

EDIT | DATE | DESIG. | CHECK | DESCRIPTION

DESIG. 1985・09・09 | DRAWN | CHECK | APPR.

FUJITSU LIMITED | SHEET 001 / 3

49. 4 FDXA-4902-3

CONTENTS

MODEL NO. & NAME: M2361A Mini-Disk Drives

EDIT.	DATE	DESIG.	CHECK	DESCRIPTION
DESIG.		DRAWN	CHECK	APPR.

TITLE

DRAW. NO B03Q — 4825 — 0010A CUST. 6

FUJITSU LIMITED SHEET 002/

49. 4 FDXA-4902-3

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MODEL NO. & NAME: M2361A Mini-Disk Drives

EDIT.	DATE	DESIG.	CHECK	DESCRIPTION

DESIG. | DRAWN | CHECK | APPR.

TITLE

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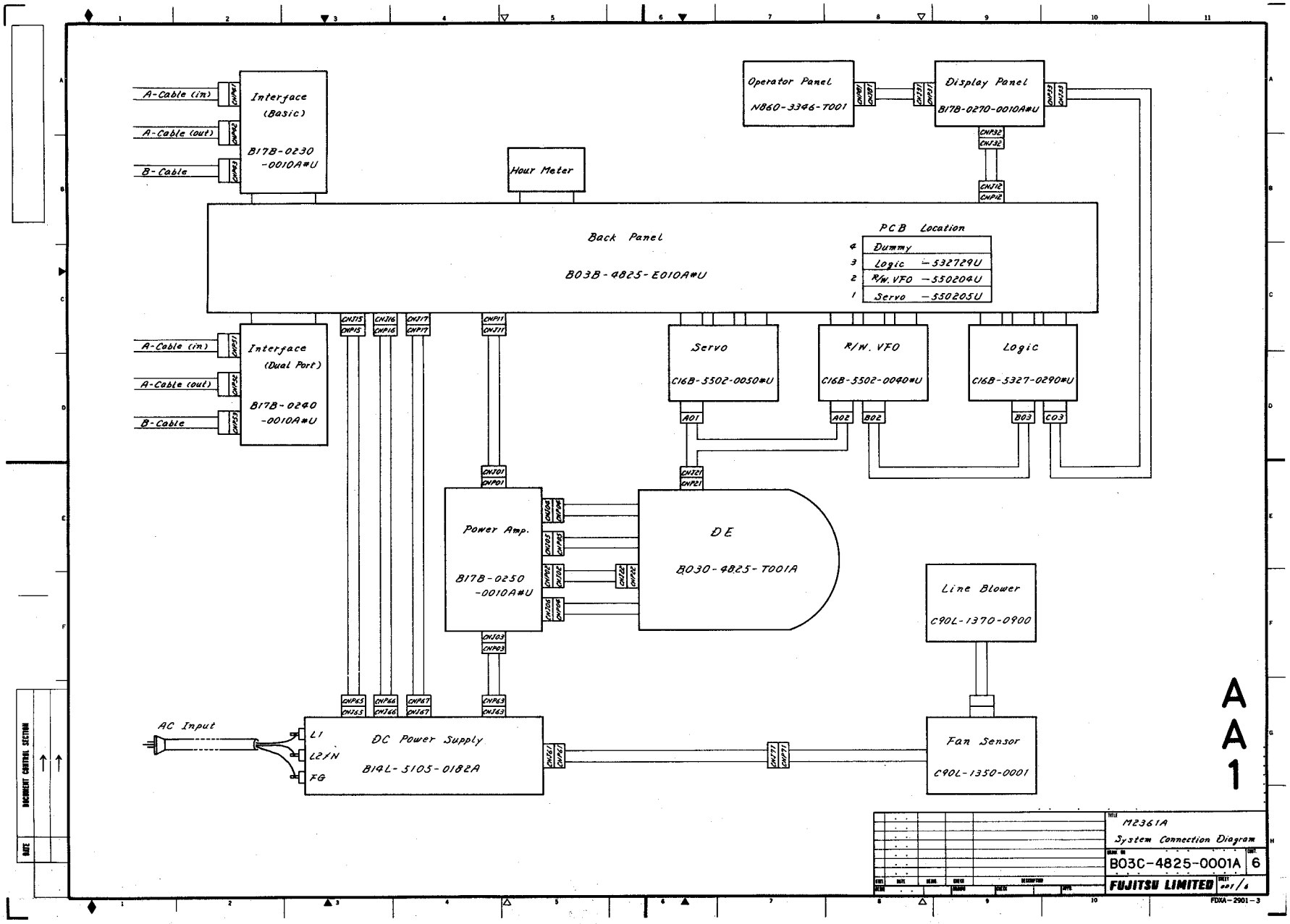
FUJITSU LIMITED | SHEET 003 / 3

49. 4 FDXA-4902-3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A-Cable (out)
B-Cable
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Hour Meter
Operator Panel
N860-3346-T001
Display Panel
B17B-0270-0010A#U
Back Panel
B03B-4825-E010A#U
PCB Location
4 Dummy
3 Logic -532729U
2 R/W. VFO -550204U
1 Servo -550205U
Interface (Dual Port)
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Servo
C16B-5502-0050#U
R/W. VFO
C16B-5502-0040#U
Logic
C16B-5327-0290#U
Power Amp.
B17B-0250 -0010A#U
DE
B030-4825-T001A
Line Blower
C90L-1370-0900
AC Input
L1
L2/N
FG
DC Power Supply
B14L-5105-0182A
Fan Sensor
C90L-1350-0001
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FUJITSU LIMITED
FDXA-2901-3

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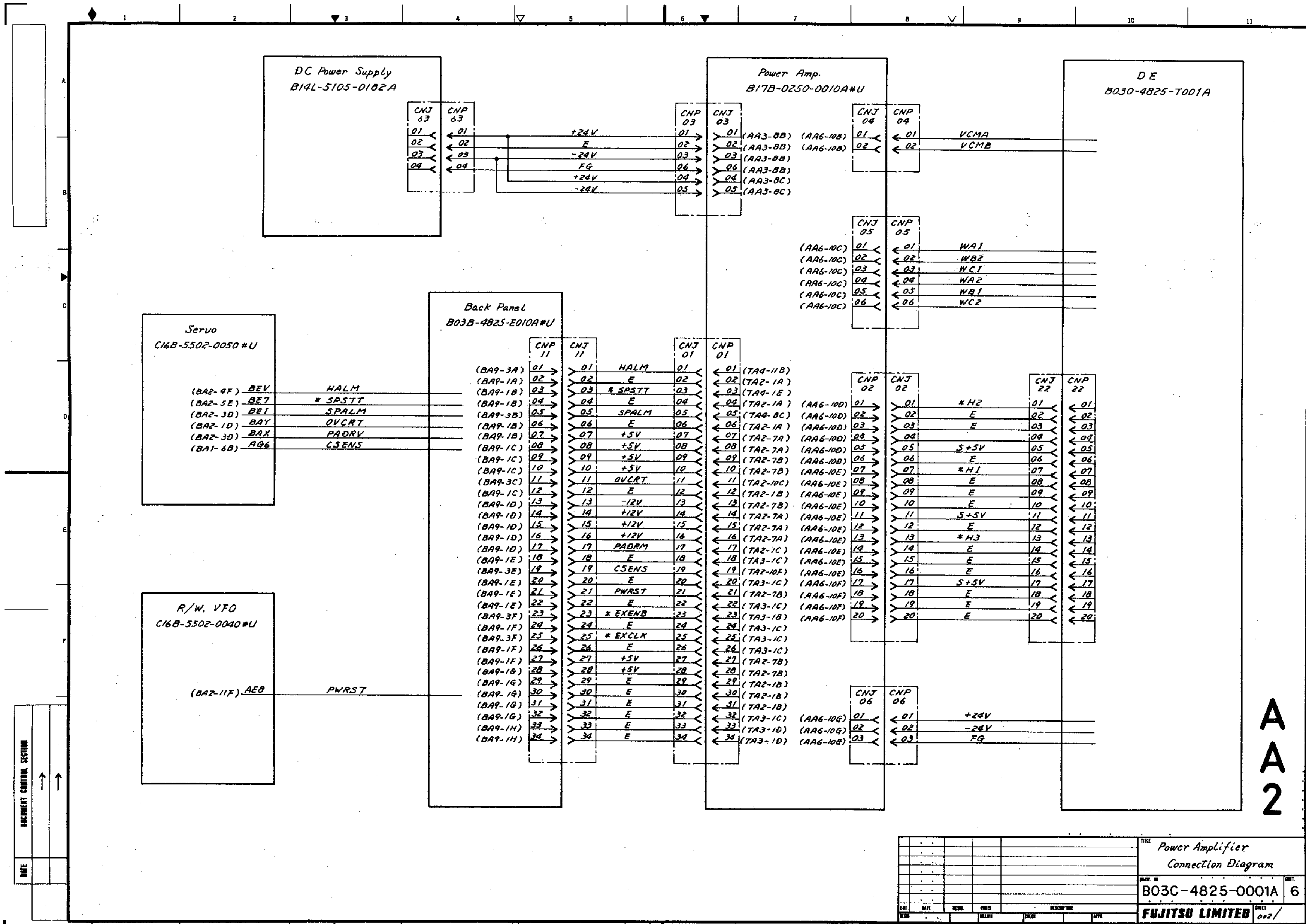


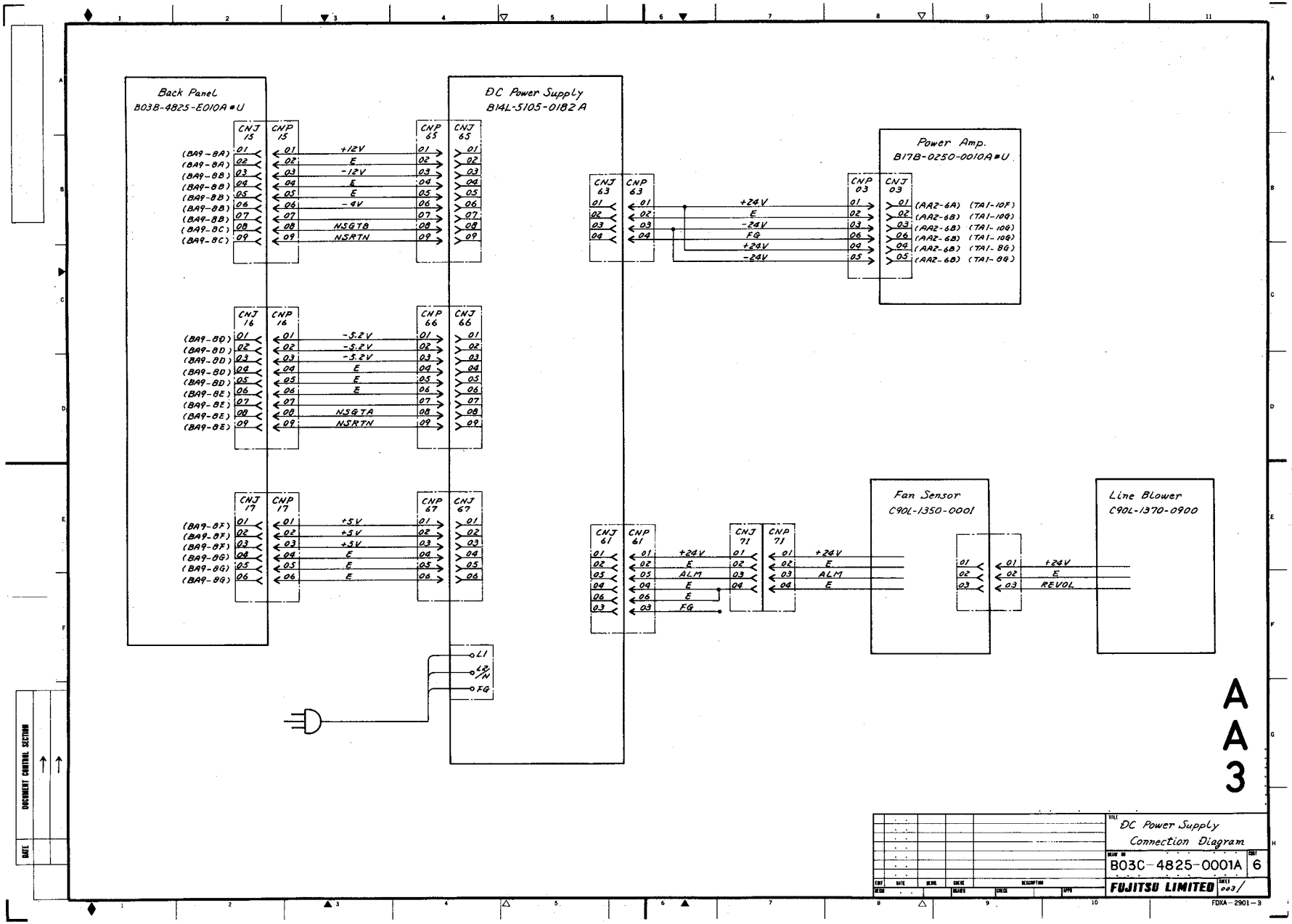
AA2

Power Amplifier Connection Diagram

B03C-4825-0001A 6

FUJITSU LIMITED 002/

FDXA-2901-3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DC Power Supply
B14L-5105-0182A
Power Amp.
B17B-0250-0010A*U
Fan Sensor
C90L-1350-0001
Line Blower
C90L-1370-0900
CNJ 15
CNP 15
CNP 65
CNJ 65
(BA9-8A) 01
(BA9-8A) 02
(BA9-8B) 03
(BA9-8B) 04
(BA9-8B) 05
(BA9-8B) 06
(BA9-8B) 07
(BA9-8B) 08
(BA9-8C) 09
+12V
E
-12V
E
E
-4V
NSGTB
NSRTN
CNJ 16
CNP 16
CNP 66
CNJ 66
(BA9-8D) 01
(BA9-8D) 02
(BA9-8D) 03
(BA9-8D) 04
(BA9-8D) 05
(BA9-8E) 06
(BA9-8E) 07
(BA9-8E) 08
(BA9-8E) 09
-5.2V
-5.2V
-5.2V
E
E
E
NSGTA
NSRTN
CNJ 17
CNP 17
CNP 67
CNJ 67
(BA9-8F) 01
(BA9-8F) 02
(BA9-8F) 03
(BA9-8G) 04
(BA9-8G) 05
(BA9-8G) 06
+5V
+5V
+5V
E
E
E
CNJ 63
CNP 63
CNP 03
CNJ 03
+24V
E
-24V
FG
+24V
-24V
(AA2-6A) (TA1-10F)
(AA2-6B) (TA1-10G)
(AA2-6B) (TA1-10G)
(AA2-6B) (TA1-10G)
(AA2-6B) (TA1-8G)
(AA2-6B) (TA1-8G)
CNJ 61
CNP 61
CNJ 71
CNP 71
+24V
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ALM
E
E
FG
+24V
E
ALM
E
+24V
E
REVOL
L1
L2/N
FG
A3
DOCUMENT CONTROL SECTION
DATE
TITLE
DC Power Supply
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DRAW NO
B03C-4825-0001A
REV
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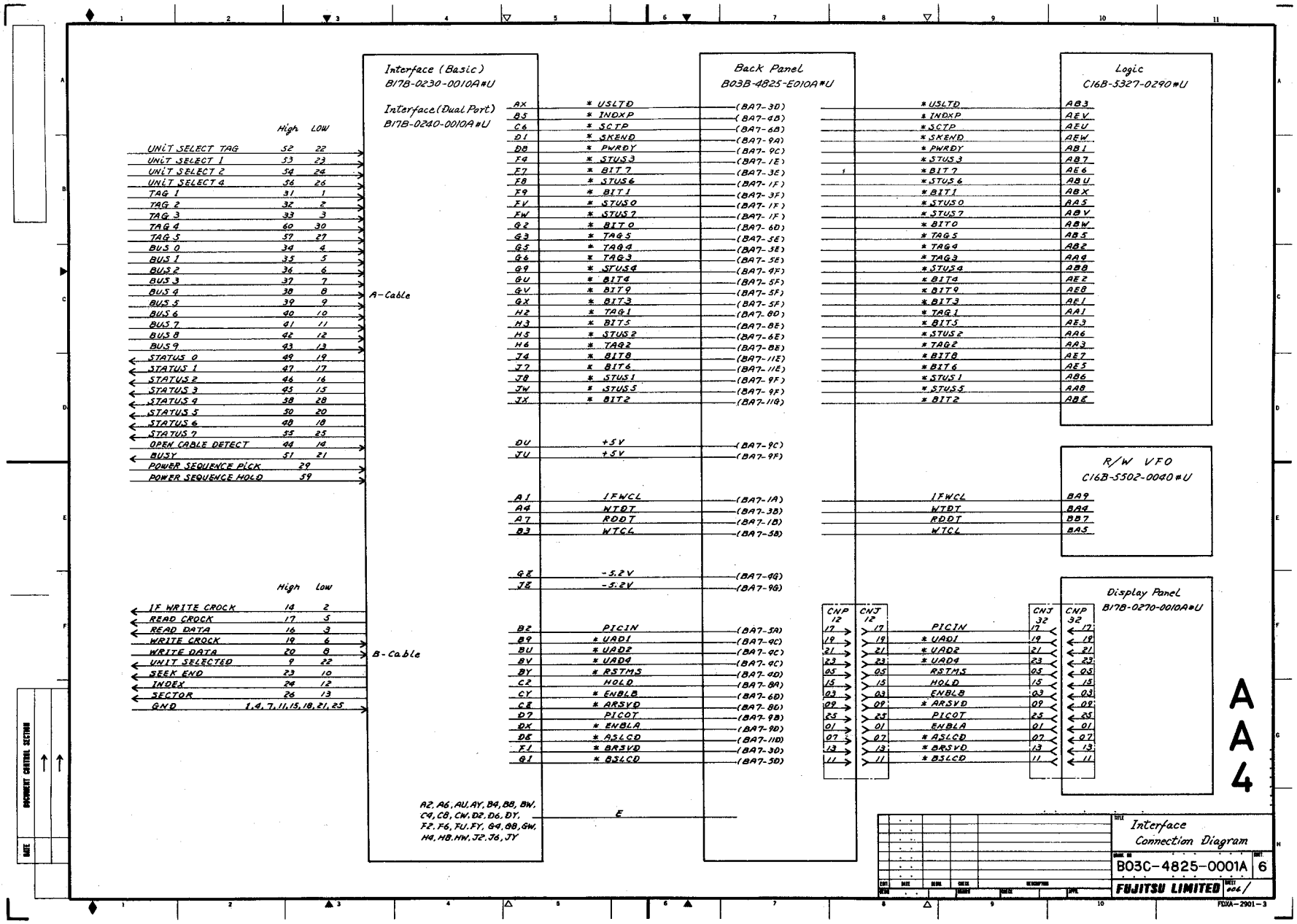
FUJITSU LIMITED
SHEET
003/
FDXA-2901-3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Interface(Dual Port)
B17B-0240-0010A*U
Back Panel
B03B-4825-E010A*U
Logic
C16B-5327-0290*U
R/W VFO
C16B-5502-0040*U
Display Panel
B17B-0270-0010A*U
A-Cable
B-Cable
UNIT SELECT TAG
UNIT SELECT 1
UNIT SELECT 2
UNIT SELECT 4
TAG 1
TAG 2
TAG 3
TAG 4
TAG 5
BUS 0
BUS 1
BUS 2
BUS 3
BUS 4
BUS 5
BUS 6
BUS 7
BUS 8
BUS 9
STATUS 0
STATUS 1
STATUS 2
STATUS 3
STATUS 4
STATUS 5
STATUS 6
STATUS 7
OPEN CABLE DETECT
BUSY
POWER SEQUENCE PICK
POWER SEQUENCE HOLD
IF WRITE CROCK
READ CROCK
READ DATA
WRITE CROCK
WRITE DATA
UNIT SELECTED
SEEK END
INDEX
SECTOR
GND
* USLTD
* INDXP
* SCTP
* SKEND
* PWRDY
* STUS3
* BIT 7
* STUS6
* BIT1
* STUS0
* STUS7
* BIT0
* TAG5
* TAG4
* TAG3
* STUS4
* BIT4
* BIT9
* BIT3
* TAG1
* BIT5
* STUS2
* TAG2
* BIT8
* BIT6
* STUS1
* STUS5
* BIT2
+5V
-5.2V
IFWCL
WTDT
RDDT
WTCL
PICIN
* UAD1
* UAD2
* UAD4
* RSTMS
HOLD
* ENBLB
* ARSVD
PICOT
* ENBLA
* ASLCD
* BRSVD
* BSLCD
E
A2, A6, AU, AY, B4, B8, BW, C4, C8, CW, D2, D6, DY, F2, F6, FU, FY, G4, G8, GW, H4, H8, HW, J2, J6, JY
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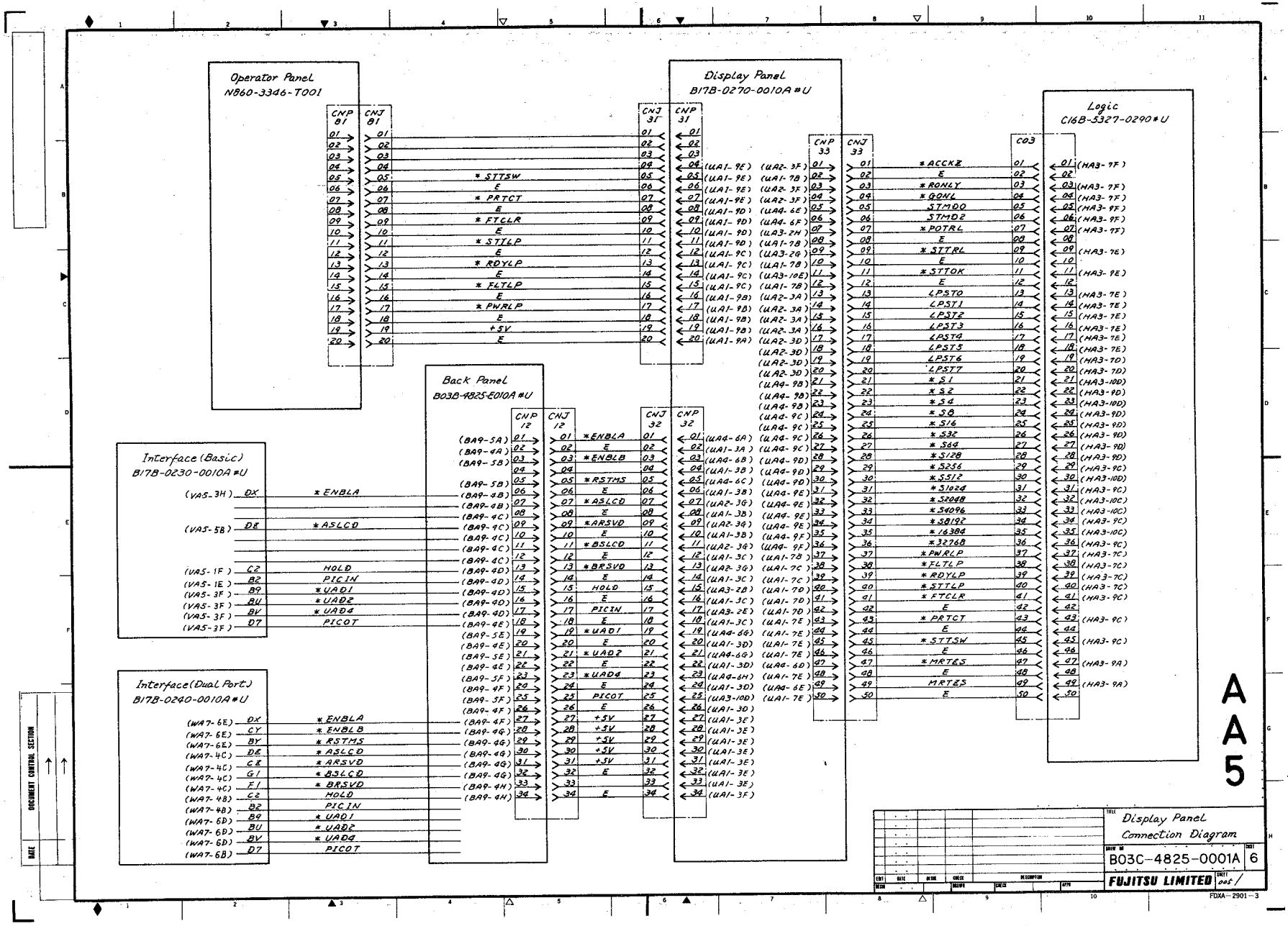
FUJITSU LIMITED
A4
FDXA-2901-3


Operator Panel
N860-3346-T001
CNP 81
CNJ 81
* STTSW
E
* PRTCT
E
* FTCLR
E
* STTLP
E
* RDYLP
E
* FLTLP
E
* PWRLP
E
+5V
E
Display Panel
B17B-0270-0010A#U
CNJ 31
CNP 31
CNP 33
CNJ 33
Logic
C16B-5327-0290#U
C03
* ACCKE
E
* RONLY
* GONL
STMD0
STMD2
* POTRL
E
* STTRL
E
* STTOK
E
LPST0
LPST1
LPST2
LPST3
LPST4
LPST5
LPST6
LPST7
* S1
* S2
* S4
* S8
* S16
* S32
* S64
* S128
* S256
* S512
* S1024
* S2048
* S4096
* S8192
* S16384
* S32768
* PWRLP
* FLTLP
* RDYLP
* STTLP
* FTCLR
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* PRTCT
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* STTSW
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* MRTES
E
MRTES
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Back Panel
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CNP 12
CNJ 12
CNJ 32
CNP 32
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E
* ENBLB
* RSTMS
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* ASLCD
E
* ARSVD
E
* BSLCD
E
* BRSVD
E
HOLD
E
PICIN
E
* UAD1
E
* UAD2
E
* UAD4
E
PICOT
E
+5V
+5V
+5V
+5V
E
Interface (Basic)
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* ASLCD
HOLD
PICIN
* UAD1
* UAD2
* UAD4
PICOT
Interface (Dual Port)
B17B-0240-0010A#U
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* ENBLB
* RSTMS
* ASLCD
* ARSVD
* BSLCD
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* UAD4
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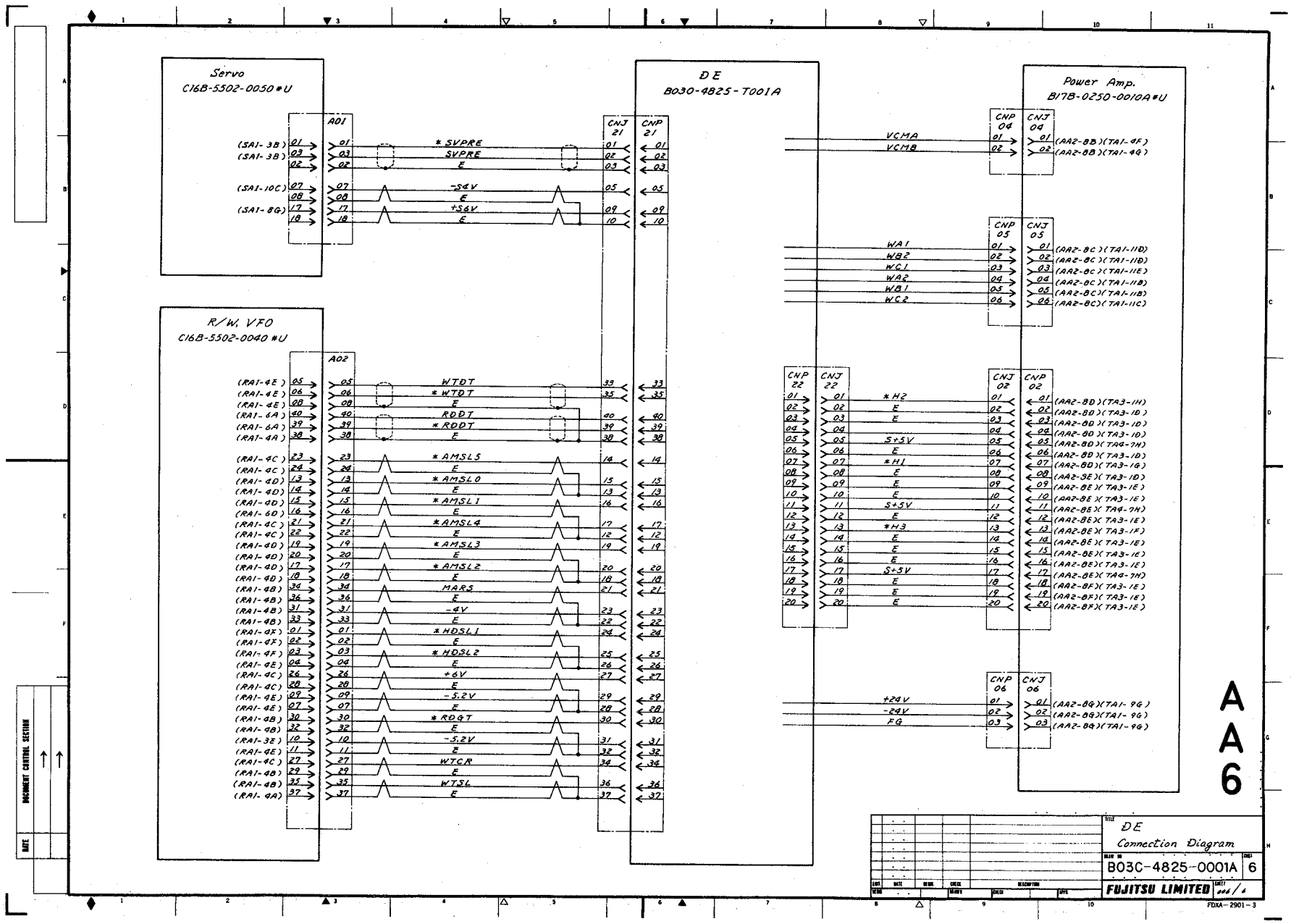
FDXA-2901-3


Servo
C16B-5502-0050*U
A01
(SA1-3B) 01 → 01 * SVPRE → CNJ 21 01 / CNP 21 01
(SA1-3B) 03 → 03 SVPRE → 02 / 02
02 → 02 E → 03 / 03
(SA1-10C) 07 → 07 -S4V → 05 / 05
08 → 08 E
(SA1-8G) 17 → 17 +S6V → 09 / 09
18 → 18 E → 10 / 10
R/W, VFO
C16B-5502-0040*U
A02
(RA1-4E) 05 → 05 WTDT → 33 / 33
(RA1-4E) 06 → 06 * WTDT → 35 / 35
(RA1-4E) 08 → 08 E
(RA1-6A) 40 → 40 RDDT → 40 / 40
(RA1-6A) 39 → 39 * RDDT → 39 / 39
(RA1-4A) 38 → 38 E → 38 / 38
(RA1-4C) 23 → 23 * AMSL5 → 14 / 14
(RA1-4C) 24 → 24 E
(RA1-4D) 13 → 13 * AMSL0 → 15 / 15
(RA1-4D) 14 → 14 E → 13 / 13
(RA1-4D) 15 → 15 * AMSL1 → 16 / 16
(RA1-6D) 16 → 16 E
(RA1-4C) 21 → 21 * AMSL4 → 17 / 17
(RA1-4C) 22 → 22 E → 12 / 12
(RA1-4D) 19 → 19 * AMSL3 → 19 / 19
(RA1-4D) 20 → 20 E
(RA1-4D) 17 → 17 * AMSL2 → 20 / 20
(RA1-4D) 18 → 18 E → 18 / 18
(RA1-4B) 34 → 34 MARS → 21 / 21
(RA1-4B) 36 → 36 E
(RA1-4B) 31 → 31 -4V → 23 / 23
(RA1-4B) 33 → 33 E → 22 / 22
(RA1-4F) 01 → 01 * HDSL1 → 24 / 24
(RA1-4F) 02 → 02 E
(RA1-4F) 03 → 03 * HDSL2 → 25 / 25
(RA1-4E) 04 → 04 E → 26 / 26
(RA1-4C) 26 → 26 +6V → 27 / 27
(RA1-4C) 28 → 28 E
(RA1-4E) 09 → 09 -5.2V → 29 / 29
(RA1-4E) 07 → 07 E → 28 / 28
(RA1-4B) 30 → 30 * RDGT → 30 / 30
(RA1-4B) 32 → 32 E
(RA1-3E) 10 → 10 -5.2V → 31 / 31
(RA1-4E) 11 → 11 E → 32 / 32
(RA1-4C) 27 → 27 WTCR → 34 / 34
(RA1-4B) 29 → 29 E
(RA1-4B) 35 → 35 WTSL → 36 / 36
(RA1-4A) 37 → 37 E → 37 / 37
DE
B030-4825-T001A
Power Amp.
B17B-0250-0010A*U
CNP 04 / CNJ 04
VCMA 01 → 01 (AA2-8B)(TA1-4F)
VCMB 02 → 02 (AA2-8B)(TA1-4G)
CNP 05 / CNJ 05
WA1 01 → 01 (AA2-8C)(TA1-11B)
WB2 02 → 02 (AA2-8C)(TA1-11D)
WC1 03 → 03 (AA2-8C)(TA1-11E)
WA2 04 → 04 (AA2-8C)(TA1-11B)
WB1 05 → 05 (AA2-8C)(TA1-11B)
WC2 06 → 06 (AA2-8C)(TA1-11C)
CNP 22 / CNJ 22 / CNJ 02 / CNP 02
01 → 01 * H2 → 01 / 01 (AA2-8D)(TA3-1H)
02 → 02 E → 02 / 02 (AA2-8D)(TA3-1D)
03 → 03 E → 03 / 03 (AA2-8D)(TA3-1D)
04 → 04 → 04 / 04 (AA2-8D)(TA3-1D)
05 → 05 S+5V → 05 / 05 (AA2-8D)(TA4-7H)
06 → 06 E → 06 / 06 (AA2-8D)(TA3-1D)
07 → 07 * H1 → 07 / 07 (AA2-8D)(TA3-1G)
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10 → 10 E → 10 / 10 (AA2-8E)(TA3-1E)
11 → 11 S+5V → 11 / 11 (AA2-8E)(TA4-7H)
12 → 12 E → 12 / 12 (AA2-8E)(TA3-1E)
13 → 13 * H3 → 13 / 13 (AA2-8E)(TA3-1F)
14 → 14 E → 14 / 14 (AA2-8E)(TA3-1E)
15 → 15 E → 15 / 15 (AA2-8E)(TA3-1E)
16 → 16 E → 16 / 16 (AA2-8E)(TA3-1E)
17 → 17 S+5V → 17 / 17 (AA2-8E)(TA4-7H)
18 → 18 E → 18 / 18 (AA2-8F)(TA3-1E)
19 → 19 E → 19 / 19 (AA2-8F)(TA3-1E)
20 → 20 E → 20 / 20 (AA2-8F)(TA3-1E)
CNP 06 / CNJ 06
+24V 01 → 01 (AA2-8G)(TA1-9G)
-24V 02 → 02 (AA2-8G)(TA1-9G)
FG 03 → 03 (AA2-8G)(TA1-9G)
AA6
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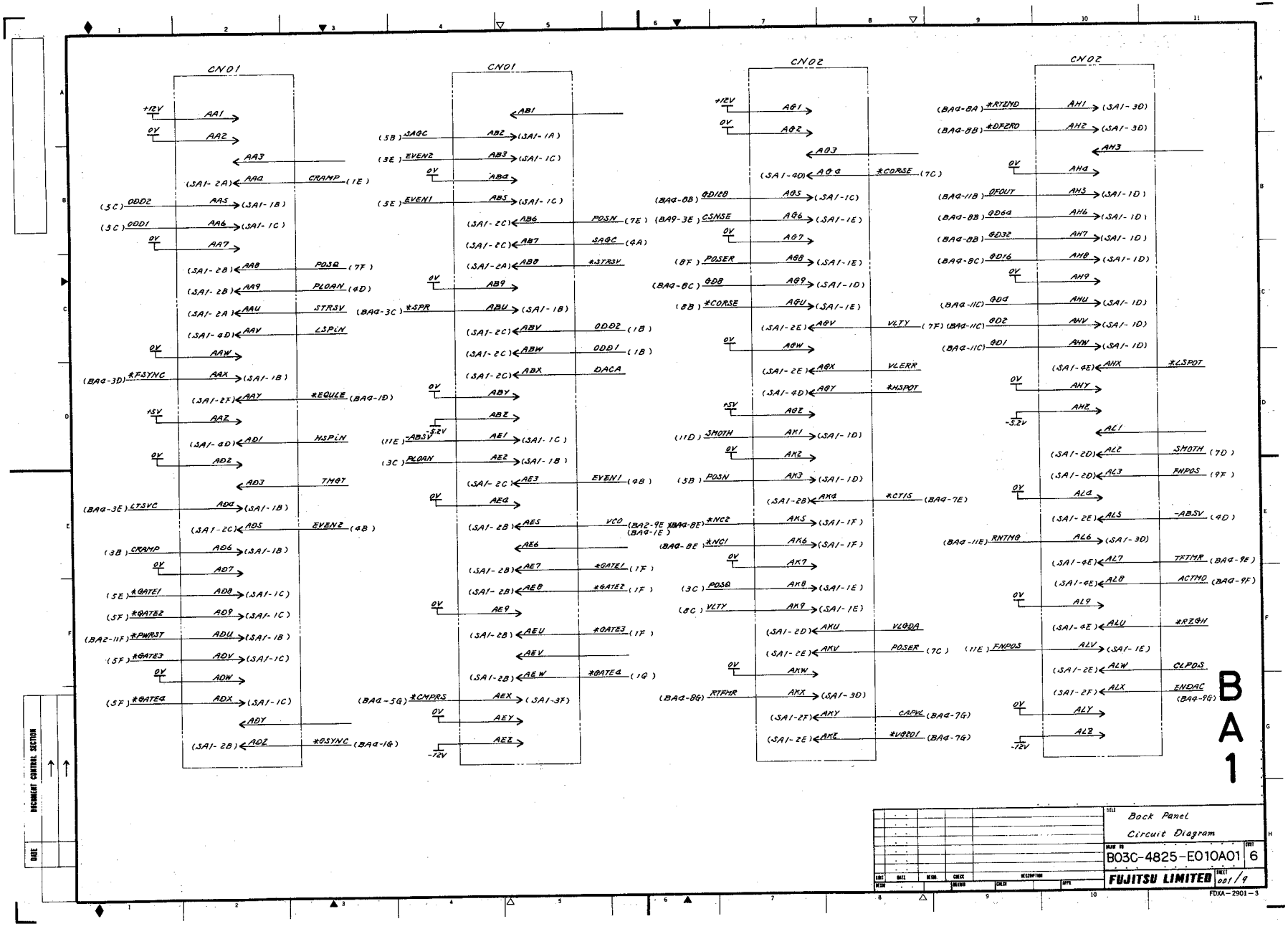
FUJITSU LIMITED
FDXA-2901-3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Back Panel
Circuit Diagram
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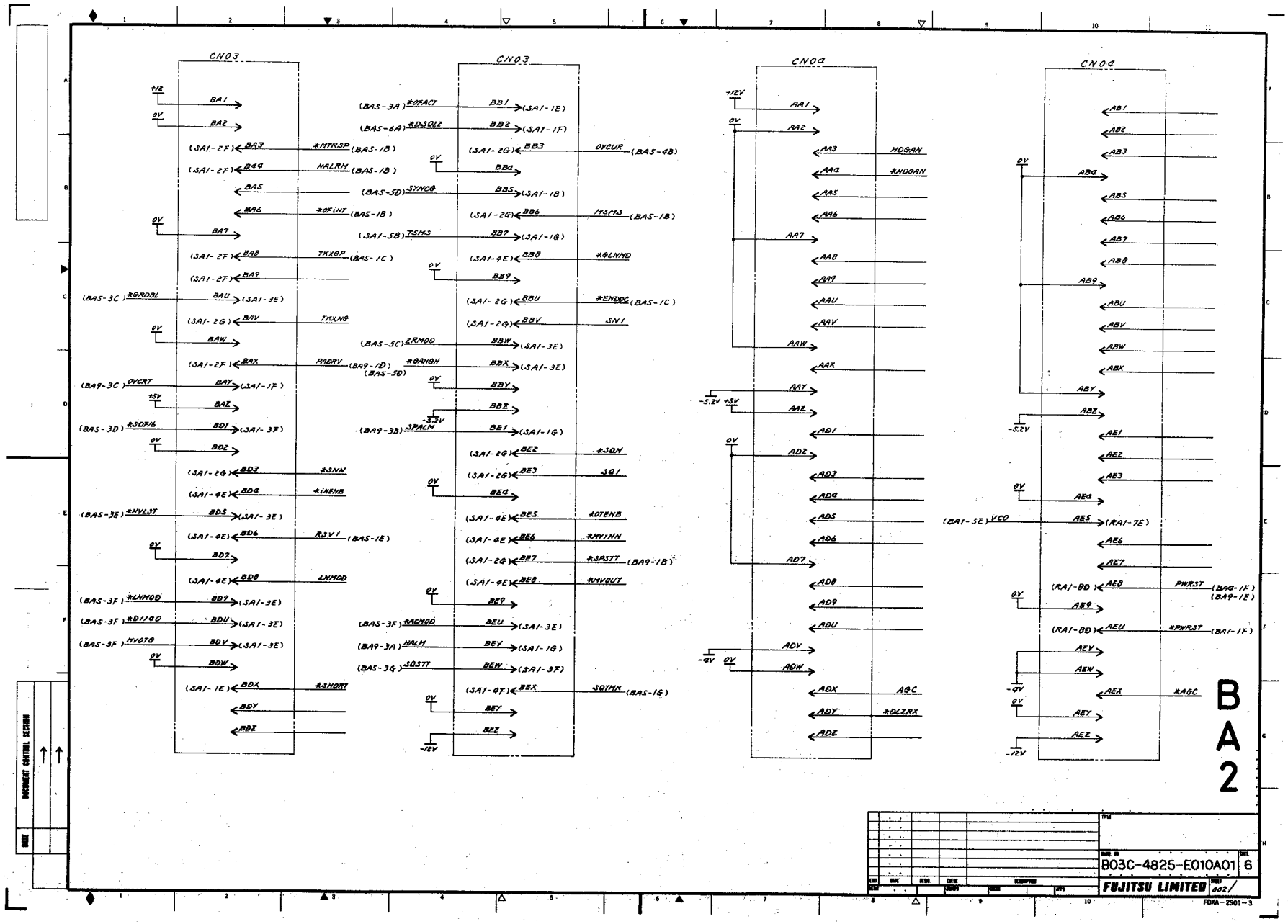
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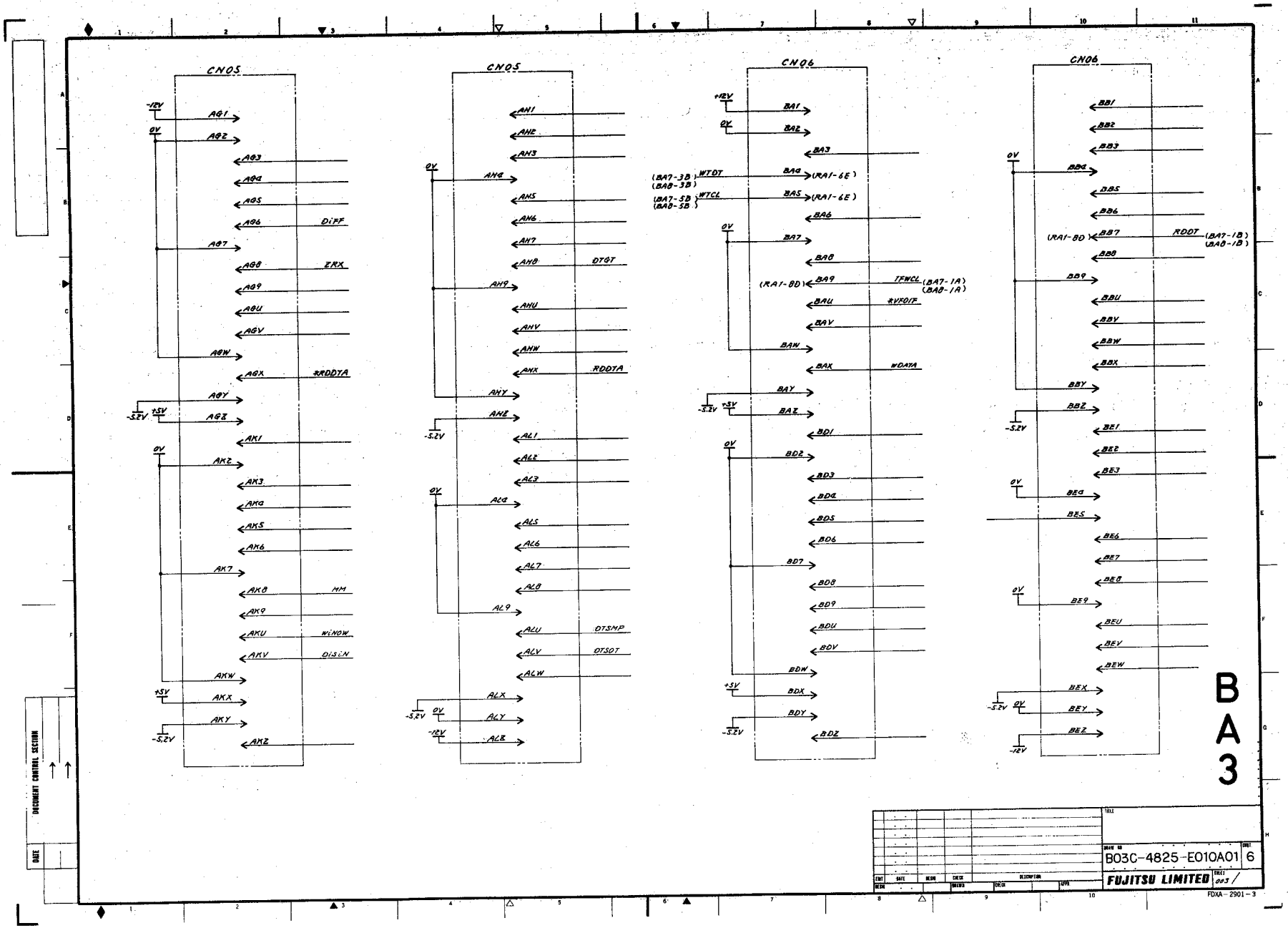
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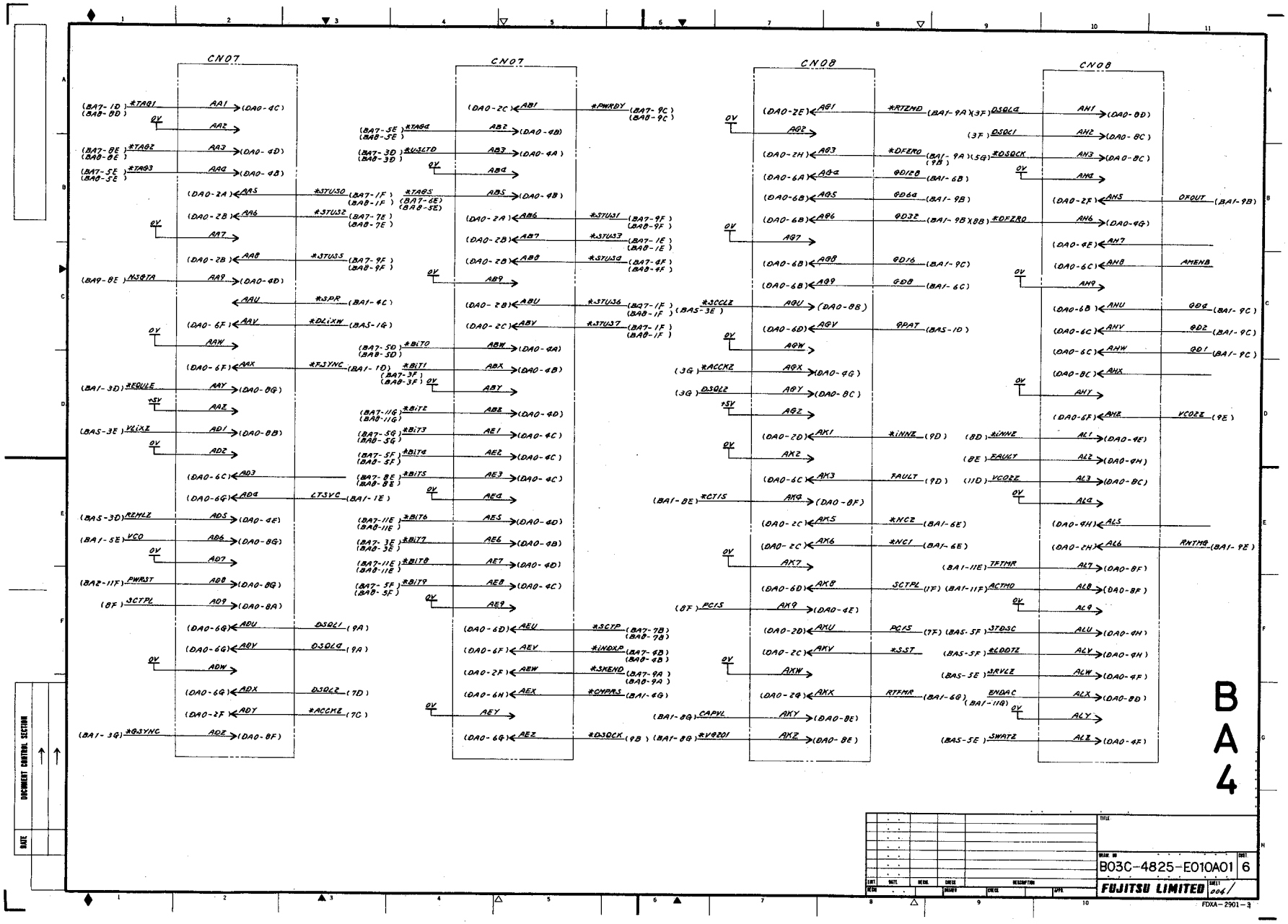
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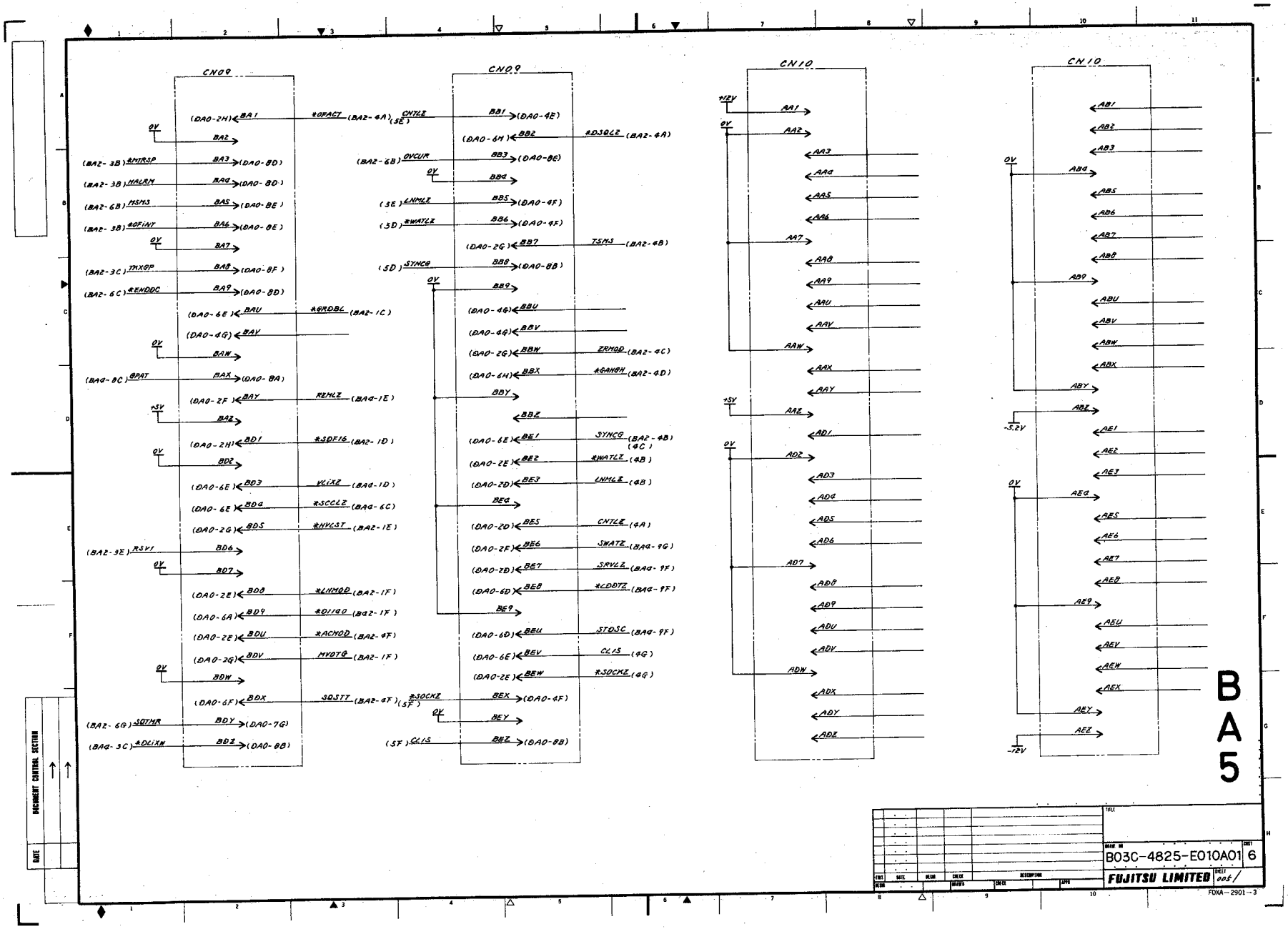
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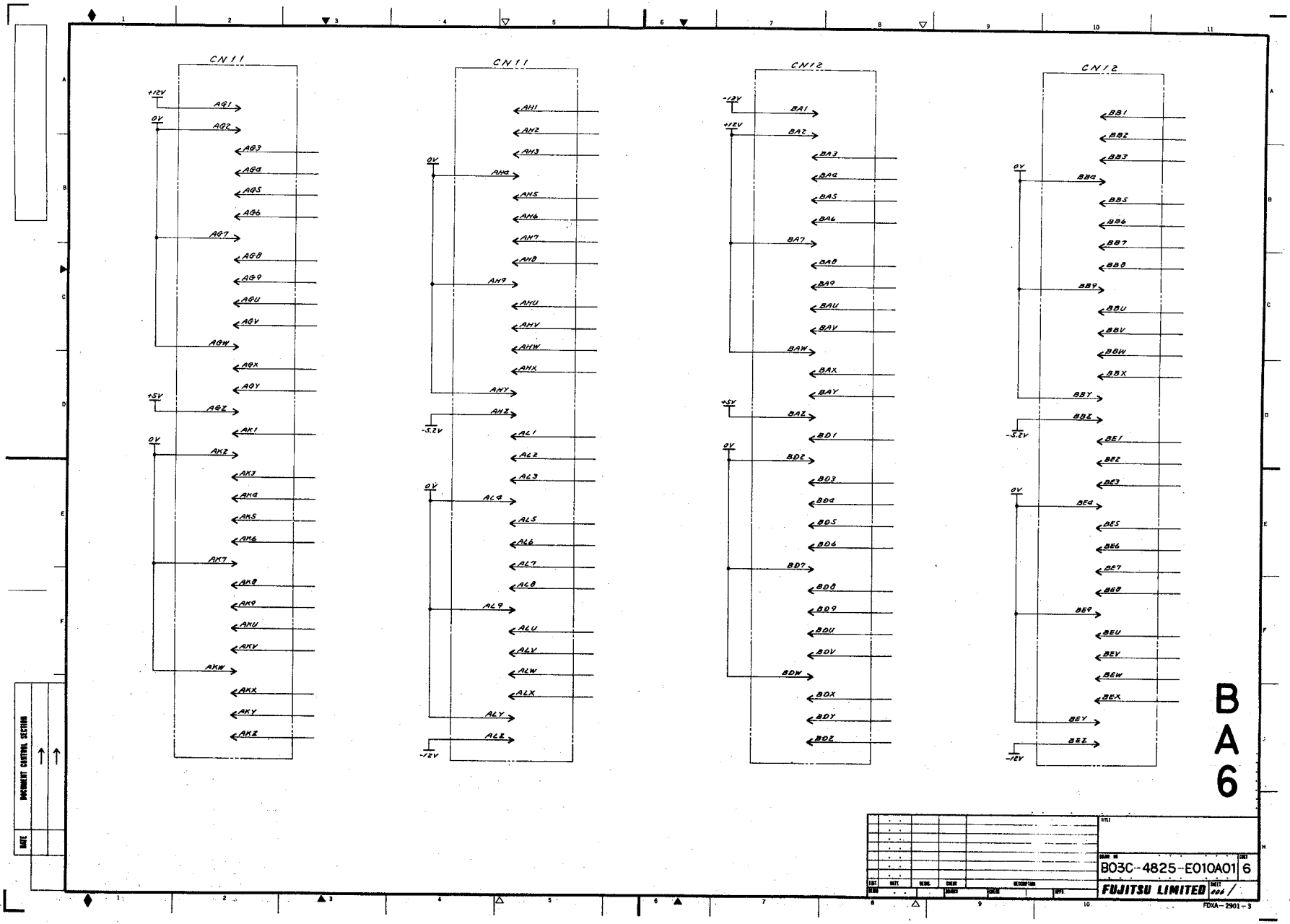
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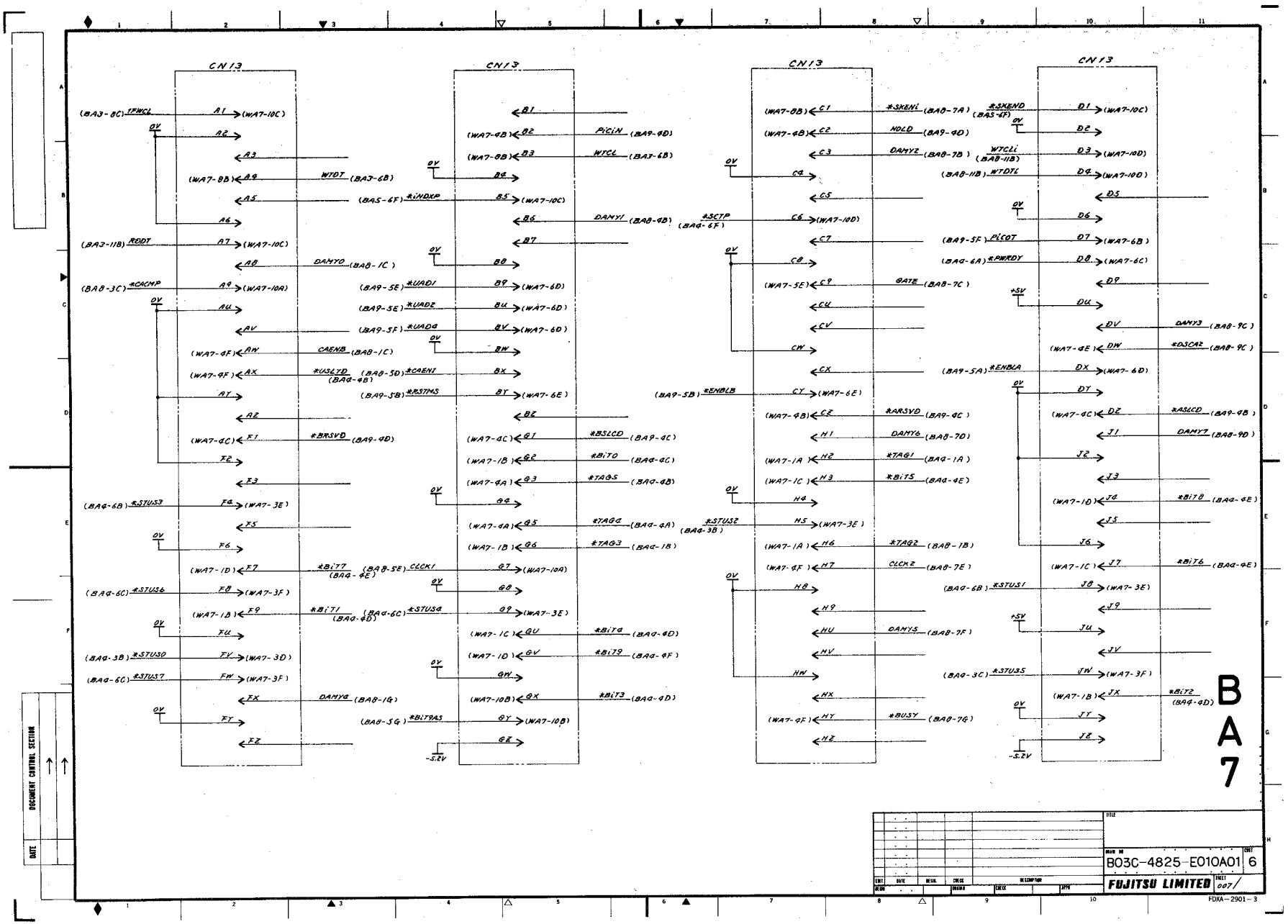
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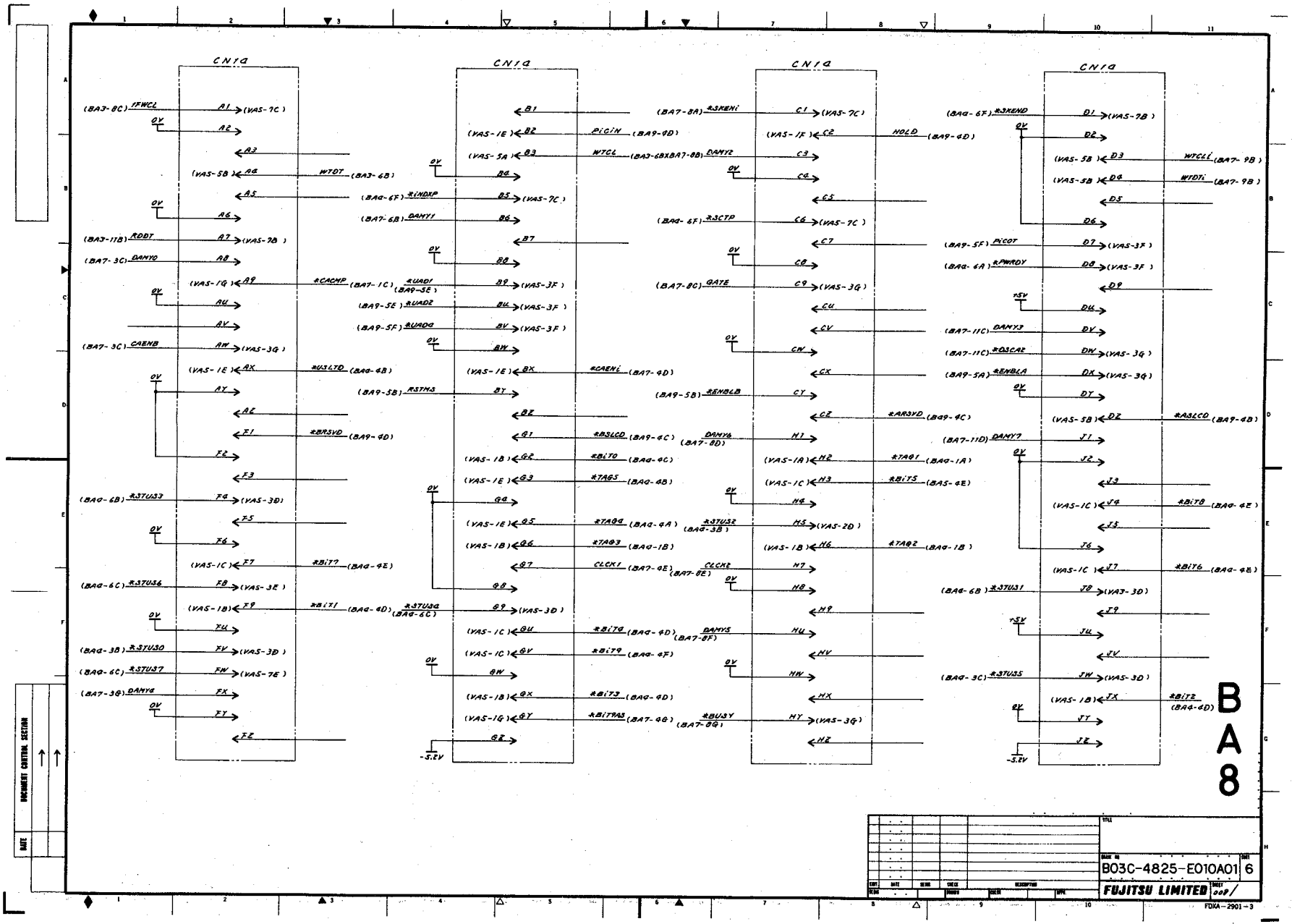
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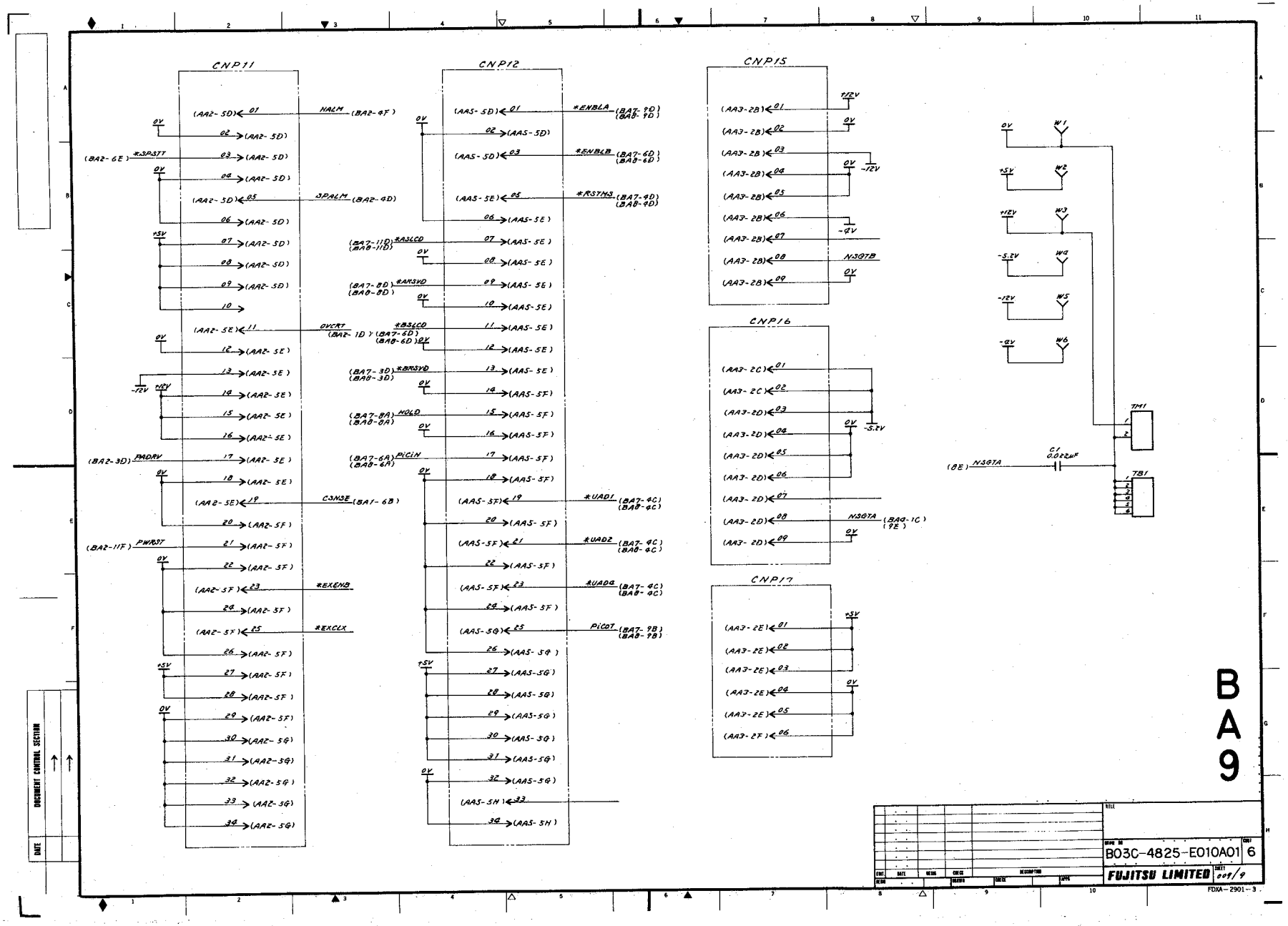
FUJITSU LIMITED
FDXA-2901-3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CNP16
CNP17
HALM
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SPALM
OVCRT
PADRV
PWRST
*EXENB
*EXCLK
C3NSE
*ENBLA
*ENBLB
*RSTNS
*RASLCD
*BSLCD
*BMSYD
*AMSYD
HOLD
PICIN
*UAD1
*UAD2
*UAD4
PICOT
NSGTB
NSGTA
C1 0.022μF
TM1
TB1
B
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B03C-4825-E010A01
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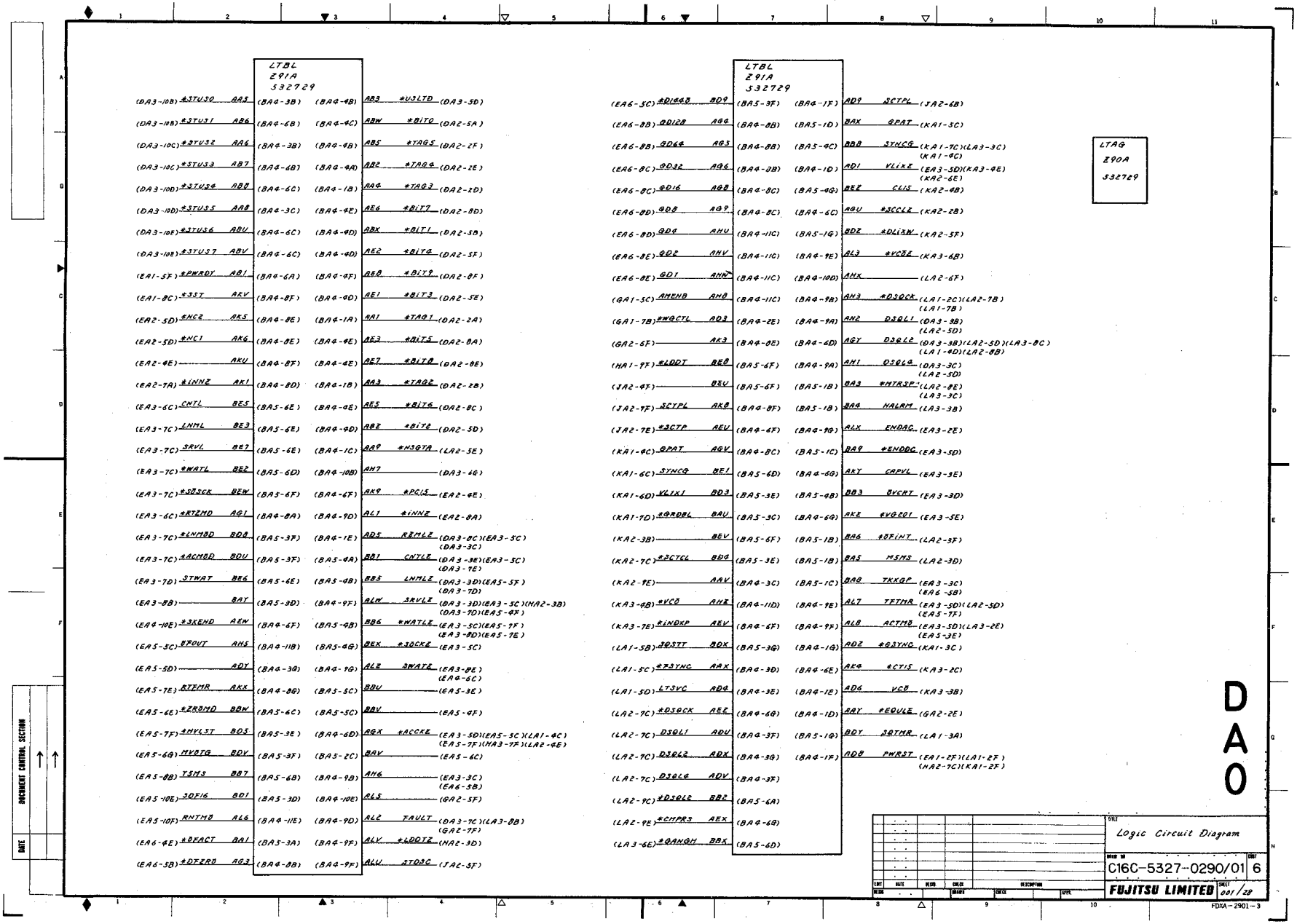
FUJITSU LIMITED
FDXA-2901-3
DOCUMENT CONTROL SECTION
DATE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LTBL Z91A 532729
LTAG Z90A 532729
(DA3-10B) *STUS0 AA5 (BA4-3B) (BA4-4B) AB3 *U3LTD (DA3-5D)
(DA3-10B) *STUS1 AB6 (BA4-6B) (BA4-9C) ABW *BITO (DA2-5A)
(DA3-10C) *STUS2 AA6 (BA4-3B) (BA4-4B) AB5 *TAG5 (DA2-2F)
(DA3-10C) *STUS3 AB7 (BA4-6B) (BA4-9A) AB6 *TAG4 (DA2-2E)
(DA3-10D) *STUS4 AB8 (BA4-6C) (BA4-1B) AA6 *TAG3 (DA2-2D)
(DA3-10D) *STUS5 AA8 (BA4-3C) (BA4-4E) AE6 *BIT7 (DA2-8D)
(DA3-10E) *STUS6 ABU (BA4-6C) (BA4-9D) ABX *BIT1 (DA2-5B)
(DA3-10E) *STUS7 ABV (BA4-6C) (BA4-9D) AE2 *BIT6 (DA2-5F)
(EA1-5F) *PWRDY AB1 (BA4-6A) (BA4-6F) AE8 *BIT9 (DA2-8F)
(EA1-8C) *SST AKV (BA4-8F) (BA4-9D) AE1 *BIT2 (DA2-5E)
(EA2-5D) *NC2 AK5 (BA4-8E) (BA4-1A) AA1 *TAG1 (DA2-2A)
(EA2-5D) *NC1 AK6 (BA4-8E) (BA4-4E) AE3 *BIT5 (DA2-8A)
(EA2-6E) AKU (BA4-8F) (BA4-4E) AE7 *BIT8 (DA2-8E)
(EA2-7A) *INNZ AK1 (BA4-8D) (BA4-1B) AA3 *TAG2 (DA2-2B)
(EA3-6C) CNTL BE5 (BA5-6E) (BA4-4E) AE5 *BIT4 (DA2-8C)
(EA3-7C) LNML BE3 (BA5-6E) (BA4-9D) AB2 *BIT0 (DA2-5D)
(EA3-7C) SRVL BE7 (BA5-6E) (BA4-1C) AA9 *MSGTA (LA2-5E)
(EA3-7C) *WATL BE2 (BA5-6D) (BA4-10B) AH7 (DA3-4G)
(EA3-7C) *32SCK BEW (BA5-6F) (BA4-6F) AK9 *PCIS (EA2-6E)
(EA3-6C) *RTEMD AG1 (BA4-8A) (BA4-9D) AL1 *INNE (EA2-8A)
(EA3-7C) *LNMBD BD8 (BA5-3F) (BA4-1E) AD5 RZMLE (DA3-8C)(EA3-5C) (DA3-3C)
(EA3-7C) *ACMBD BDU (BA5-3F) (BA5-4A) BB1 CNTLE (DA3-3E)(EA3-5C) (DA3-7E)
(EA3-7D) STWAT BE6 (BA5-6E) (BA5-4B) BB5 LNMLE (DA3-3D)(EA5-5F) (DA3-7D)
(EA3-8B) BAT (BA5-3D) (BA4-9F) ALW SRVLE (DA3-3D)(EA3-5C)(HA2-3B) (DA3-7D)(EA5-4F)
(EA4-10E) *3XEND AEW (BA4-6F) (BA5-4B) BB6 *WATLE (EA3-5C)(EA5-7F) (EA3-8D)(EA5-7E)
(EA5-5C) BFOUT AH5 (BA4-11B) (BA5-4G) BEK *3BCKE (EA3-5C)
(EA5-5D) ADT (BA4-3G) (BA4-9G) AL2 3WATE (EA3-8E) (EA4-6C)
(EA5-7E) RTEMR AKK (BA5-8G) (BA5-5C) BBU (EA5-3E)
(EA5-6E) *ZRDMD BBW (BA5-6C) (BA5-5C) BBV (EA5-4F)
(EA5-7F) *MVLST BD5 (BA5-3E) (BA4-6D) AGX *ACCKE (EA3-5D)(EA5-5C)(LA1-4C) (EA5-7F)(HA3-7F)(LA2-4E)
(EA5-6G) MVRTG BDV (BA5-3F) (BA5-2C) BAV (EA5-6C)
(EA5-8B) TSMS BB7 (BA5-6B) (BA4-9B) AH6 (EA3-3C) (EA6-5B)
(EA5-10E) 3DF16 BD1 (BA5-3D) (BA4-10E) AL5 (GA2-5F)
(EA5-10F) RNTM8 AL6 (BA4-11E) (BA4-9D) AL2 FAULT (DA3-7C)(LA3-8B) (GA2-7F)
(EA6-4E) *DFACT BA1 (BA5-3A) (BA4-9F) ALV *LDDTZ (HA2-3D)
(EA6-5B) *DTZRO AG3 (BA4-8B) (BA4-9F) ALW STO2C (JA2-5F)
(EA6-5C) *DIAGB BD9 (BA5-3F) (BA4-1F) AD9 SCTPL (JA2-6B)
(EA6-8B) QD128 AG4 (BA4-8B) (BA5-1D) BAX GPAT (KA1-5C)
(EA6-8B) QD64 AG5 (BA4-8B) (BA5-9C) BBB SYNCG (KA1-7C)(LA3-3C) (KA1-9C)
(EA6-8C) QD32 AG6 (BA4-8B) (BA4-1D) AD1 VLIXZ (EA3-5D)(KA3-9E) (KA2-6E)
(EA6-8C) QD16 AGB (BA4-8C) (BA5-4G) BEZ CLIS (KA2-4B)
(EA6-8D) QD8 AG9 (BA4-8C) (BA4-6C) AGU *SCCLZ (KA2-2B)
(EA6-8D) QD4 AHU (BA4-11C) (BA5-1G) BDZ *DLIXW (KA2-3F)
(EA6-8E) QD2 AHV (BA4-11C) (BA4-9E) AL3 *VCDZ (KA3-6B)
(EA6-8E) QD1 AHW (BA4-11C) (BA4-10D) AHX (LA2-6F)
(GA1-5C) AMENB AH8 (BA4-11C) (BA4-9B) AH3 *DSGCK (LA1-2C)(LA2-7B) (LA1-7B)
(GA1-7B) **WQCTL AD3 (BA4-2E) (BA4-9A) AH2 DSGL1 (DA3-3B) (LA2-5D)
(GA2-6F) AK3 (BA4-8E) (BA4-6D) AGY DSGL2 (DA3-3B)(LA2-5D)(LA3-8C) (LA1-4D)(LA2-8B)
(HA1-9F) *LDDT BE8 (BA5-6F) (BA4-9A) AH1 DSGL6 (DA3-3C) (LA2-5D)
(JA2-4F) BEV (BA5-6F) (BA5-1B) BA3 *MTRSP (LA2-8E) (LA3-3C)
(JA2-7F) SCTPL AK8 (BA4-8F) (BA5-1B) BA8 HALRM (LA3-3B)
(JA2-7E) *3CTP AEU (BA4-4F) (BA4-9G) ALX ENDAC (EA3-2E)
(KA1-6C) GPAT AGV (BA4-8C) (BA5-1C) BA9 *ENDDC (EA3-5D)
(KA1-6C) SYNCG BE1 (BA5-6D) (BA4-6G) AKT CAPVL (EA3-3E)
(KA1-6D) VLIX1 BD3 (BA5-3E) (BA5-4B) BB3 BVCRT (EA3-3D)
(KA1-7D) *GRDBL BAU (BA5-3C) (BA4-6G) AK2 *VG201 (EA3-5E)
(KA2-3B) BEV (BA5-6F) (BA5-1B) BA6 *DFINT (LA2-3F)
(KA2-7C) *2CTCL BD4 (BA5-3E) (BA5-1B) BA5 MSMS (LA2-3D)
(KA2-7E) AAV (BA4-3C) (BA5-1C) BA0 TKKGF (EA3-3C) (EA6-5B)
(KA3-6B) *VCC AHE (BA4-11D) (BA4-9E) AL7 TFTMR (EA3-5D)(LA2-5D) (EA5-7F)
(KA3-7E) *INDXP AEV (BA4-6F) (BA4-9F) AL8 ACTM8 (EA3-5D)(LA3-2E) (EA5-3E)
(LA1-5B) 30STT BDX (BA5-3G) (BA4-1G) AD2 *6SYNC (KA1-3C)
(LA1-5C) *7SYNC AAX (BA4-3D) (BA4-6E) AK4 *CTIS (KA3-2C)
(LA1-5D) LTSVC AD4 (BA4-3E) (BA4-1E) AD6 VCO (KA3-3B)
(LA2-7C) *DSGCK AEC (BA4-6B) (BA4-1D) AAT *EQULE (GA2-2E)
(LA2-7C) DSGL1 ADU (BA4-3F) (BA5-1G) BDY SDTMR (LA1-3A)
(LA2-7C) DSGL2 ADX (BA4-3G) (BA4-1F) AD8 PWRST (EA1-2F)(LA1-2F) (HA2-7C)(KA1-2F)
(LA2-7C) DSGL6 ADV (BA4-3F)
(LA2-9C) *DSGL2 BB2 (BA5-6A)
(LA2-9E) *CMPRS AEX (BA4-6B)
(LA3-6E) *QANGH BBX (BA5-6D)
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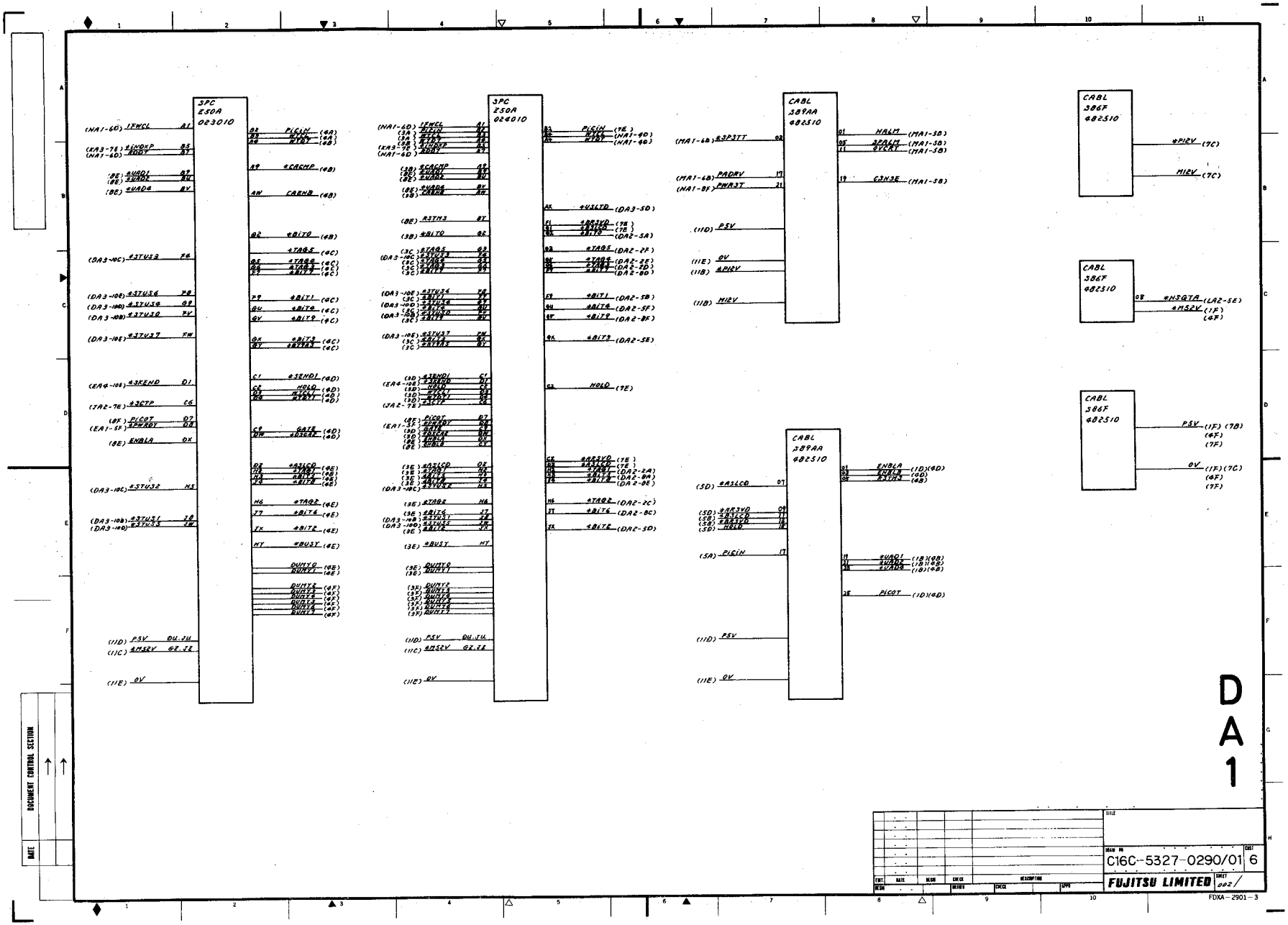
DRAW NO C16C-5327-0290/01 REV 6
FUJITSU LIMITED SHEET 001/28
FDXA-2901-3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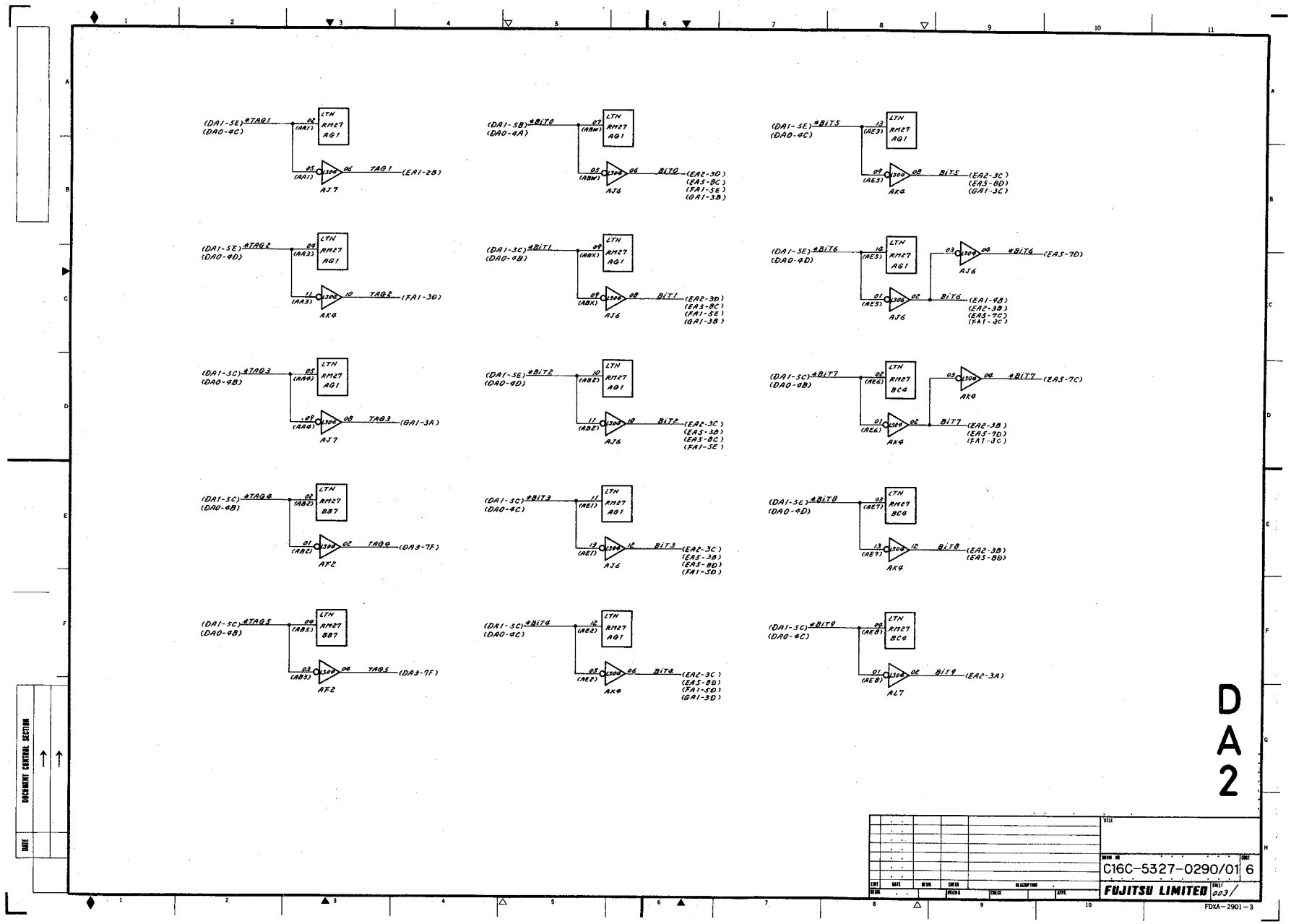
FDXA-2901-3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(DA0-4C)
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LS08
AJ7
TAG1
(EA1-2B)
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(DA0-4A)
(ABW)
AJ6
BIT0
(EA2-3D)
(EA3-8C)
(FA1-5E)
(GA1-3B)
(DA1-5E) *BIT5
(DA0-4C)
(AE3)
AK4
BIT5
(EA2-3C)
(EA3-8D)
(GA1-3C)
(DA1-5E) *TAG2
(DA0-4D)
(AA3)
AK4
TAG2
(FA1-3D)
(DA1-3C) *BIT1
(DA0-4B)
(ABX)
AJ6
BIT1
(EA2-3D)
(EA3-8C)
(FA1-5E)
(GA1-3B)
(DA1-5E) *BIT6
(DA0-4D)
(AE5)
AJ6
BIT6
(EA1-4B)
(EA2-3B)
(EA3-7C)
(FA1-3C)
*BIT6
(EA3-7D)
(DA1-3C) *TAG3
(DA0-4B)
(AA9)
AJ7
TAG3
(GA1-3A)
(DA1-5E) *BIT2
(DA0-4D)
(ABZ)
AJ6
BIT2
(EA2-3C)
(EA3-3B)
(EA3-8C)
(FA1-5E)
(DA1-3C) *BIT7
(DA0-4B)
(AE6)
AK4
BIT7
(EA2-3B)
(EA3-7D)
(FA1-3C)
*BIT7
(EA3-7C)
(DA1-3C) *TAG4
(DA0-4B)
(AB2)
BB7
AF2
TAG4
(DA3-7F)
(DA1-3C) *BIT3
(DA0-4C)
(AE7)
AJ6
BIT3
(EA2-3C)
(EA3-3B)
(EA3-8D)
(FA1-5D)
(DA1-5E) *BIT8
(DA0-4D)
(AE7)
AK4
BIT8
(EA2-3B)
(EA3-8B)
(DA1-3C) *TAG5
(DA0-4B)
(AB3)
AF2
TAG5
(DA3-7F)
(DA1-3C) *BIT4
(DA0-4C)
(AE2)
AK4
BIT4
(EA2-3C)
(EA3-8D)
(FA1-5D)
(GA1-3D)
(DA1-3C) *BIT9
(DA0-4C)
(AE8)
AL7
BIT9
(EA2-3A)
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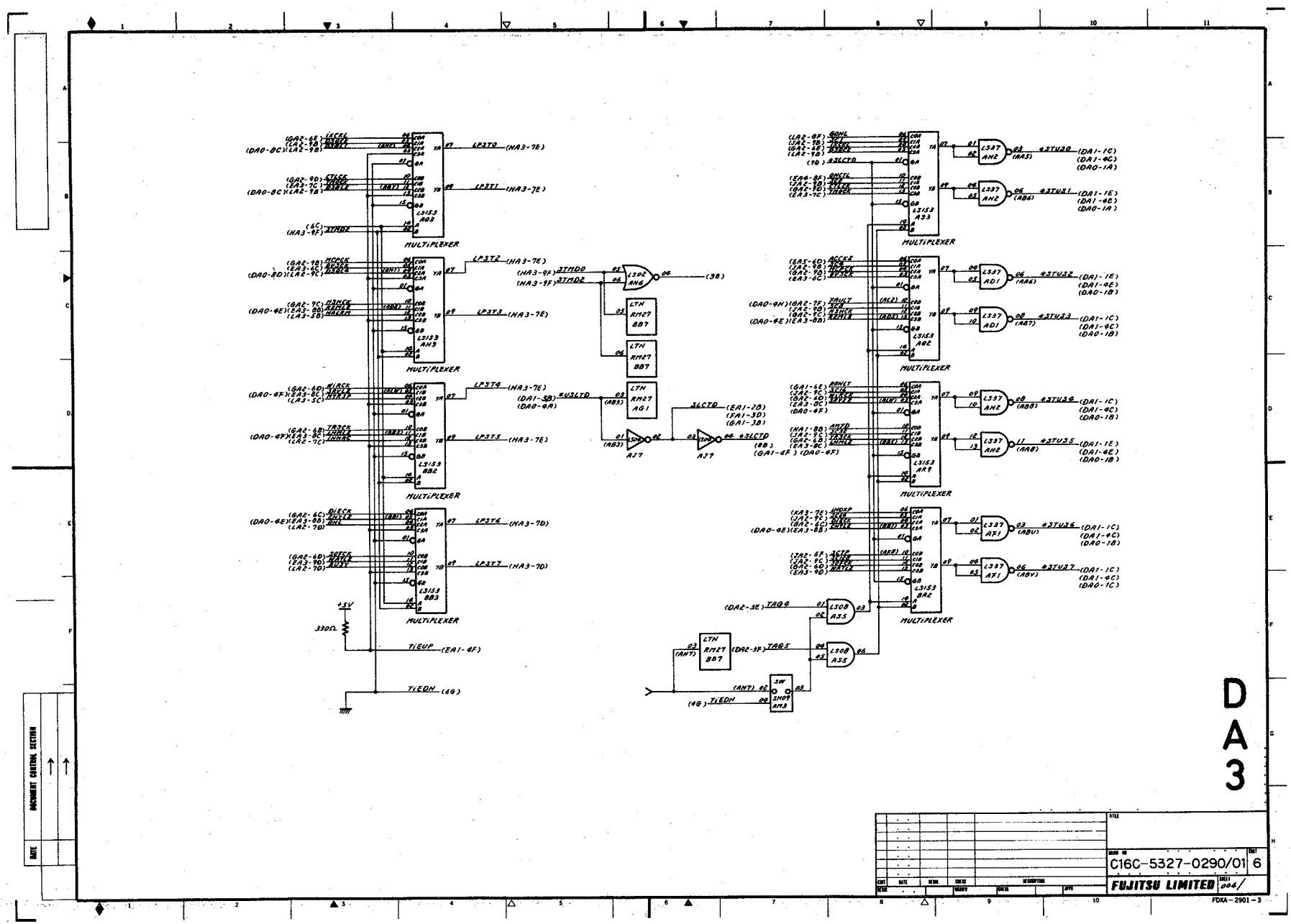
C16C-5327-0290/01 6
FUJITSU LIMITED
FDXA-2901-3


MULTIPLEXER
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MULTIPLEXER
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+5V
330Ω
TiEUP
TiEDN
DOCUMENT CONTROL SECTION
DATE
DA
3
C16C-5327-0290/01
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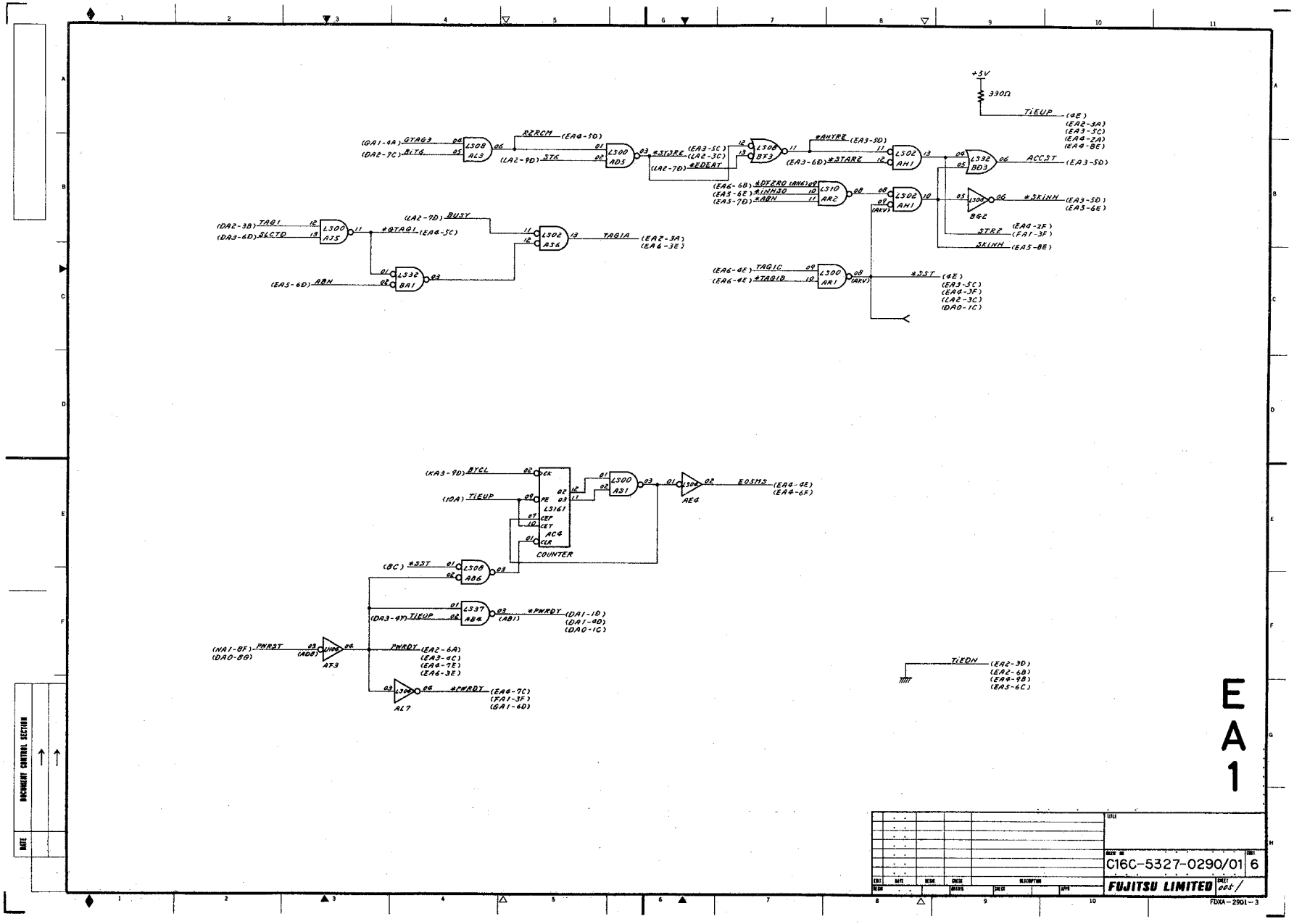
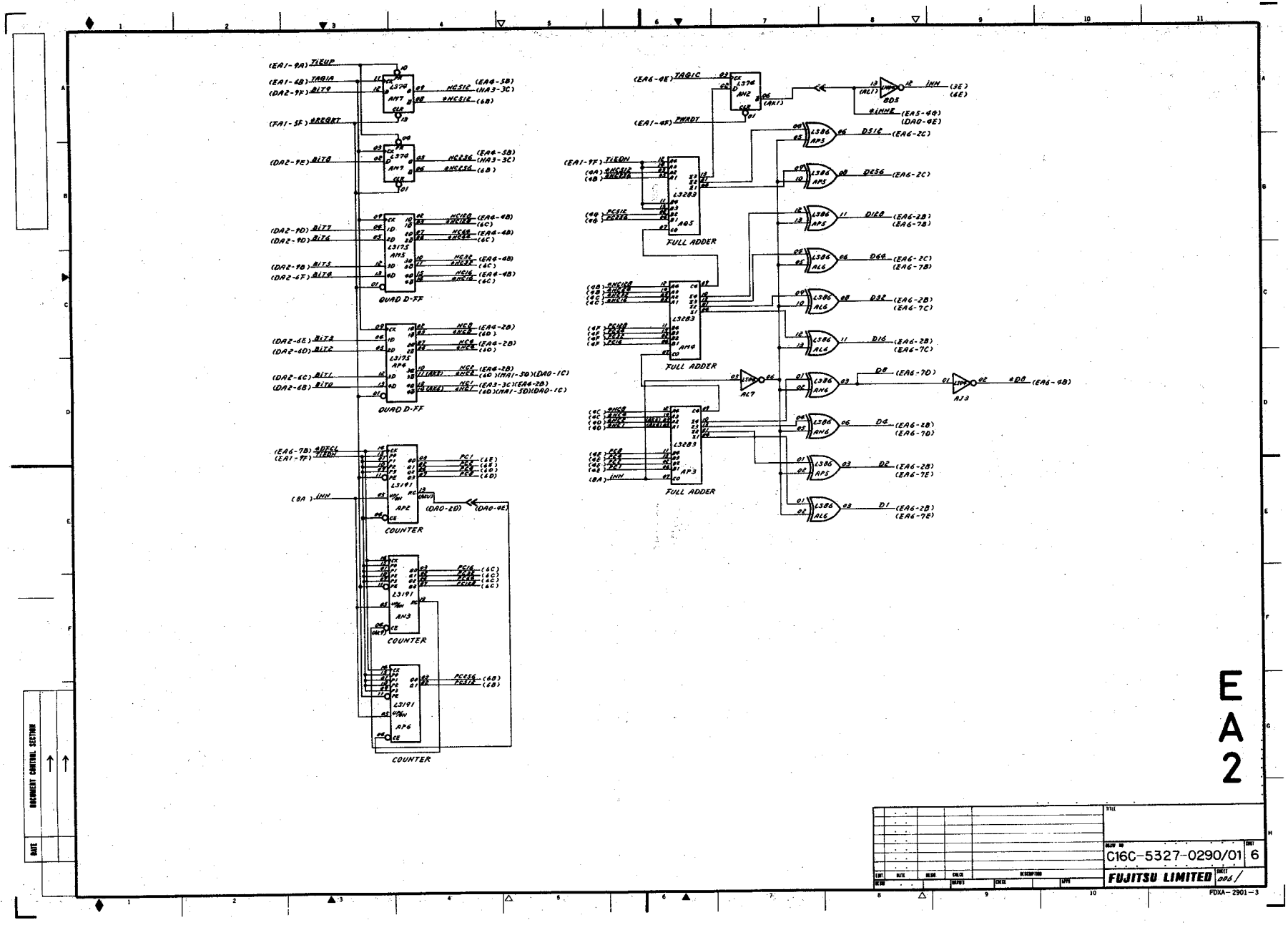
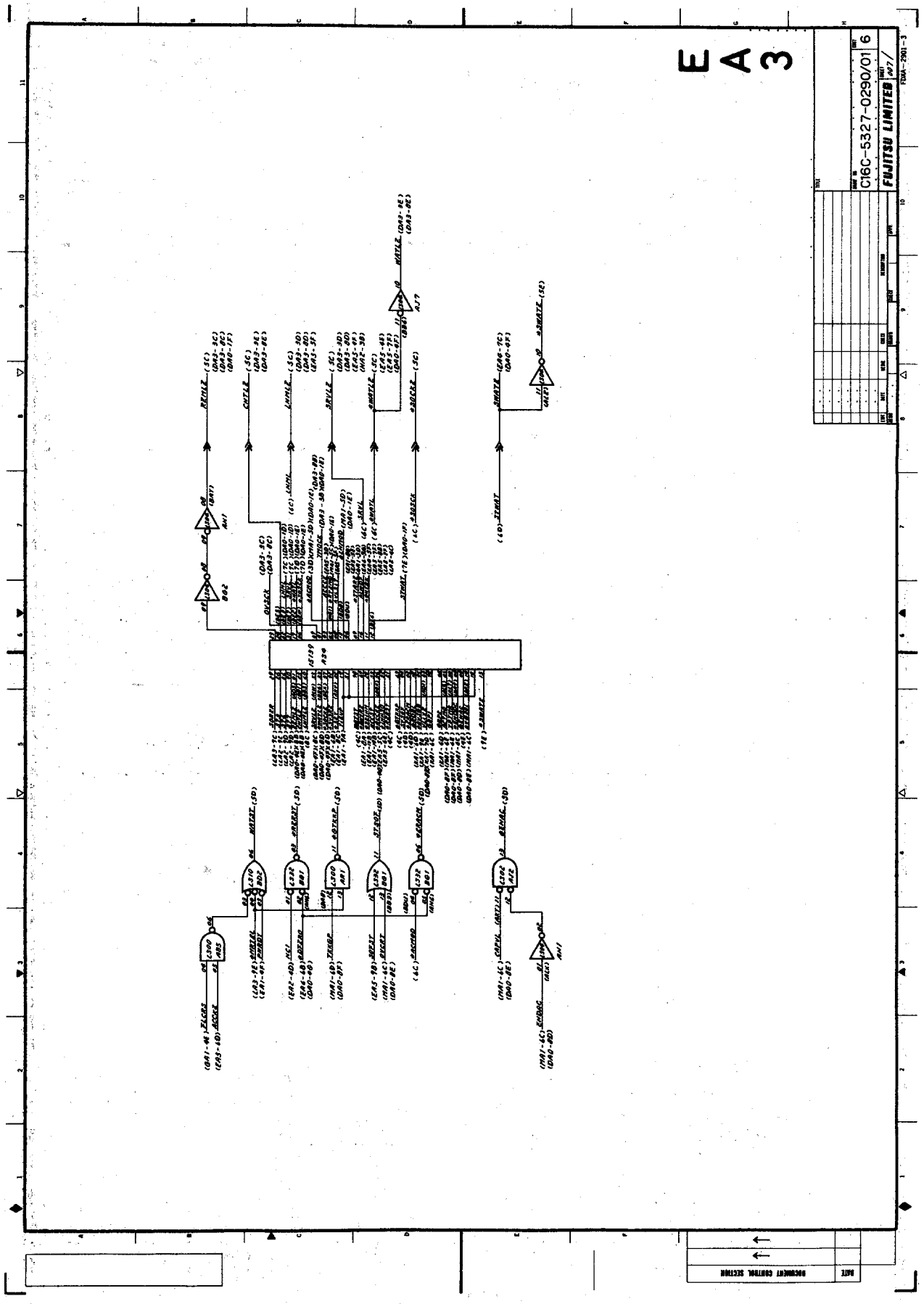
FUJITSU LIMITED
FDXA-2901-3


+5V
330Ω
TIEUP
(4E)
(EA3-3A)
(EA3-5C)
(EA4-2A)
(EA4-8E)
(GA1-4A) GTAG3
(DA2-7C) RITG
LS08 AL3
RZRCM (EA4-5D)
(LA2-9D) STG
LS00 AD5
*STORE (EA3-5C) (LA2-3C)
(LA2-7D) *EDEAT
LS08 BF3
*ANTRE (EA3-5D)
(EA3-6D) *STARE
LS02 AH1
LS32 BD3
ACCST (EA3-5D)
LS04 BG2
*SKINH (EA3-5D) (EA3-6E)
STRE (EA4-2F) (FA1-3F)
SKINH (EA5-8E)
(EA6-6B) *DXZERO (ANS)
(EA5-6E) *LINK30
(EA3-7D) *ABN
LS10 AR2
LS02 AH1
(ARV)
(DA2-3B) TAQ1
(DA3-6D) SLCTD
LS00 AJ5
(LA2-7D) BUSY
#QTAG1 (EA4-5C)
LS02 AJ6
TAGIA (EA2-3A) (EA6-3E)
(EA5-6D) ABN
LS32 BA1
(EA6-4E) TAGIC
(EA6-4E) *TAGIB
LS00 AR1
(ARV)
*SST (4E) (EA3-5C) (EA6-3F) (LA2-3C) (DA0-1C)
(KA3-9D) BYCL
(10A) TIEUP
LS00 AS1
AE4
EOSMS (EA4-6E) (EA4-6F)
LS161 COUNTER
(8C) *SST
LS08 AB6
LS37 AB4
(AB1)
*PWRDY (DA1-1D) (DA1-4D) (DA0-1C)
(DA3-9F) TIEUP
(NA1-8F) PWRST
(DA0-8G)
(AD8)
AF3
PWRDY (EA2-6A) (EA3-4C) (EA4-7E) (EA6-3E)
AL7
*PWRDY (EA6-7C) (FA1-3F) (GA1-6D)
TIEDN (EA2-3D) (EA2-6B) (FA4-9B) (EA5-6C)
DOCUMENT CONTROL SECTION
DATE
EA1
C16C-5327-0290/01
6
FUJITSU LIMITED
FDXA-2901-3


QUAD D-FF
QUAD D-FF
COUNTER
COUNTER
COUNTER
FULL ADDER
FULL ADDER
FULL ADDER
E
A
2
C16C-5327-0290/01
6
FUJITSU LIMITED
FDXA-2901-3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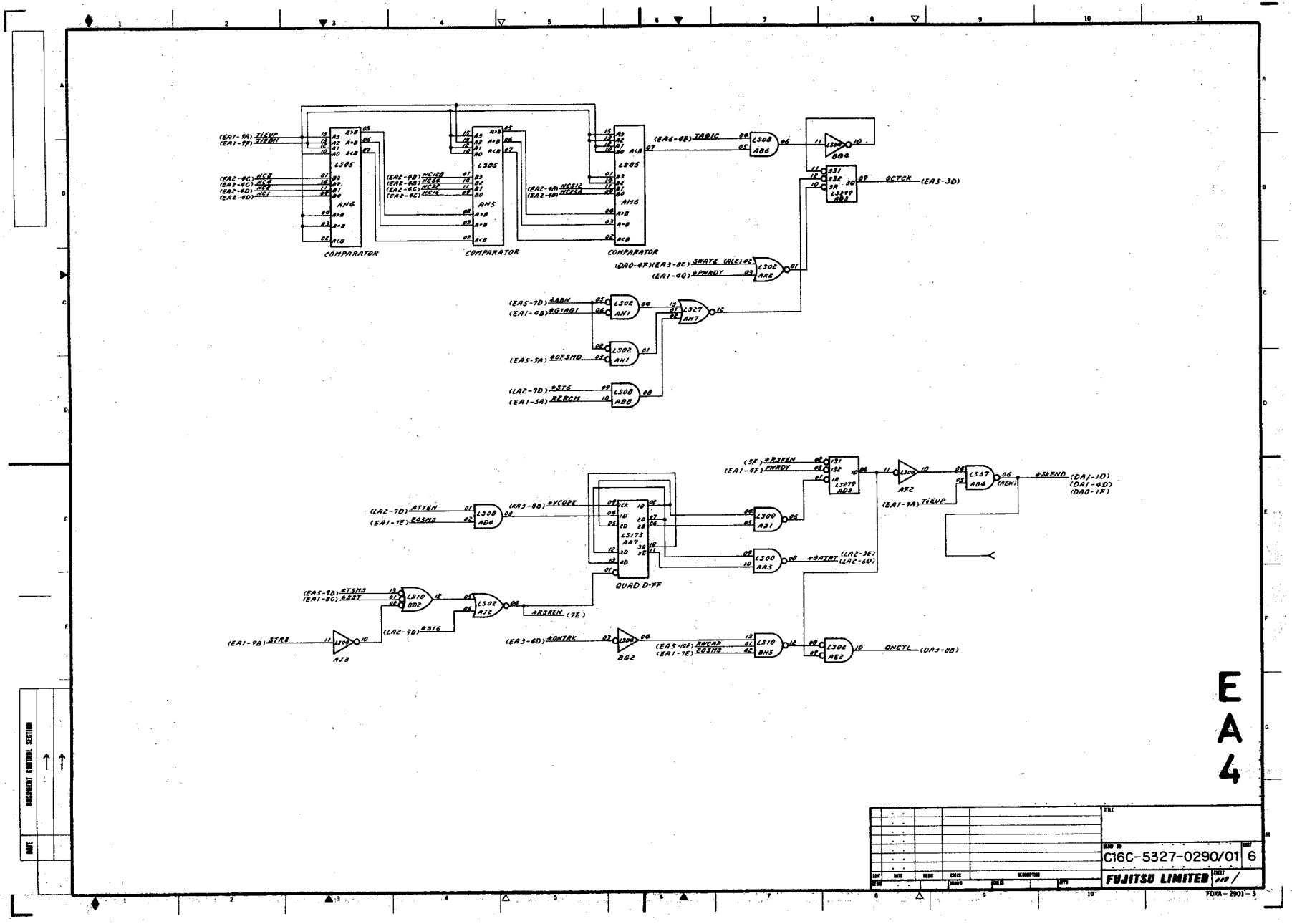
C16C-5327-0290/01
FUJITSU LIMITED


COMPARATOR
COMPARATOR
COMPARATOR
QUAD D-TF
DOCUMENT CONTROL SECTION
E
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4
C16C-5327-0290/01
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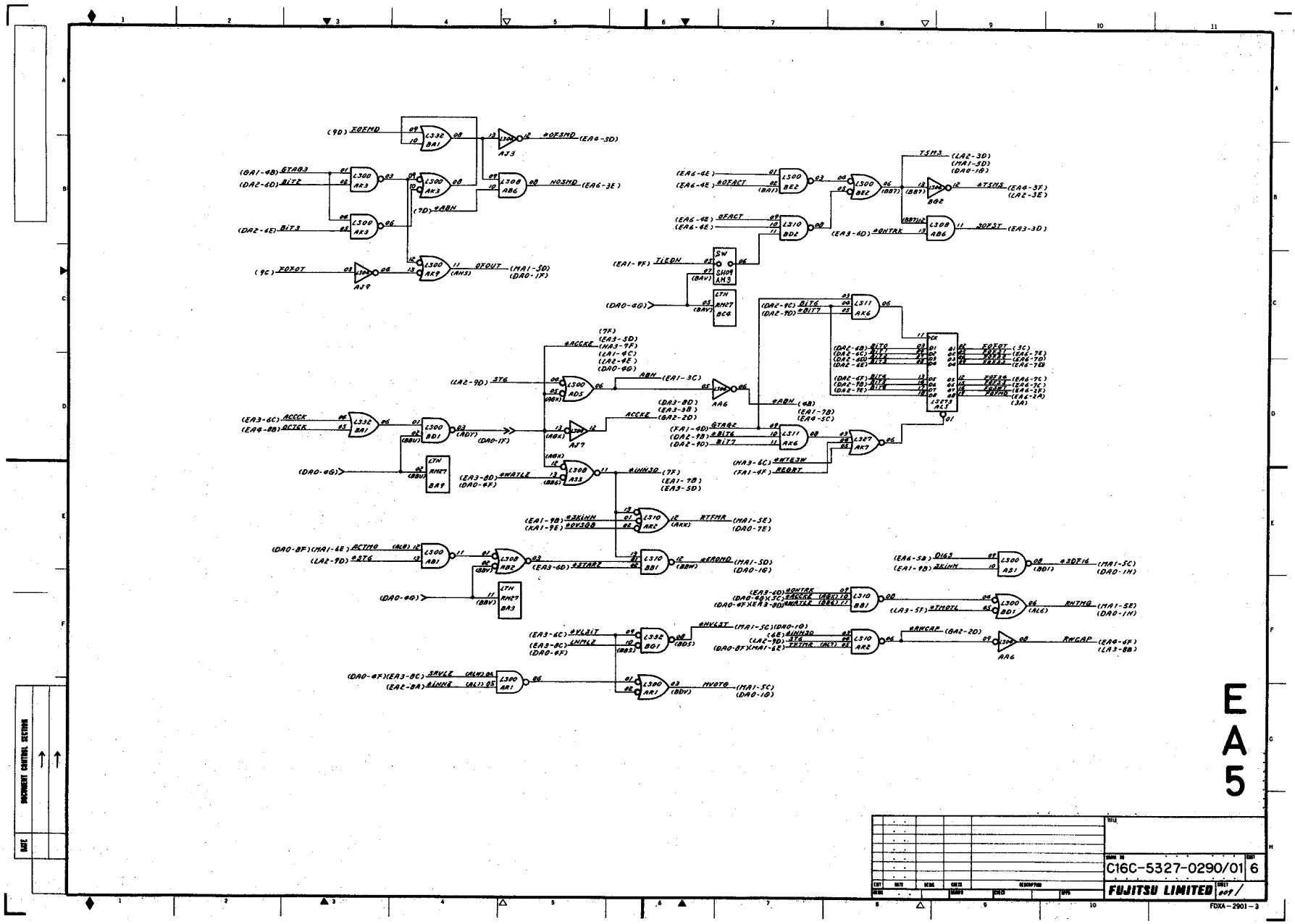
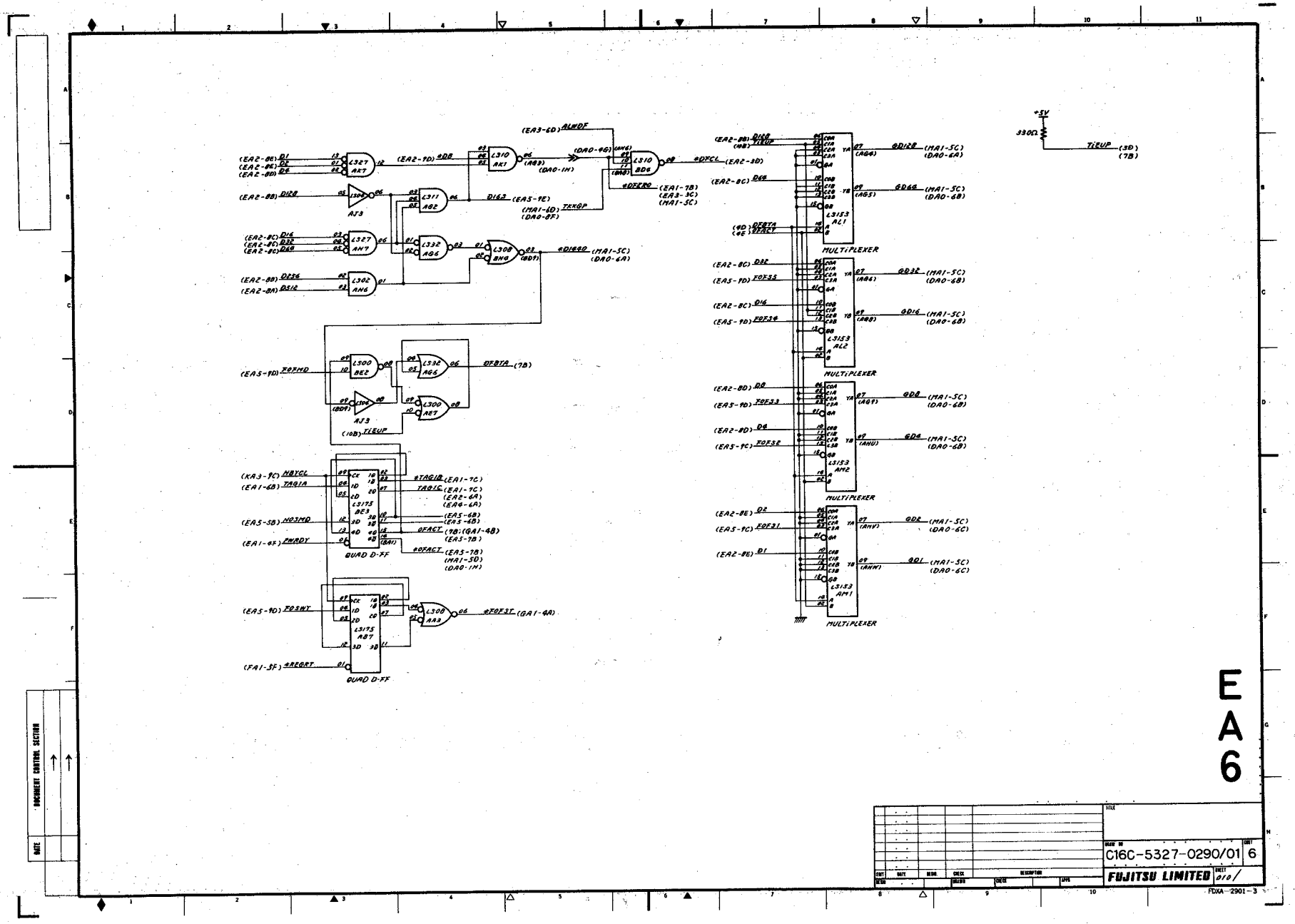
FUJITSU LIMITED
FDXA-2901-3


E A 5
C16C-5327-0290/01 6
FUJITSU LIMITED
FDXA-2901-3



E A 6

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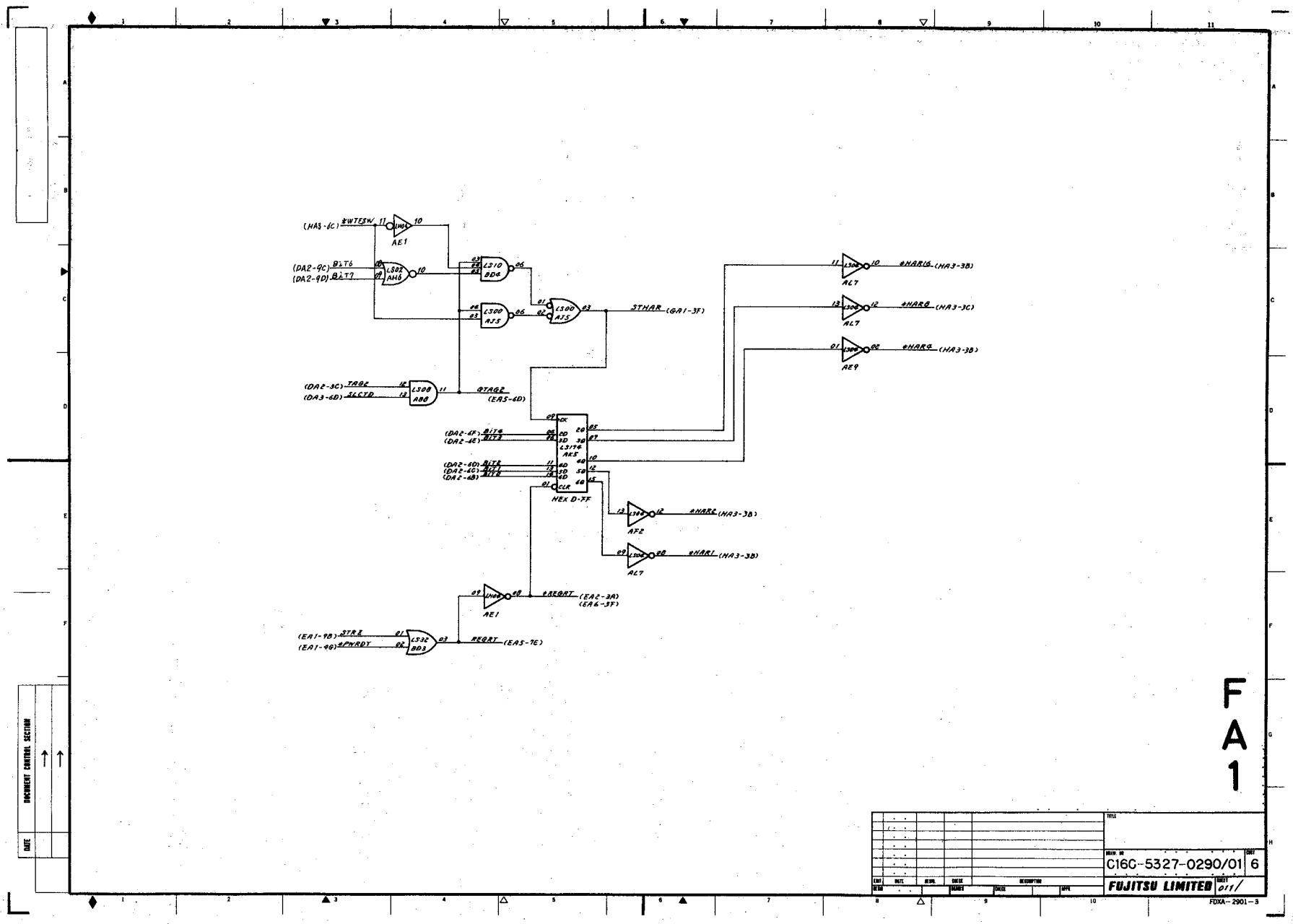
CRT NO.	DATE	DESIGN	CHECK	DESCRIPTION	DRAWN	CHECK	APPR FUJITSU LIMITED SHEET 010/

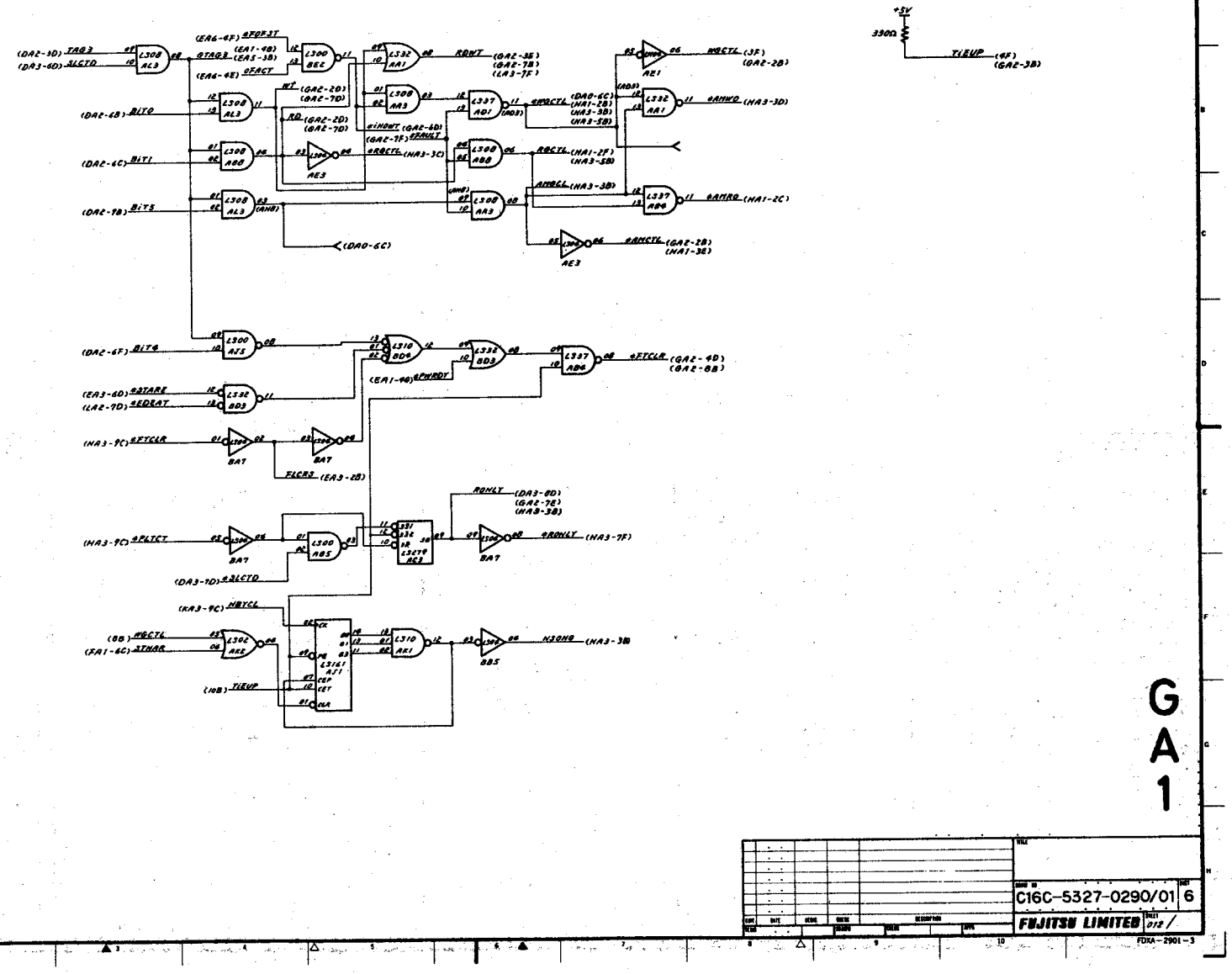
FDXA-2901-3

DOCUMENT CONTROL SECTION

DATE

B03P-4825-0002A...01A


(HA3-1C) *WTESW
AE1
(DA2-9C) BIT6
(DA2-9D) BIT7
AH6
LS10 BD6
LS00 AJ5
STHAR (GA1-3F)
(DA2-3C) TAB2
(DA3-6D) SLCTD
AB8
QTAG2 (EA5-6D)
(DA2-4F) BIT4
(DA2-4E) BIT5
(DA2-4D) BIT6
(DA2-4C) BIT7
(DA2-4B)
LS374 AK5
HEX D-FF
*HAR6 (HA3-3B)
AF2
*HAR1 (HA3-3B)
AL7
*HAR16 (HA3-3B)
*HAR8 (HA3-3C)
*HAR4 (HA3-3B)
AE9
*REQRT (EA2-3A) (EA6-3F)
(EA1-9B) STRE
(EA1-4B) *PNRDY
LS32 BD3
REQRT (EA5-7E)
DOCUMENT CONTROL SECTION
DATE
F A 1
TITLE
DRAW NO C16C-5327-0290/01
REV 6
FUJITSU LIMITED
SHEET 011
FDXA-2901-3



G
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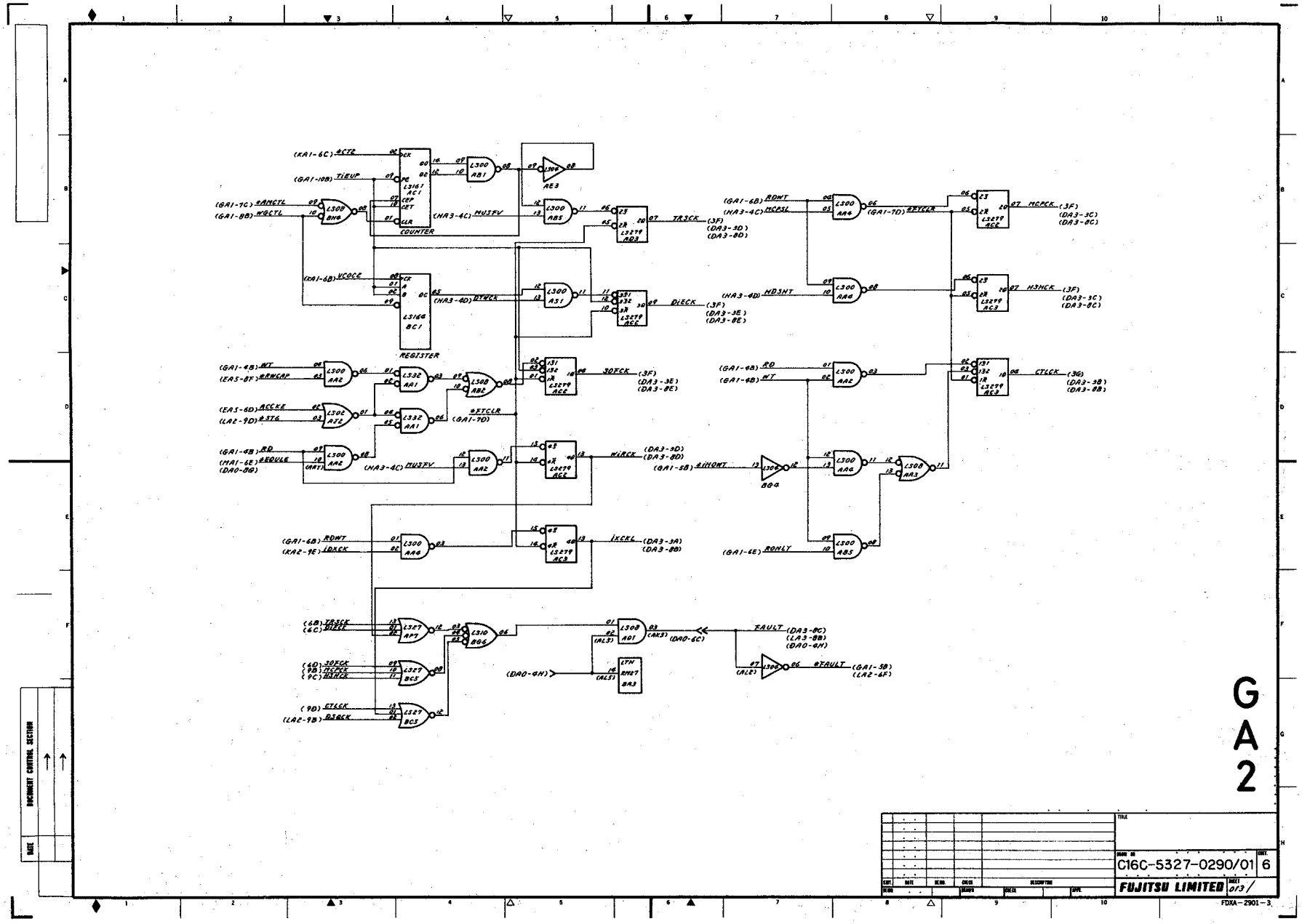
		TITLE
		DWG NO C16C-5327-0290/01 REV 6
		FUJITSU LIMITED SHEET 012 /

FDXA-2901-3

DOCUMENT CONTROL SECTION

DATE

B03P-4825-0002A...01A


(KA1-6C) ACTE
(GA1-10B) TIEUP
(GA1-7C) #ANCTL
(GA1-8B) WGCTL
COUNTER
(KA1-6B) VCOCE
REGISTER
(GA1-4B) WT
(EA5-8F) #RWGAP
(EA5-6D) ACCKE
(LA2-9D) #STG
(GA1-4B) RD
(MA1-4E) #EQULE
(DA0-0G)
(HA3-4C) MUSFV
(GA1-6B) RDWT
(KA2-9E) IDXCK
(6B) TR3CK
(6C) DIECK
(6D) 30FCK
(9B) MCPCK
(9C) H3HCK
(9B) CTLCK
(LA2-9B) G3CCK
(GA1-6B) RDWT
(HA3-4C) MCPCL
(GA1-7D) #PTCLR
(HA3-4D) HD3HT
(GA1-6B) RD
(GA1-6B) WT
(GA1-5B) #1HONT
(GA1-6E) RDHLY
(DA0-6N)
(ALS)
(AK3)
(DA0-6C)
FAULT
(DA3-9C)
(LA3-8B)
(DA0-4N)
(AL2)
#FAULT
(GA1-5B)
(LA2-8F)
(3F)
(DA3-3C)
(DA3-8C)
(DA3-3E)
(DA3-8E)
(DA3-9D)
(DA3-8D)
(DA3-3A)
(DA3-8B)
(3G)
(DA3-9B)
#FTCLR
(GA1-7D)
#WIRCK
IKCKL
#30FCK
TR3CK
DIECK
MCPCK
H3HCK
CTLCK
DOCUMENT CONTROL SECTION
DATE
G
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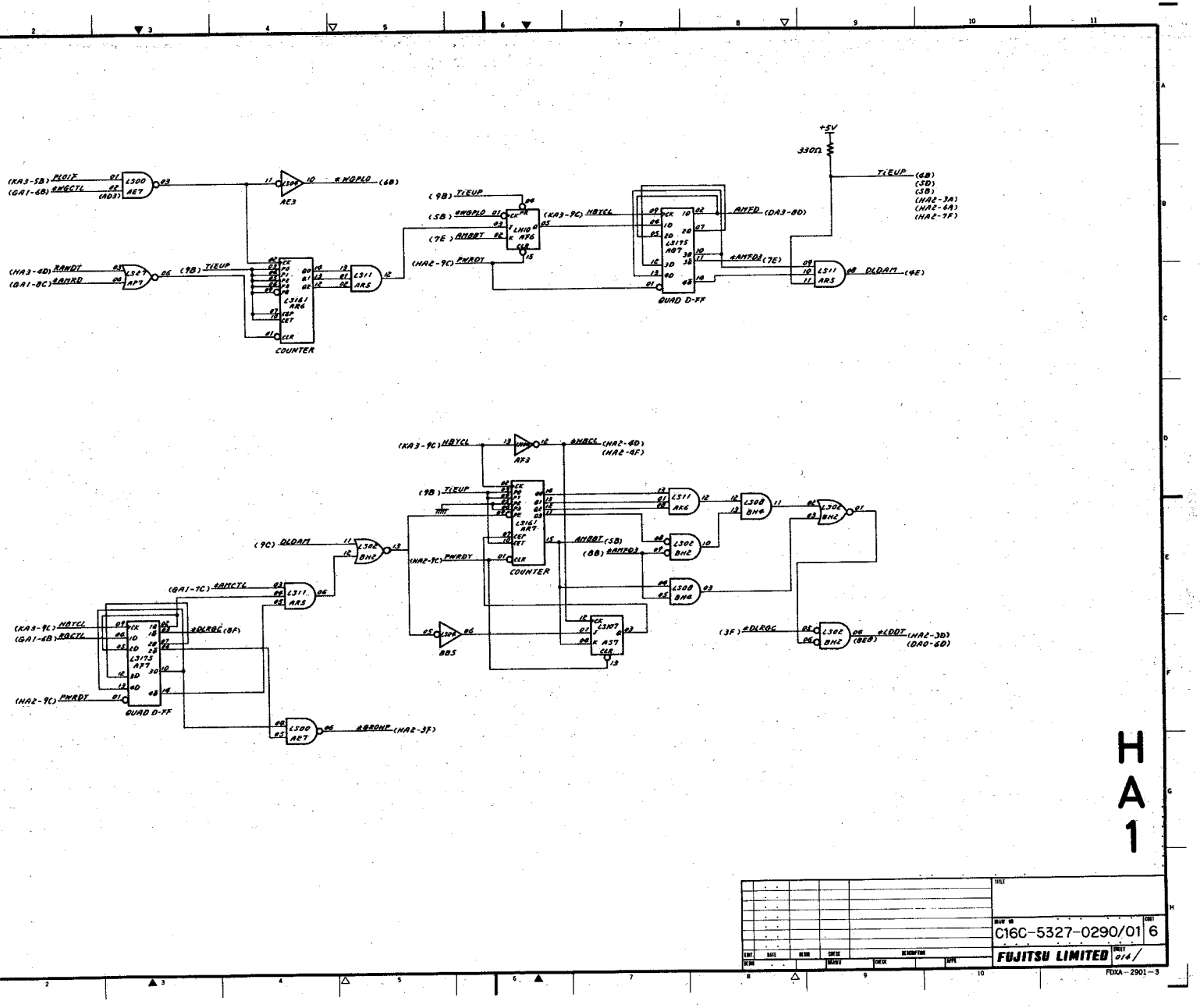
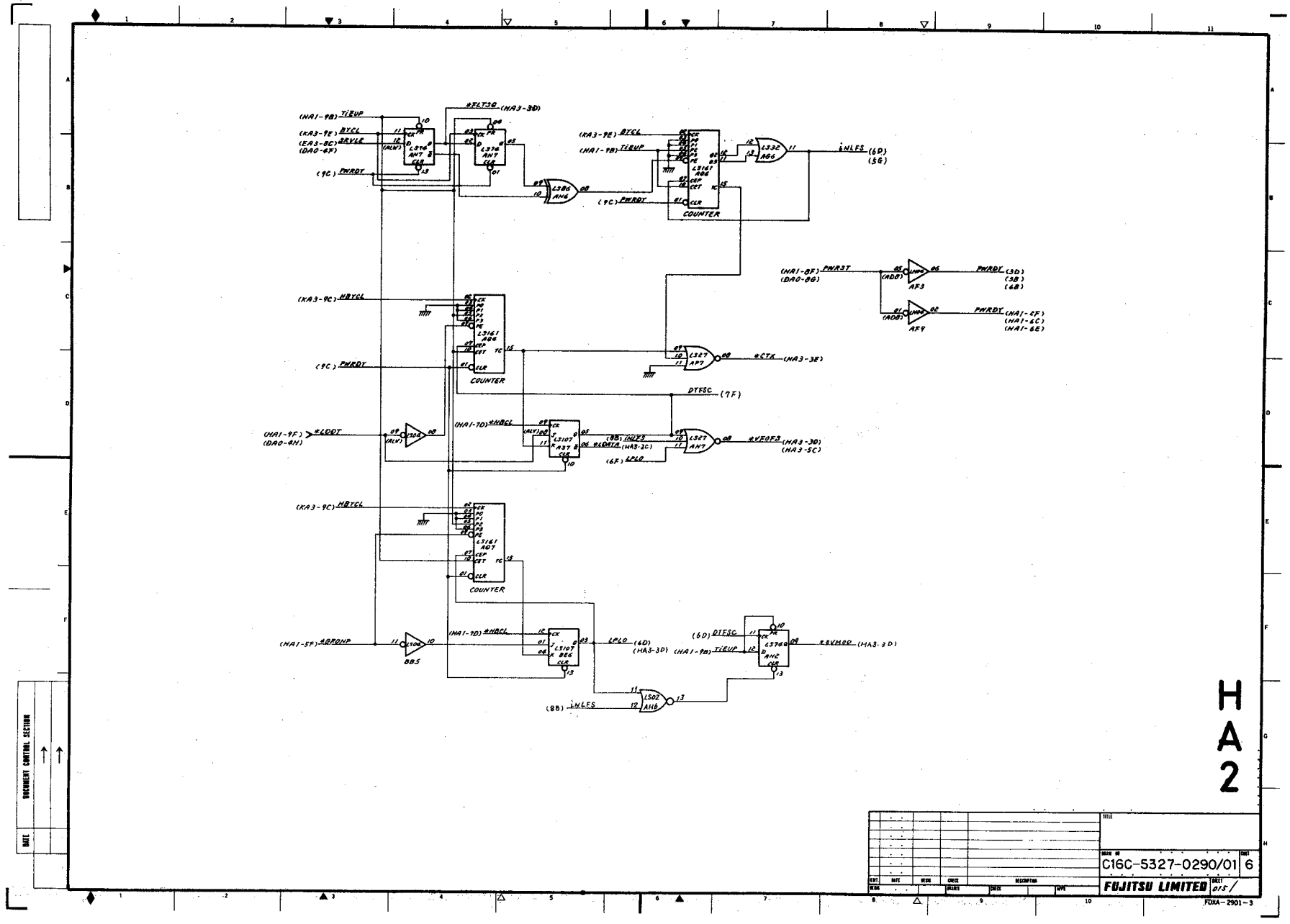
TITLE
DRAWING NO
C16C-5327-0290/01
SHEET 6
FUJITSU LIMITED
SHEET 013
FDXA-2901-3


+5V
330Ω
T/EUP
COUNTER
QUAD D-FF
DLDAM
HBYCL
PWRDY
AMPD3
AMFD
BBS
QUAD D-FF
COUNTER
DLDAM
HA1


(HA1-9B) TIEUP
(HA3-9E) BYCL
(EA3-8E) ARVLR
(DA0-4F)
(9C) PWRDY
*FLT3G (HA3-3D)
LS74 ANT
LS86 AN6
(KA3-9E) BYCL
(HA1-9B) TIEUP
LS161 AB6
LS32 AB6
COUNTER
↓NLFS (6D) (5G)
(HA1-8F) PWR3T
(DA0-8G)
LS04 AF3
LS04 AF9
PWRDY (3D) (5B) (6B)
PWRDY (HA1-4F) (HA1-6C) (HA1-6E)
(KA3-9C) HBYCL
LS161 AB6
LS27 AP7
*CTX (HA3-3E)
DTFSC (7F)
(HA1-9F) *LDDT
(DA0-8H)
LS04 AL9
(HA1-7D) *HBCL
LS107 A37
(8B) INLFS
*LDMTA (HA3-2C)
(6F) LPLO
LS27 AN7
*VFOFS (HA3-3D) (HA3-5C)
LS161 A07
(HA1-5F) *BRDNP
LS04 BB5
LS107 B66
LPLO (6D) (HA3-3D)
(6D) DTFSC
(HA1-9B) TIEUP
LS74 BN2
*SVMOD (HA3-3D)
(8B) ↓NLFS
LS02 AH6
DOCUMENT CONTROL SECTION
DATE
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C16C-5327-0290/01
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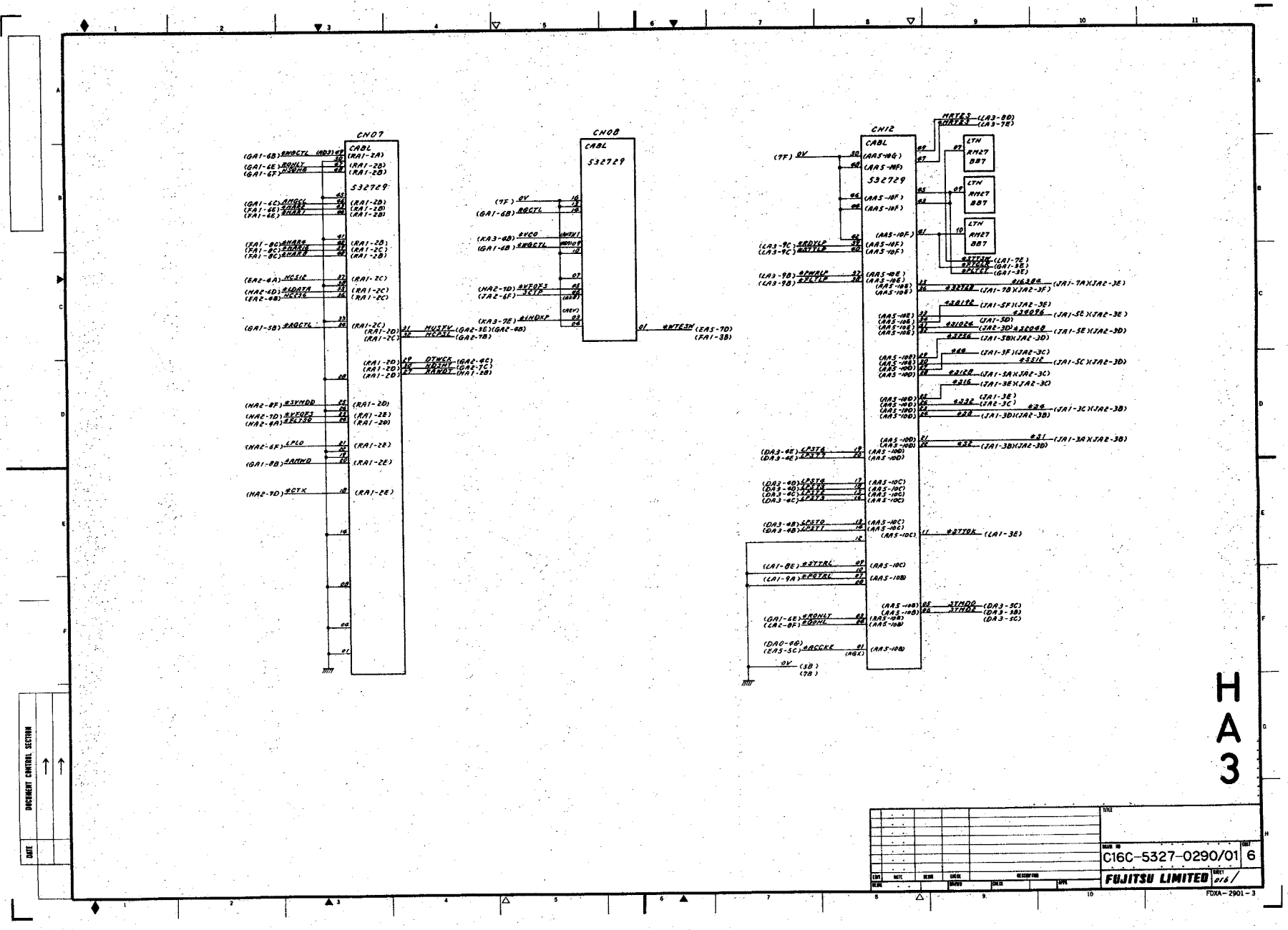
FUJITSU LIMITED
FDXA-2901-3


CN07
CABL
532729
CN08
CABL
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CN12
CABL
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FUJITSU LIMITED
C16C-5327-0290/01
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FDXA-2901-3
H
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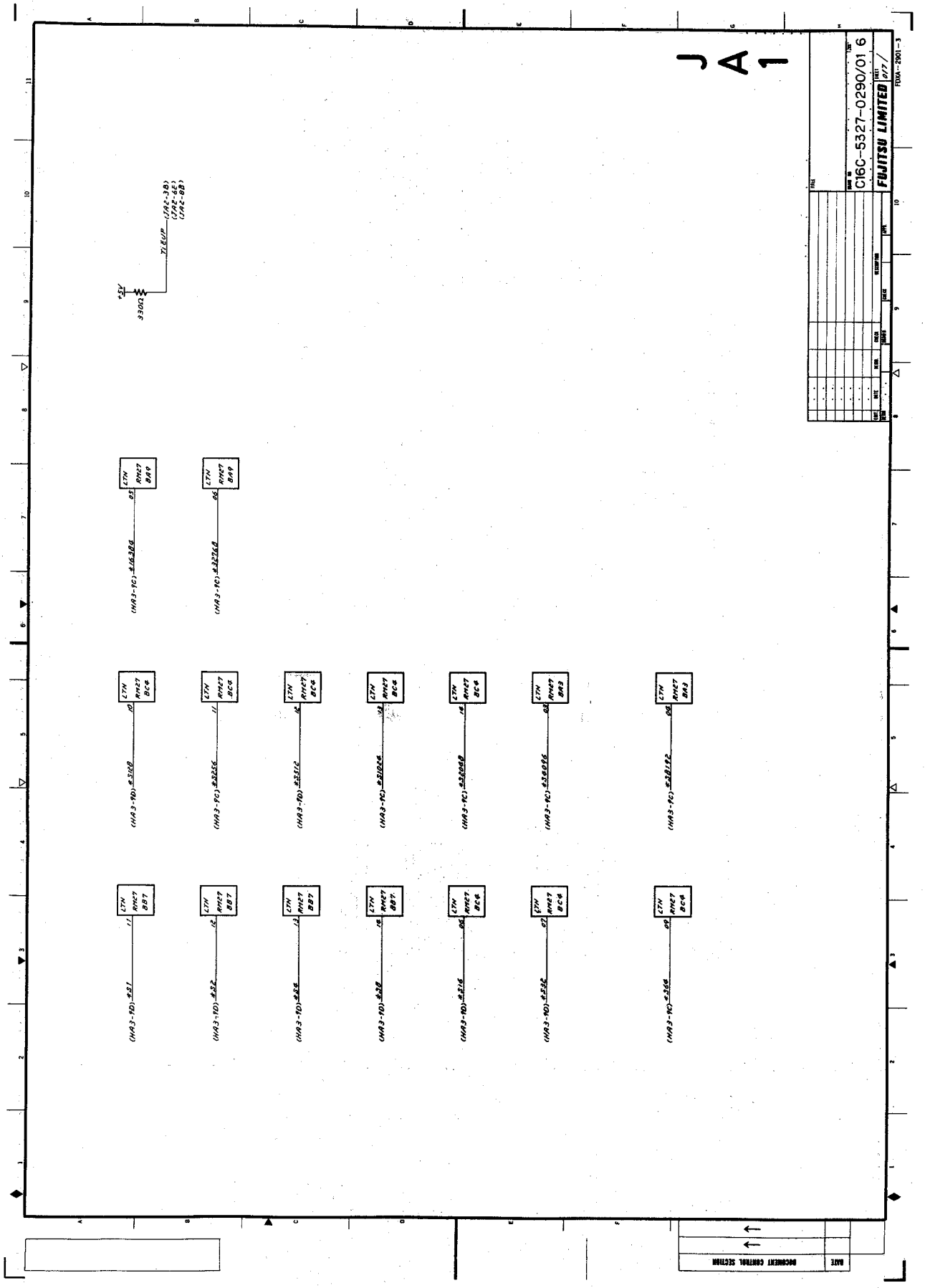
DOCUMENT CONTROL SECTION
DATE


J
A
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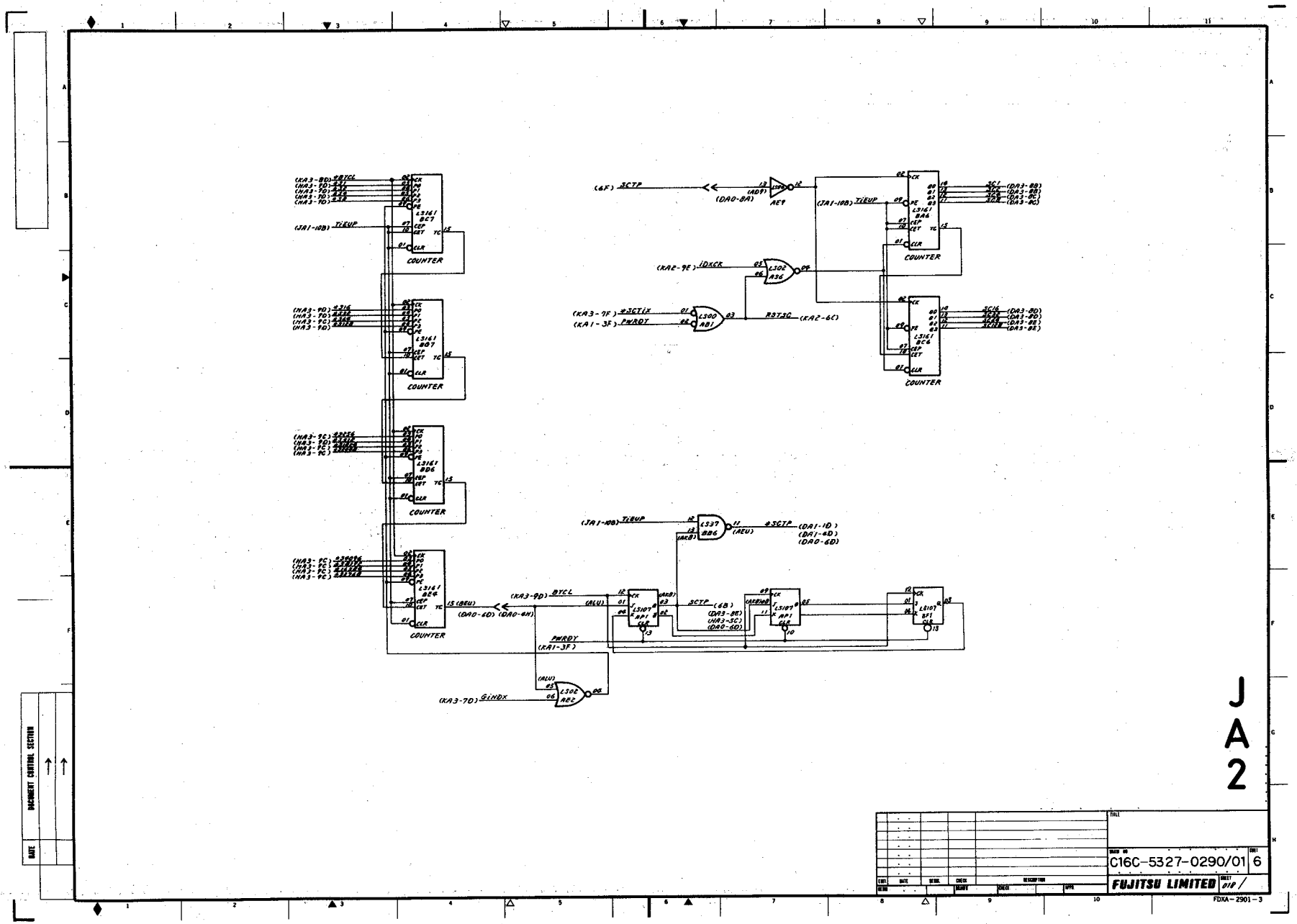
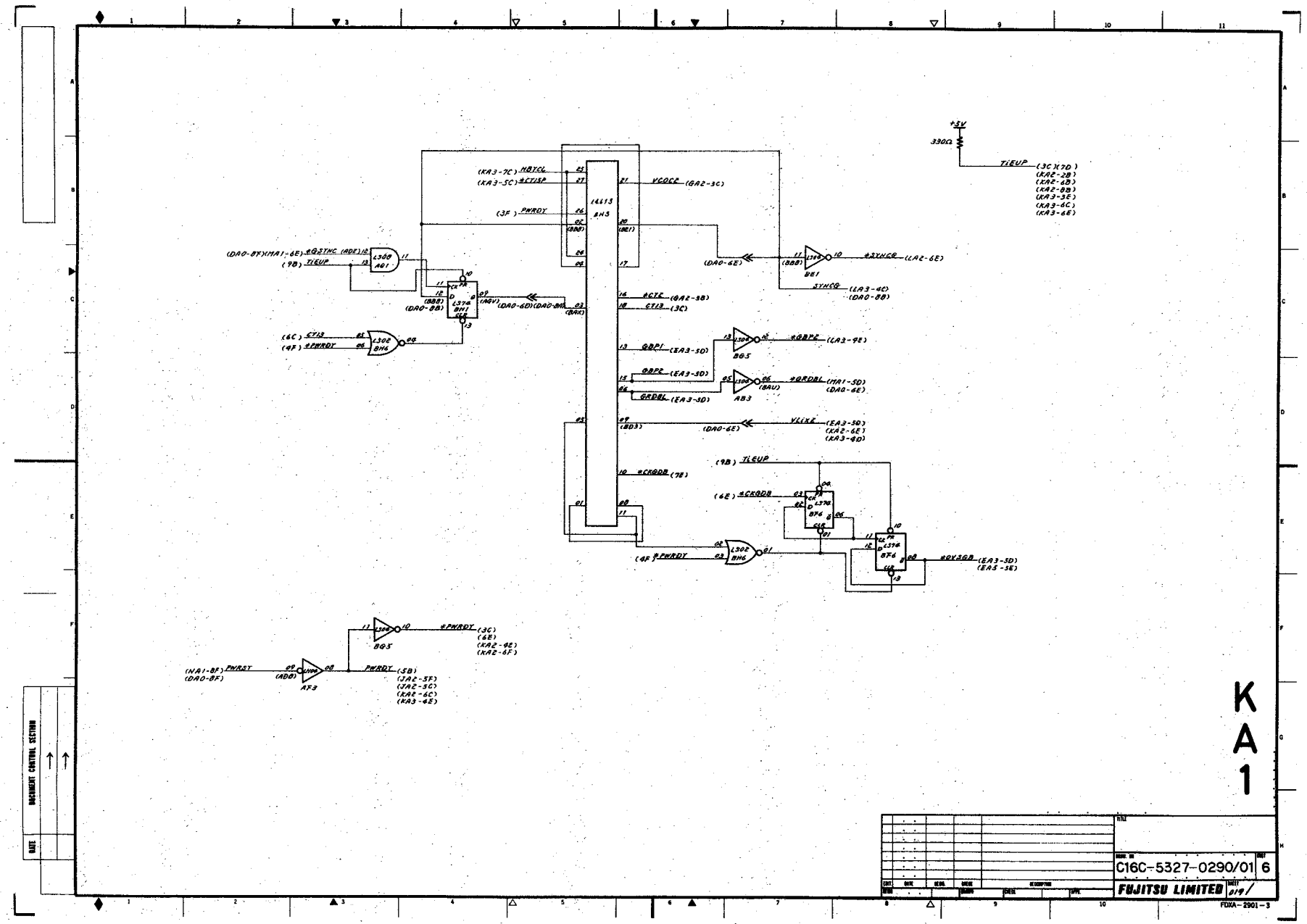
C16C-5327-0290/01 6
FUJITSU LIMITED
FDXA-2901-3
DOCUMENT CONTROL SECTION
DATE


COUNTER
COUNTER
COUNTER
COUNTER
COUNTER
TIEUP
SCTP
IDXCK
PWRDY
BYCL
GINDX
RSTSG
(DA0-6D)
(DA0-6H)
(ALU)
(AEU)
(ARB)
(DA0-8A)
(DA1-1D)
(DA1-6D)
(DA3-8E)
(DA3-3C)
(DA3-6D)
(KA3-9D)
(KA3-7D)
(KA3-7F)
(KA1-3F)
(KA2-9E)
(KA2-6C)
(JA1-10B)
(6F)
(48)
JA2
C16C-5327-0290/01
6
FUJITSU LIMITED
FDXA-2901-3


+5V
330Ω
TLEUP
(3C)(7D)
(KA2-2B)
(KA2-4B)
(KA2-8B)
(KA3-3E)
(KA3-6C)
(KA3-6E)
(KA3-7C) MRTCL
(KA3-5C) *CTISP
(3F) PWRDY
VCOCE (GA2-3C)
LA613 BH5
(DA0-6F)(MA1-6E) *GSTNC (ADE)
(9B) TLEUP
LS08 AG1
LS74 BH1
(DA0-6D)(DA0-BH)
(DA0-6E)
LS04 BE1
*SYNCR (LA2-6E)
SYNCG (LA3-4C) (DA0-8B)
(6C) CTI3
(4F) *PWRDY
LS02 BH6
RCTE (GA2-9B)
CTI3 (3C)
GBPI (EA3-5D)
GBPE (EA3-3D)
GRDBL (EA3-3D)
LS04 BG5
*GBPE (LA3-9E)
LS04 AB3
*GRDBL (MA1-5D) (DA0-6E)
VLIKE (EA3-5D) (KA2-6E) (KA3-4D)
(9B) TLEUP
*CKRDR (7E)
(6E) *CKRDR
LS74 BT4
LS02 BH6
*QVSGB (EA3-5D) (EA3-3E)
(NA1-8F) PWRST
(DA0-8F)
LS04 AF3
*PWRDY (3C) (6E) (KA2-9E) (KA2-6F)
PWRDY (5B) (JA2-5F) (JA2-5C) (KA2-6C) (KA3-6E)
MAINMENT CONTROL SECTION
DATE
KA
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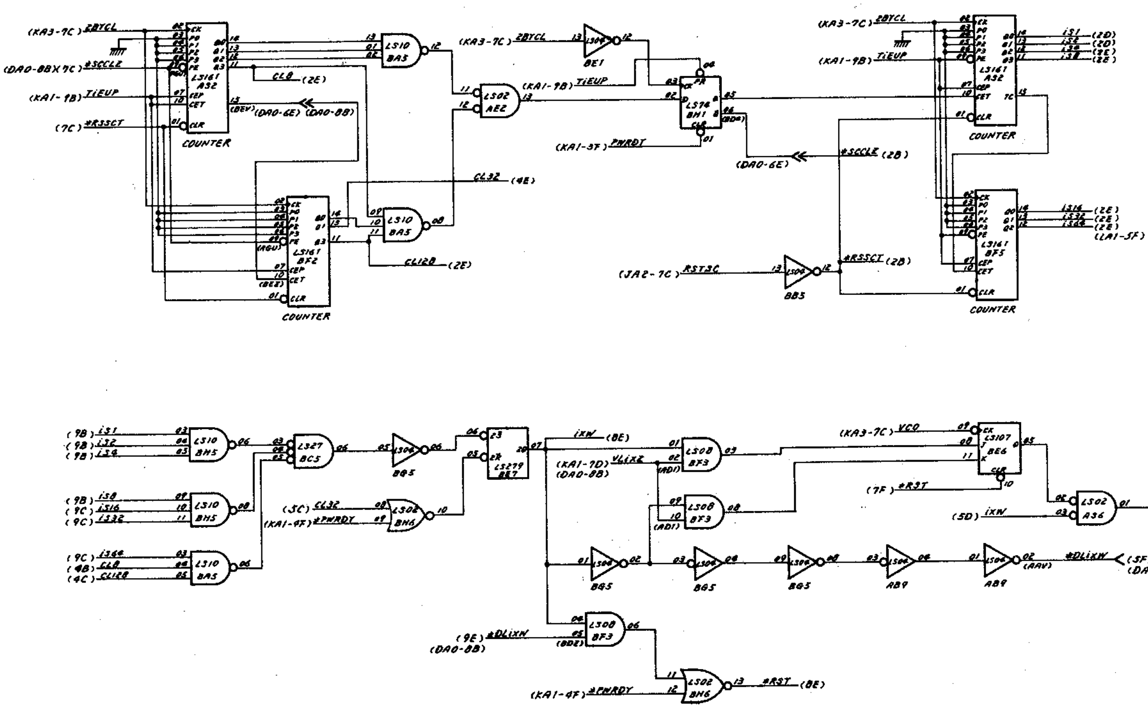
C16C-5327-0290/01
6
FUJITSU LIMITED
FDXA-2901-3



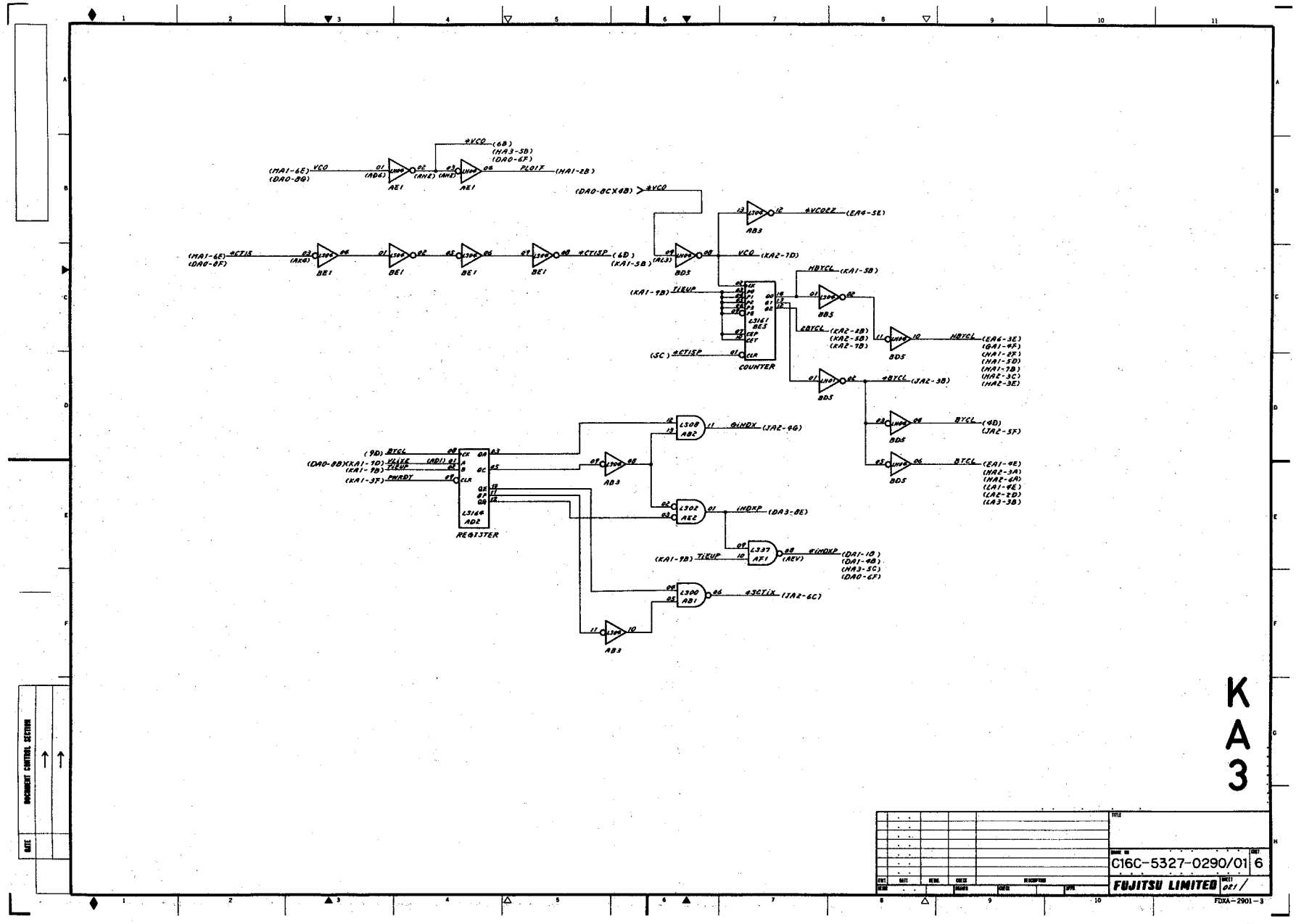
KA2

C16C-5327-0290/01 6

FUJITSU LIMITED

FDXA-2901-3

DOCUMENT CONTROL SECTION


K
A
3
COUNTER
REGISTER
DOCUMENT CONTROL SECTION
C16C-5327-0290/01
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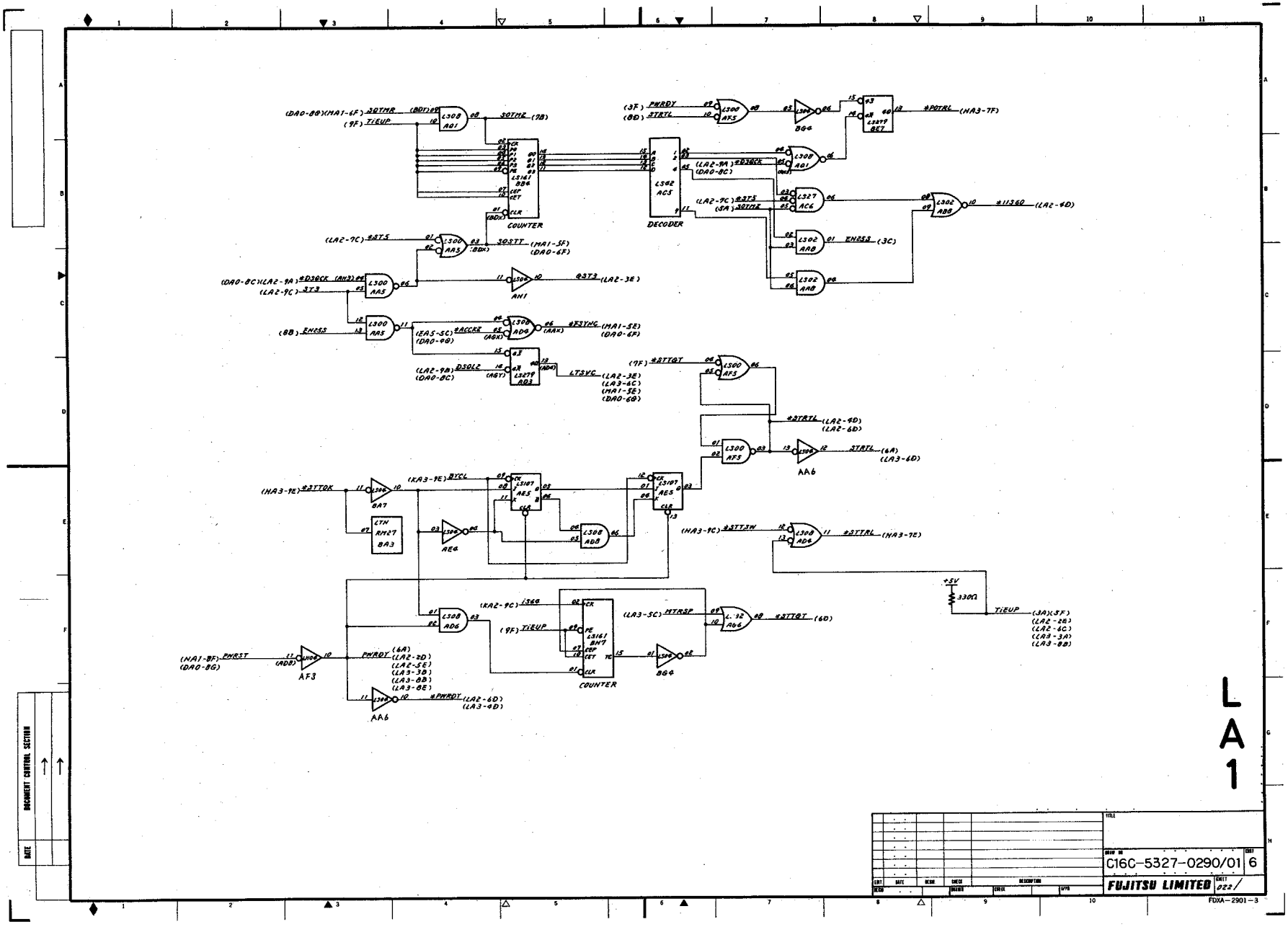
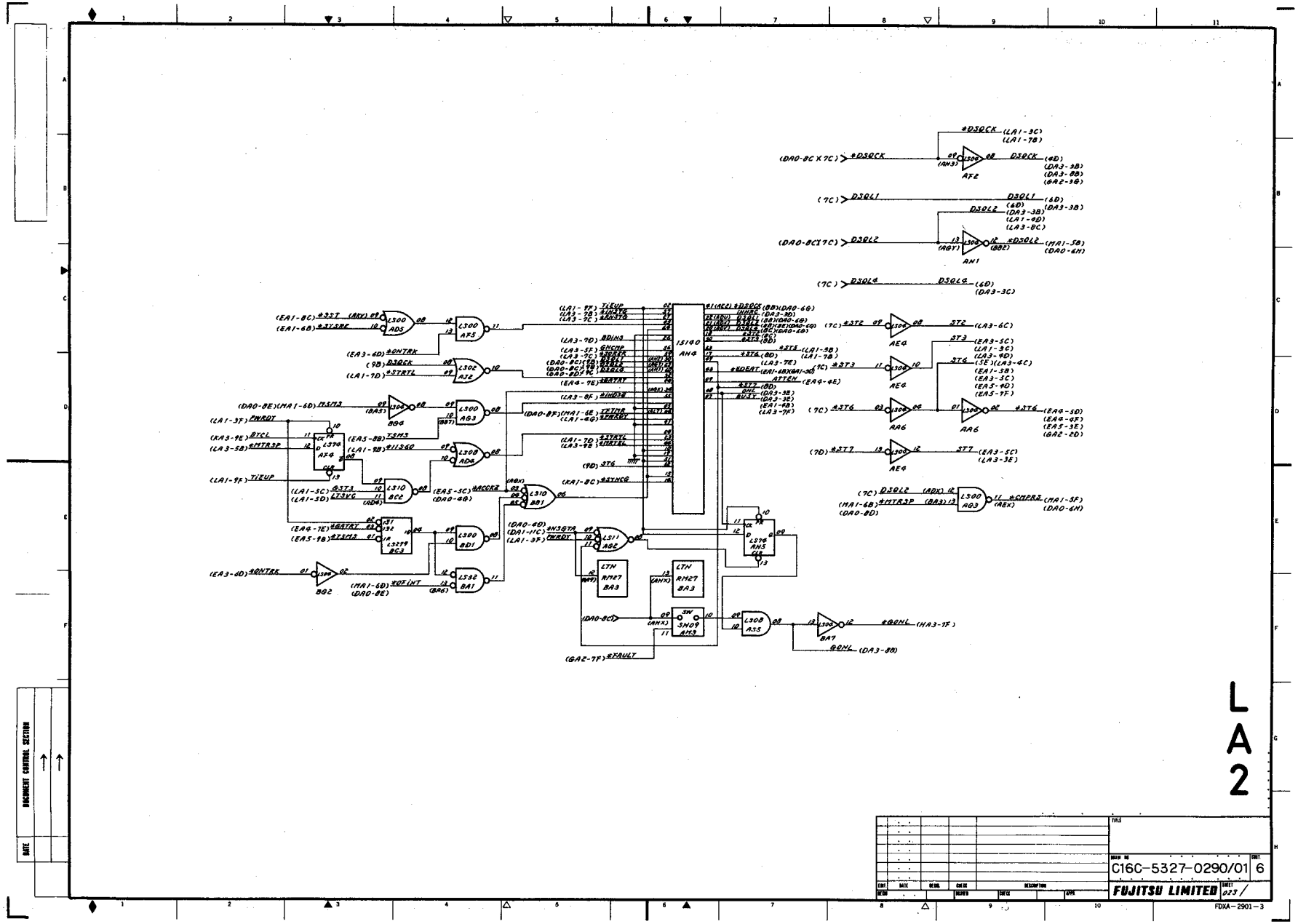
FUJITSU LIMITED
FDXA-2901-3


COUNTER
DECODER
COUNTER
AA6
AF3
AA6
BG4
BG4
330Ω
+5V
TIEUP
L
A
1
C16C-5327-0290/01
6
FUJITSU LIMITED
FDXA-2901-3
DOCUMENT CONTROL SECTION
DATE


LA2
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DATE
C16C-5327-0290/01
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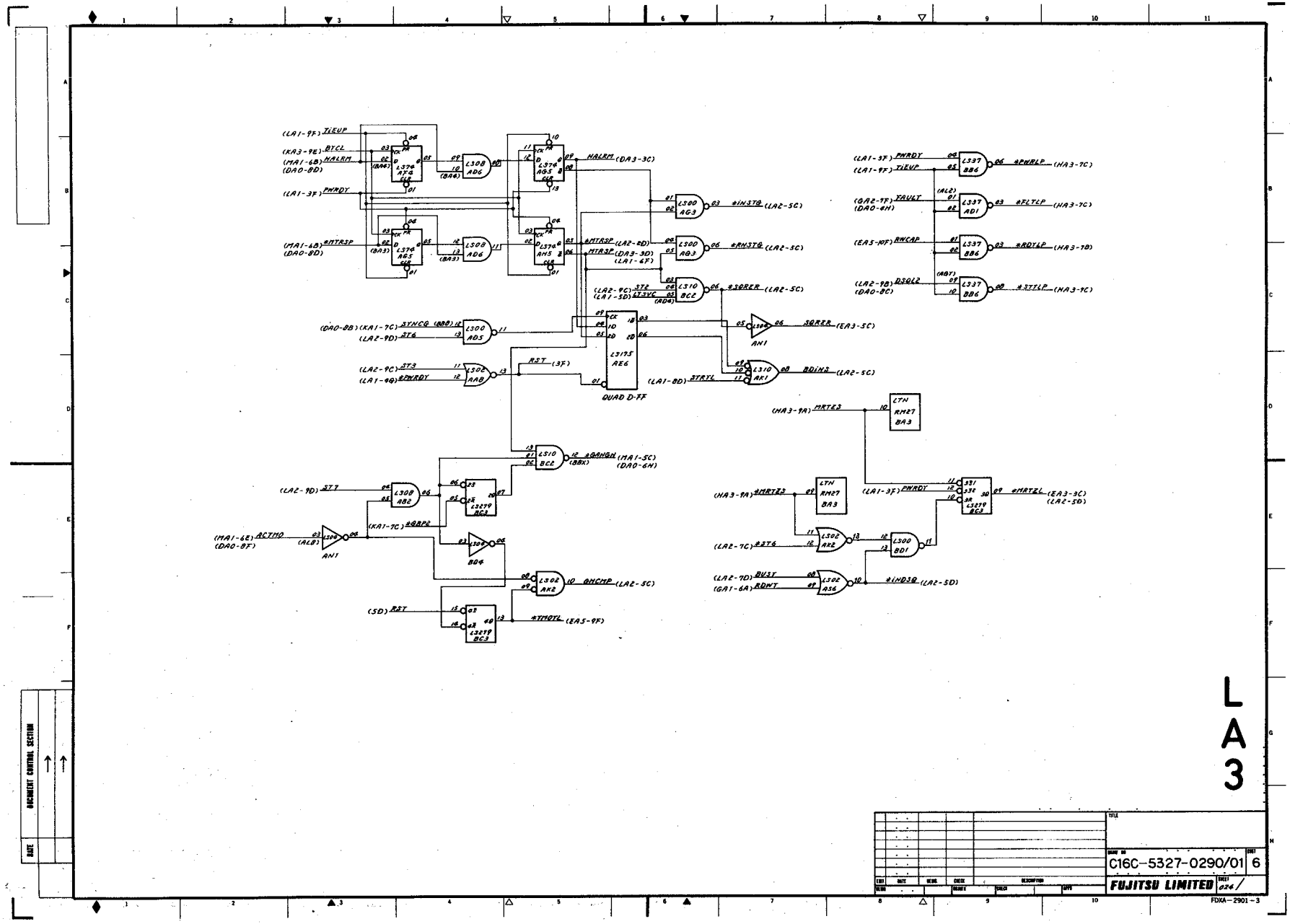
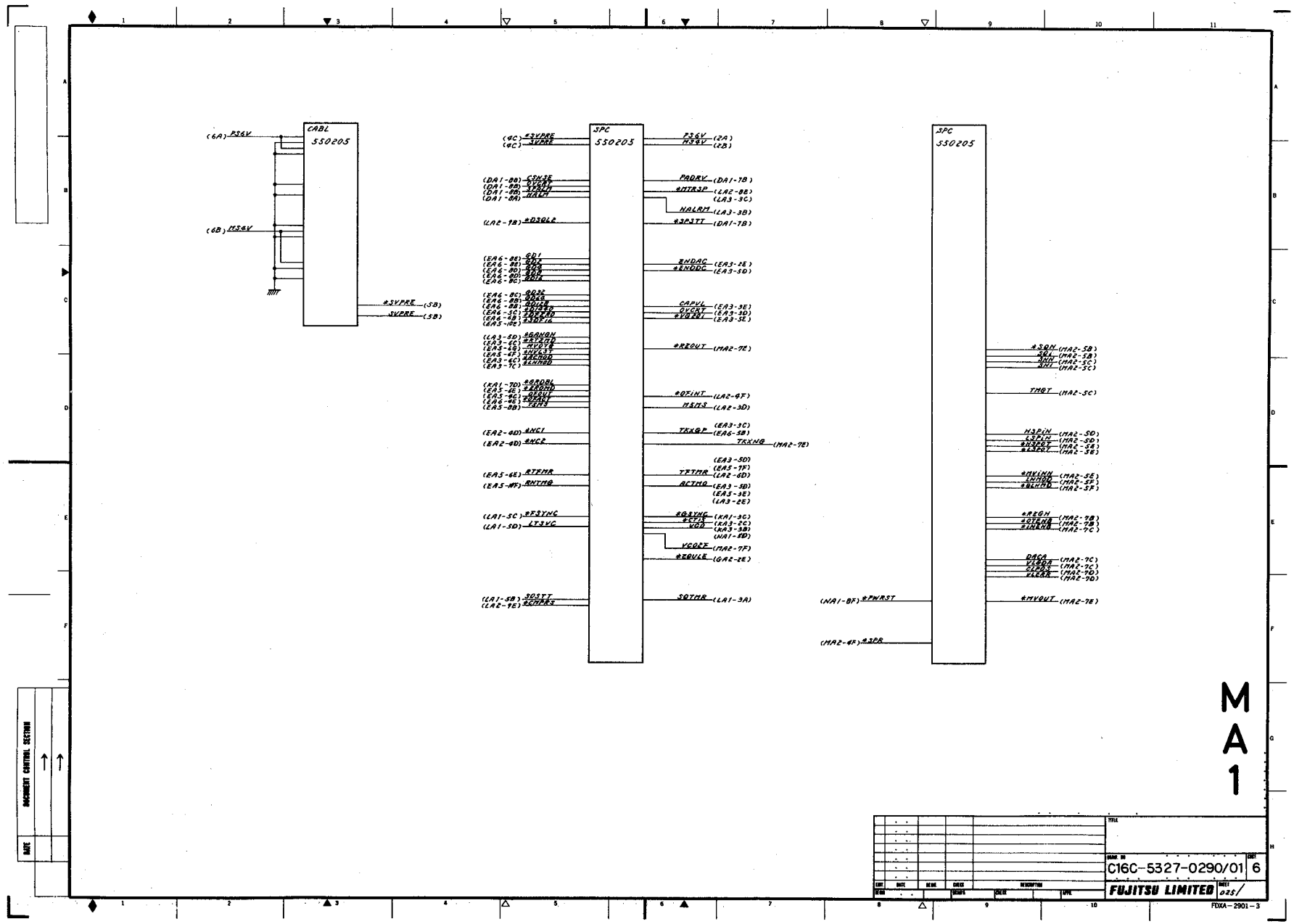
FUJITSU LIMITED
FDXA-2901-3


(LA1-9F) TIEUP
(KA3-9E) BTCL
(MA1-6B) HALRM
(DA0-8D)
(LA1-3F) PWRDY
(MA1-6B) #MTRSP
(DA0-8D)
L374 MT8 AE5
L374 AB5
L374 AM5
L308 AD6
L308 AD6
HALRM (DA3-3C)
MTRSP (LA2-8D)
MTR3P (DA3-3D) (LA1-6F)
L300 AG3
L300 AB3
L310 BC2
#INSTG (LA2-5C)
#RMSTG (LA2-5C)
#SORER (LA2-5C)
(LA2-7C) ST2
(LA1-5D) ST3VC
(AD4)
(DA0-8B) (KA1-7C) SYNCG (B80)
(LA2-9D) ST6
L300 AD5
L3175 AE6
QUAD D-FF
L300 AN1
SORER (EA3-5C)
(LA2-9C) ST3
(LA1-4G) #PWRDY
L302 AA8
RST (3F)
(LA1-8D) STRTL
L310 AR1
BDINS (LA2-5C)
(LA2-9D) ST7
L308 AB2
L3279 BC3
L310 BC2
#GAHGH (MA1-5C) (DA0-6H)
(B8X)
(MA1-6E) ACTIO
(DA0-8F)
(KA1-7C) #GBPE
(AL8)
L304 AN1
L304 BD4
L302 AK2
GMCMP (LA2-5C)
(5D) RST
L3279 BC3
#TMOTG (EA5-9F)
(LA1-9F) PWRDY
(LA1-9F) TIEUP
(GA2-7F) FAULT
(DA0-6H)
(EA5-10F) RWCAP
(LA2-9B) DSOL2
(DA0-8C)
L397 BB6
L397 AD1
L397 BB6
L397 BB6
#PWRLP (HA3-7C)
#FLTLP (HA3-7C)
#RDYLP (HA3-7D)
#STTLP (HA3-7C)
(HA3-9A) MRTE3
LTN RM27 BA3
(HA3-9A) #MRTE3
LTN RM27 BA3
(LA1-3F) PWRDY
L3279 BC3
#MRTEL (EA3-3C) (LA2-5D)
(LA2-7C) #ST6
L302 AK2
L300 BD1
(LA2-7D) BUST
(GA1-6A) RDMT
L302 AS6
#MDSG (LA2-5D)
L A 3
C16C-5327-0290/01
6
FUJITSU LIMITED
FDXA-2901-3
DOCUMENT CONTROL SECTION
DATE


CABL
550205
SPC
550205
SPC
550205
(6A) PS6V
(6B) PS6V
*SVPRE (5B)
SVPRE (5B)
(9C) *SVPRE
(9C) SVPRE
PS6V (2A)
HS6V (2B)
PADRV (DA1-7B)
*MTRSP (LA2-8E)
(LA3-9C)
HALRM (LA3-3B)
*SPSTT (DA1-7B)
*ENDAC (EA3-3E)
*ENDDC (EA3-5D)
CAPVL (EA3-3E)
OVCNT (EA3-3D)
*VQZRT (EA3-3E)
*REQUT (MA2-7E)
*QTINT (LA2-9F)
MSTS (LA2-3D)
(EA3-3C)
TRXQP (EA6-5B)
TRXHQ (MA2-7E)
(EA3-5D)
(EA3-7F)
TPTMR (LA2-4D)
ACTMQ (EA3-5D)
(EA3-3E)
(LA3-2E)
*QSYNC (KA1-3C)
*ETAS (KA3-5C)
VQD (KA3-3D)
(VA1-3D)
VCQZT (MA2-7F)
*ZBULE (GA2-2E)
SQTMR (LA1-3A)
*SQN (MA2-5B)
SNI (MA2-5B)
SNH (MA2-5C)
SNI (MA2-5C)
TMGT (MA2-5C)
HSPIN (MA2-5D)
LSPIN (MA2-5D)
*HSPST (MA2-5E)
*LSPST (MA2-5E)
*MVINH (MA2-5E)
LNHBQ (MA2-5F)
*BLNHQ (MA2-5F)
*REQH (MA2-7B)
*QTENB (MA2-7B)
*ZINHB (MA2-7C)
DACQ (MA2-7C)
VIBQA (MA2-7C)
CLPZQ (MA2-7D)
VLERR (MA2-7D)
*MVQUT (MA2-7E)
(EA6-0B) SD1
(EA6-0B) SD2
(EA6-0B) SD3
(EA6-0B) SD4
(EA6-0C) SD5
(EA6-0C) SD6
(EA6-0B) SDPAR
(EA6-0B) SHUNT
(EA6-5C) *SDTRQ
(EA6-5B) *SDTRG
(EA5-1H6) *SDTRG
(LA3-5D) *EAGNQH
(EA3-6C) *EXTQT
(EA5-4B) *TTQTE
(EA5-4F) *INTEST
(EA3-6C) *EXTMQ
(EA3-7C) *ENTMQ
(KA1-7D) *EAGNQL
(EA3-6E) *EAGNQ
(EA5-8C) *EQUT
(EA6-9E) *EQART
(EA5-8B) *EINT
(EA2-6D) ANCI
(EA2-9D) ANCE
(EA5-6E) RTFMR
(EA5-MF) RNTMQ
(LA1-5C) *FSYNC
(LA1-5D) LT3VC
(LA1-5B) SQSTT
(LA2-9E) SCMPRS
(MA1-8F) *PWRST
(MA2-4F) *SPR
MA1
DOCUMENT CONTROL SECTION
DATE
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C16C-5327-0290/01
REV
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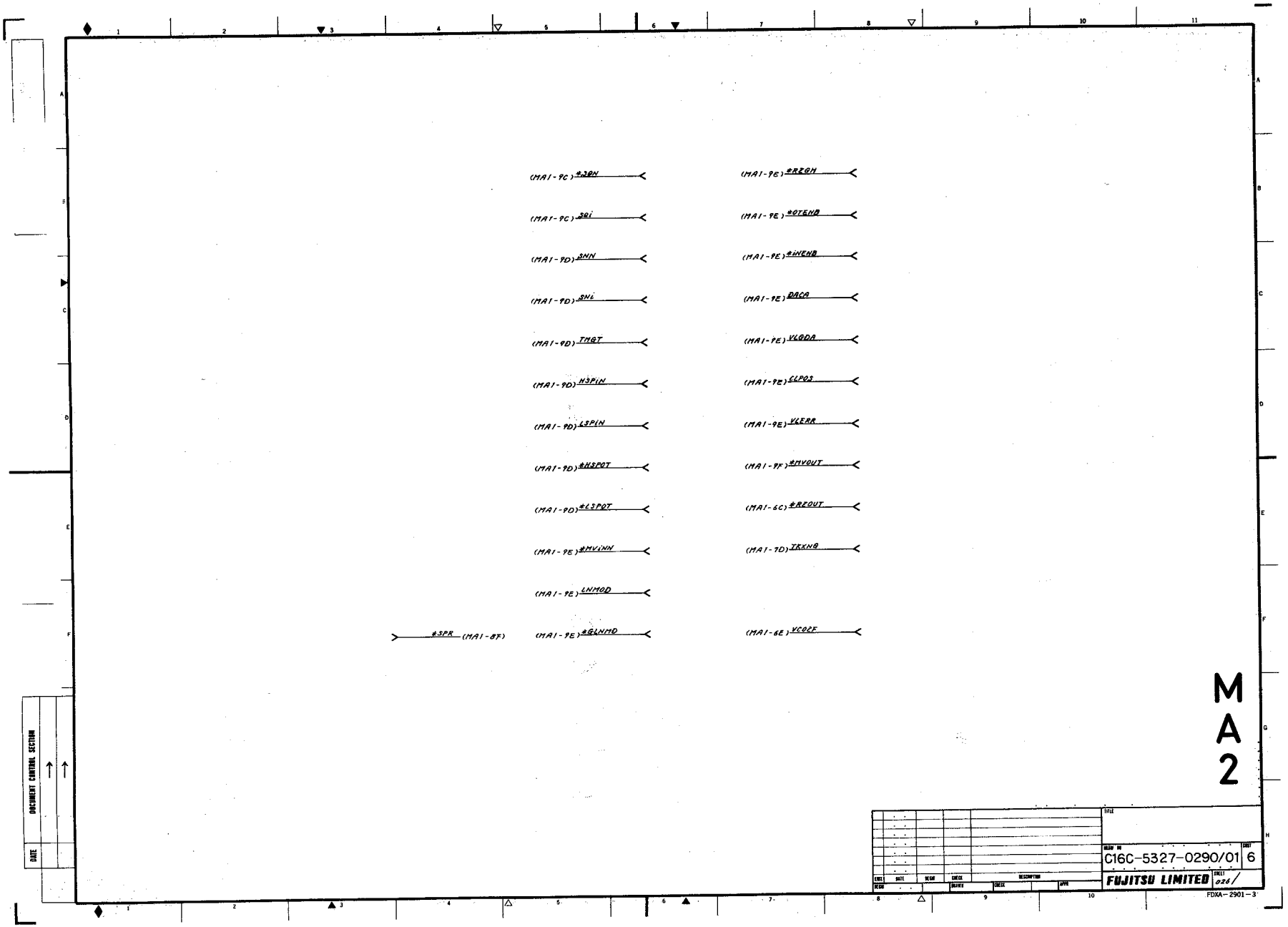
FUJITSU LIMITED
SHEET
035/
FDXA-2901-3


(MA1-9C) *3BN
(MA1-9C) SRi
(MA1-9D) SNN
(MA1-9D) SNi
(MA1-9D) TMGT
(MA1-9D) H3PiN
(MA1-9D) L3PiN
(MA1-9D) *H3POT
(MA1-9D) *L3POT
(MA1-9E) *MViNN
(MA1-9E) LNMOD
*SPR (MA1-8F)
(MA1-9E) *GLNMD
(MA1-9E) *RZGM
(MA1-9E) *OTENB
(MA1-9E) *INENB
(MA1-9E) DACA
(MA1-9E) VLGDA
(MA1-9E) CLPOS
(MA1-9E) VLERR
(MA1-9F) *MVOUT
(MA1-6C) *RZOUT
(MA1-7D) IKKNG
(MA1-6E) VCOZF
DOCUMENT CONTROL SECTION
DATE
M
A
2
C16C-5327-0290/01
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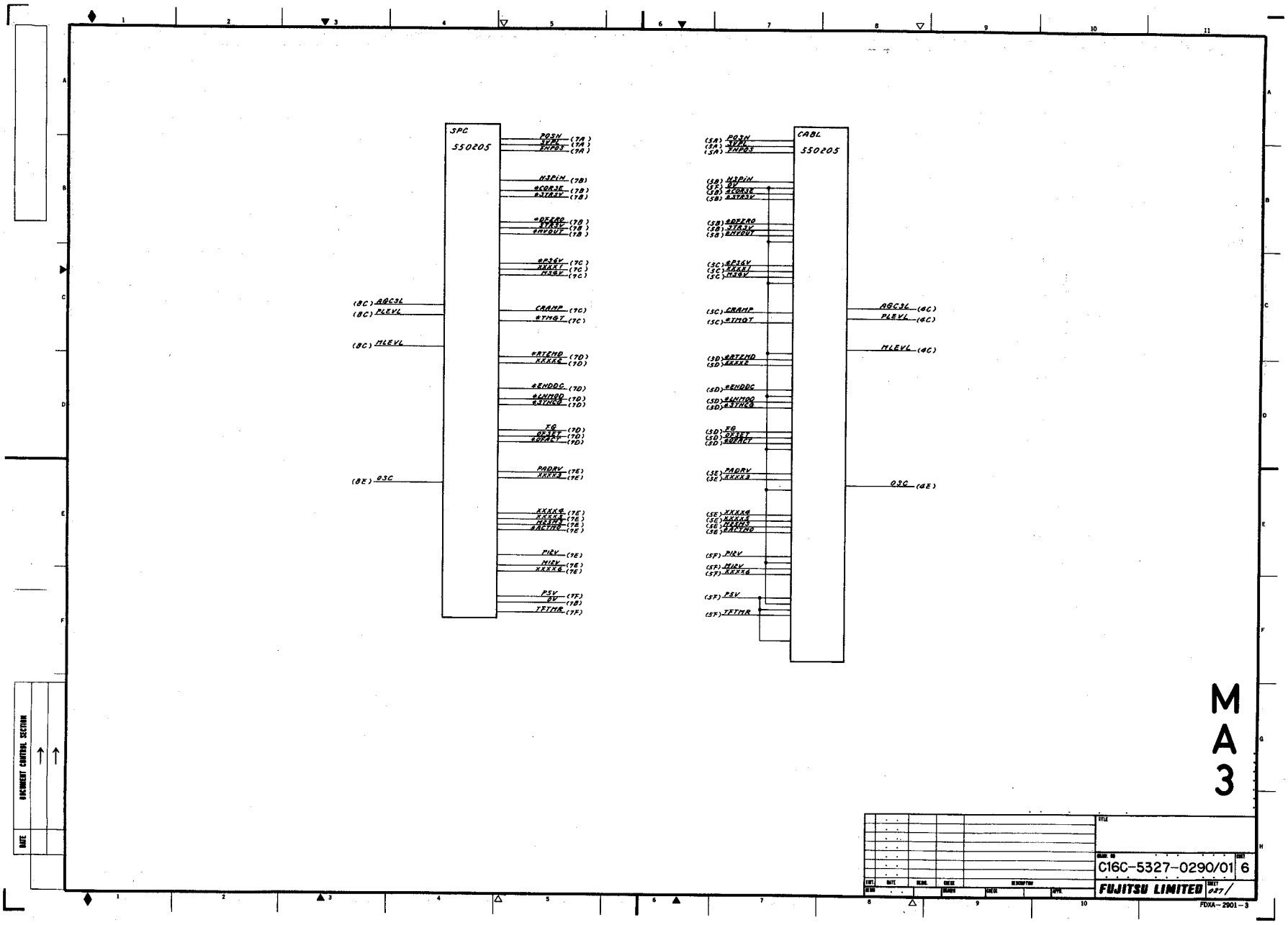
FUJITSU LIMITED
026/
FDXA-2901-3


SPC
550205
POSN (7A)
SYNC (7A)
SYNDS (7A)
HSPIN (7B)
#CORSE (7B)
#STRSV (7B)
#DFERR (7B)
STRSV (7B)
#MFOUT (7B)
#PSEV (7C)
XXXXT (7C)
MSEV (7C)
(8C) AGC3L
(8C) PLEVL
CRAMP (7C)
#TMGT (7C)
(8C) MLEVL
#RTEND (7D)
XXXXR (7D)
#ENDDC (7D)
#LWMOD (7D)
#STMCR (7D)
FG (7D)
OFSET (7D)
#DFACT (7D)
(8E) OSC
PADRV (7E)
XXXXB (7E)
XXXXX (7E)
XXXXX (7E)
XXXXX (7E)
#ACTIND (7E)
PIEV (7E)
MIEV (7E)
XXXXG (7E)
PSV (7E)
DV (7B)
TFTMR (7F)
CABL
550205
(5A) POSN
(5A) SYNC
(5A) SYNDS
(5B) HSPIN
(5B) #CORSE
(5B) #STRSV
(5B) #DFERR
(5B) STRSV
(5B) #MFOUT
(5C) #PSEV
(5C) XXXXT
(5C) MSEV
(5C) CRAMP
(5C) #TMGT
(5D) #RTEND
(5D) XXXXR
(5D) #ENDDC
(5D) #LWMOD
(5D) #STMCR
(5D) FG
(5D) OFSET
(5D) #DFACT
(5E) PADRV
(5E) XXXXB
(5E) XXXXX
(5E) XXXXX
(5E) XXXXX
(5E) #ACTIND
(5F) PIEV
(5F) MIEV
(5F) XXXXG
(5F) PSV
(5F) TFTMR
AGC3L (4C)
PLEVL (4C)
MLEVL (4C)
OSC (4E)
MA3
C16C-5327-0290/01
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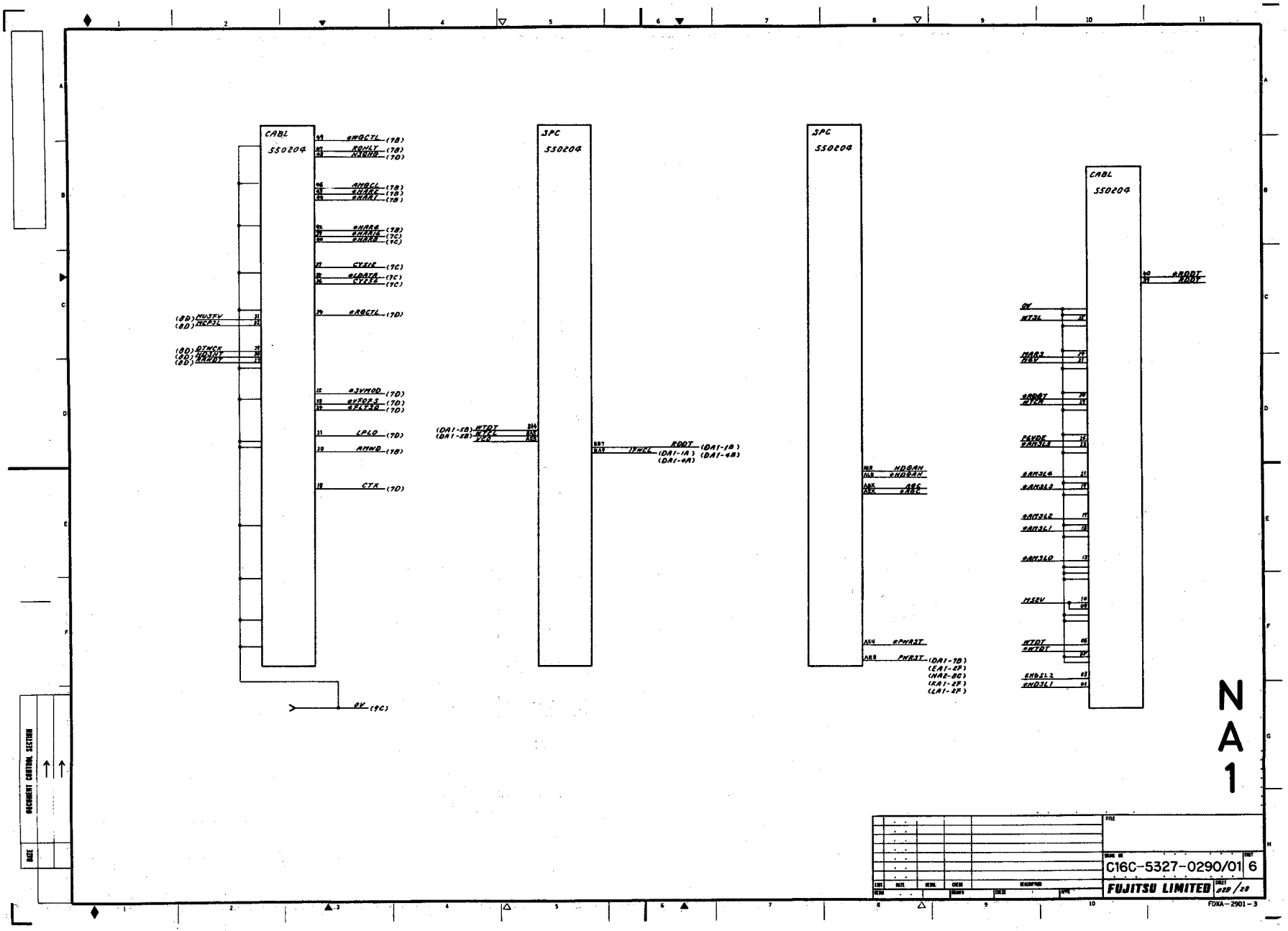
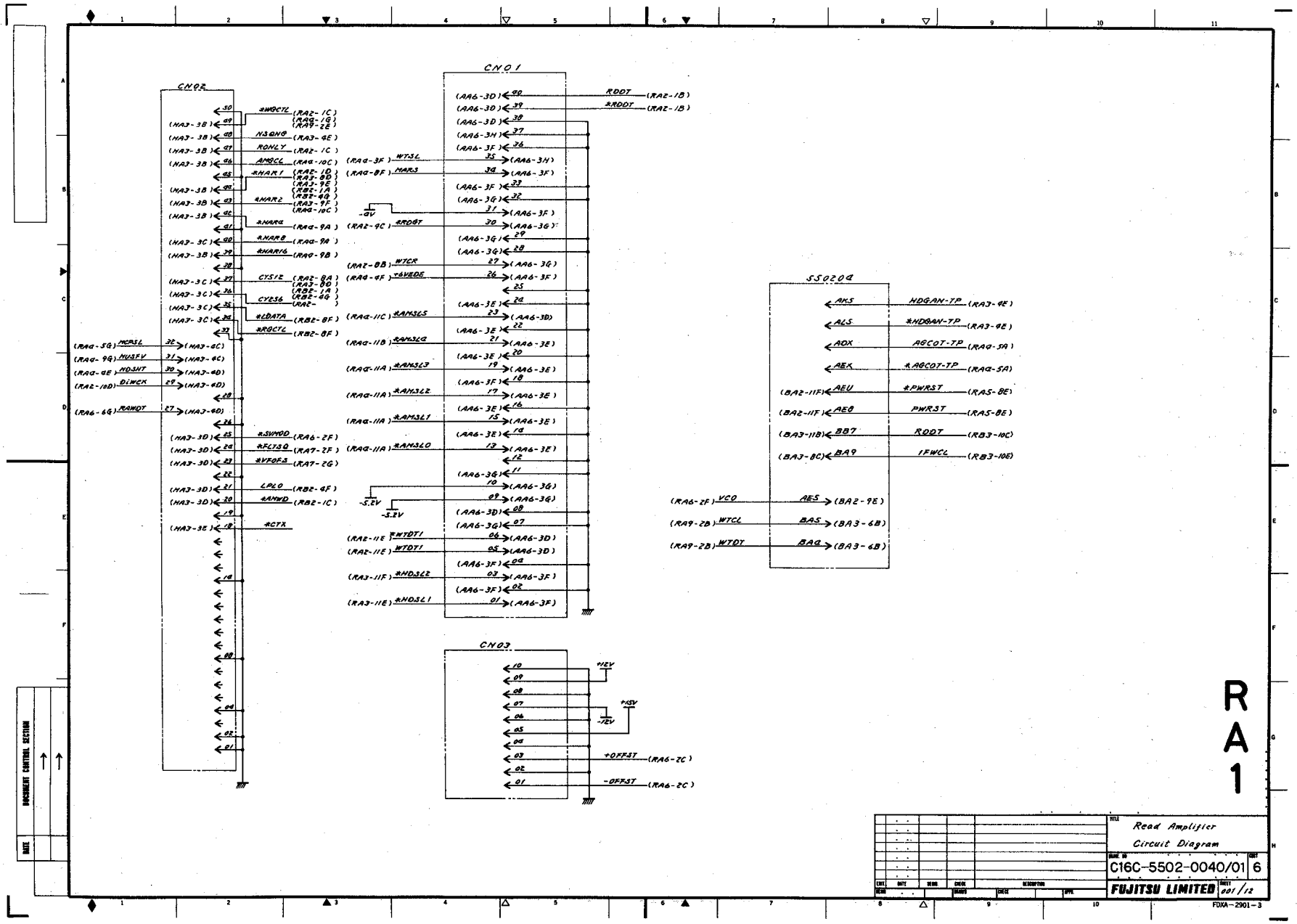
FUJITSU LIMITED
FDXA-2901-3


CABL
550204
SPC
550204
SPC
550204
CABL
550204
NA1
C16C-5327-0290/01 6
FUJITSU LIMITED
FDXA-2901-3


CN02
CN01
CN03
SS0204
*WGCTL
NSGNG
RONLY
AMGCL
*HAR1
*HAR2
*HARA
*HARB
*HARIG
CYS12
CY256
*LDATA
*RGCTL
*SWHOD
*FCTSG
*VFOFS
LPLO
*ANWD
*CTX
MCRSL
HUSFV
HDSHT
DIWCK
RAWDT
WTSL
MARS
*RDGT
WTCR
+6VEDE
*AMSLC
*AMSL3
*AMSL2
*AMSL1
*AMSLO
*WTDT1
WTDT1
*HDSL2
*HDSL1
RDDT
*RDDT
+12V
+5V
-7.2V
+OFFST
-OFFST
-6V
-5.2V
AMS
ALS
AOX
AEX
AEU
AE0
BB7
BA9
*HDGAN-TP
*HDGAN-TP
AGCOT-TP
*AGCOT-TP
*PWRST
PWRST
RDDT
IFWCL
VCO
WTCL
WTDT
AES
BAS
BAQ
RA1
Read Amplifier
Circuit Diagram
C16C-5502-0040/01
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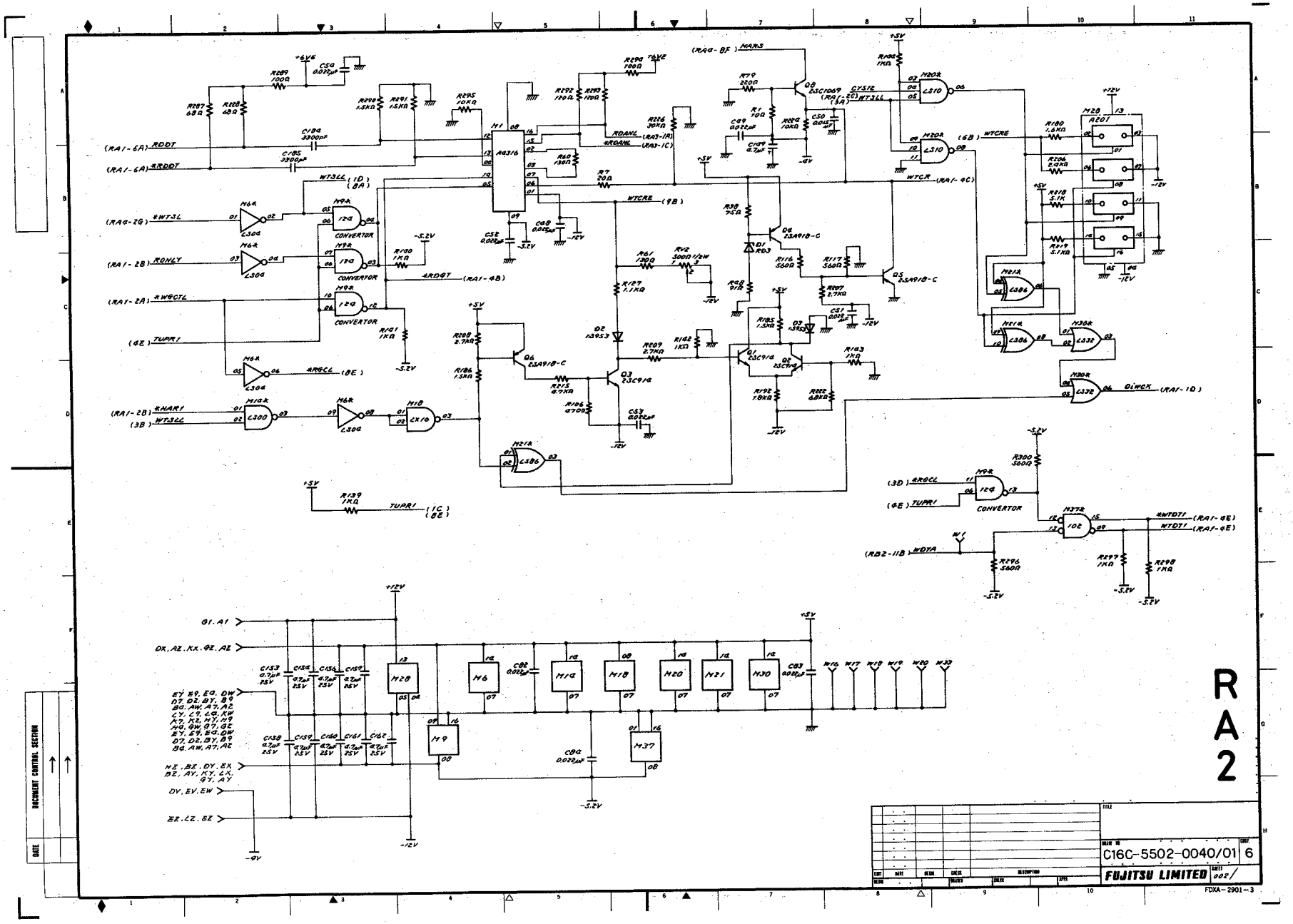
FUJITSU LIMITED
001/12
FDXA-2901-3
DOCUMENT CONTROL SECTION


RA2
C16C-5502-0040/01
FUJITSU LIMITED
FDXA-2901-3
DOCUMENT CONTROL SECTION
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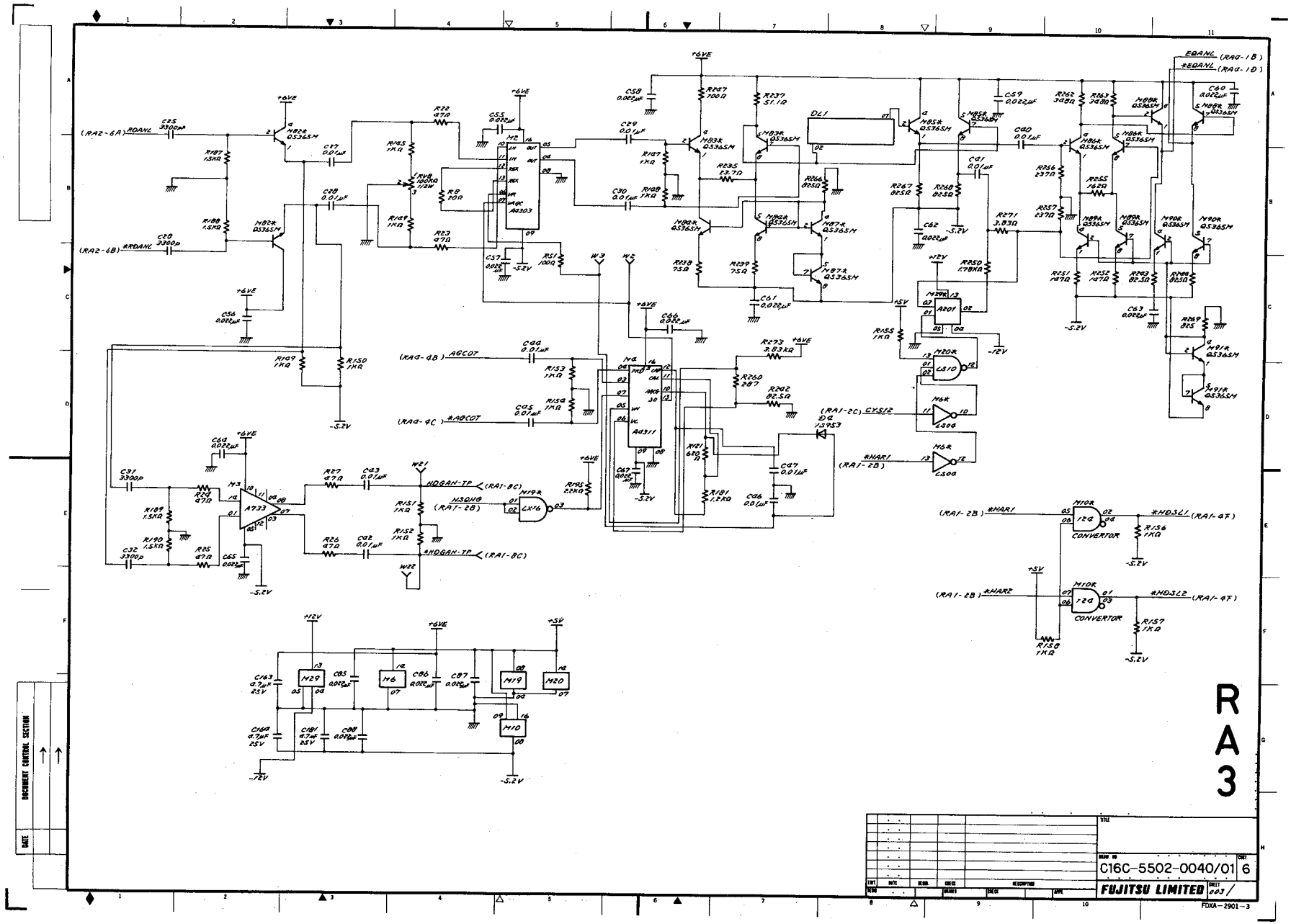
RA3
C16C-5502-0040/01
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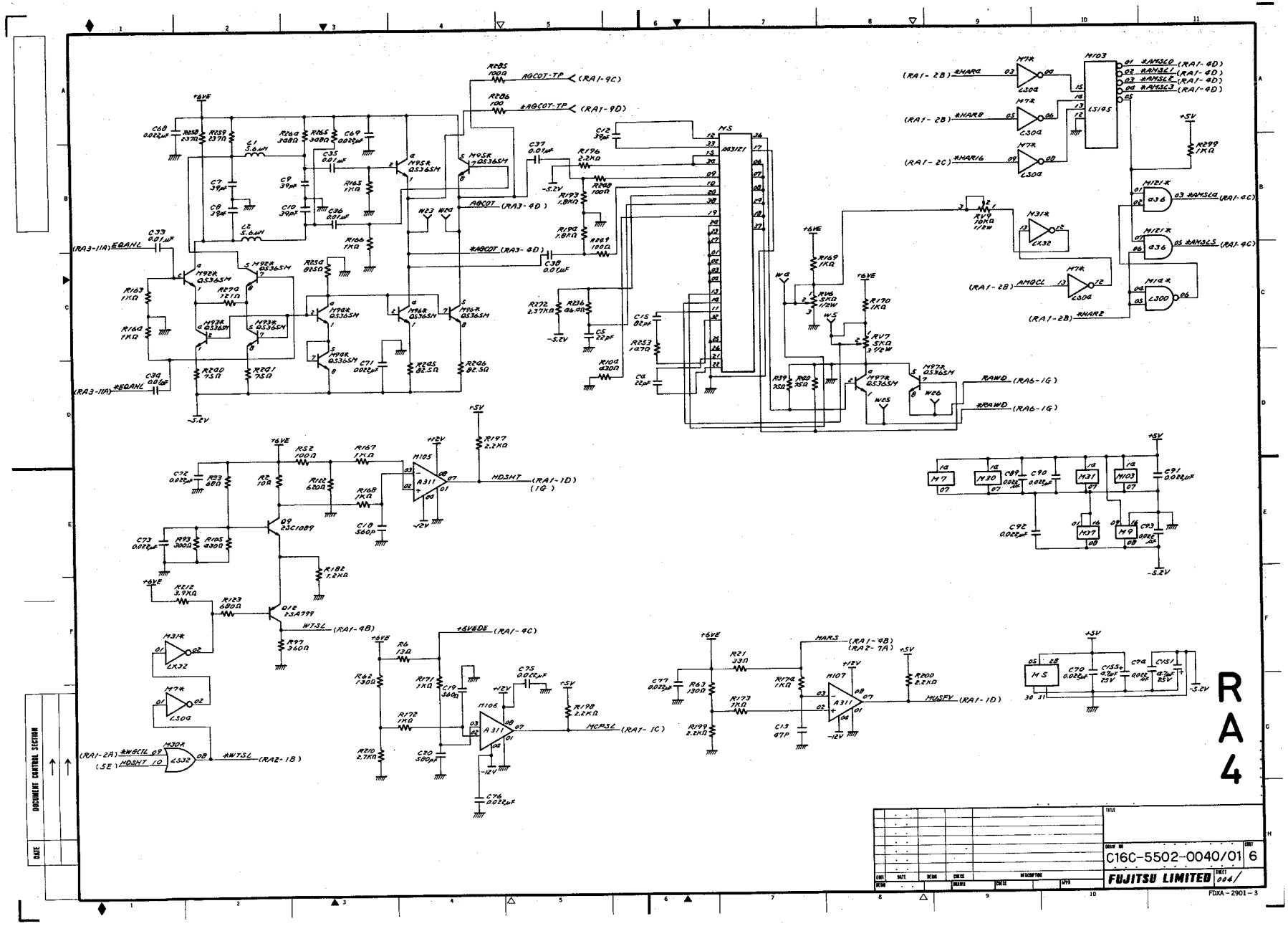
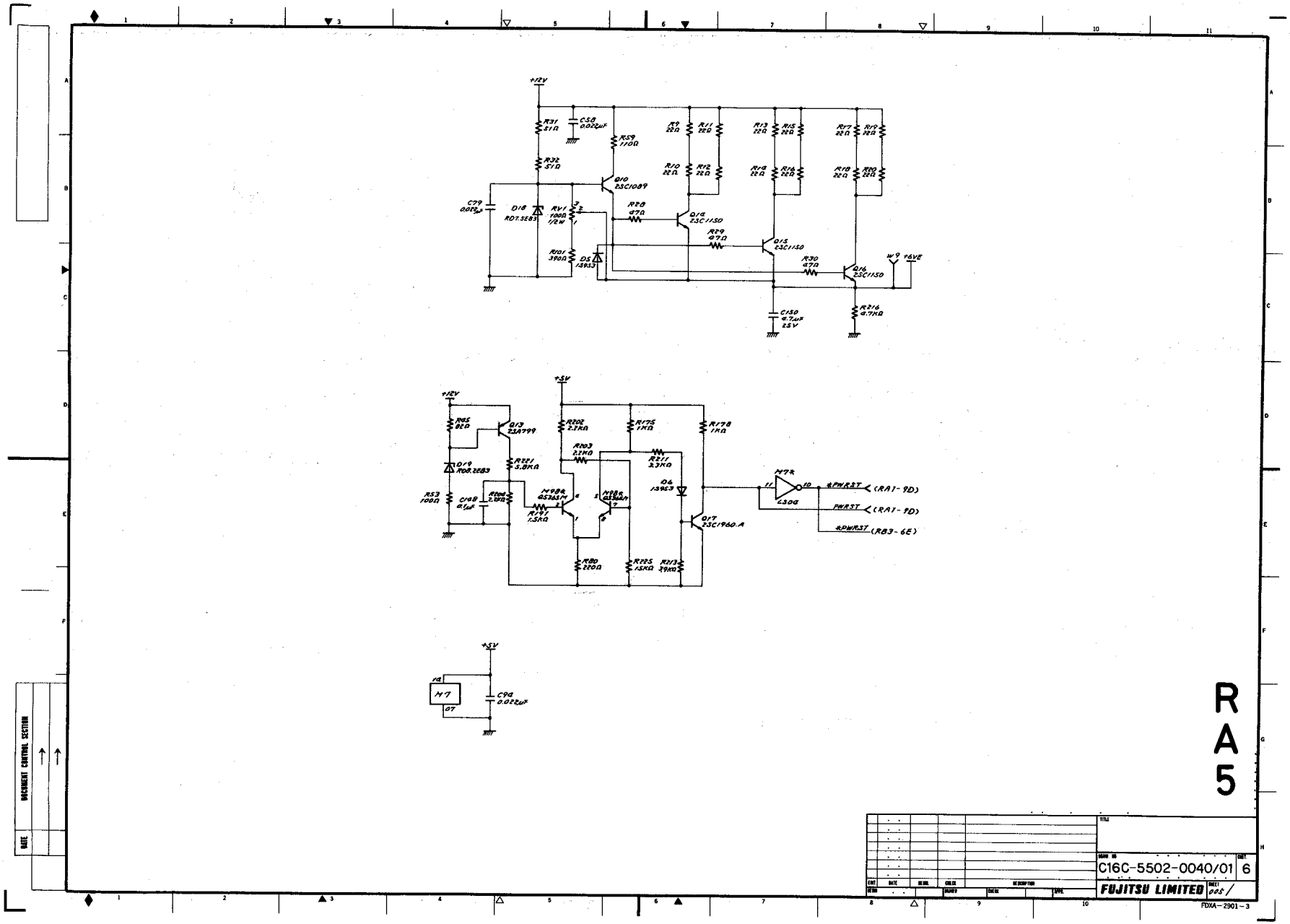
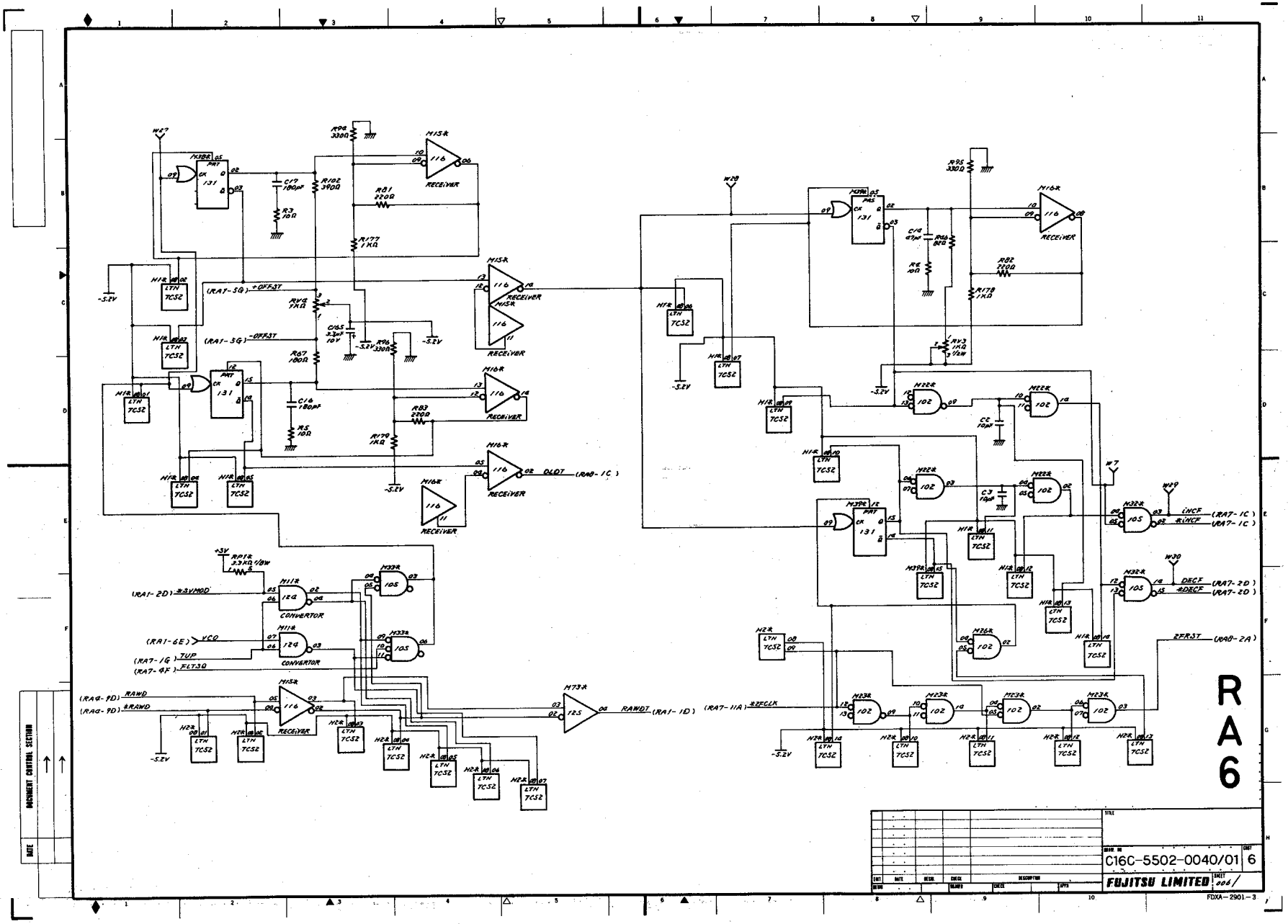
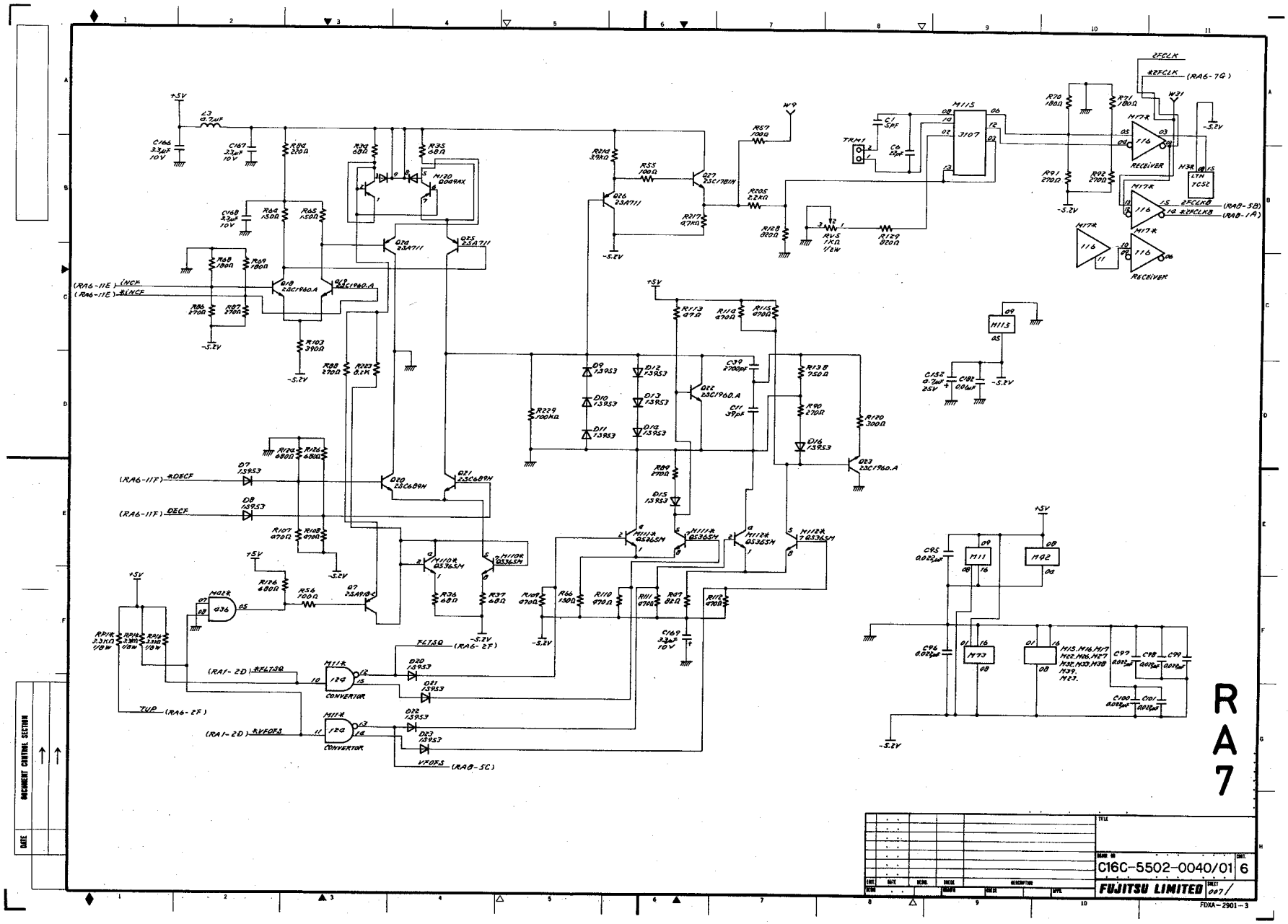
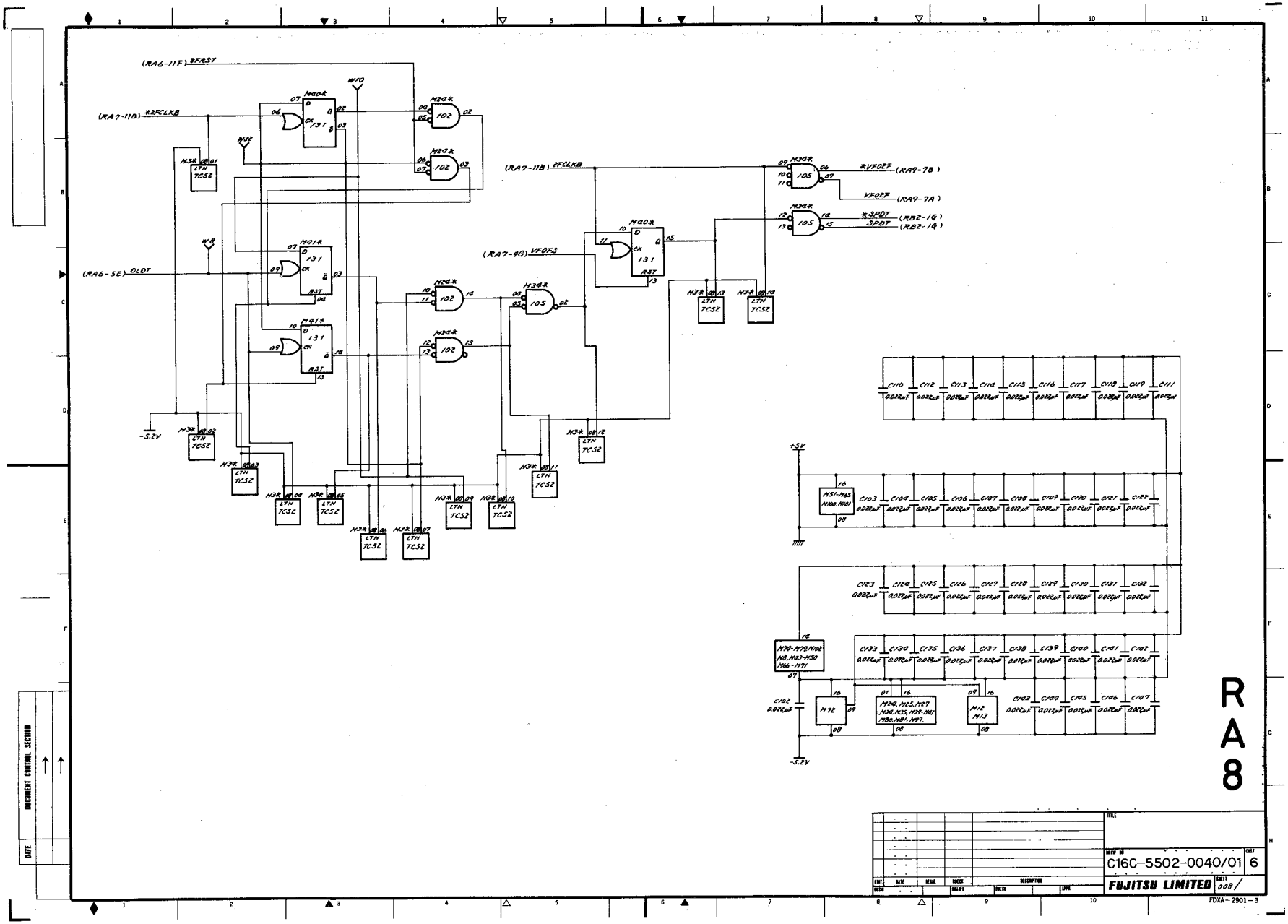
FUJITSU LIMITED
FDXA-2901-3
DOCUMENT CONTROL SECTION
DATE
CONVERTOR
CONVERTOR

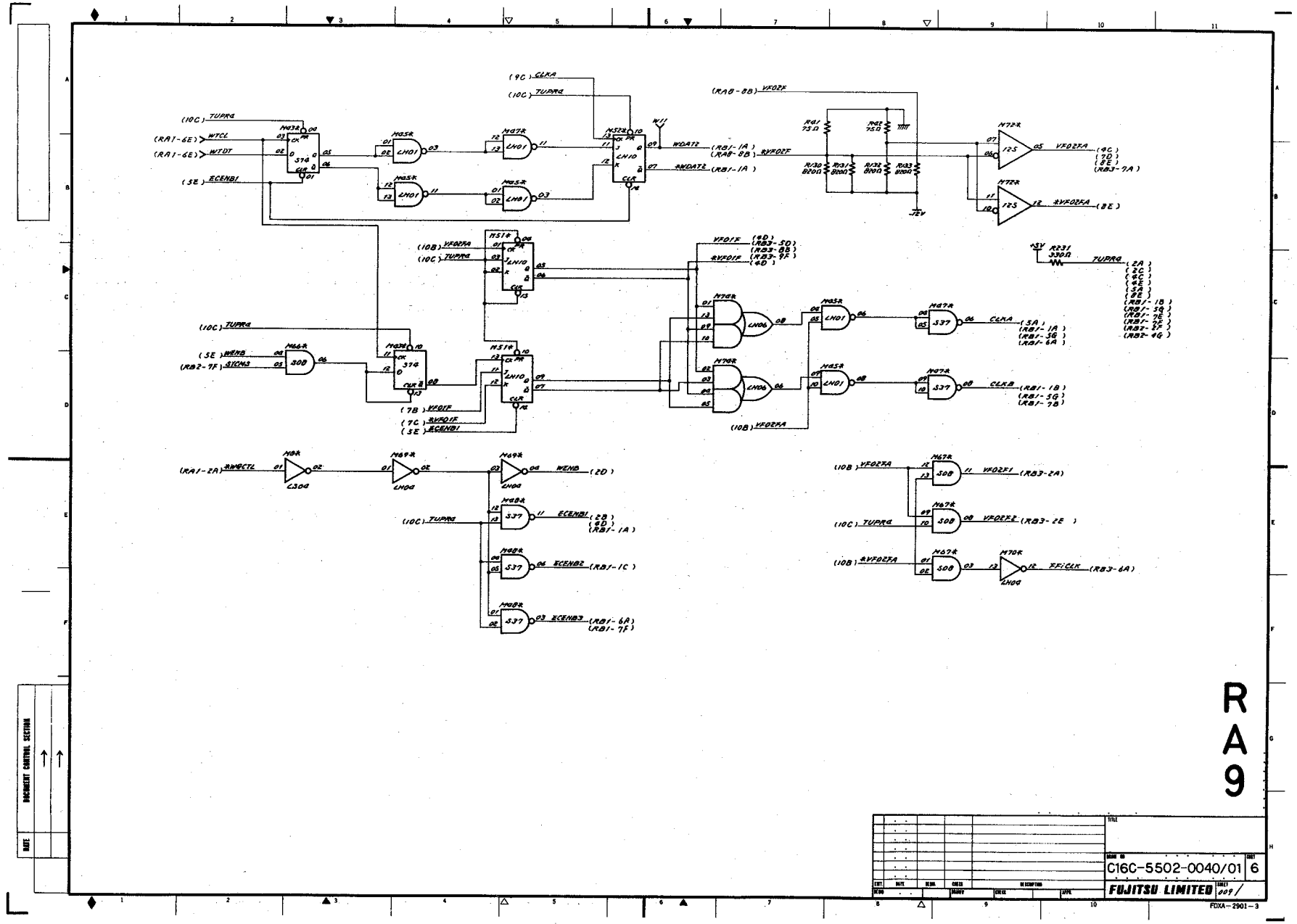

AGCOT-TP (RA1-9C)
*AGCOT-TP (RA1-9D)
AGCOT (RA3-4D)
*AGCOT (RA3-4D)
(RA3-11A) EQANL
(RA3-11A) *EQANL
RAWD (RA6-1G)
*RAWD (RA6-1G)
MDSHT (RA1-1D) (1G)
WTSL (RA1-4B)
*WTSL (RA2-1B)
(RA1-2A) *WGCTL
(SE) MDSHT
+6VEDE (RA1-4C)
MCPSL (RA1-1C)
MARS (RA1-4B) (RA2-7A)
MUSFV (RA1-1D)
(RA1-2B) *HAR4
(RA1-2B) *HAR8
(RA1-2C) *HAR16
*AMSC0 (RA1-4D)
*AMSC1 (RA1-4D)
*AMSC2 (RA1-4D)
*AMSC3 (RA1-4D)
*AMSC4 (RA1-4C)
*AMSC5 (RA1-4C)
AMSC1 (RA1-2B)
*HAR2 (RA1-2B)
+6VE
+5V
+12V
-12V
-5.2V
RA4
C16C-5502-0040/01
FUJITSU LIMITED
FDXA-2901-3
DOCUMENT CONTROL SECTION
DATE


+12V
R31 51Ω
C58 0.022μF
R59 110Ω
R32 51Ω
Q10 2SC1089
C79 0.022μF
D18 RD7.5EB3
RV1 100Ω 1/2W
R28 47Ω
Q14 2SC1150
R29 47Ω
Q15 2SC1150
R30 47Ω
Q16 2SC1150
W9 +6VE
R101 390Ω
D5 1S953
C150 47μF 25V
R216 47KΩ
R9 22Ω
R11 22Ω
R13 22Ω
R15 22Ω
R17 22Ω
R19 22Ω
R10 22Ω
R12 22Ω
R14 22Ω
R16 22Ω
R18 22Ω
R20 22Ω
+5V
+12V
R65 0Ω
Q13 2SA799
D19 RD8.2EB3
R201 5.8KΩ
R53 100Ω
C148 47μF
R64 2.2KΩ
M98R 65363FP
R171 1.5KΩ
R202 2.2KΩ
R203 2.2KΩ
R175 1KΩ
R178 1KΩ
R211 3.3KΩ
D4 1S953
M77R
LS04
Q17 2SC1960-A
R180 220Ω
R225 1.5KΩ
R213 39KΩ
*PWRST (RA1-9D)
PWRST (RA1-9D)
*PWRST (RB3-6E)
+5V
M7
C94 0.022μF
RA5
C16C-5502-0040/01 6
FUJITSU LIMITED
FDXA-2901-3
DOCUMENT CONTROL SECTION
NOTE


RECEIVER
CONVERTOR
(RA1-2D) *SVMOD
(RA1-6E) VCO
(RA7-1G) TUP
(RA7-9F) FLT3Q
(RA9-9D) RAWD
(RA9-9D) *RAWD
RAWDT (RA1-1D)
(RA1-5G) +OFFST
(RA1-5G) -OFFST
DLDT (RA0-1C)
(RA7-11A) *ZFCLK
LNCF (RA7-1C) (RA7-1C)
DECF (RA7-2D) (RA7-2D)
ZFRST (RA9-2A)
-5.2V
+5V
R A 6
C16C-5502-0040/01 6
FUJITSU LIMITED
FDXA-2901-3


RA7
C16C-5502-0040/01
FUJITSU LIMITED
FDXA-2901-3
DOCUMENT CONTROL SECTION
DATE
(RA6-11E) LINCK
(RA6-11E) RLNCF
(RA6-11F) RDECF
(RA6-11F) DECF
(RA1-2D) RFLTSQ
(RA1-2D) RVEOFS
TUP (RA6-2F)
FLTSQ (RA6-2F)
VEOFS (RA8-5C)
2FCLK
R2FCLK (RA6-7G)
(RA8-5B)
(RA8-1A)
RECEIVER
CONVERTOR


(RA6-11F) *2FRST
(RA7-11B) *2FCLKB
(RA6-5E) DLDT
(RA7-9G) VFDFS
(RA7-11B) *2FCLKB
*VFD2F
(RA9-7B)
VFD2F
(RA9-7A)
*3PDT
(RB2-1G)
3PDT
(RB2-1G)
-5.2V
+5V
DOCUMENT CONTROL SECTION
DATE
RA8
C16C-5502-0040/01
6
FUJITSU LIMITED
FDXA-2901-3


R9
C16C-5502-0040/01
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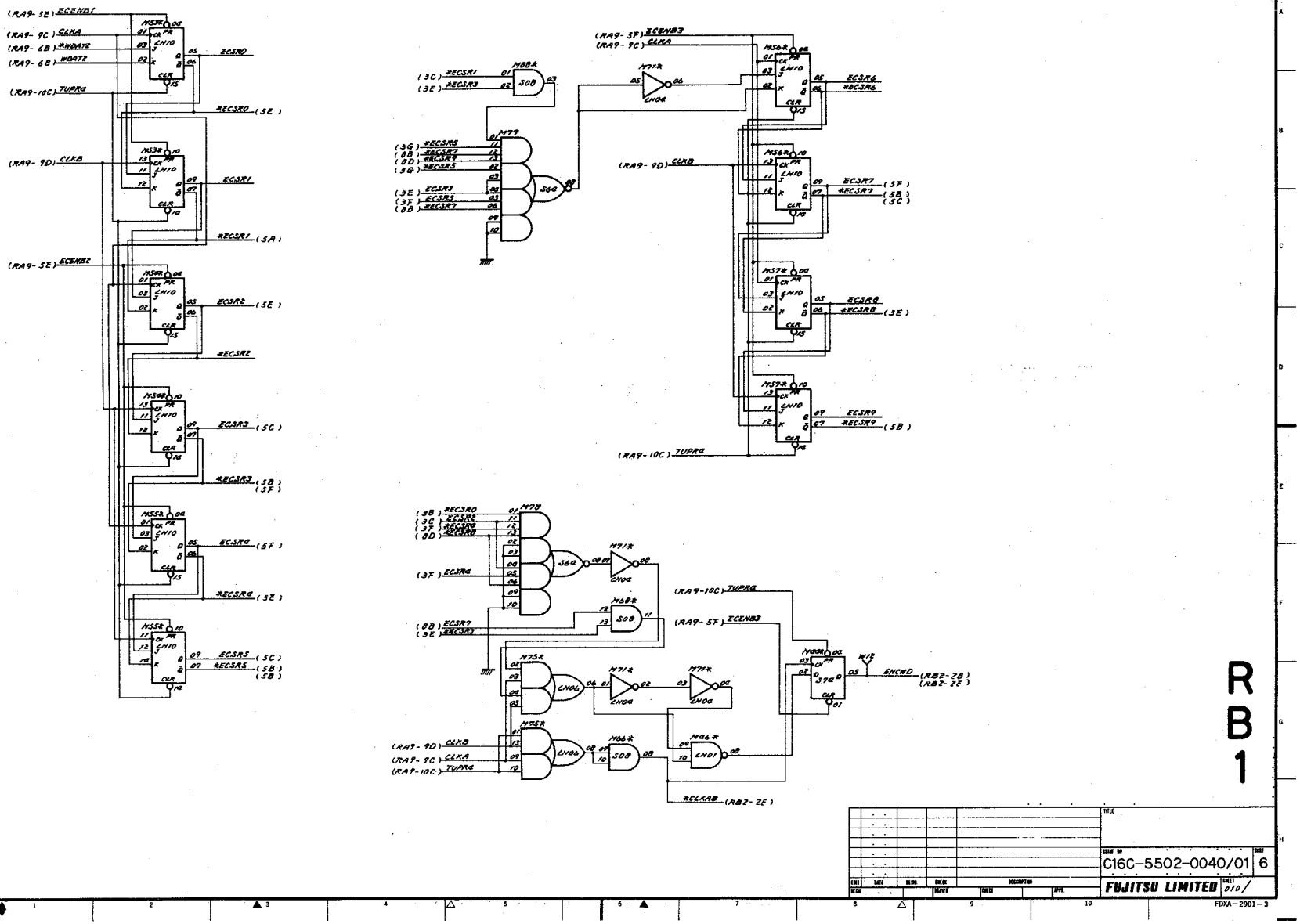
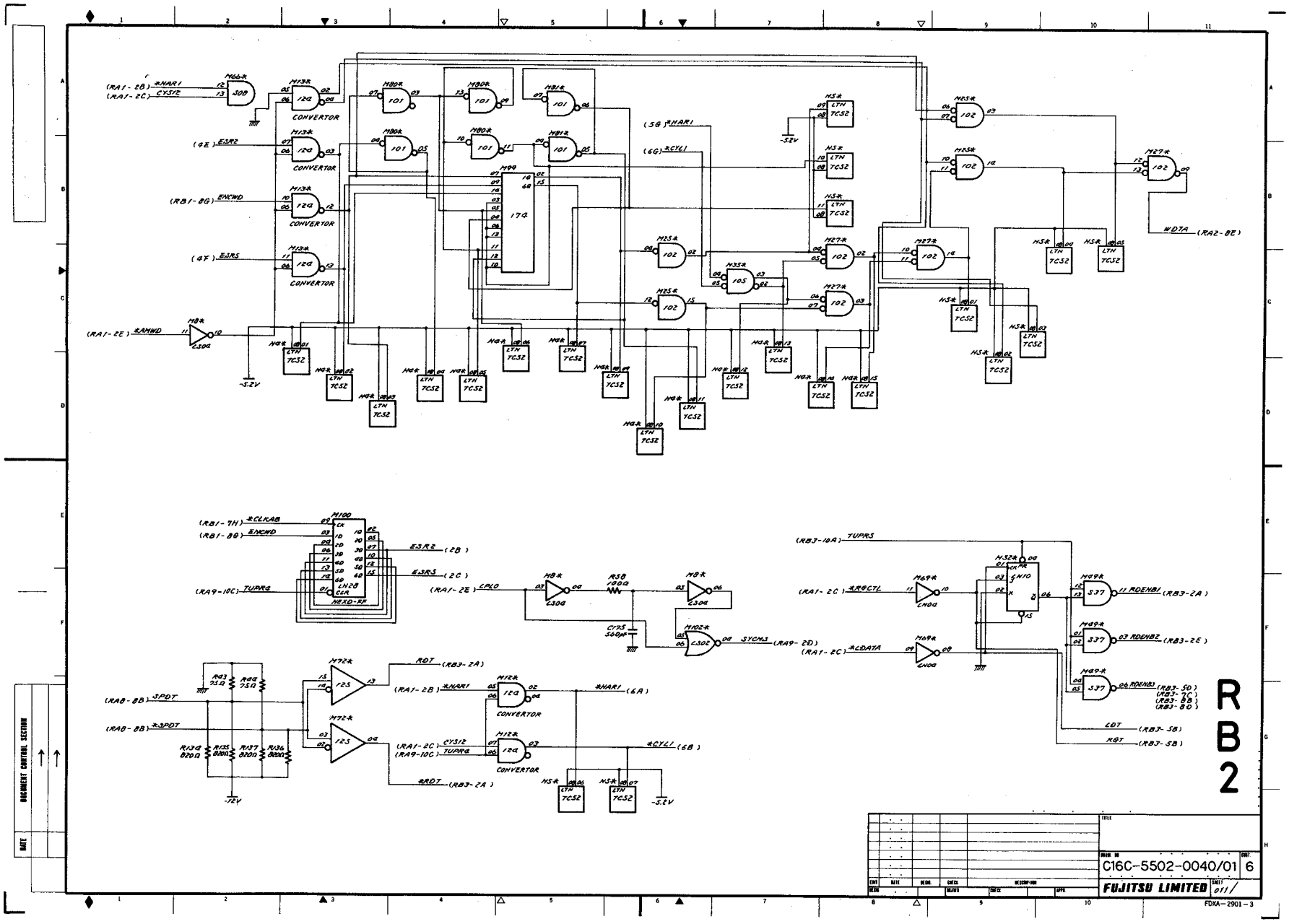
FUJITSU LIMITED
FDXA-2901-3


(RA9-5E) ECENB1
(RA9-9C) CLKA
(RA9-6B) *WDATZ
(RA9-6B) WDATZ
(RA9-10C) TUPRQ
(RA9-9D) CLKB
(RA9-5E) ECENB2
(RA9-5F) ECENB3
(RA9-9C) CLKA
(RA9-9D) CLKB
(RA9-10C) TUPRQ
ECSR0
ECSR1
ECSR2
ECSR3
ECSR4
ECSR5
ECSR6
ECSR7
RECSR0 (5E)
RECSR1 (5A)
RECSR2
RECSR3 (5B) (5F)
RECSR4 (5E)
RECSR5 (5C) (5B) (5B)
RECSR6
RECSR7 (5F) (5B) (5C)
RECSR9 (5B)
RECSR9 (3E)
(3C) RECSR1
(3E) RECSR3
(3G) RECSR5
(8B) RECSR7
(9D) RECSR9
(3E) ECSR3
(3F) ECSR5
(8B) ECSR7
(3B) RECSR0
(3C) RECSR2
(3F) RECSR4
(8D) RECSR8
(3F) ECSR4
(8B) ECSR7
(3E) RECSR3
(RA9-10C) TUPRQ
(RA9-5F) ECENB3
ENCWD (RB2-2B) (RB2-2E)
(RA9-9D) CLKB
(RA9-9C) CLKA
(RA9-10C) TUPRQ
RCLKAB (RB2-2E)
RB1
C16C-5502-0040/01 6
FUJITSU LIMITED
FDXA-2901-3
DOCUMENT CONTROL SECTION
DATE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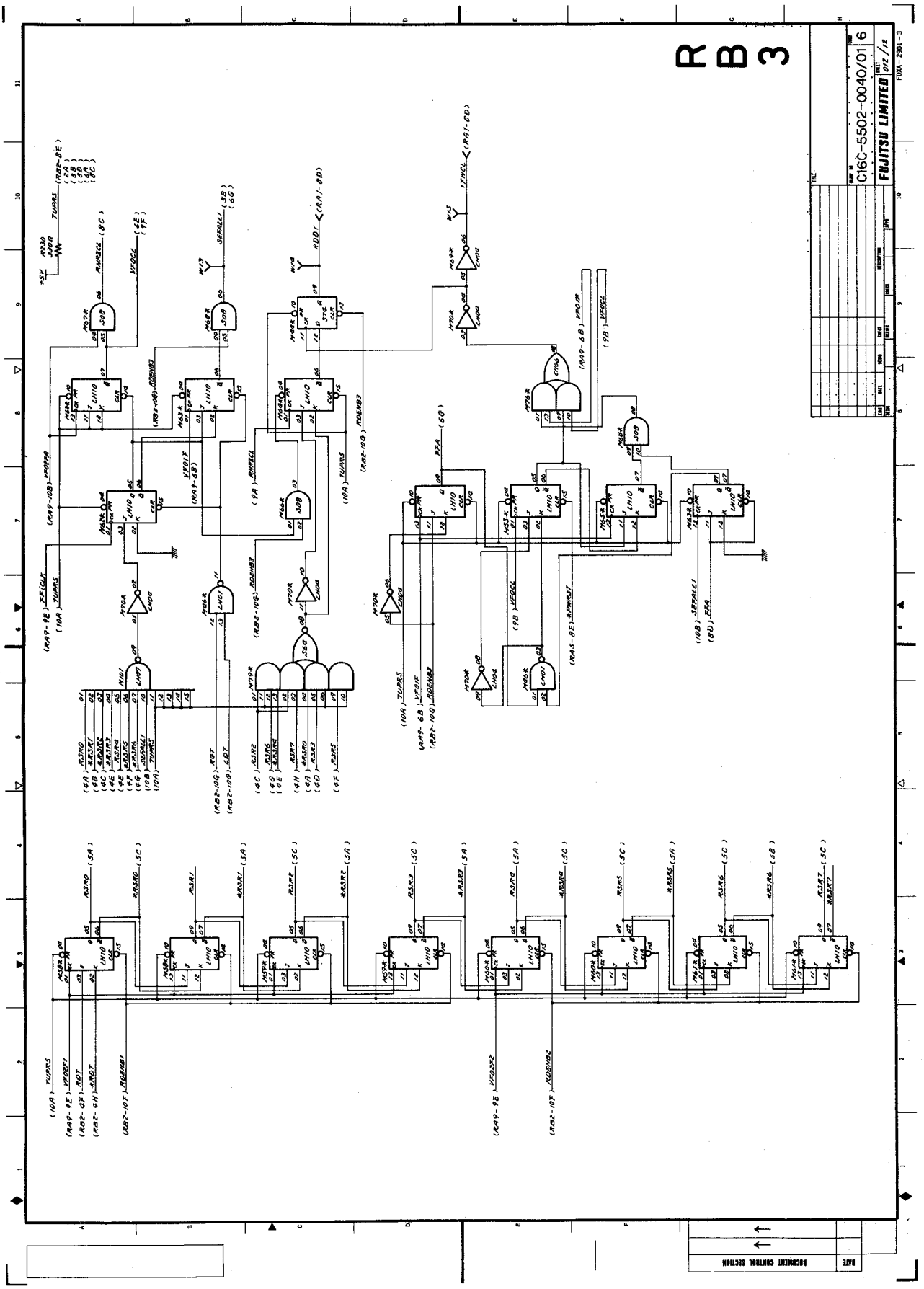
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FUJITSU LIMITED

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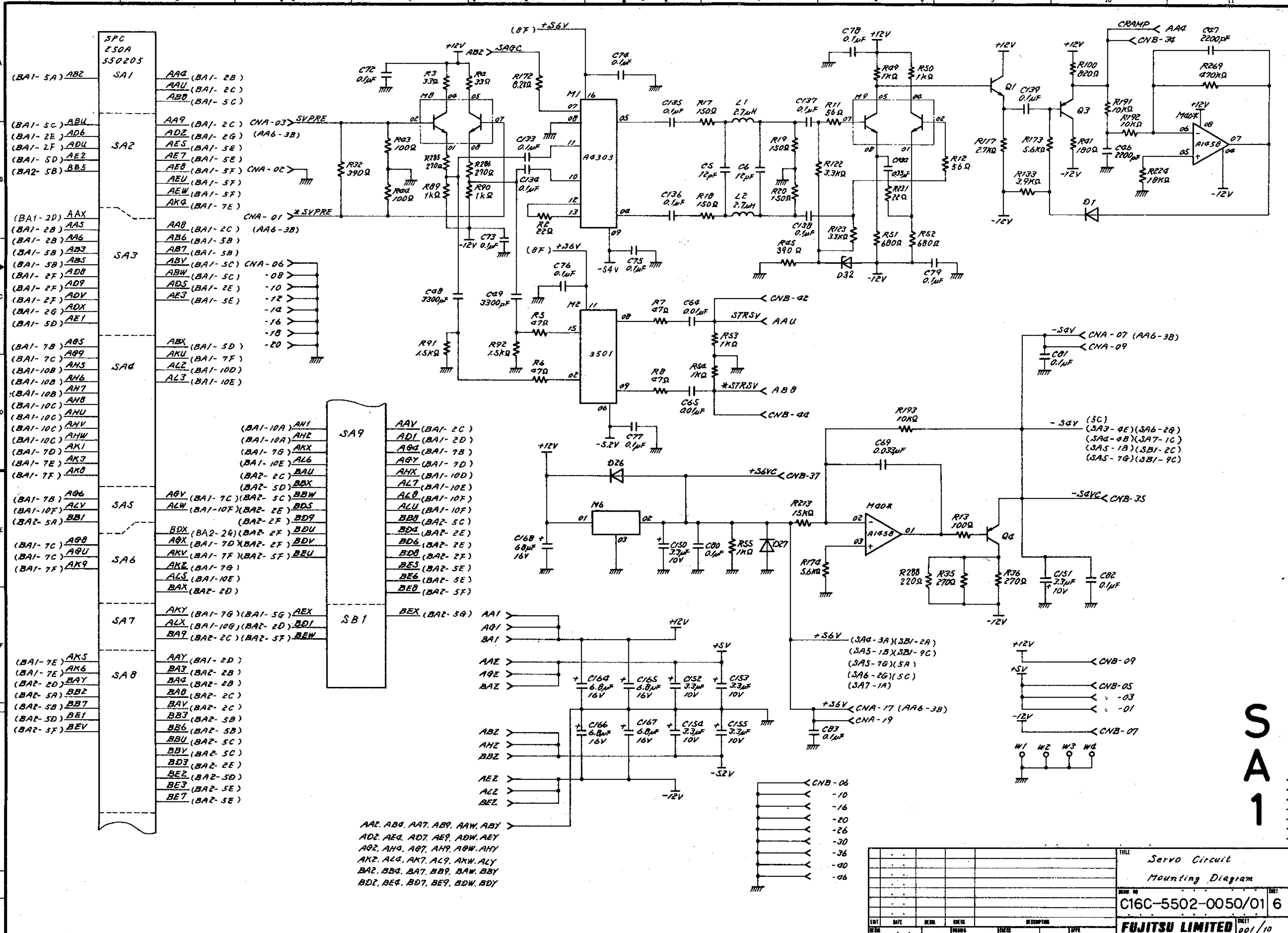

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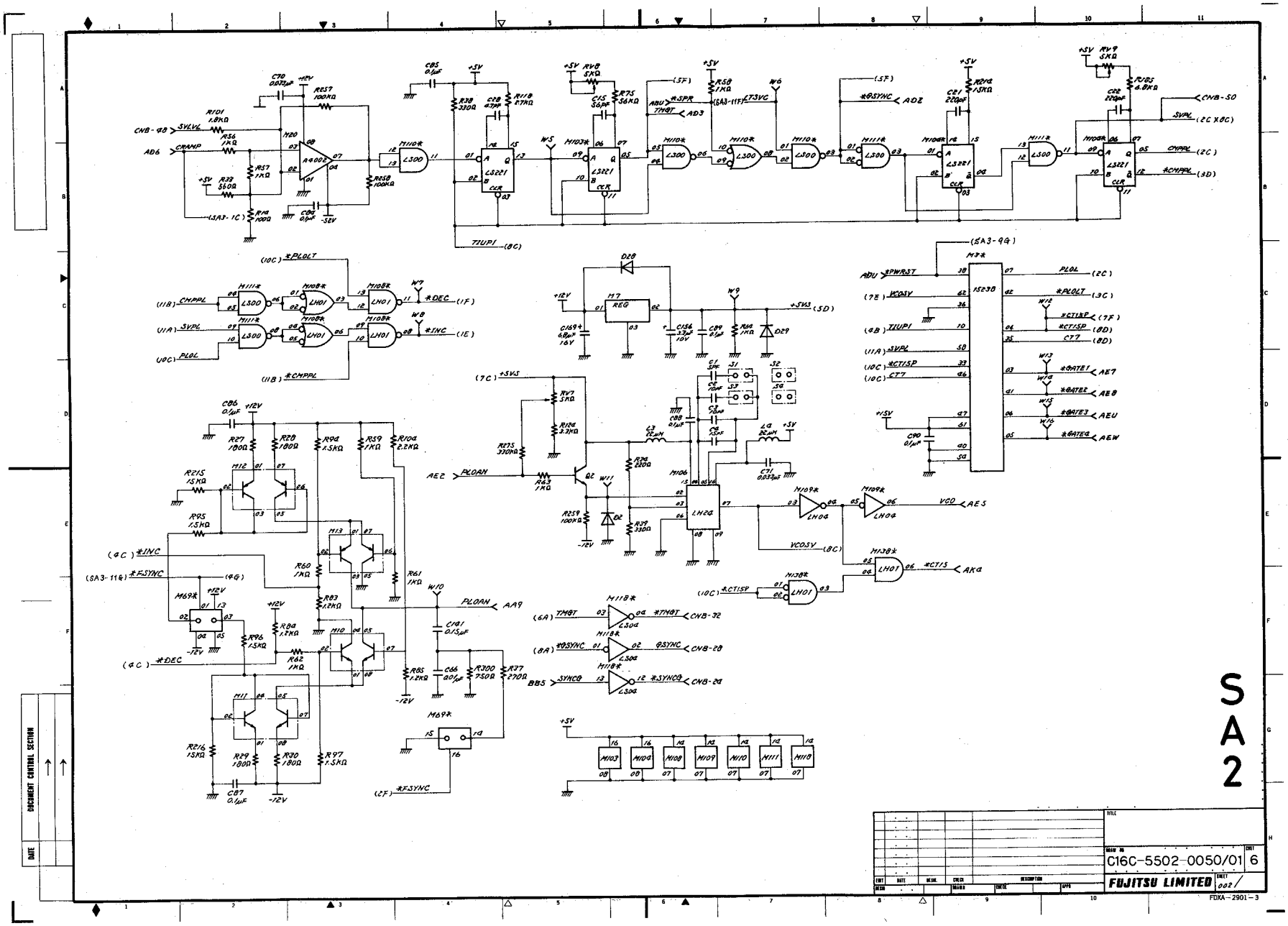
DRAW. NO. C16C-5502-0050/01 | 6

FUJITSU LIMITED | SHEET 001/10

FDXA-2901-3


SA2
FUJITSU LIMITED
C16C-5502-0050/01
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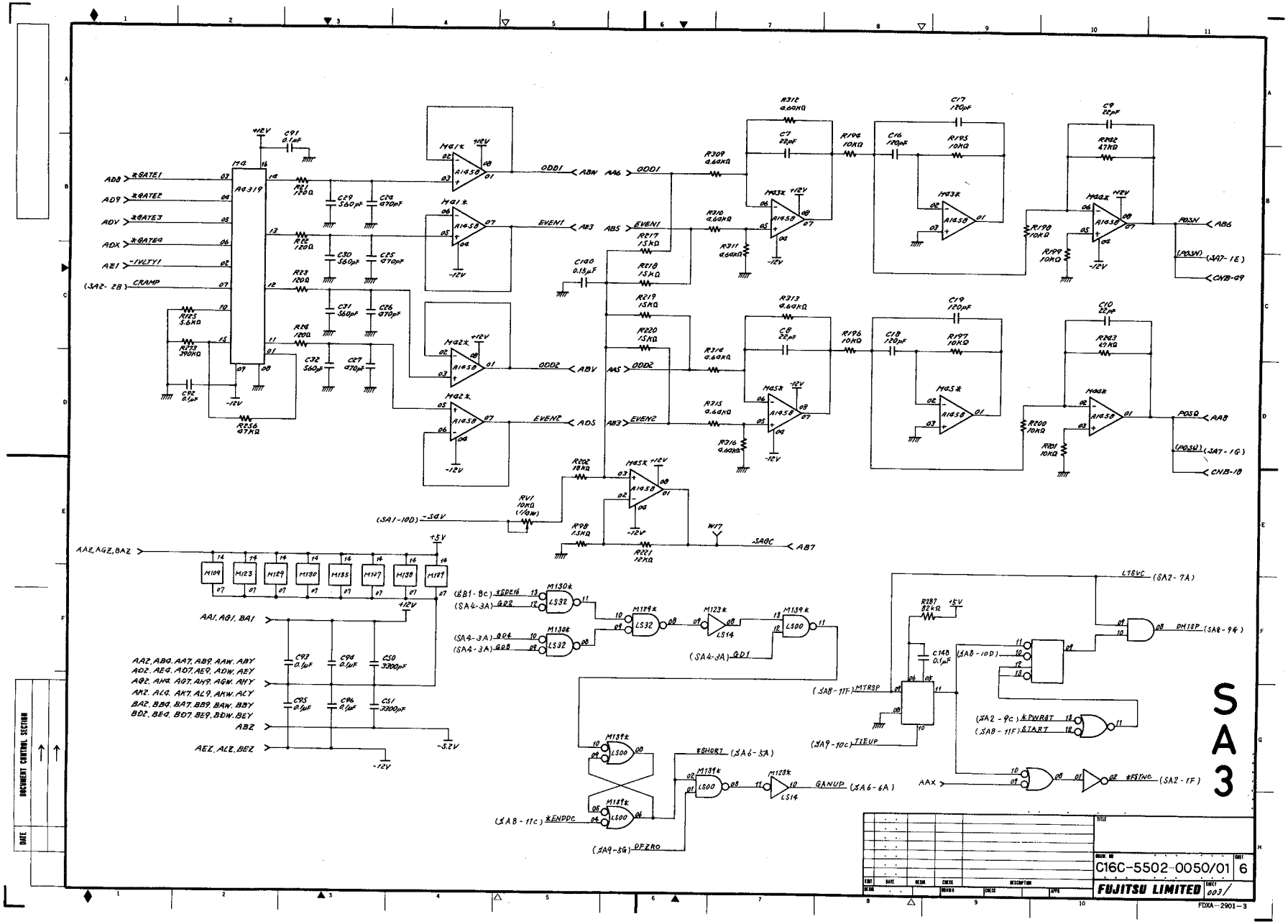
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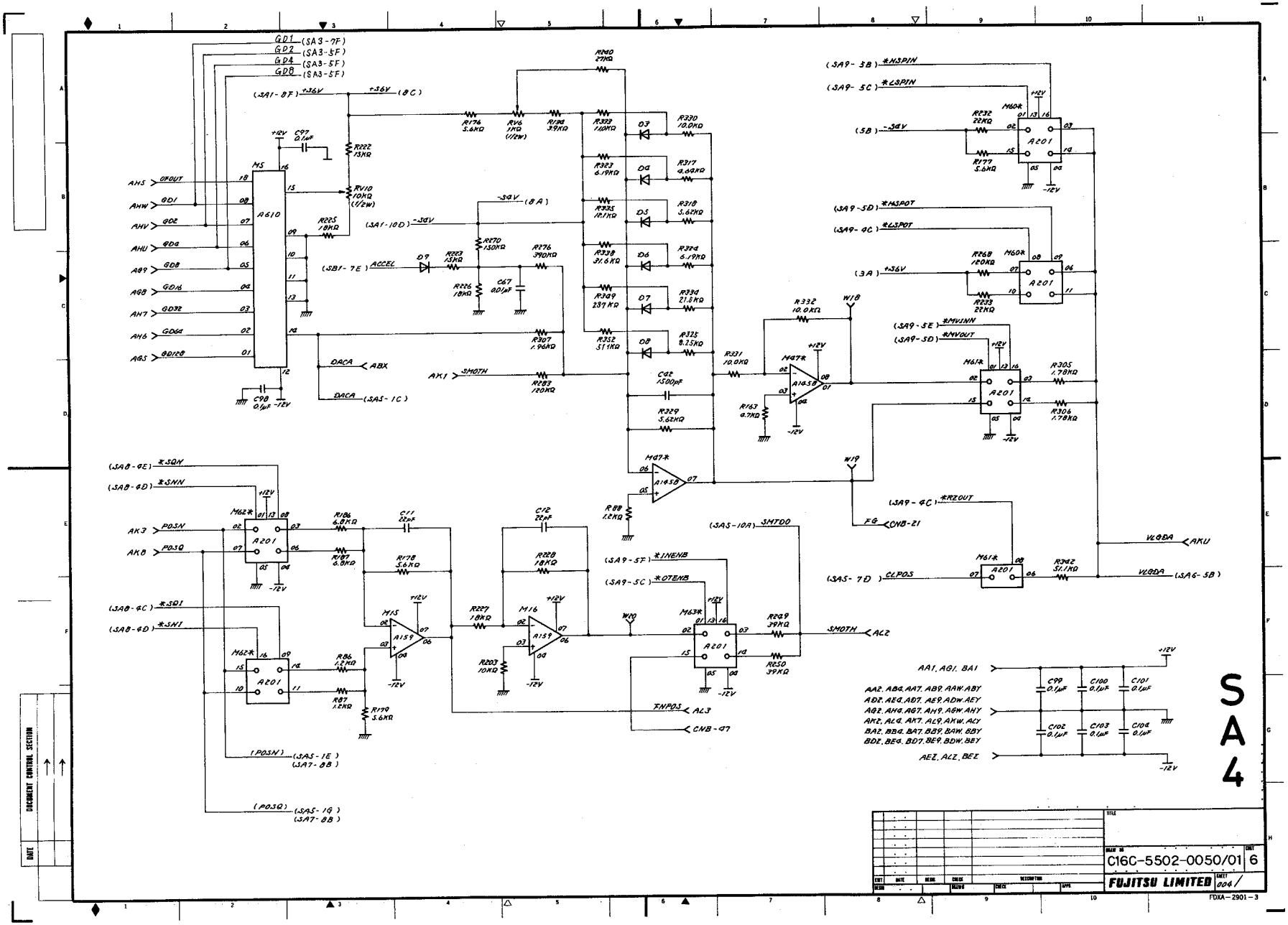
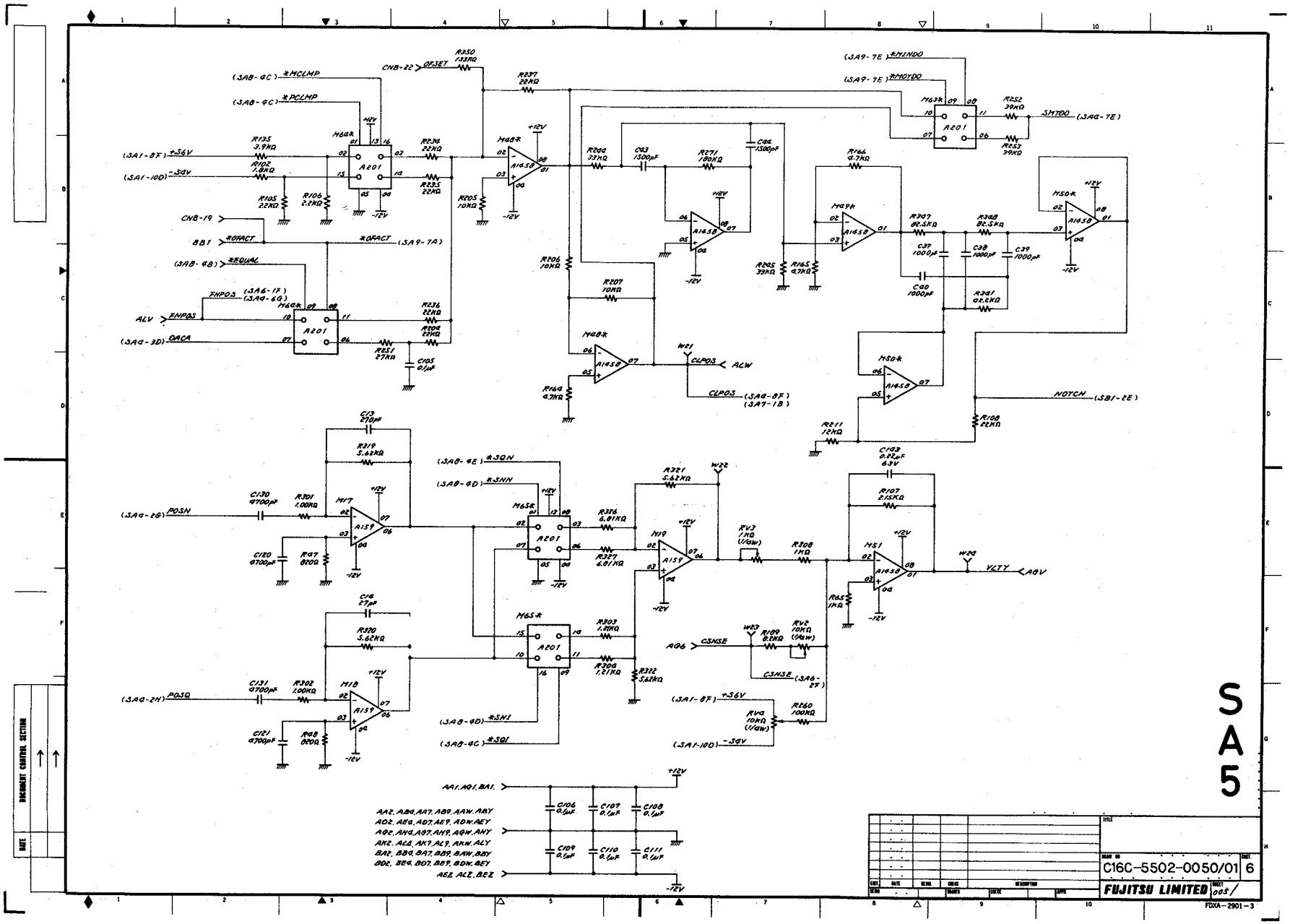
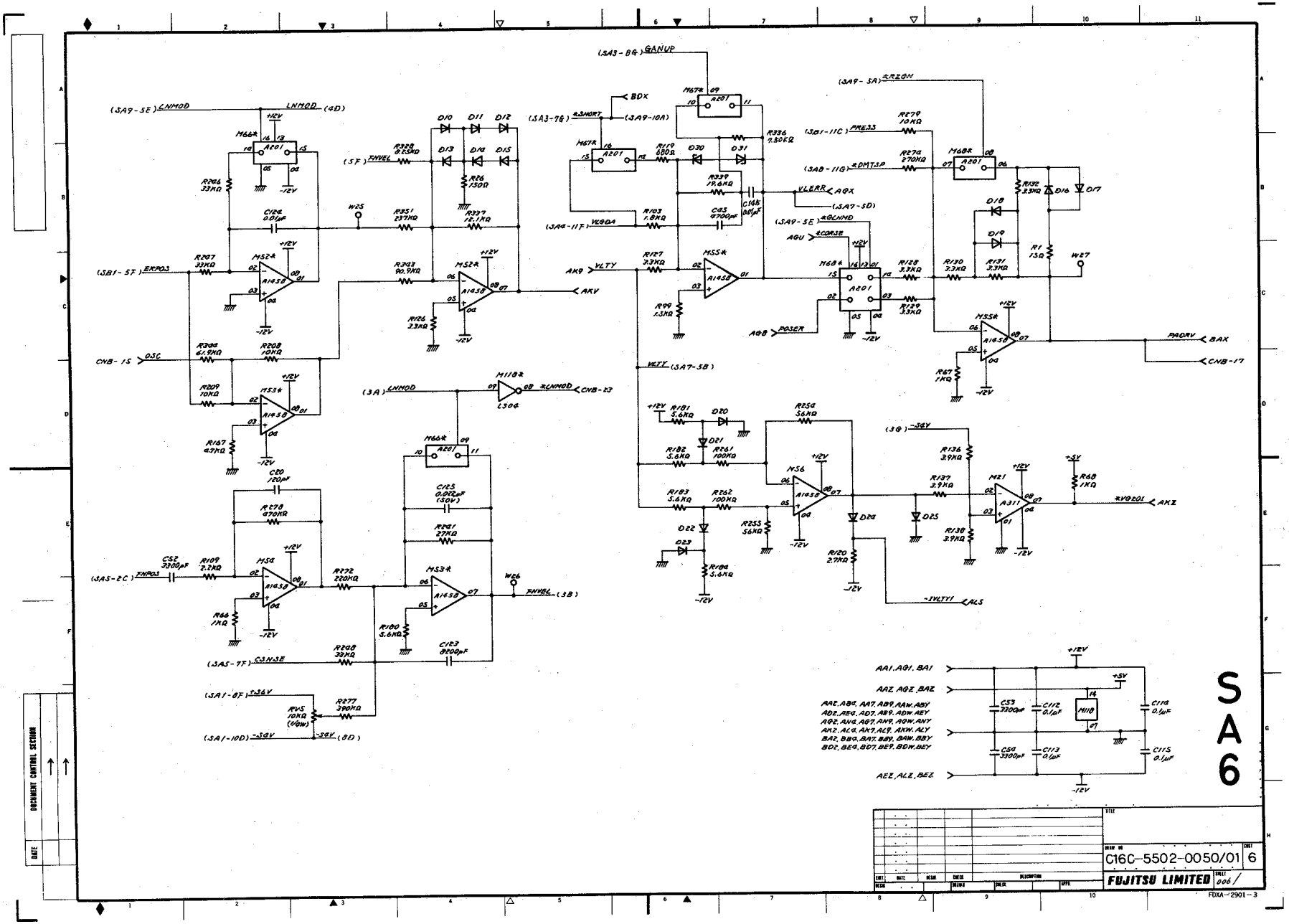
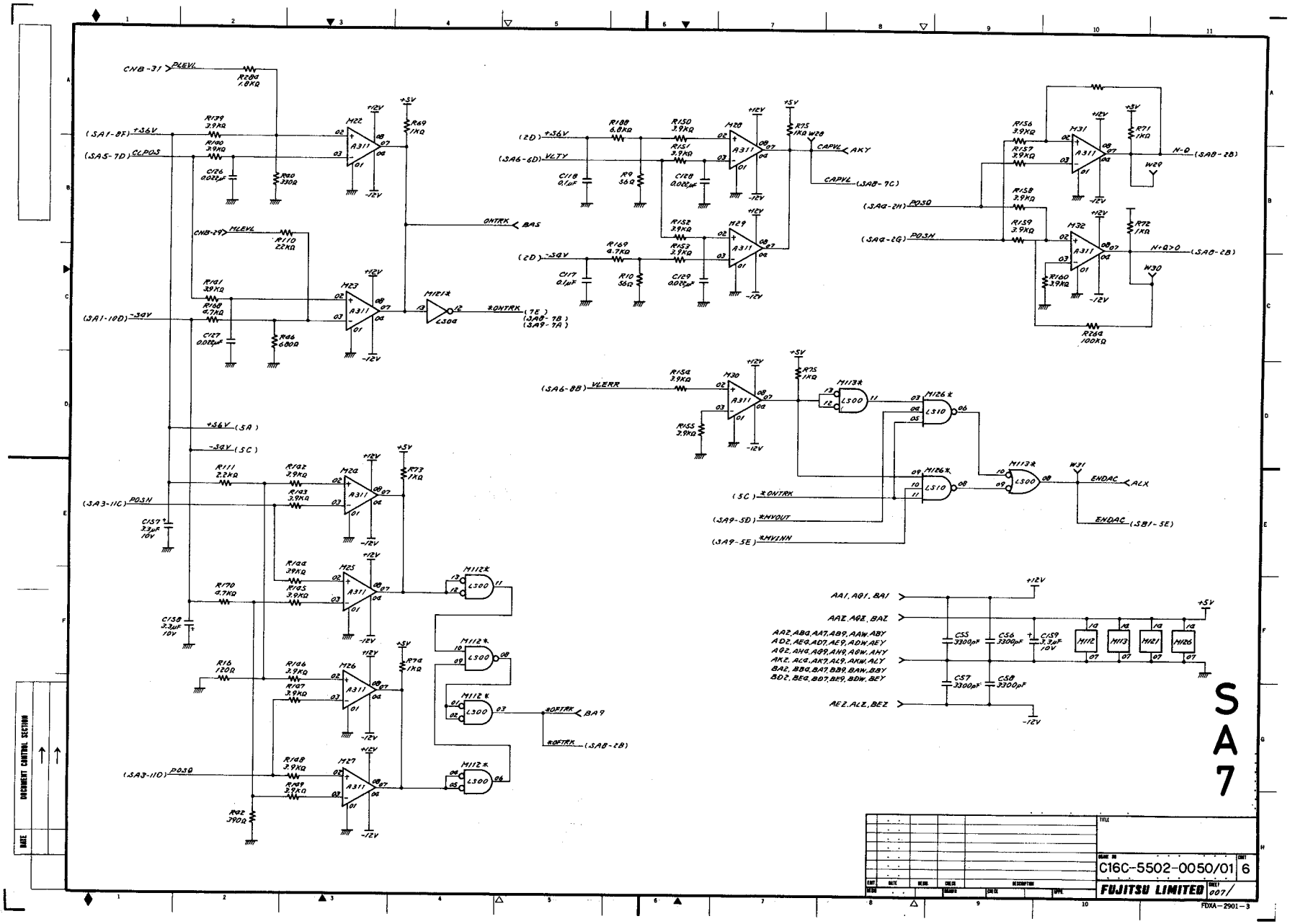
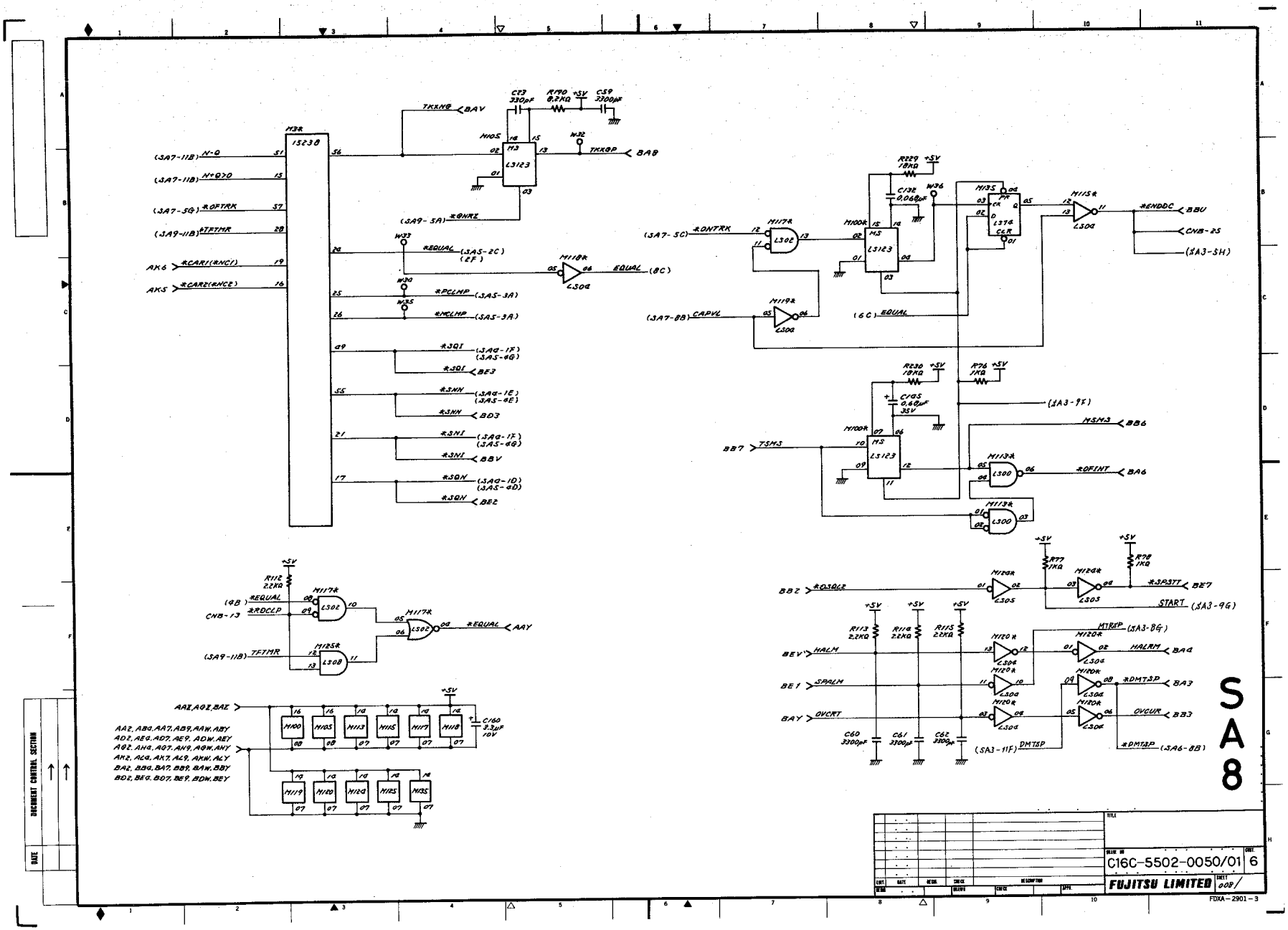
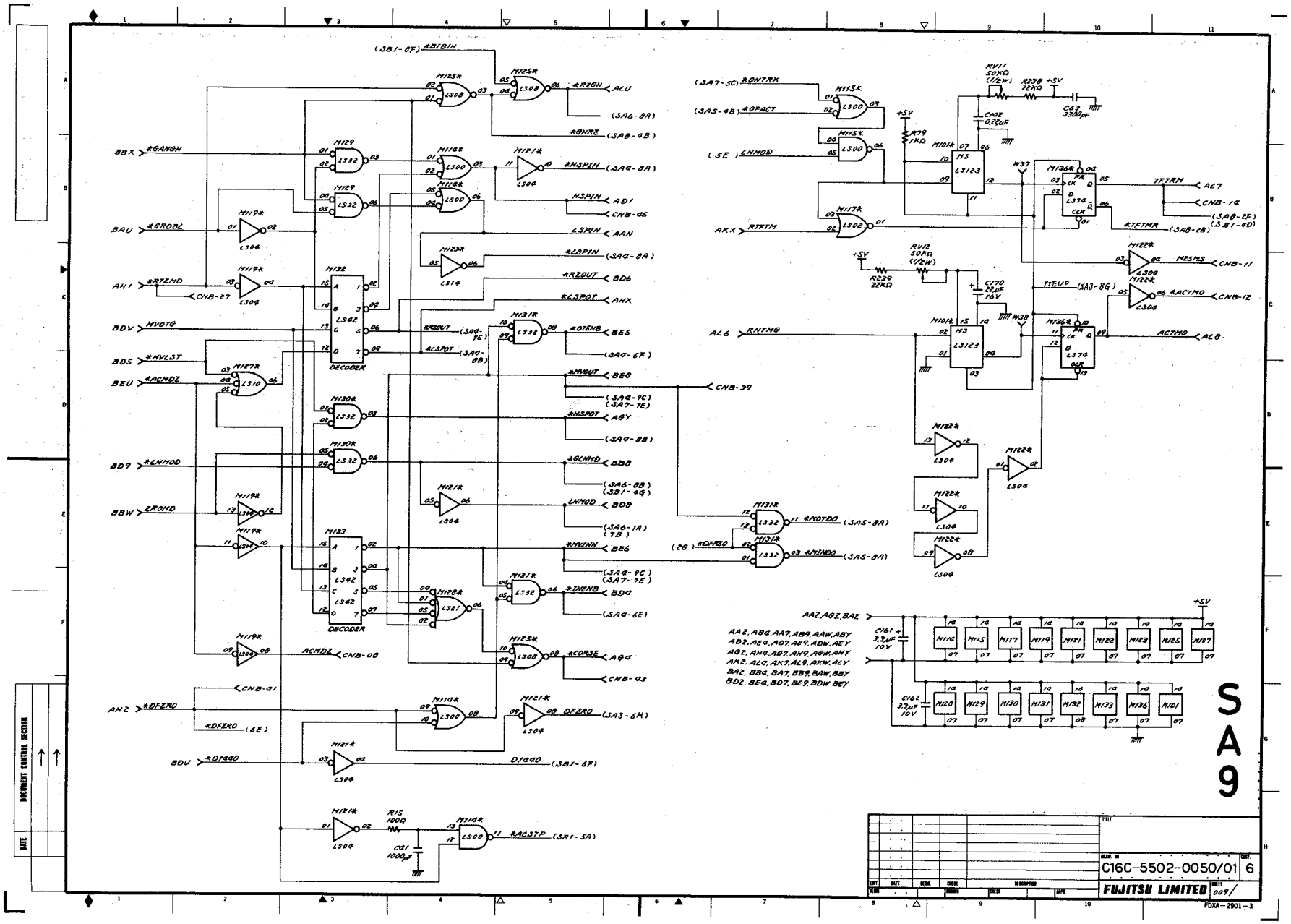

GD1 (SA3-7F)
GD2 (SA3-5F)
GD4 (SA3-5F)
GD8 (SA3-5F)
(SA1-8F) +36V
+36V (8C)
+12V
C97 0.1μF
R222 73KΩ
RV10 10KΩ (1/2W)
R225 10KΩ
AH5 OFOUT
AHW GD1
AHV GD2
AHU GD4
AH9 GD8
AG8 GD16
AH7 GD32
AH6 GD64
AG5 GD128
M5
A610
C98 0.1μF -12V
DACA ABX
DACA (SA5-1C)
-5AV (8A)
(SA1-10D) -5AV
(SB1-7E) ACCEL
D9
R223 15KΩ
R226 10KΩ
C67 0.01μF
R270 150KΩ
R276 390KΩ
AK1 SMOTH
R283 120KΩ
R307 1.96KΩ
R176 5.6KΩ
RV6 1KΩ (1/2W)
R178 3.9KΩ
R340 27KΩ
R333 110KΩ
R330 10.0KΩ
D3
R323 6.19KΩ
R317 4.64KΩ
D4
R335 12.1KΩ
R318 5.62KΩ
D5
R338 31.6KΩ
R324 6.19KΩ
D6
R309 237KΩ
R334 21.5KΩ
D7
R352 51.1KΩ
R325 8.25KΩ
D8
C92 1500pF
R329 5.62KΩ
M17*
A1458
R88 1.2KΩ
R331 10.0KΩ
R332 10.0KΩ
W18
M47*
A1458
R163 4.7KΩ
W19
(SA9-3B) *H3PIN
(SA9-5C) *L3PIN
M60*
A201
R232 22KΩ
R179 5.6KΩ
(5B) -5AV
(SA9-5D) *H3POT
(SA9-4C) *L3POT
R268 120KΩ
R223 22KΩ
(3A) +36V
(SA9-5E) *MVINN
(SA9-5D) *MVOUT
M61*
R305 1.78KΩ
R304 1.78KΩ
(SA9-4C) *RZOUT
FG CNB-21
VLGDA AKU
(SA5-7D) CLPOS
R342 51.1KΩ
VLGDA (SA6-5B)
(SA8-4E) *SQN
(SA8-6D) *SNN
M62*
AK3 POSN
AK8 POSQ
R186 6.8KΩ
R187 6.8KΩ
C11 22pF
R178 5.6KΩ
M15
A159
R86 1.2KΩ
R87 1.2KΩ
R179 5.6KΩ
(SA8-4C) *SQ1
(SA8-6D) *SN1
(POSN) (SAS-1E) (SA7-8B)
(POSQ) (SAS-1G) (SA7-8B)
C12 22pF
R228 18KΩ
R227 1.8KΩ
M16
A159
R203 10KΩ
(SAS-10A) SMTDO
(SA9-5F) *INENB
(SA9-5C) *OTENB
W20
M63*
R249 39KΩ
R250 39KΩ
SMOTH ACL2
INPOS ACL3
CNB-17
AA1, AG1, BA1
AA2, AB4, AA7, AB9, AAW, ABY
AD2, AE4, AD7, AE9, ADW, AEY
AG2, AH4, AG7, AH9, AGW, AHY
AK2, AL4, AK7, AL9, AKW, ACY
BA2, BB4, BA7, BB9, BAW, BBY
BD2, BE4, BD7, BE9, BDW, BEY
AE2, AL2, BE2
C99 0.1μF
C100 0.1μF
C101 0.1μF
C102 0.1μF
C103 0.1μF
C104 0.1μF
-12V
SA4
DOCUMENT CONTROL SECTION
DATE
C16C-5502-0050/01 6
FUJITSU LIMITED
FDXA-2901-3

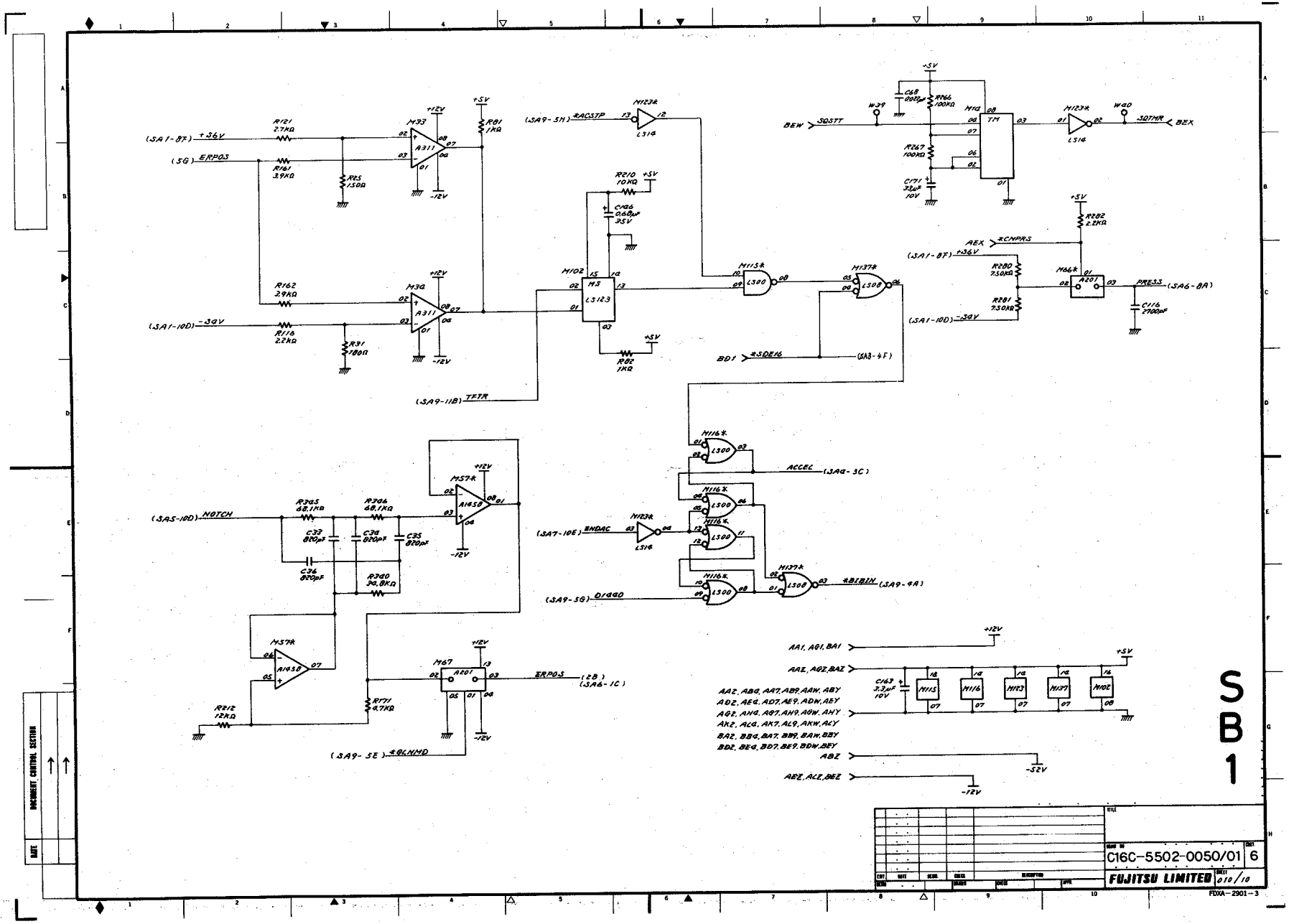

SA5
C16C-5502-0050/01
FUJITSU LIMITED
FOXA-2901-3
DOCUMENT CONTROL SECTION
DATE
*MCLMP
*PCLMP
OFSET
*MINDO
*MOYDO
SMTDO
*OFACT
*EQUAL
FNPOS
DACA
CLPOS
ACW
NOTCH
POSN
POSQ
*SQN
*SNN
*SQI
*SNI
CSNSE
VCTY
ABV
AA1, AQ1, BA1,
AA2, AB9, AA7, AB9, AAW, ABY
AD2, AE9, AD7, AE9, ADW, AEY
AG2, AH9, AG7, AH9, AGW, ANY
AK2, AL9, AK7, AL9, AKW, ALY
BA2, BB9, BA7, BB9, BAW, BBY
BD2, BE9, BD7, BE9, BDW, BEY
AE2, AL2, BE2


SA6
C16C-5502-0050/01
FUJITSU LIMITED
DOCUMENT CONTROL SECTION
DATE
FDXA-2901-3

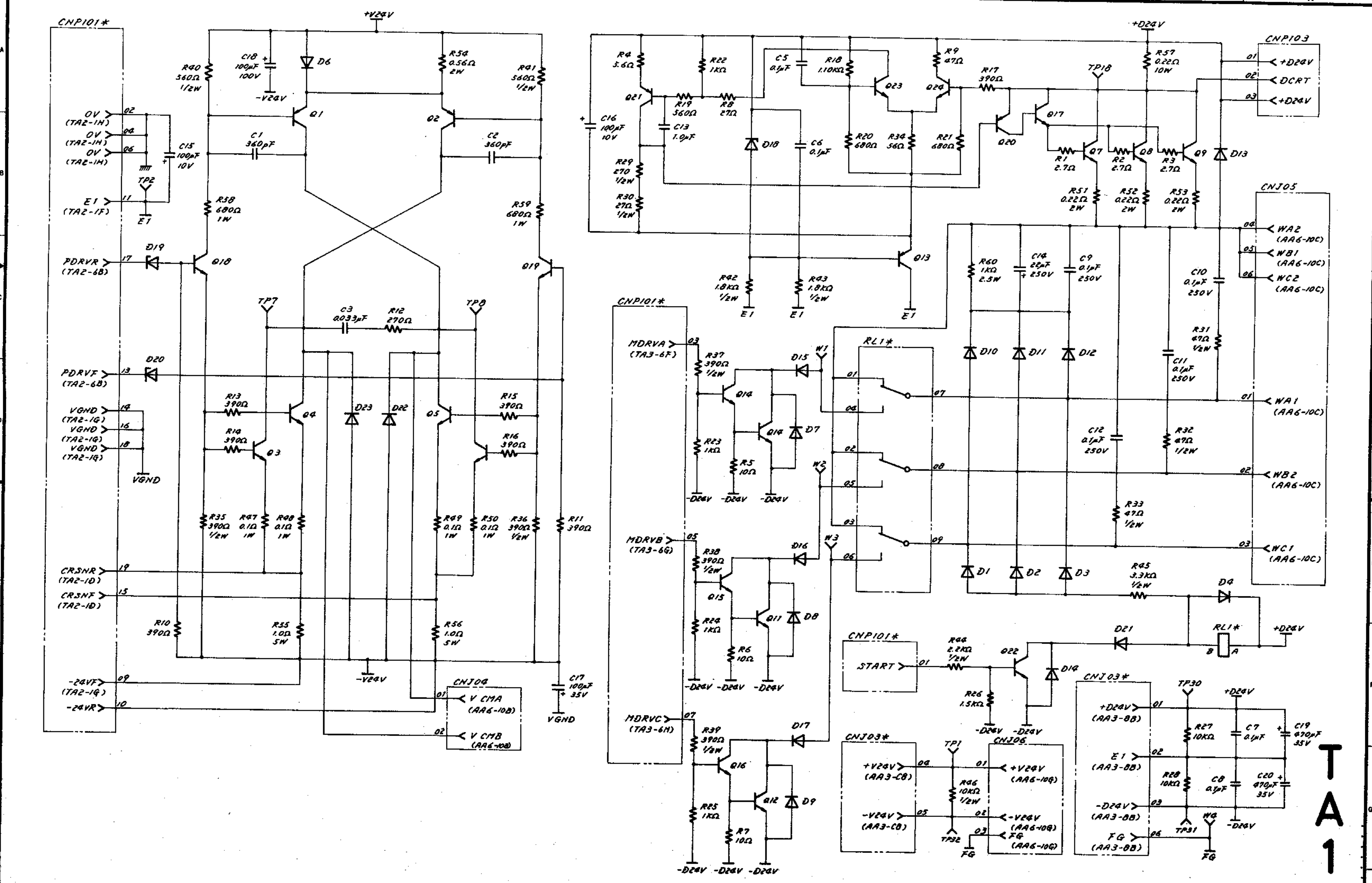

CNB-31 PLEVL
R204 1.8KΩ
(SA1-8F) +36V
(SA5-7D) CLPOS
R139 3.9KΩ
R140 3.9KΩ
C126 0.022μF
R60 330Ω
M22
A311
+12V
+5V
-12V
R49 1KΩ
CNB-29 MLEVL
R110 22KΩ
(SA1-10D) -36V
R141 3.9KΩ
R168 4.7KΩ
C127 0.022μF
R46 680Ω
M23
ONTRK < BAS
M121*
LS04
*ONTRK (7E) (SA8-7B) (SA9-7A)
(2D) +36V
R188 6.8KΩ
C118 0.1μF
R9 36Ω
R150 3.9KΩ
R151 3.9KΩ
C128 0.022μF
M28
R75 1KΩ W28
CAPVL < AKY
CAPVL (SA8-7C)
(SA6-6D) VLTY
R152 3.9KΩ
R153 3.9KΩ
C129 0.022μF
M29
(2D) -36V
R169 4.7KΩ
C117 0.1μF
R10 36Ω
R156 3.9KΩ
R157 3.9KΩ
M31
R71 1KΩ
W29
N-0 (SA8-2B)
(SA9-2H) POS0
R158 3.9KΩ
R159 3.9KΩ
M32
R72 1KΩ
W30
N-0>0 (SA8-2B)
(SA9-2G) POSN
R160 3.9KΩ
R264 100KΩ
(SA6-8B) VLERR
R154 3.9KΩ
R155 3.9KΩ
M30
R75 1KΩ
M113*
LS00
M126*
LS10
W31
ENDAC < ALX
ENDAC (SB1-5E)
(5C) *ONTRK
(SA9-5D) *MYOUT
(SA9-5E) *MYINN
+5V (SA)
-36V (5C)
R111 2.2KΩ
(SA3-11C) POSN
R102 3.9KΩ
R103 3.9KΩ
M24
R73 1KΩ
C157 3.3μF 10V
R104 3.9KΩ
R105 3.9KΩ
M25
M112*
R170 4.7KΩ
C158 3.3μF 10V
R16 120Ω
R106 3.9KΩ
R107 3.9KΩ
M26
R74 1KΩ
*OPTRK < BA9
*OPTRK (SA8-2B)
(SA3-11D) POS0
R108 3.9KΩ
R109 3.9KΩ
M27
R92 390Ω
AA1, AG1, BA1
AA2, AG2, BA2
AA2, ABG, AA7, AB9, AAW, ABY
AD2, AEG, AD7, AE9, ADW, AEY
AG2, AHG, AG9, AHG, AGW, AHY
AK2, ALG, AK7, AL9, AKW, ALY
BA2, BBG, BA7, BB9, BAW, BBY
BD2, BEG, BD7, BE9, BDW, BEY
AE2, ALZ, BEZ
C55 3300pF
C56 3300pF
C159 3.3μF 10V
C57 3300pF
C58 3300pF
M112
M113
M121
M126
SA7
DOCUMENT CONTROL SECTION
DATE
TITLE
DRAWING NO C16C-5502-0050/01
CODE 6
FUJITSU LIMITED
SHEET 007/
FDXA-2901-3


SA8
C16C-5502-0050/01
FUJITSU LIMITED
FDXA-2901-3
DOCUMENT CONTROL SECTION
DATE
TKRNG
BAV
TKRQP
BA8
*QNRE
(SA9-5A)
*EQUAL
(SA5-2C)
(2F)
EQUAL
(8C)
*RPCLMP
(SA5-3A)
*RMCLMP
(SA5-3A)
*SQI
(SA9-1F)
(SA5-6G)
BE3
*SNN
(SA9-1E)
(SA5-4E)
BD3
*SNI
(SA9-1F)
(SA5-6G)
BBV
*SQN
(SA9-1D)
(SA5-6D)
BE2
*CARI(*RNCI)
*CARE(*RNCE)
*QNTRK
CAPVL
(6C) EQUAL
*ENDDC
BBU
CNB-25
(SA3-5H)
(SA3-9F)
TSMS
BB7
*SMS
BB6
*QFINT
BA6
*QSOGE
BB2
*SPSTT
BE7
START
(SA3-9G)
REQUAL
(9B)
*RDCLP
CNB-13
*EQUAL
AAY
TFTMR
(SA9-11B)
HALM
BEV
HALRM
BA4
SPALM
BE1
*DMTSP
BA3
OVCRT
BAY
OVCUR
BB3
(SA3-11F) DMTSP
(SA6-8B)
AA2, AB9, AA7, AB9, AAW, ABY
AD2, AE9, AD7, AE9, ADW, AEY
AG2, AH9, AG7, AH9, AGW, AHY
AK2, AL9, AK7, AL9, AKW, ALY
BA2, BB9, BA7, BB9, BAW, BBY
BD2, BE9, BD7, BE9, BDW, BEY


SA9
C16C-5502-0050/01 6
FUJITSU LIMITED
FDXA-2901-3
DECODER
DECODER
DOCUMENT CONTROL SECTION


SB1
C16C-5502-0050/01
6
FUJITSU LIMITED
FDXA-2901-3
INCORRECT CONTROL SECTION
DATE

B03P-4825-0002A...01A



TA1

DOCUMENT CONTROL SECTION

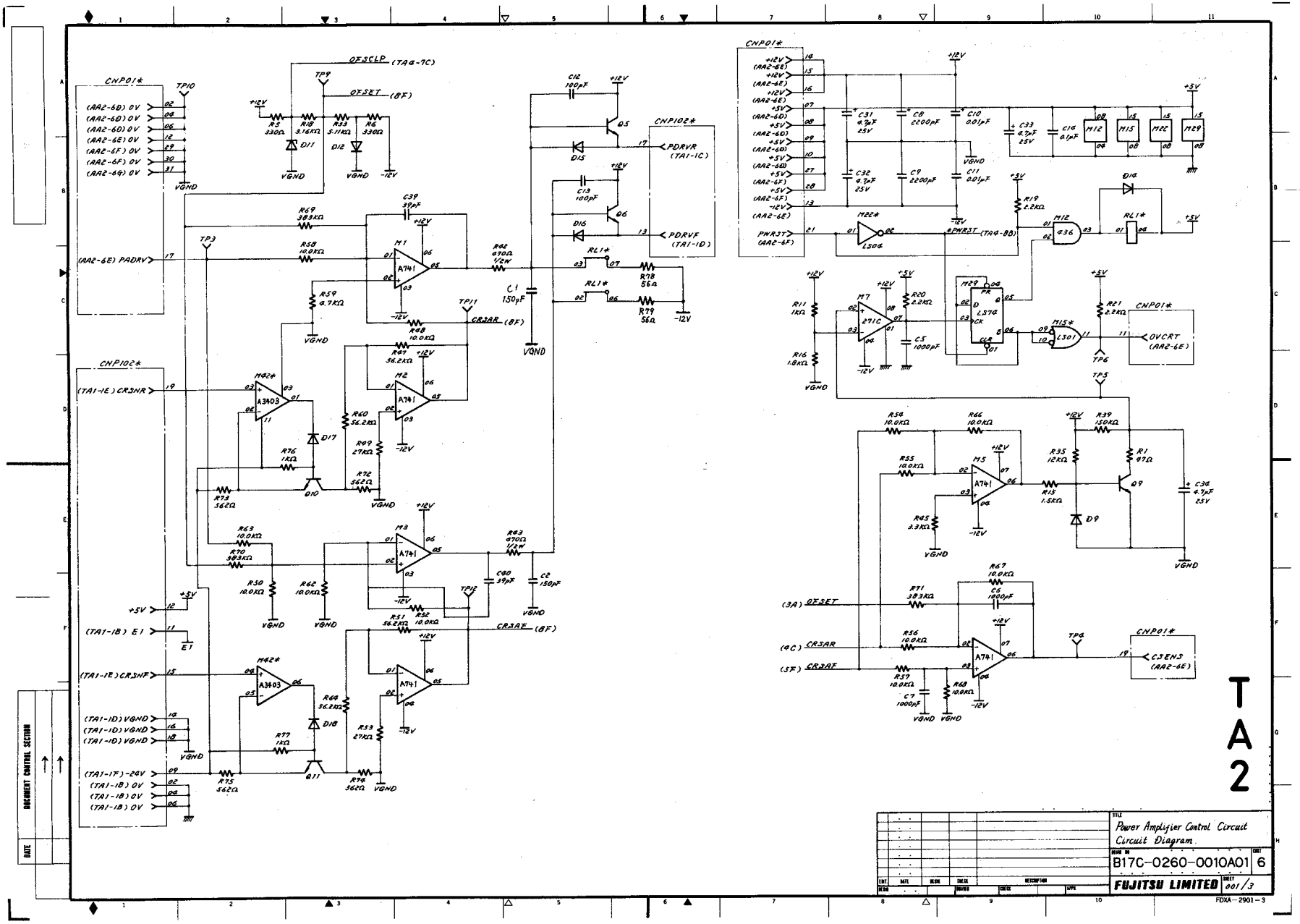
DATE

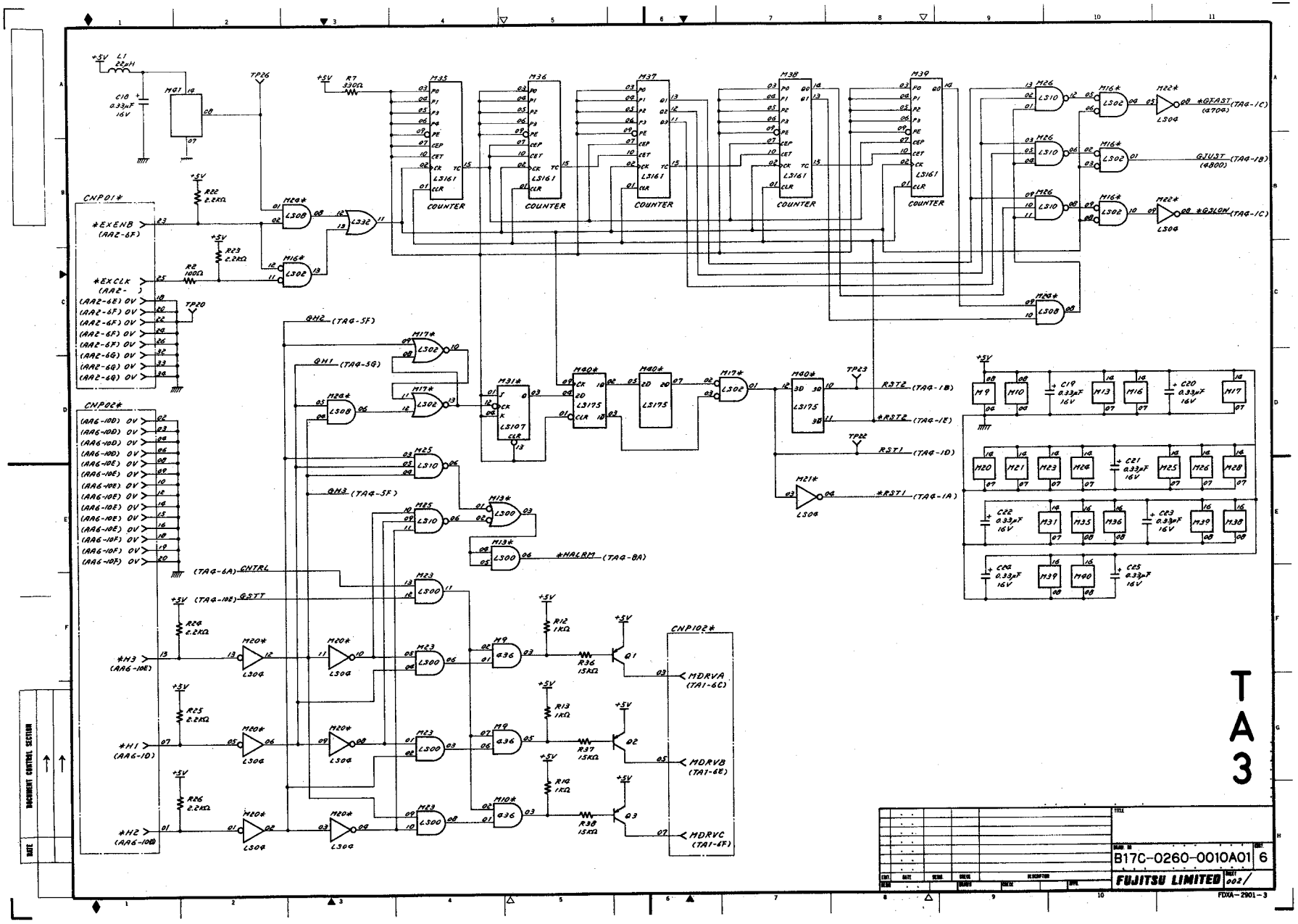
TITLE: Power Amplifier Circuit Diagram.

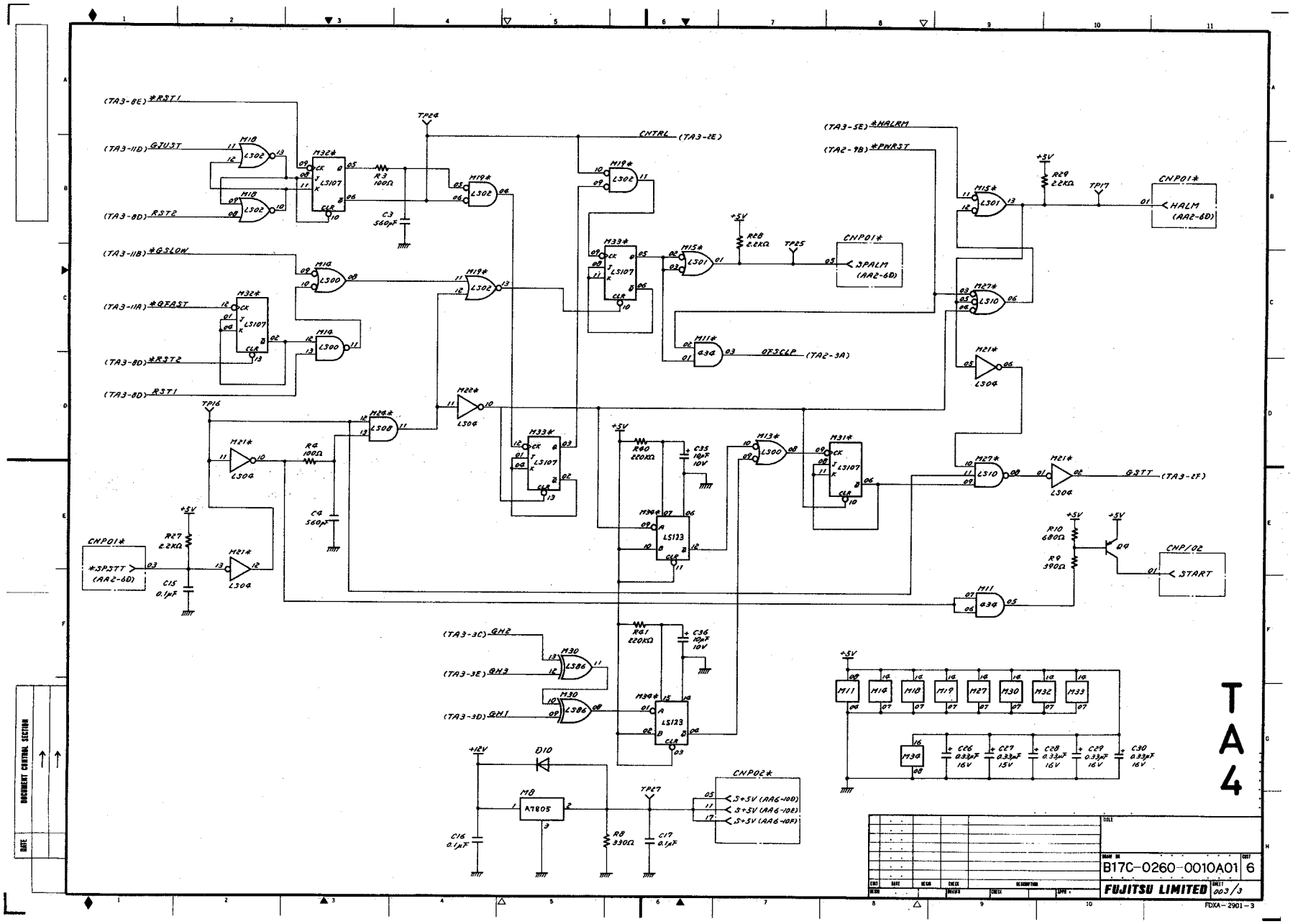
B17C-0250-0010A01 | 6

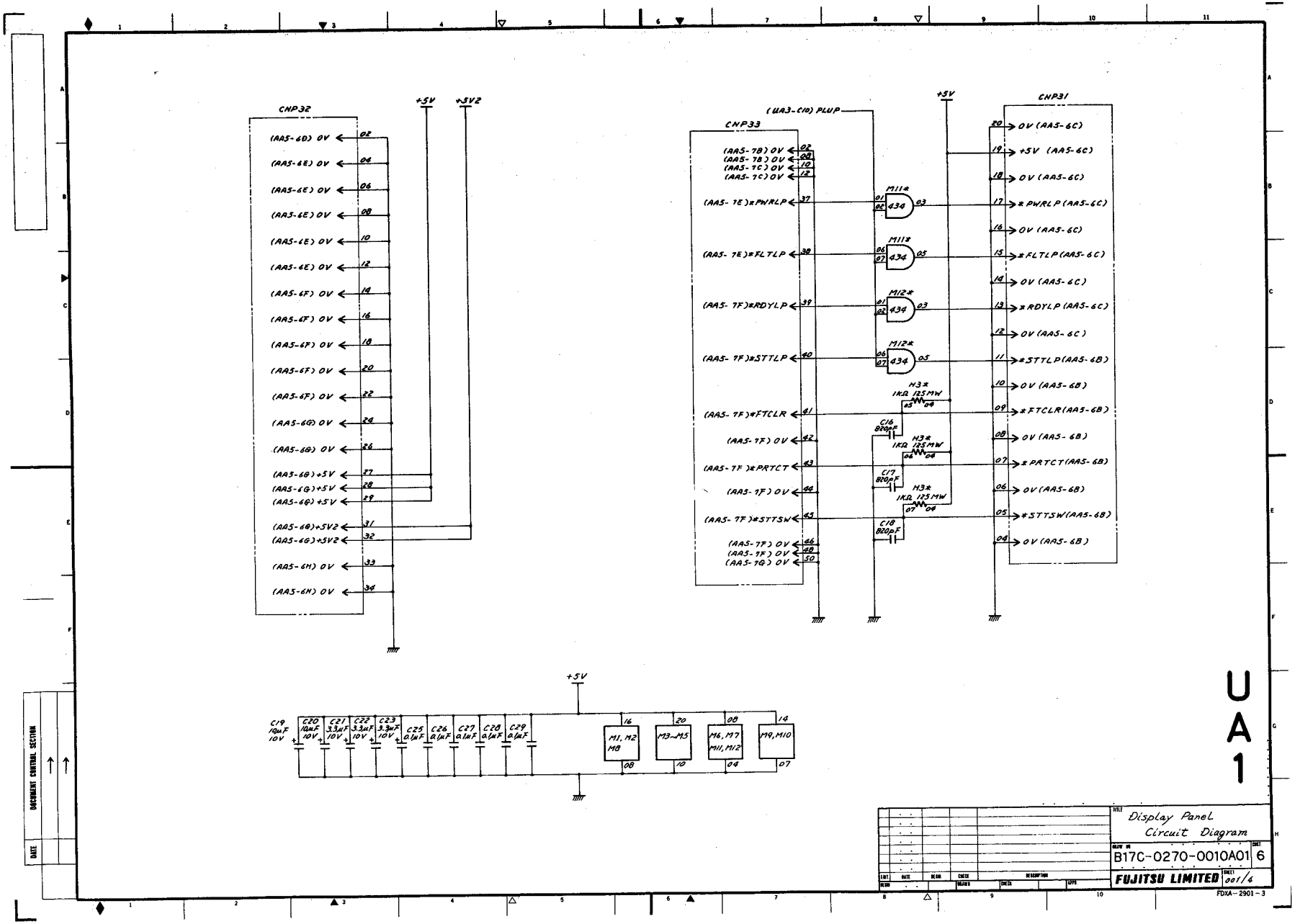
FUJITSU LIMITED | SHEET 001/1

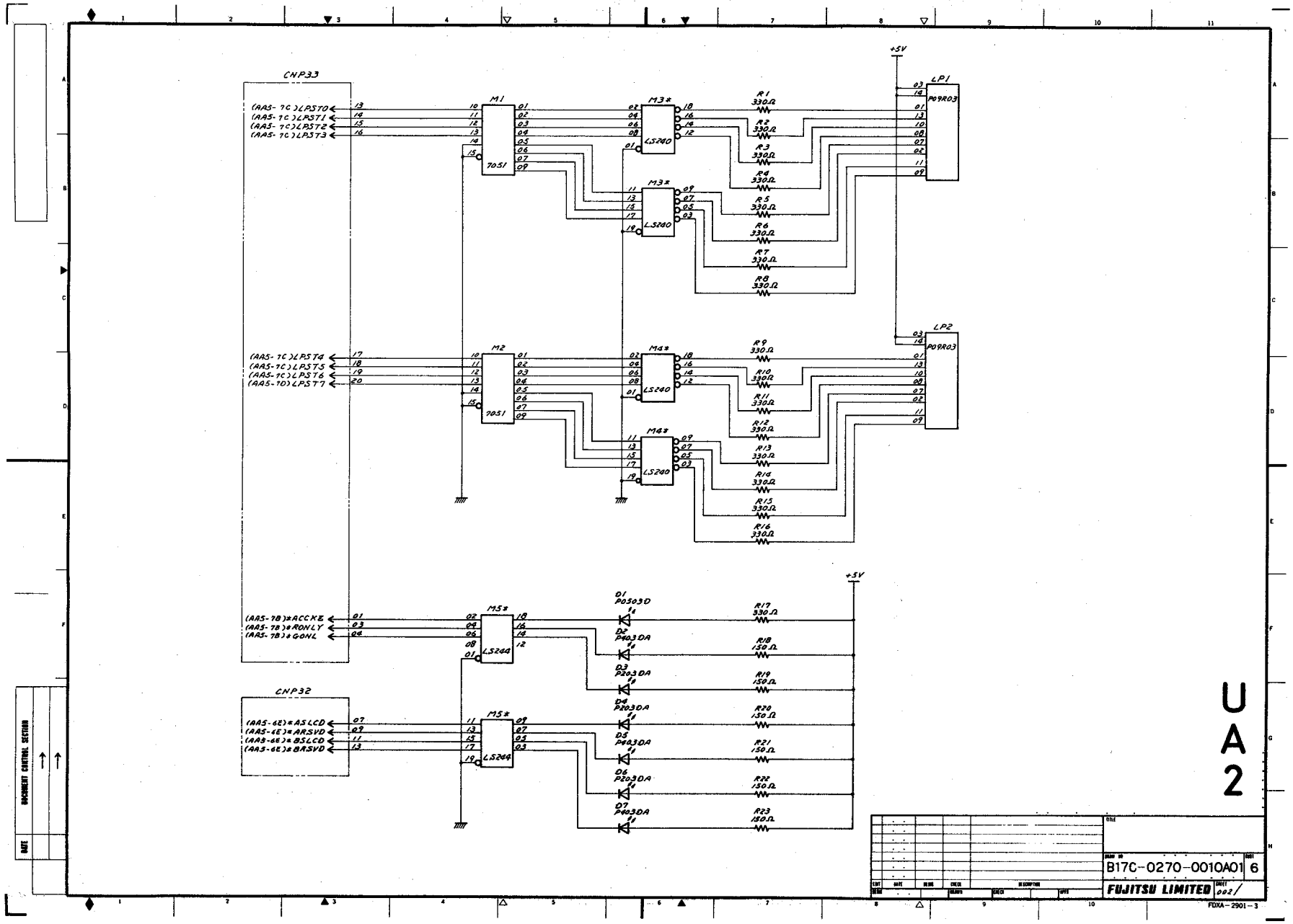
FDXA-2901-3

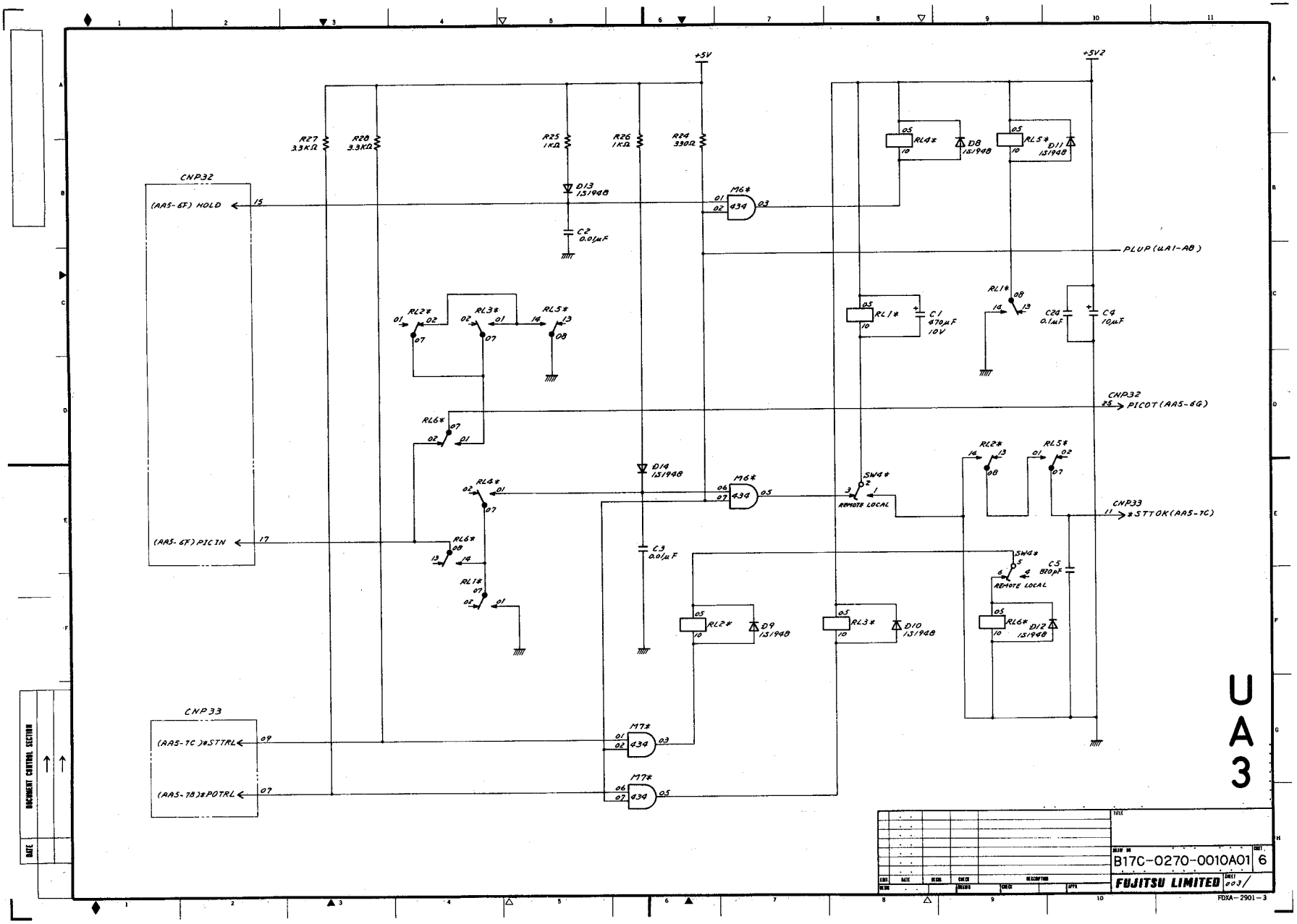

TA2
Power Amplifier Control Circuit
Circuit Diagram
B17C-0260-0010A01
6
FUJITSU LIMITED
001/3
FDXA-2901-3
DOCUMENT CONTROL SECTION
DATE

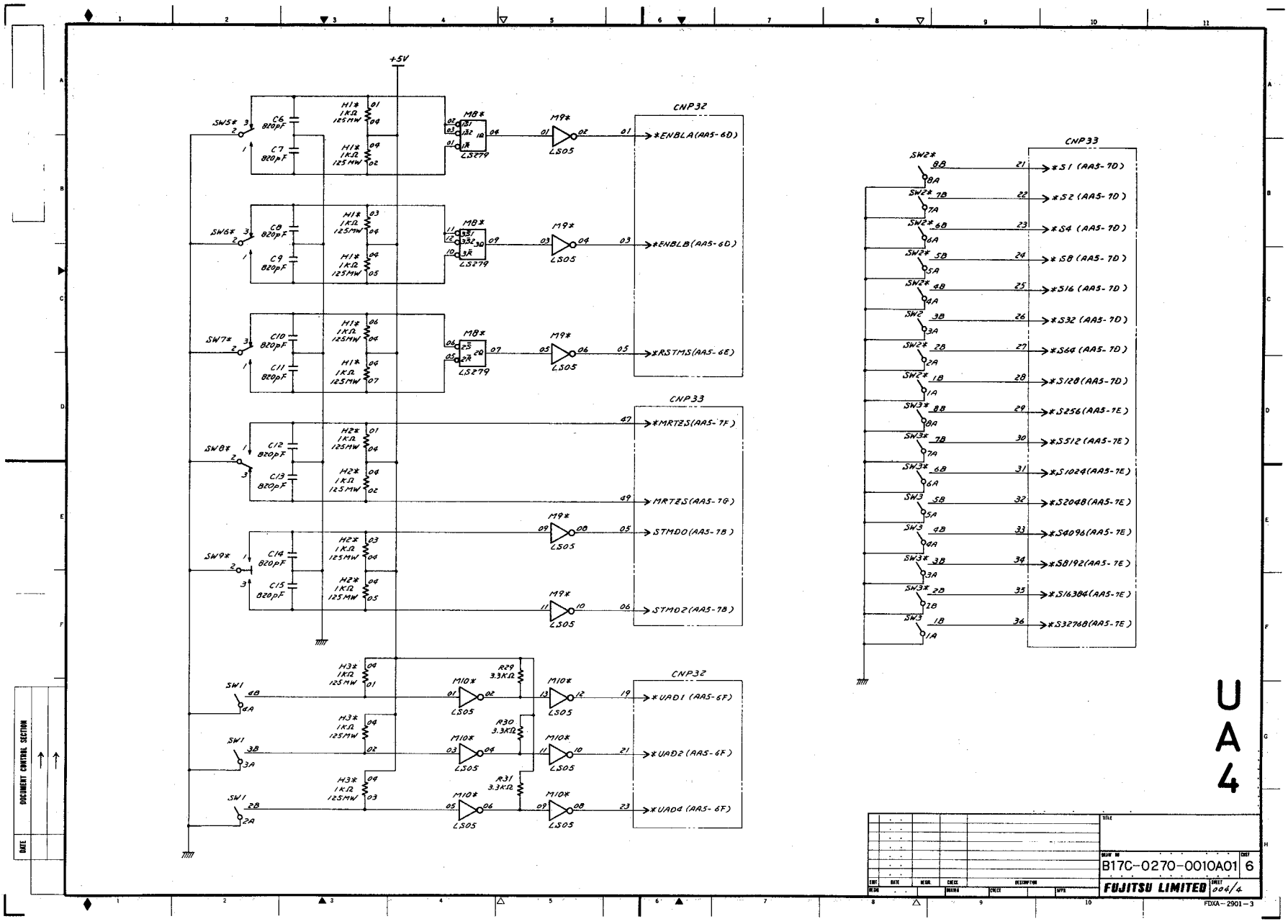

TA3
COUNTER
LS161
LS08
LS32
LS02
LS04
LS10
LS00
LS175
LS107
LS36
CNP01*
CNP02*
CNP102*
*EXENB (AA2-6F)
*EXCLK (AA2-)
(AA2-6E) 0V
(AA2-6F) 0V
(AA2-6F) 0V
(AA2-6F) 0V
(AA2-6F) 0V
(AA2-6G) 0V
(AA2-6G) 0V
(AA2-6G) 0V
(AA6-10D) 0V
(AA6-10D) 0V
(AA6-10D) 0V
(AA6-10D) 0V
(AA6-10E) 0V
(AA6-10E) 0V
(AA6-10E) 0V
(AA6-10E) 0V
(AA6-10E) 0V
(AA6-10F) 0V
(AA6-10F) 0V
(AA6-10F) 0V
GH2 (TAG-5F)
GH1 (TAG-5G)
GH3 (TAG-5F)
(TAG-6A) CNTRL
(TAG-10B) GATT
*H3 (AA6-10E)
*H1 (AA6-1D)
*H2 (AA6-10D)
R3ST2 (TAG-1B)
*RST2 (TAG-1E)
RST1 (TAG-1D)
*RST1 (TAG-1A)
*HALRM (TAG-8A)
GFAST (TAG-1C)
GJUST (4800) (TAG-1B)
*GJLON (TAG-1C)
MDRVA (TA1-6C)
MDRVB (TA1-6E)
MDRVC (TA1-4F)
DOCUMENT CONTROL SECTION
DATE
B17C-0260-0010A01
6
FUJITSU LIMITED
002/
FDXA-2901-3


TA4
FUJITSU LIMITED
B17C-0260-0010A01 6
FDXA-2901-3
(TA3-8E) *RST1
(TA3-11D) GJUST
(TA3-8D) RST2
(TA3-11B) *GSLOW
(TA3-11A) *QFAST
(TA3-8D) *R3T2
(TA3-8D) R3T1
(TA3-5E) *HALRM
(TA2-9B) *PNR3T
CNTRL (TA3-2E)
QF3CLR (TA2-3A)
(TA3-3C) GH2
(TA3-3E) GH3
(TA3-3D) GH1
GSTT (TA3-2F)
HALM (AA2-6D)
3PALM (AA2-6D)
*3PSTT (AA2-6D)
START
+5V (AA6-10D)
+5V (AA6-10E)
+5V (AA6-10F)
A7805
DOCUMENT CONTROL SECTION
DATE


CNP32
+5V
+5V2
(AA5-6D) 0V
(AA5-6E) 0V
(AA5-6E) 0V
(AA3-6E) 0V
(AA5-6E) 0V
(AA5-6E) 0V
(AA5-6F) 0V
(AA5-6F) 0V
(AA5-6F) 0V
(AA5-6F) 0V
(AA5-6F) 0V
(AA5-6G) 0V
(AA5-6G) 0V
(AA3-6G)+5V
(AA5-6G)+5V
(AA5-6G)+5V
(AA5-6G)+5V2
(AA5-6G)+5V2
(AA5-6H) 0V
(AA5-6H) 0V
(UA3-C10) PLUP
CNP33
(AA5-7B) 0V
(AA5-7B) 0V
(AA5-7C) 0V
(AA5-7C) 0V
(AA5-7E)*PWRLP
(AA5-7E)*FLTLP
(AA5-7F)*RDYLP
(AA5-7F)*STTLP
(AA5-7F)*FTCLR
(AA5-7F) 0V
(AA5-7F)*PRTCT
(AA5-7F) 0V
(AA5-7F)*STTSW
(AA5-7F) 0V
(AA5-7F) 0V
(AA5-7G) 0V
M11*
M11*
M12*
M12*
M3*
1KΩ 125MW
C16 820pF
M3*
1KΩ 125MW
C17 820pF
M3*
1KΩ 125MW
C18 820pF
CNP31
0V (AA5-6C)
+5V (AA5-6C)
0V (AA5-6C)
*PWRLP (AA5-6C)
0V (AA5-6C)
*FLTLP (AA5-6C)
0V (AA5-6C)
*RDYLP (AA5-6C)
0V (AA5-6C)
*STTLP (AA5-6B)
0V (AA5-6B)
*FTCLR (AA5-6B)
0V (AA5-6B)
*PRTCT (AA5-6B)
0V (AA5-6B)
*STTSW (AA5-6B)
0V (AA5-6B)
+5V
C19 10uF 10V
C20 10uF 10V
C21 3.3uF 10V
C22 3.3uF 10V
C23 3.3uF 10V
C25 0.1uF
C26 0.1uF
C27 0.1uF
C28 0.1uF
C29 0.1uF
M1, M2 M8
M3~M5
M6, M7 M11, M12
M9, M10
DOCUMENT CONTROL SECTION
DATE
UA 1
Display Panel Circuit Diagram
B17C-0270-0010A01
6
FUJITSU LIMITED
001/6
FDXA-2901-3


CNP33
(AA5-7C)LPST0
(AA5-7C)LPST1
(AA5-7C)LPST2
(AA5-7C)LPST3
(AA5-7C)LPST4
(AA5-7C)LPST5
(AA5-7C)LPST6
(AA5-7D)LPST7
(AA5-7B)*ACCKE
(AA5-7B)*RONLY
(AA5-7B)*GONL
CNP32
(AA5-6E)*ASLCD
(AA5-6E)*ARSVD
(AA5-6E)*BSLCD
(AA5-6E)*BASVD
M1
M2
M3*
M4*
M5*
7051
LS240
LS244
R1 330Ω
R2 330Ω
R3 330Ω
R4 330Ω
R5 330Ω
R6 330Ω
R7 330Ω
R8 330Ω
R9 330Ω
R10 330Ω
R11 330Ω
R12 330Ω
R13 330Ω
R14 330Ω
R15 330Ω
R16 330Ω
R17 330Ω
R18 150Ω
R19 150Ω
R20 150Ω
R21 150Ω
R22 150Ω
R23 150Ω
D1 P03D3D
D2 P203DA
D3 P203DA
D4 P203DA
D5 P203DA
D6 P203DA
D7 P203DA
+5V
LP1
LP2
P09R03
MAINUNIT CONTROL SECTION
U
A
2
B17C-0270-0010A01
6
FUJITSU LIMITED
FDXA-2901-3


+5V
+5V2
R27 3.3KΩ
R28 3.3KΩ
R25 1KΩ
R26 1KΩ
R24 330Ω
CNP32
(AA5-6F) HOLD
D13 1S1948
C2 0.01μF
M6*
434
RL4*
D8 1S1948
RL5*
D11 1S1948
PLUP(UA1-A8)
RL2*
RL3*
RL5*
RL1*
C1 470μF 10V
C24 0.1μF
C4 10μF
CNP32
25 PICOT(AA5-6G)
RL6*
D14 1S1948
SW4*
REMOTE LOCAL
CNP33
11 *STTOK(AA5-7C)
(AA5-6F)PICIN
C3 0.01μF
C5 820pF
D9 1S1948
D10 1S1948
D12 1S1948
CNP33
(AA5-7C)*STTRL
(AA5-7B)*POTRL
M7*
DOCUMENT CONTROL SECTION
DATE
UA3
B17C-0270-0010A01
6
FUJITSU LIMITED
003/
FDXA-2901-3


+5V
SW5*
SW6*
SW7*
SW8*
SW9*
SW1
SW2*
SW3*
SW2
SW3
C6 820pF
C7 820pF
C8 820pF
C9 820pF
C10 820pF
C11 820pF
C12 820pF
C13 820pF
C14 820pF
C15 820pF
H1* 1KΩ 125MW
H2* 1KΩ 125MW
H3* 1KΩ 125MW
M8* LS279
M9* LS05
M10* LS05
R29 3.3KΩ
R30 3.3KΩ
R31 3.3KΩ
CNP32
CNP33
*ENBLA(AA5-6D)
*ENBLB(AA5-6D)
*RSTMS(AA5-6E)
*MRTES(AA5-7F)
*MRTES(AA5-7G)
STMDO(AA5-7B)
STMD2(AA5-7B)
*UAD1 (AA5-6F)
*UAD2 (AA5-6F)
*UAD4 (AA5-6F)
*S1 (AA5-7D)
*S2 (AA5-7D)
*S4 (AA5-7D)
*S8 (AA5-7D)
*S16 (AA5-7D)
*S32 (AA5-7D)
*S64 (AA5-7D)
*S128(AA5-7D)
*S256(AA5-7E)
*S512(AA5-7E)
*S1024(AA5-7E)
*S2048(AA5-7E)
*S4096(AA5-7E)
*S8192(AA5-7E)
*S16384(AA5-7E)
*S32768(AA5-7E)
DOCUMENT CONTROL SECTION
DATE
U A 4
B17C-0270-0010A01
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FUJITSU LIMITED
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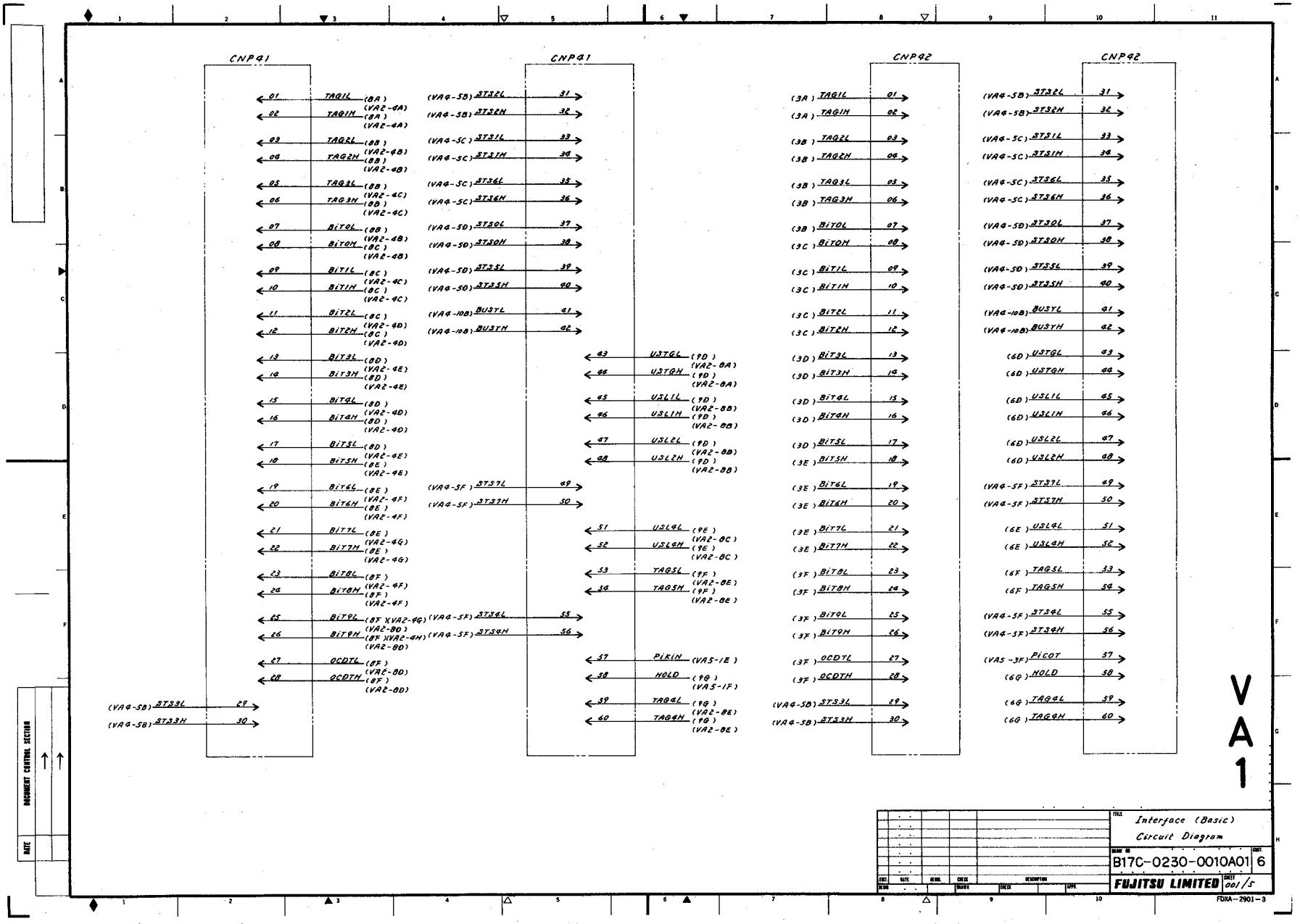
CNP41
CNP41
CNP42
CNP42
TAG1L (8A) (VA2-4A)
TAG1H (8A) (VA2-4A)
TAG2L (8B) (VA2-4B)
TAG2H (8B) (VA2-4B)
TAG3L (8B) (VA2-4C)
TAG3H (8B) (VA2-4C)
BIT0L (8B) (VA2-4B)
BIT0H (8C) (VA2-4B)
BIT1L (8C) (VA2-4C)
BIT1H (8C) (VA2-4C)
BIT2L (8C) (VA2-4D)
BIT2H (8C) (VA2-4D)
BIT3L (8D) (VA2-4E)
BIT3H (8D) (VA2-4E)
BIT4L (8D) (VA2-4D)
BIT4H (8D) (VA2-4D)
BIT5L (8D) (VA2-4E)
BIT5H (8E) (VA2-4E)
BIT6L (8E) (VA2-4F)
BIT6H (8E) (VA2-4F)
BIT7L (8E) (VA2-4G)
BIT7H (8E) (VA2-4G)
BIT8L (8F) (VA2-4F)
BIT8H (8F) (VA2-4F)
BIT9L (8F X VA2-4G) (VA2-8D)
BIT9H (8F X VA2-4H) (VA2-8D)
OCDTL (8F) (VA2-8D)
OCDTH (8F) (VA2-8D)
(VA4-5B) ST31L 29
(VA4-5B) ST31H 30
(VA4-5B) ST32L 31
(VA4-5B) ST32H 32
(VA4-5C) ST33L 33
(VA4-5C) ST33H 34
(VA4-5C) ST34L 35
(VA4-5C) ST34H 36
(VA4-5D) ST35L 37
(VA4-5D) ST35H 38
(VA4-5D) ST36L 39
(VA4-5D) ST36H 40
(VA4-10B) BUSYL 41
(VA4-10B) BUSYH 42
(VA4-5F) ST37L 49
(VA4-5F) ST37H 50
(VA4-5F) ST38L 55
(VA4-5F) ST38H 56
USTGL (9D) (VA2-8A)
USTGH (9D) (VA2-8A)
USL1L (9D) (VA2-8B)
USL1H (9D) (VA2-8B)
USL2L (9D) (VA2-8B)
USL2H (9D) (VA2-8B)
USL4L (9E) (VA2-8C)
USL4H (9E) (VA2-8C)
TAG5L (9F) (VA2-8E)
TAG5H (9F) (VA2-8E)
PIKIN (VA5-1E)
HOLD (9G) (VA5-1F)
TAG4L (9G) (VA2-8E)
TAG4H (9G) (VA2-8E)
(3A) TAG1L 01
(3A) TAG1H 02
(3B) TAG2L 03
(3B) TAG2H 04
(3B) TAG3L 05
(3B) TAG3H 06
(3B) BIT0L 07
(3C) BIT0H 08
(3C) BIT1L 09
(3C) BIT1H 10
(3C) BIT2L 11
(3C) BIT2H 12
(3D) BIT3L 13
(3D) BIT3H 14
(3D) BIT4L 15
(3D) BIT4H 16
(3D) BIT5L 17
(3E) BIT5H 18
(3E) BIT6L 19
(3E) BIT6H 20
(3E) BIT7L 21
(3E) BIT7H 22
(3F) BIT8L 23
(3F) BIT8H 24
(3F) BIT9L 25
(3F) BIT9H 26
(3F) OCDTL 27
(3F) OCDTH 28
(VA4-5B) ST33L 29
(VA4-5B) ST33H 30
(VA4-5B) ST32L 31
(VA4-5B) ST32H 32
(VA4-5C) ST31L 33
(VA4-5C) ST31H 34
(VA4-5C) ST36L 35
(VA4-5C) ST36H 36
(VA4-5D) ST30L 37
(VA4-5D) ST30H 38
(VA4-5D) ST35L 39
(VA4-5D) ST35H 40
(VA4-10B) BUSYL 41
(VA4-10B) BUSYH 42
(6D) USTGL 43
(6D) USTGH 44
(6D) USL1L 45
(6D) USL1H 46
(6D) USL2L 47
(6D) USL2H 48
(VA4-5F) ST37L 49
(VA4-5F) ST37H 50
(6E) USL4L 51
(6E) USL4H 52
(6F) TAG5L 53
(6F) TAG5H 54
(VA4-5F) ST34L 55
(VA4-5F) ST34H 56
(VA5-3F) PICOT 57
(6G) HOLD 58
(6G) TAG4L 59
(6G) TAG4H 60
DOCUMENT CONTROL SECTION
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V A 1
Interface (Basic) Circuit Diagram
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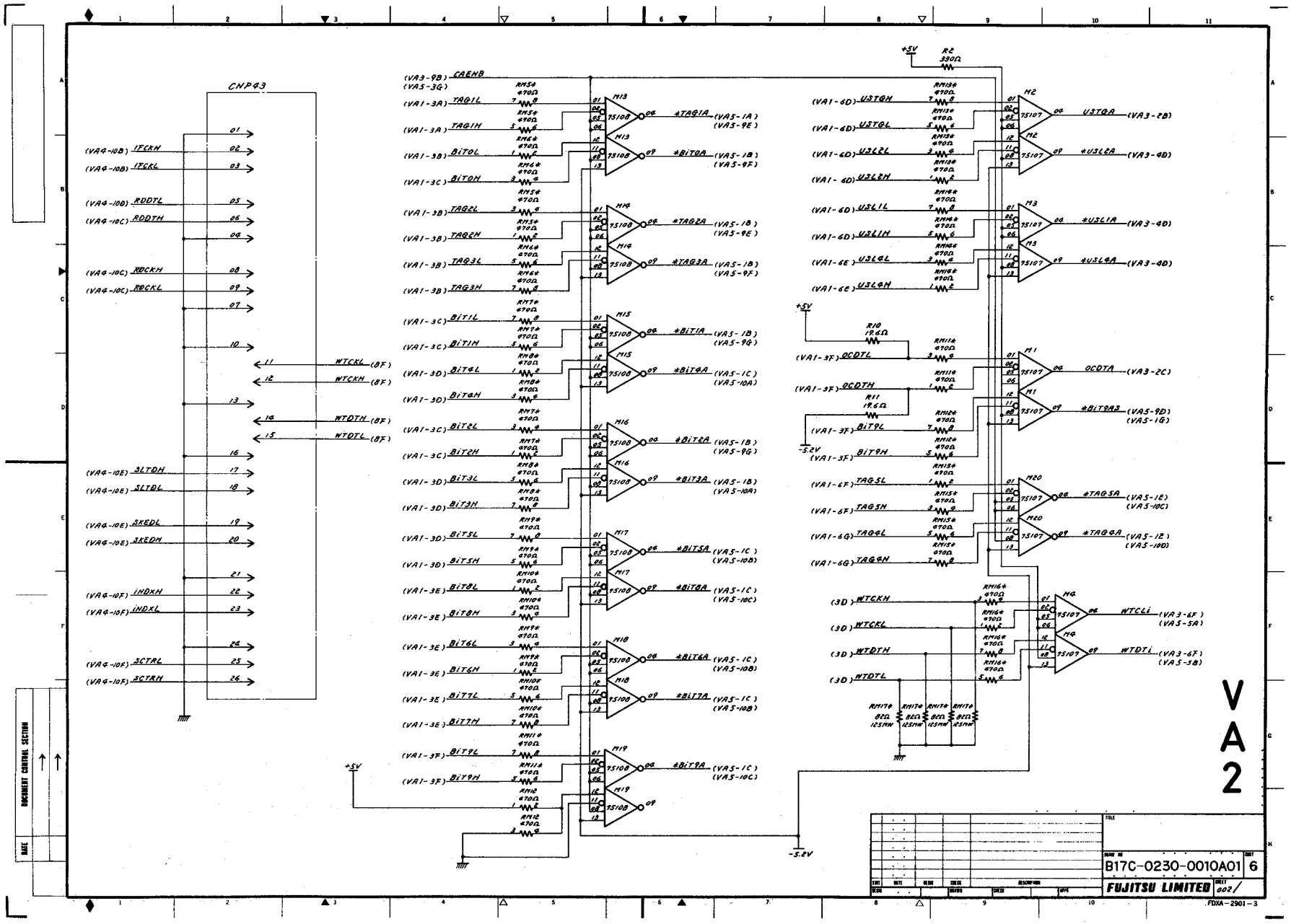
CNP43
(VA3-9B) CAENB
(VA5-3G)
(VA1-3A) TAG1L
(VA1-3A) TAG1H
(VA1-3B) BIT0L
(VA1-3C) BIT0H
(VA1-3B) TAG2L
(VA1-3B) TAG2H
(VA1-3B) TAG3L
(VA1-3B) TAG3H
(VA1-3C) BIT1L
(VA1-3C) BIT1H
(VA1-3D) BIT4L
(VA1-3D) BIT4H
(VA1-3C) BIT2L
(VA1-3C) BIT2H
(VA1-3D) BIT3L
(VA1-3D) BIT3H
(VA1-3D) BIT5L
(VA1-3D) BIT5H
(VA1-3E) BIT0L
(VA1-3E) BIT0H
(VA1-3E) BIT6L
(VA1-3E) BIT6H
(VA1-3E) BIT7L
(VA1-3E) BIT7H
(VA1-3F) BIT9L
(VA1-3F) BIT9H
(VA4-10B) ITCKH
(VA4-10B) ITCKL
(VA4-10D) RDDTL
(VA4-10C) RDDTH
(VA4-10C) RDCKH
(VA4-10C) RDCKL
(VA4-10E) SLTDH
(VA4-10E) SLTDL
(VA4-10E) SKEDL
(VA4-10E) SKEDH
(VA4-10F) INDXH
(VA4-10F) INDXL
(VA4-10F) SCTRL
(VA4-10F) SCTRH
WTCKL (8F)
WTCKH (8F)
WTDTH (8F)
WTDTL (8F)
M13
M14
M15
M16
M17
M18
M19
75108
*TAG1A (VA5-1A) (VA5-9E)
*BIT0A (VA5-1B) (VA5-9F)
*TAG2A (VA5-1B) (VA5-9E)
*TAG3A (VA5-1B) (VA5-9F)
*BIT1A (VA5-1B) (VA5-9G)
*BIT4A (VA5-1C) (VA5-10A)
*BIT2A (VA5-1B) (VA5-9G)
*BIT3A (VA5-1B) (VA5-10A)
*BIT5A (VA5-1C) (VA5-10B)
*BIT0A (VA5-1C) (VA5-10C)
*BIT6A (VA5-1C) (VA5-10B)
*BIT7A (VA5-1C) (VA5-10B)
*BIT9A (VA5-1C) (VA5-10C)
+5V
-5.2V
R2 330Ω
R10 19.6Ω
R11 19.6Ω
(VA1-6D) USTQH
(VA1-6D) USTQL
(VA1-6D) USL2L
(VA1- 6D) USL2H
(VA1-6D) USL1L
(VA1-6D) USL1H
(VA1-6E) USL0L
(VA1-6E) USL0H
(VA1-3F) OCDTL
(VA1-3F) OCDTH
(VA1-3F) BIT9L
(VA1-3F) BIT9H
(VA1-6F) TAG3L
(VA1-6F) TAG3H
(VA1-6G) TAG2L
(VA1-6G) TAG2H
M12
M13
M11
M1
M20
M4
75107
USTQA (VA3-2B)
*USL2A (VA3-4D)
*USL1A (VA3-4D)
*USL0A (VA3-4D)
OCDTA (VA3-2C)
*BIT9AS (VA5-9D) (VA5-1G)
*TAG3A (VA5-1E) (VA5-10C)
*TAG2A (VA5-1E) (VA5-10D)
(3D) WTCKH
(3D) WTCKL
(3D) WTDTH
(3D) WTDTL
WTCLI (VA3-6F) (VA5-5A)
WTDTI (VA3-6F) (VA5-5B)
RM17 82Ω 1/2SIP
RM18 82Ω 1/2SIP
RM19 82Ω 1/2SIP
RM20 82Ω 1/2SIP
DOCUMENT CONTROL SECTION
DATE
VA2
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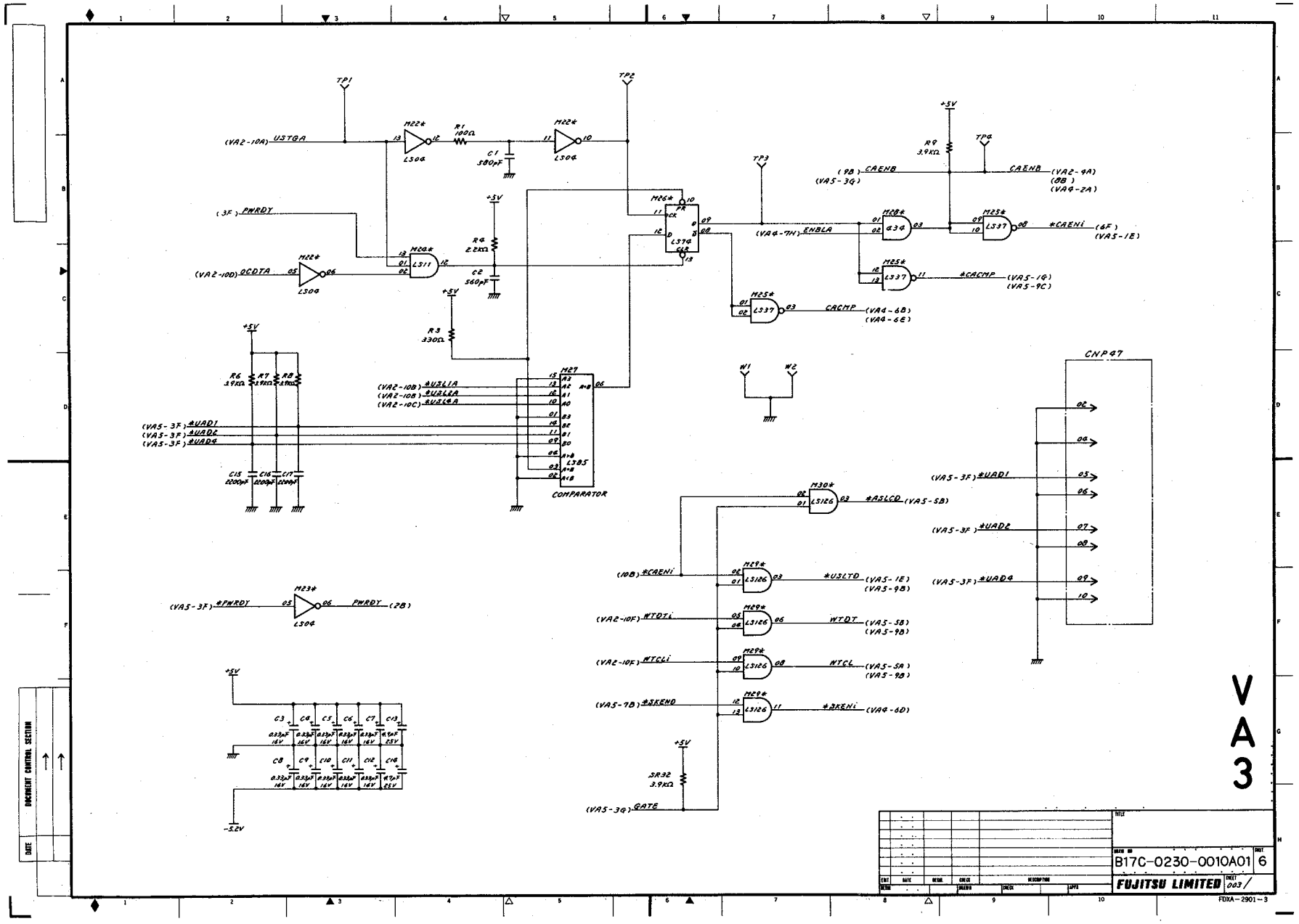
TP1
TP2
TP3
TP4
(VA2-10A) USTGA
M22*
LS04
R1 100Ω
C1 580pF
(3F) PWRDY
(VA2-10D) QCDTA
M26*
LS11
R4 2.2KΩ
C2 560pF
+5V
R3 330Ω
M26*
LS74
(VA4-7H) ENBLA
(9B) CAENB
(VA5-3G)
R9 3.9KΩ
M08*
LS32
M25*
LS37
*CAENI (6F) (VA5-1E)
*CACMP (VA5-1G) (VA5-9C)
CACMP (VA4-6B) (VA4-6E)
R6 3.9KΩ
R7 3.9KΩ
R8 3.9KΩ
(VA5-3F) *UAD1
(VA5-3F) *UAD2
(VA5-3F) *UAD4
C15 2200pF
C16 2200pF
C17 2200pF
(VA2-10B) *U2LLA
(VA2-10B) *U2LRA
(VA2-10C) *U2LQA
M27
LS85
COMPARATOR
W1
W2
CNP47
M30*
LS126
*A2LCD (VA5-5B)
(10B) *CAENI
M29*
*USLTD (VA5-1E) (VA5-9B)
(VA2-10F) WTDTL
WTDT (VA5-3B) (VA5-9B)
(VA2-10F) WTCLI
WTCL (VA5-3A) (VA5-9B)
(VA5-7B) *3KENO
*3KENI (VA4-6D)
M23*
(VA5-3F) *PWRDY
PWRDY (2B)
C3 C8 C5 C6 C7 C13
C8 C9 C10 C11 C12 C14
0.33μF 16V
4.7μF 25V
-5.2V
3R32 3.9KΩ
(VA5-3G) GATE
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VA3
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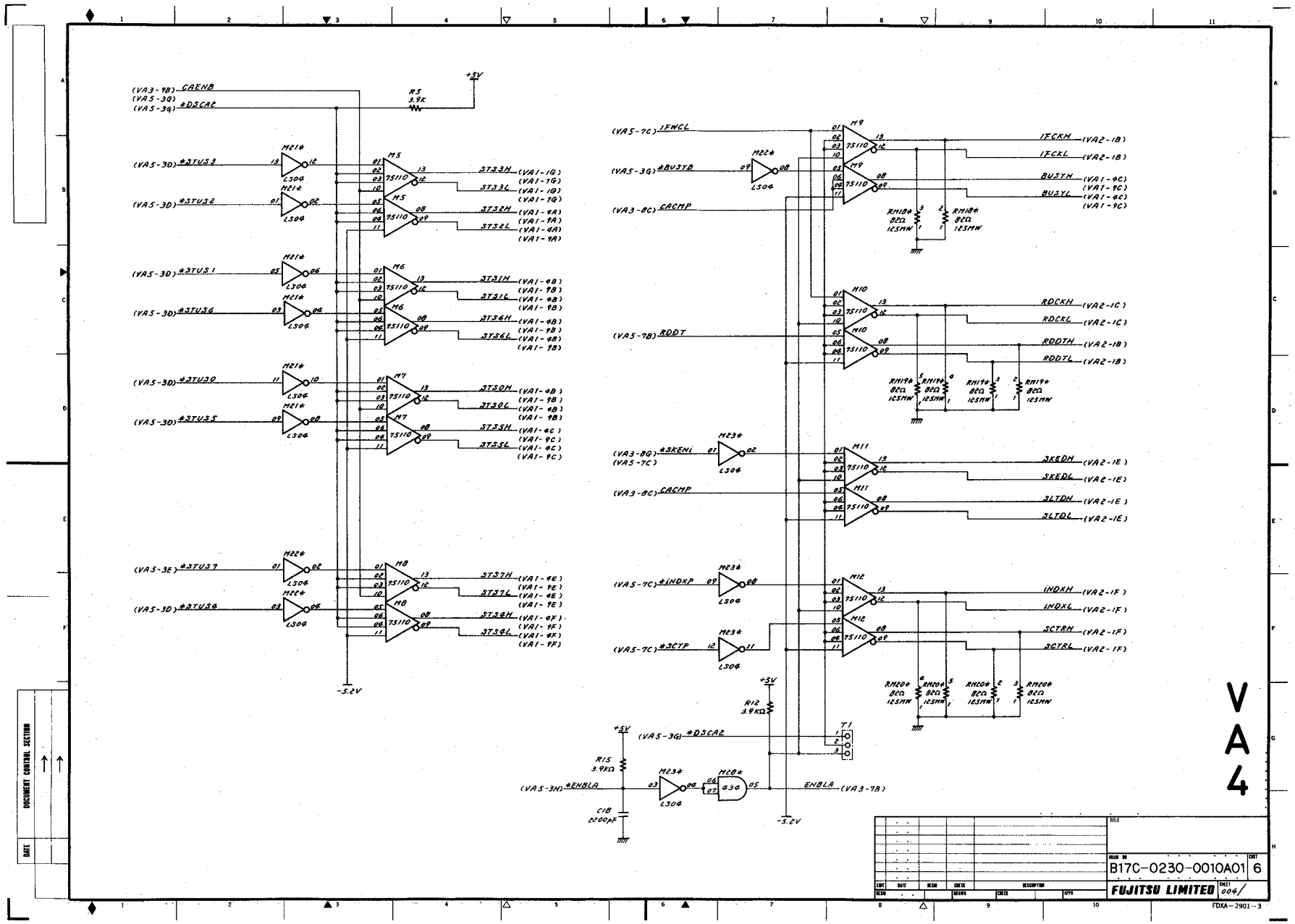
(VA3-9B) CAENB
(VA5-3G)
(VA5-3G) *DSCA2
+5V
R5 3.9K
(VA5-3D) *STUS3
(VA5-3D) *STUS2
(VA5-3D) *STUS1
(VA5-3D) *STUS6
(VA5-3D) *STUS0
(VA5-3D) *STUS5
(VA5-3E) *STUS7
(VA5-3D) *STUS4
M21* LS04
M5 M6 M7 M8 75110
ST33H (VA1-1G)
ST33L (VA1-1G)
ST32H (VA1-9A)
ST32L (VA1-9A)
ST31H (VA1-9B)
ST31L (VA1-9B)
ST36H (VA1-9B)
ST36L (VA1-9B)
ST30H (VA1-9B)
ST30L (VA1-9B)
ST35H (VA1-9C)
ST35L (VA1-9C)
ST37H (VA1-9E)
ST37L (VA1-9E)
ST34H (VA1-9F)
ST34L (VA1-9F)
-5.2V
(VA5-7C) IFWCL
(VA5-3G) *BUSYB
(VA3-8C) CACMP
(VA5-7B) RDDT
(VA3-8G) *SKENi
(VA5-7C)
(VA3-8C) CACMP
(VA5-7C) *iNDXP
(VA5-7C) *SCTP
M22* M23* LS04
M9 M10 M11 M12 75110
IFCKH (VA2-1B)
IFCKL (VA2-1B)
BUSYH (VA1-9C) (VA1-9C)
BUSYL (VA1-9C) (VA1-9C)
RDCKH (VA2-1C)
RDCKL (VA2-1C)
RDDTH (VA2-1B)
RDDTL (VA2-1B)
3KEDH (VA2-1E)
3KEDL (VA2-1E)
3LTDH (VA2-1E)
3LTDL (VA2-1E)
iNDXH (VA2-1F)
iNDXL (VA2-1F)
SCTRH (VA2-1F)
SCTRL (VA2-1F)
RM18* RM19* RM20* 82Ω 125MW
+5V
R12 3.9KΩ
T1
(VA5-3G) *DSCA2
+5V
R15 3.9KΩ
(VA5-3H) *ENBLA
M23* M20* 4.3α
ENBLA (VA3-7B)
C18 2200pF
-5.2V
VA4
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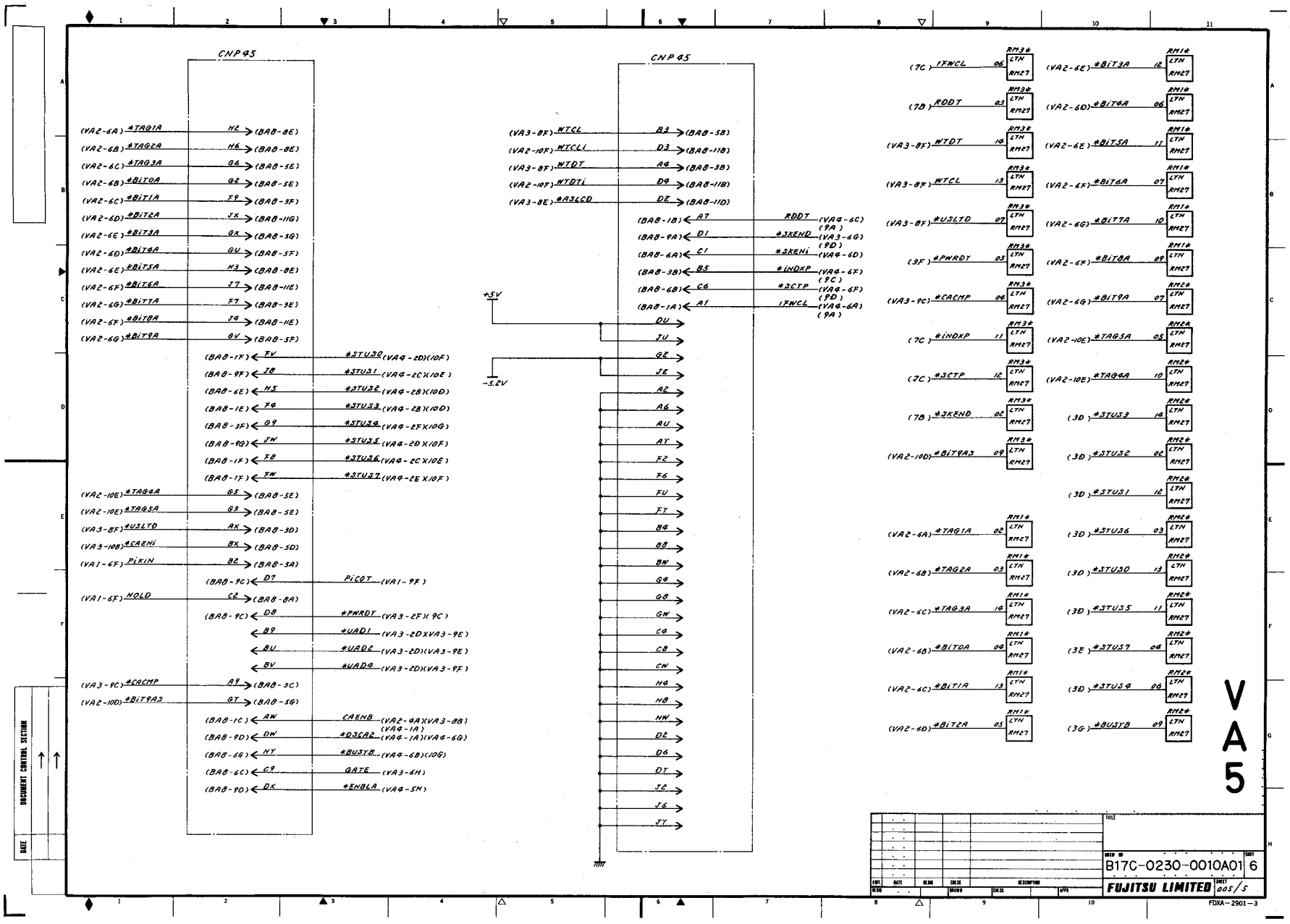
CNP45
CNP45
(VA2-6A) *TAG1A H2 (BAB-8E)
(VA2-6B) *TAG2A H6 (BAB-8E)
(VA2-6C) *TAG3A G4 (BAB-5E)
(VA2-6B) *BIT0A G2 (BAB-5E)
(VA2-6C) *BIT1A F9 (BAB-3F)
(VA2-6D) *BIT2A JX (BAB-11G)
(VA2-6E) *BIT3A GX (BAB-5G)
(VA2-6D) *BIT4A GU (BAB-5F)
(VA2-6E) *BIT5A H3 (BAB-8E)
(VA2-6F) *BIT6A J7 (BAB-11E)
(VA2-6G) *BIT7A F7 (BAB-3E)
(VA2-6F) *BIT8A J4 (BAB-11E)
(VA2-6G) *BIT9A GV (BAB-5F)
(BAB-1F) FV *STUS0 (VA4-2D)(10F)
(BAB-9F) J8 *STUS1 (VA4-2C)X10E)
(BAB-6E) H5 *STUS2 (VA4-2B)X10D)
(BAB-1E) F4 *STUS3 (VA4-2B)X10D)
(BAB-3F) G9 *STUS4 (VA4-2EX10G)
(BAB-9G) JW *STUS5 (VA4-2D)X10F)
(BAB-1F) F8 *STUS6 (VA4-2C)X10E)
(BAB-1F) FW *STUS7 (VA4-2EX10F)
(VA2-10E) *TAG4A G5 (BAB-5E)
(VA2-10E) *TAG5A G3 (BAB-5E)
(VA3-8F) *USLTD AX (BAB-3D)
(VA3-10B) *CAENI BX (BAB-5D)
(VA1-6F) PIKIN B2 (BAB-5A)
(BAB-9C) D7 PICOT (VA1-9F)
(VA1-6F) HOLD C2 (BAB-8A)
(BAB-9C) D8 *PWRDY (VA3-2F)(9C)
B9 *UAD1 (VA3-2D)XVA3-9E)
BU *UAD2 (VA3-2D)(VA3-9E)
BV *UAD4 (VA3-2D)(VA3-9F)
(VA3-9C) *CACMP A9 (BAB-3C)
(VA2-10D) *BIT9A3 GT (BAB-5G)
(BAB-1C) AW CAENB (VA2-9A)X(VA3-8B) (VA4-1A)
(BAB-9D) DW *DSCR2 (VA4-1A)(VA4-6G)
(BAB-6G) HY *BUSYB (VA4-6B)(10G)
(BAB-6C) C9 GATE (VA3-6H)
(BAB-9D) DX *ENBLA (VA4-5H)
(VA3-8F) WTCL B3 (BAB-5B)
(VA2-10F) WTCLi D3 (BAB-11B)
(VA3-8F) WTDT A4 (BAB-3B)
(VA2-10F) WTDTi D4 (BAB-11B)
(VA3-8E) *ASLCD DZ (BAB-11D)
(BAB-1B) A7 RDDT (VA4-6C)(9A)
(BAB-9A) D1 *3KEND (VA3-6G)(9D)
(BAB-6A) C1 *3KENi (VA4-6D)(9C)
(BAB-3B) B5 *iNDXP (VA4-6F)(9D)
(BAB-6B) C6 *3CTP (VA4-6F)(9A)
(BAB-1A) A1 IFWCL (VA4-6A)(9A)
+5V
-5.2V
DU
JU
GZ
JE
A2
A6
AU
AY
F2
F6
FU
FY
B4
B8
BW
G4
G8
GW
C4
C8
CW
H4
H8
HW
D2
D6
DY
J2
J6
JY
(7C) IFWCL RM3* 06
(7B) RDDT RM3* 03
(VA3-8F) WTDT RM3* 10
(VA3-8F) WTCL RM3* 13
(VA3-8F) *USLTD RM3* 07
(3F) *PWRDY RM3* 05
(VA3-9C) *CACMP RM3* 08
(7C) *iNDXP RM3* 11
(7C) *3CTP RM3* 12
(7B) *3KEND RM3* 02
(VA2-10D) *BIT9A3 RM3* 09
(VA2-6A) *TAG1A RM1* 02
(VA2-6B) *TAG2A RM1* 03
(VA2-6C) *TAG3A RM1* 14
(VA2-6B) *BIT0A RM1* 04
(VA2-6C) *BIT1A RM1* 13
(VA2-6D) *BIT2A RM1* 05
(VA2-6E) *BIT3A RM1* 12
(VA2-6D) *BIT4A RM1* 06
(VA2-6E) *BIT5A RM1* 11
(VA2-6F) *BIT6A RM1* 07
(VA2-6G) *BIT7A RM1* 10
(VA2-6F) *BIT8A RM1* 09
(VA2-6G) *BIT9A RM2* 07
(VA2-10E) *TAG5A RM2* 05
(VA2-10E) *TAG4A RM2* 10
(3D) *STUS3 RM2* 14
(3D) *STUS2 RM2* 02
(3D) *STUS1 RM2* 12
(3D) *STUS6 RM2* 03
(3D) *STUS0 RM2* 13
(3D) *STUS5 RM2* 11
(3E) *STUS7 RM2* 04
(3D) *STUS4 RM2* 06
(3G) *BUSYB RM2* 09
RM3* LTN RM27
RM1* LTN RM27
RM2* LTN RM27
VA5
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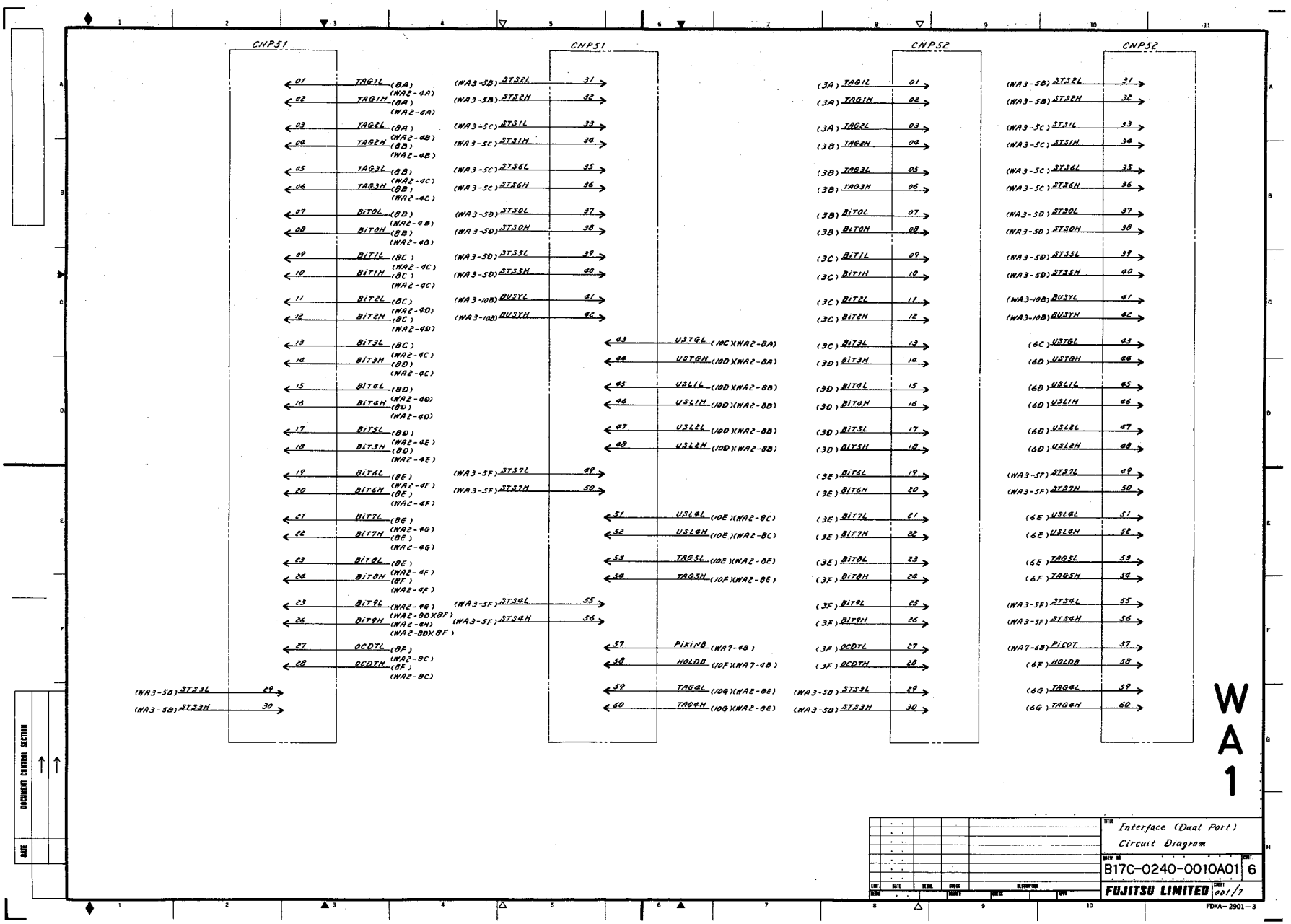
CNP51
CNP51
CNP52
CNP52
TAG1L (8A) (WA2-4A)
TAG1H (8A) (WA2-4A)
TAG2L (8A) (WA2-4B)
TAG2H (8B) (WA2-4B)
TAG3L (8B) (WA2-4C)
TAG3H (8B) (WA2-4C)
BIT0L (8B) (WA2-4B)
BIT0H (8B) (WA2-4B)
BIT1L (8C) (WA2-4C)
BIT1H (8C) (WA2-4C)
BIT2L (8C) (WA2-4D)
BIT2H (8C) (WA2-4D)
BIT3L (8C) (WA2-4C)
BIT3H (8D) (WA2-4C)
BIT4L (8D) (WA2-4D)
BIT4H (8D) (WA2-4D)
BIT5L (8D) (WA2-4E)
BIT5H (8D) (WA2-4E)
BIT6L (8E) (WA2-4F)
BIT6H (8E) (WA2-4F)
BIT7L (8E) (WA2-4G)
BIT7H (8E) (WA2-4G)
BIT8L (8E) (WA2-4F)
BIT8H (8F) (WA2-4F)
BIT9L (WA2-4G) (WA2-8DX8F)
BIT9H (WA2-4H) (WA2-8DX8F)
OCDTL (8F) (WA2-8C)
OCDTH (8F) (WA2-8C)
(WA3-5B) ST32L 31
(WA3-5B) ST32H 32
(WA3-5C) ST31L 33
(WA3-5C) ST31H 34
(WA3-5C) ST36L 35
(WA3-5C) ST36H 36
(WA3-5D) ST30L 37
(WA3-5D) ST30H 38
(WA3-5D) ST33L 39
(WA3-5D) ST33H 40
(WA3-10B) BUSYL 41
(WA3-10B) BUSYH 42
(WA3-5F) ST37L 49
(WA3-5F) ST37H 50
(WA3-5F) ST34L 55
(WA3-5F) ST34H 56
(WA3-5B) ST32L 29
(WA3-5B) ST32H 30
USTGL (10CXWA2-8A) 43
USTGH (10DXWA2-8A) 44
USLIL (10DXWA2-8B) 45
USLIH (10DXWA2-8B) 46
USL2L (10DXWA2-8B) 47
USL2H (10DXWA2-8B) 48
USL9L (10EXWA2-8C) 51
USL9H (10EXWA2-8C) 52
TAG5L (10EXWA2-8E) 53
TAG5H (10FXWA2-8E) 54
PiKiN8 (WA7-4B) 57
HOLD8 (10FXWA7-4B) 58
TAG4L (10GXWA2-8E) 59
TAG4H (10GXWA2-8E) 60
(3A) TAG1L 01
(3A) TAG1H 02
(3A) TAG2L 03
(3B) TAG2H 04
(3B) TAG3L 05
(3B) TAG3H 06
(3B) BIT0L 07
(3B) BIT0H 08
(3C) BIT1L 09
(3C) BIT1H 10
(3C) BIT2L 11
(3C) BIT2H 12
(3C) BIT3L 13
(3D) BIT3H 14
(3D) BIT4L 15
(3D) BIT4H 16
(3D) BIT5L 17
(3D) BIT5H 18
(3E) BIT6L 19
(3E) BIT6H 20
(3E) BIT7L 21
(3E) BIT7H 22
(3E) BIT8L 23
(3F) BIT8H 24
(3F) BIT9L 25
(3F) BIT9H 26
(3F) OCDTL 27
(3F) OCDTH 28
(WA3-5B) ST33L 29
(WA3-5B) ST33H 30
(WA3-5B) ST32L 31
(WA3-5B) ST32H 32
(WA3-5C) ST31L 33
(WA3-5C) ST31H 34
(WA3-5C) ST36L 35
(WA3-5C) ST36H 36
(WA3-5B) ST30L 37
(WA3-5D) ST30H 38
(WA3-5D) ST33L 39
(WA3-5D) ST33H 40
(WA3-10B) BUSYL 41
(WA3-10B) BUSYH 42
(6C) USTGL 43
(6D) USTGH 44
(6D) USLIL 45
(6D) USLIH 46
(6D) USL2L 47
(6D) USL2H 48
(WA3-5F) ST37L 49
(WA3-5F) ST37H 50
(6E) USL9L 51
(6E) USL9H 52
(6E) TAG5L 53
(6F) TAG5H 54
(WA3-5F) ST34L 55
(WA3-5F) ST34H 56
(WA7-6B) PICOT 57
(6F) HOLD8 58
(6G) TAG4L 59
(6G) TAG4H 60
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Interface (Dual Port)
Circuit Diagram
B17C-0240-0010A01
6
FUJITSU LIMITED
001/1
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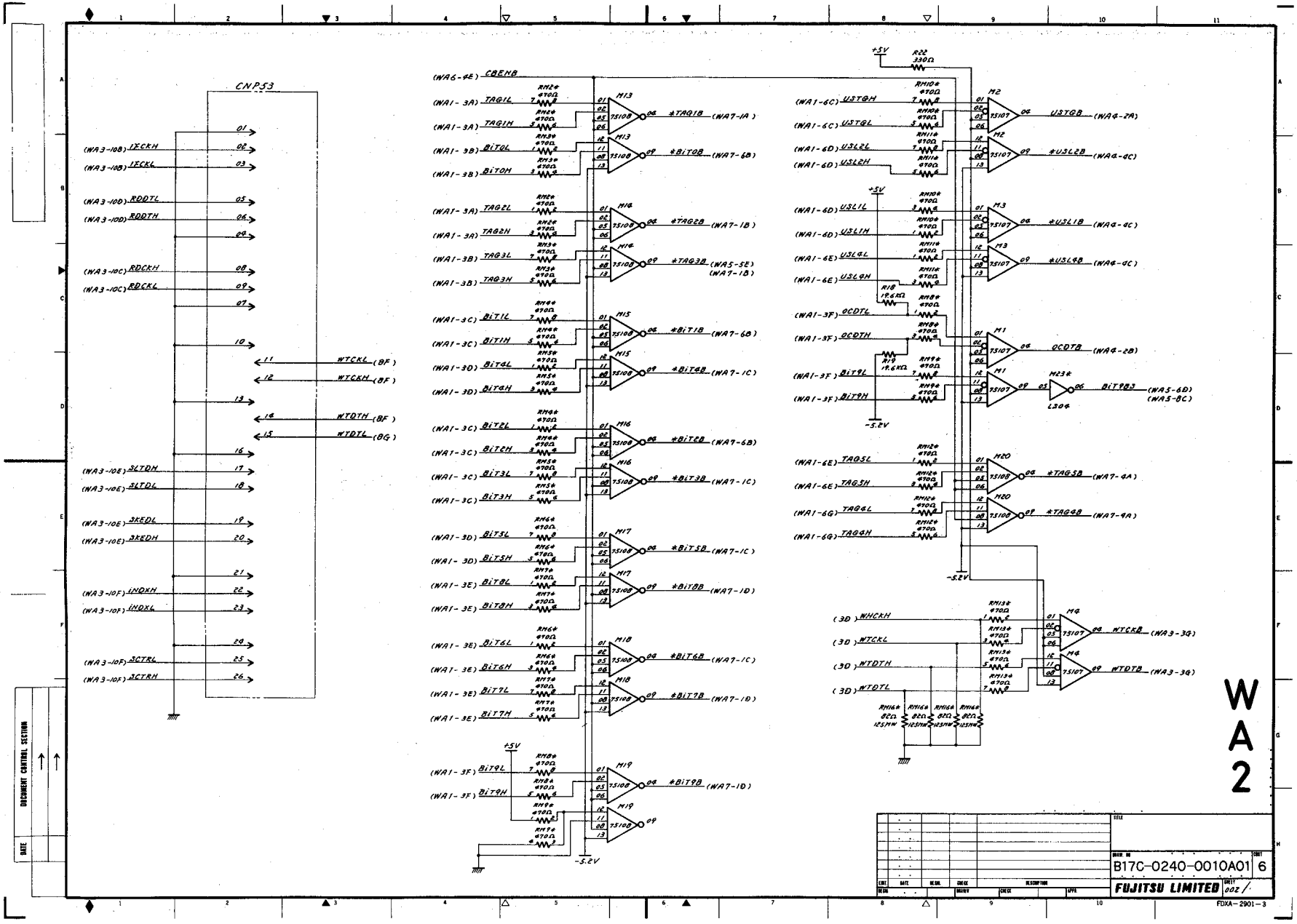
CNP53
WA2
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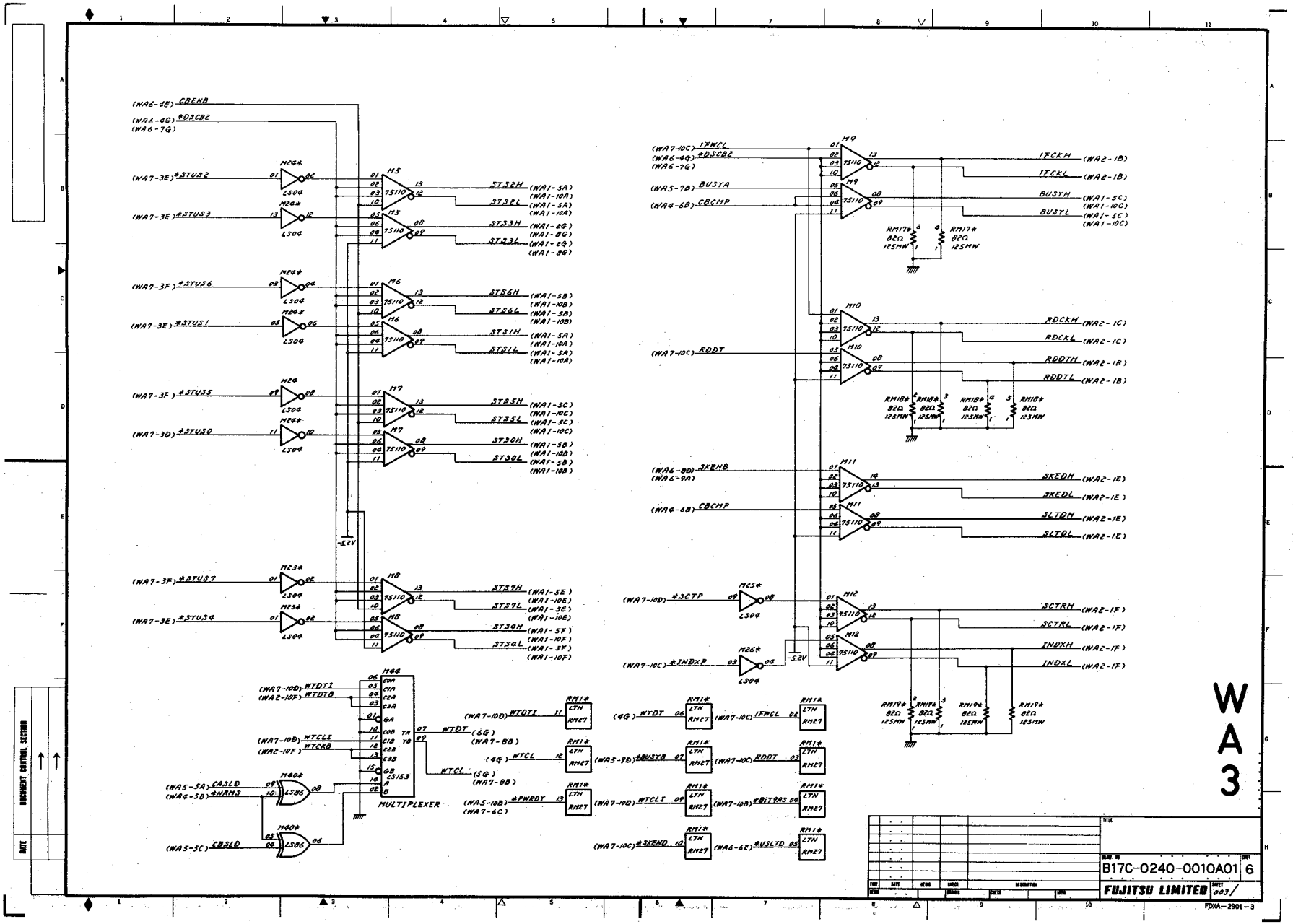
FUJITSU LIMITED
FDXA-2901-3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MULTIPLEXER
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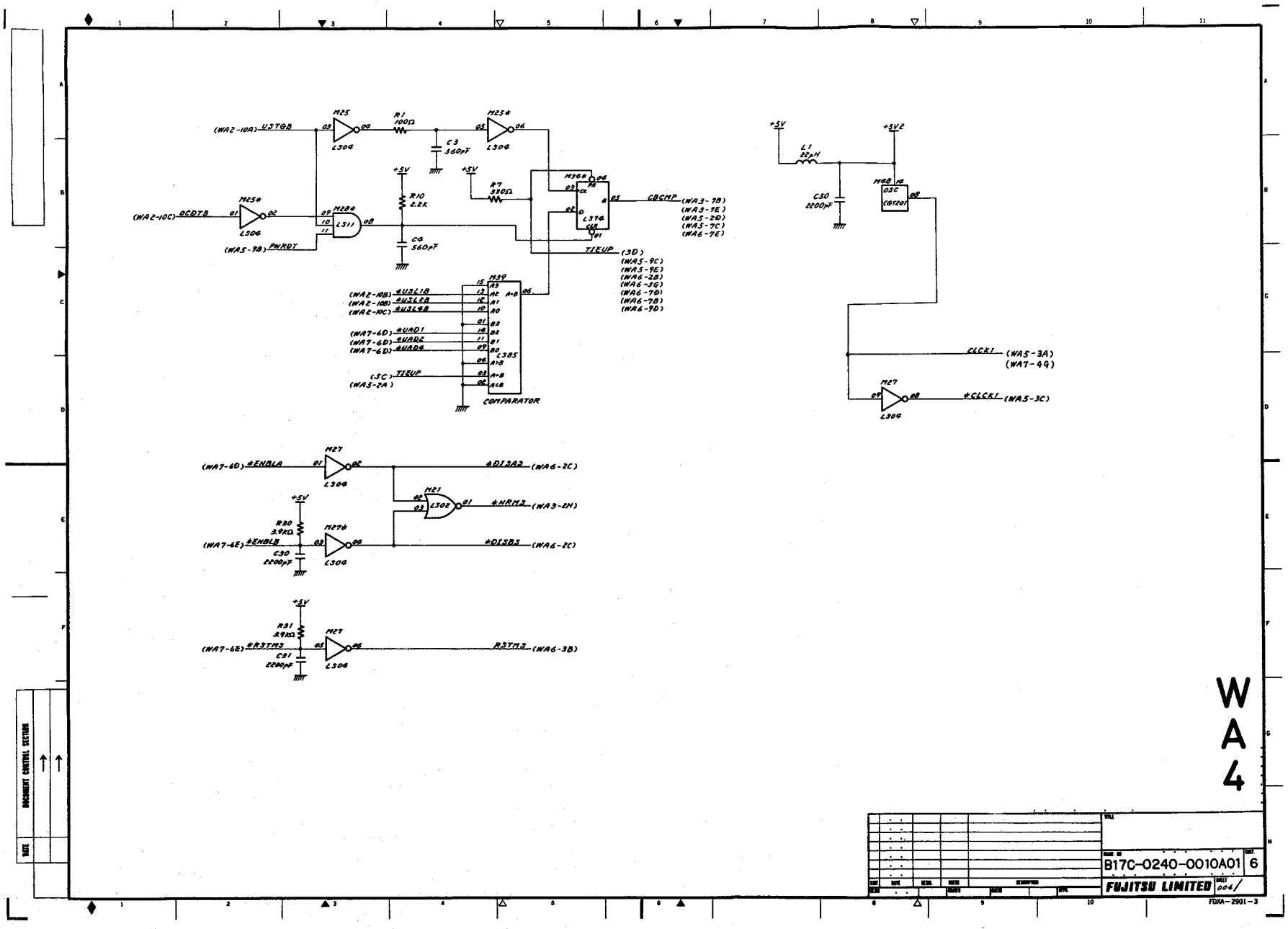
(WA2-10A) U3TGB
M25
LS04
R1 100Ω
C3 360pF
M25*
LS04
+5V
R10 2.2K
M25*
(WA2-10C) DCDTB
LS04
M28*
LS11
(WA5-9B) PWRDY
C6 560pF
+5V
R7 330Ω
M36*
LS74
CBCMP
(WA3-7B)
(WA3-9E)
(WA5-2D)
(WA5-7C)
(WA6-7E)
TIEUP
(3D)
(WA5-9C)
(WA5-9E)
(WA6-2B)
(WA6-3G)
(WA6-7D)
(WA6-7B)
(WA6-9D)
M39
LS85
COMPARATOR
(WA2-10B) *U3L1B
(WA2-10B) *U3L0B
(WA2-10C) *U3L9B
(WA7-6D) *UAD1
(WA7-6D) *UAD2
(WA7-6D) *UAD0
(3C) TIEUP
(WA5-2A)
+5V
L1 22μH
C50 2200pF
M48
OSC
CG7201
+5V2
CLCK1 (WA5-3A)
(WA7-4G)
M27
LS04
*CLCK1 (WA5-3C)
(WA7-6D) *ENBLA
M27
LS04
*DISA2 (WA6-2C)
M21
LS02
*NRM3 (WA3-2H)
+5V
R30 2.9KΩ
(WA7-6E) *ENBLB
M27*
LS04
C30 2200pF
*DISBS (WA6-2C)
+5V
R31 2.9KΩ
(WA7-6E) *RSTM3
M27
LS04
C31 2200pF
RSTM3 (WA6-3B)
DOCUMENT CONTROL SECTION
DATE
WA4
B17C-0240-0010A01
6
FUJITSU LIMITED
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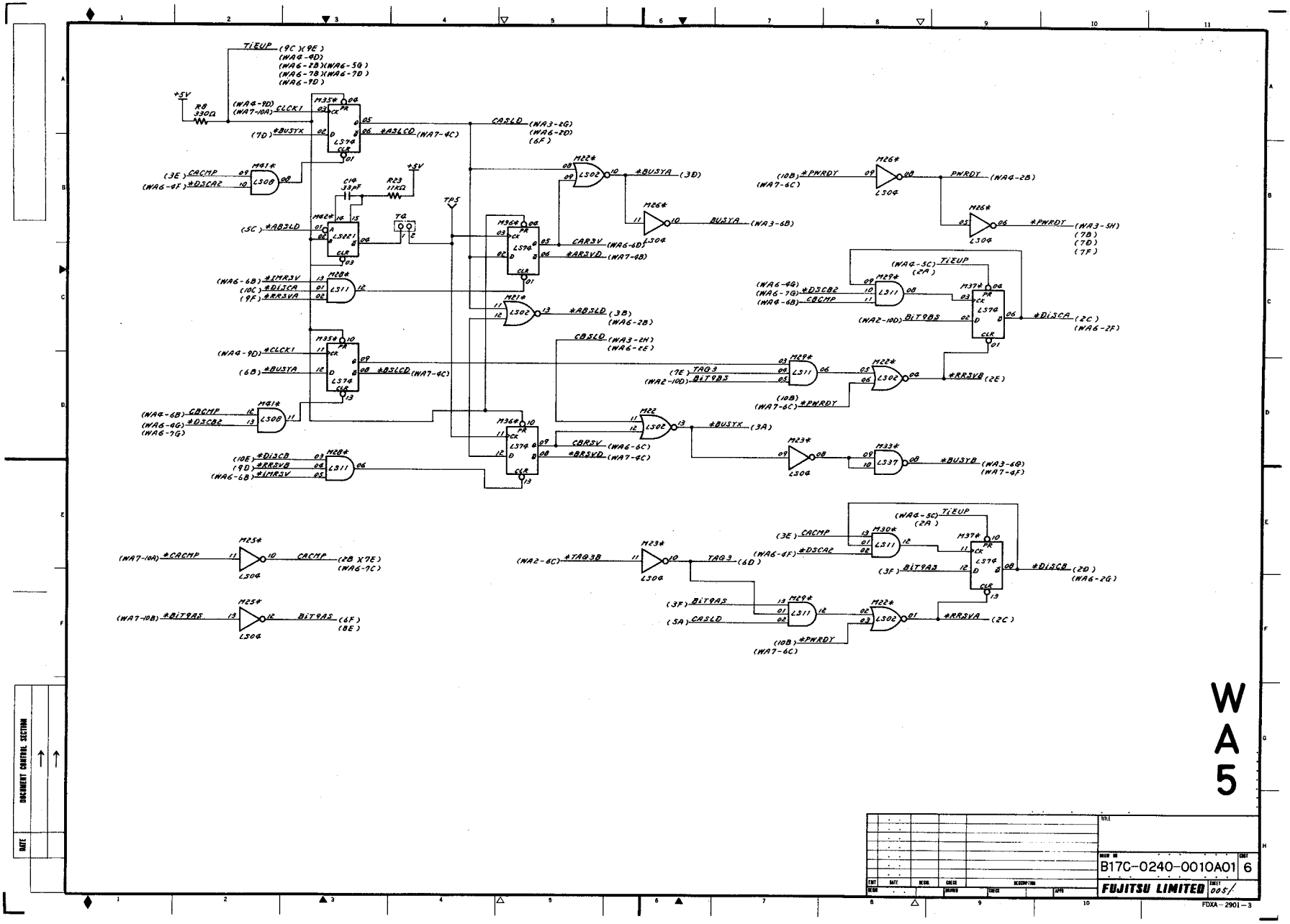
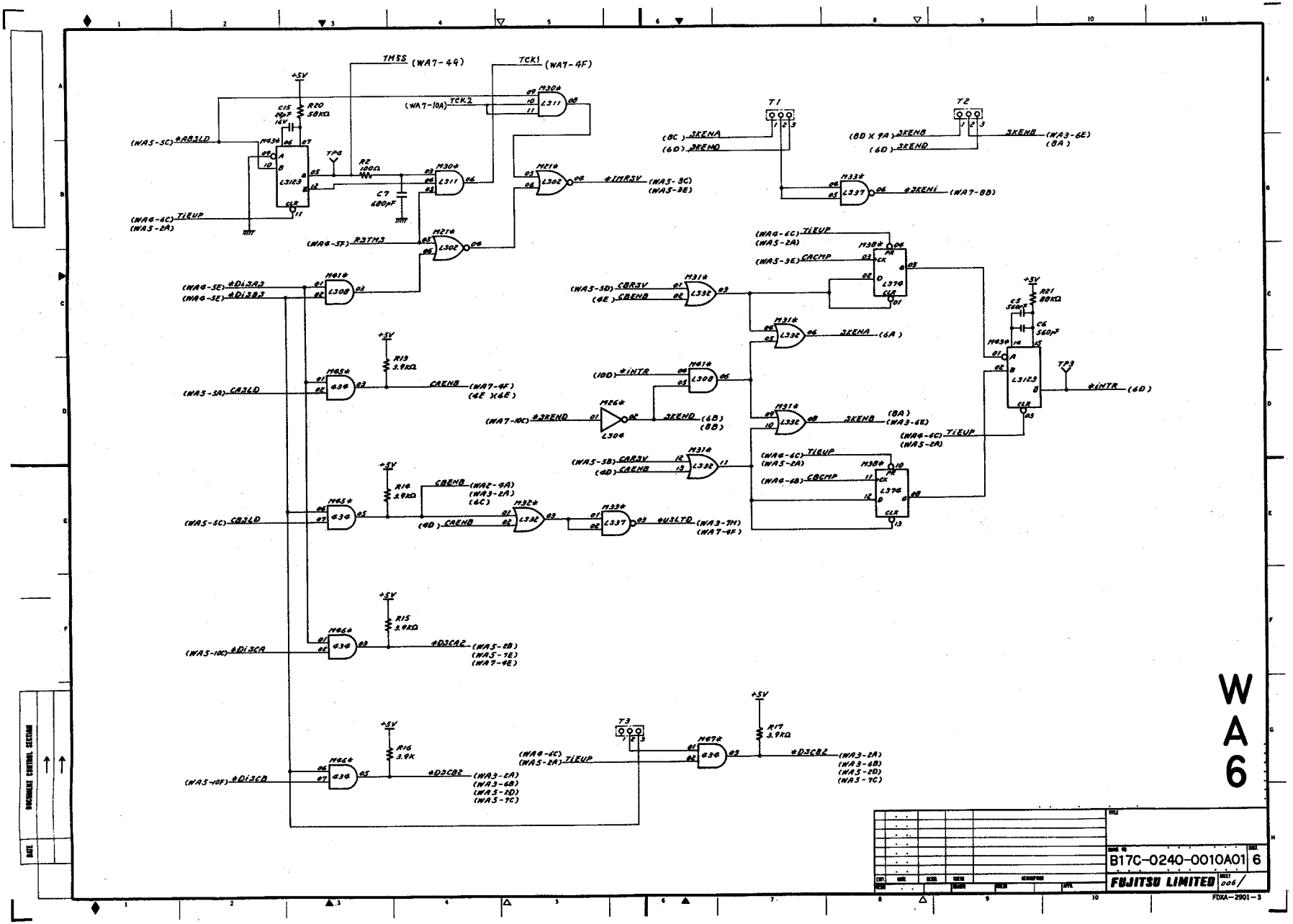
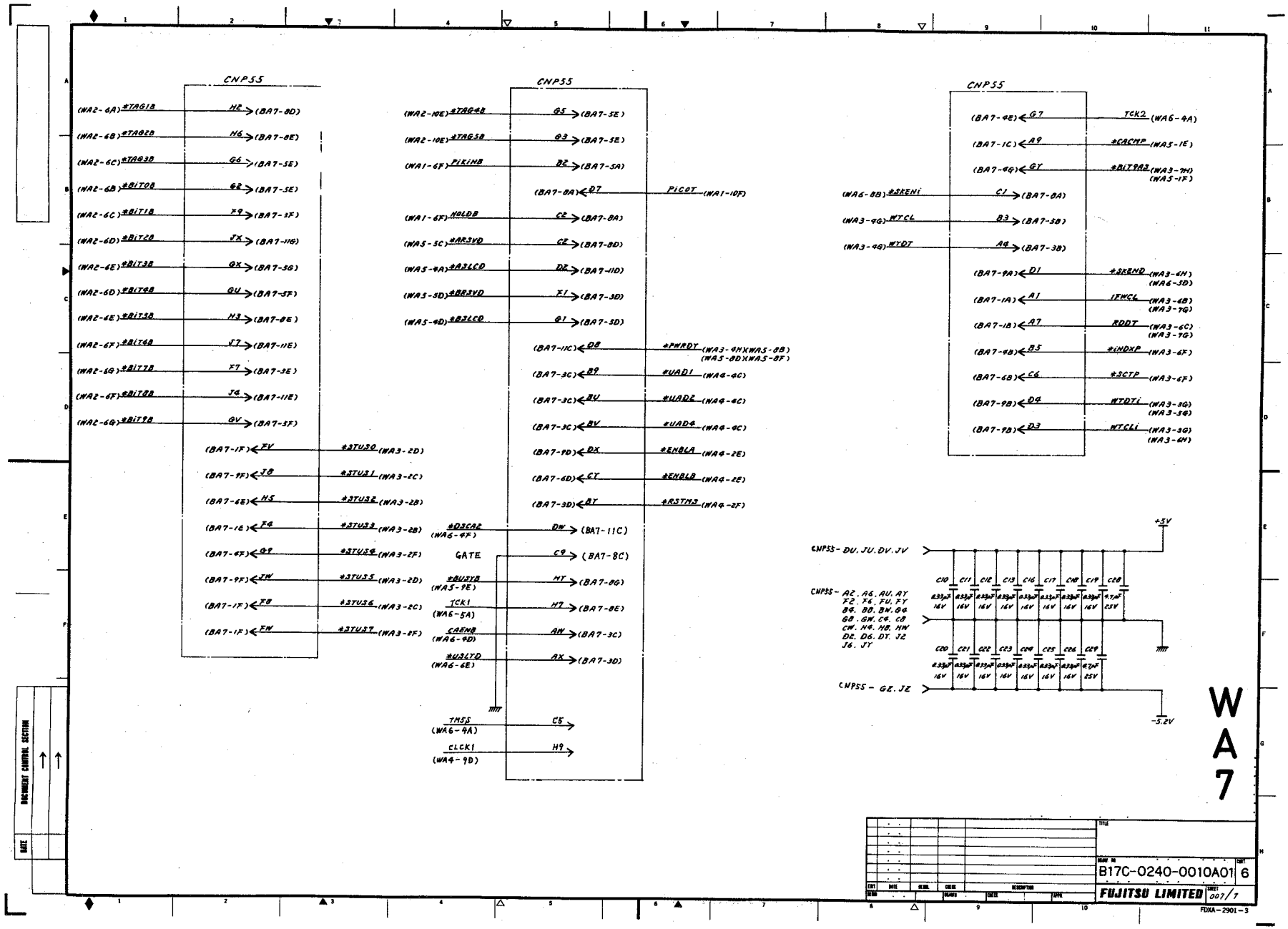

TiEUP
CASLD
CBSLD
CARSV
CBRSV
*BUSYA
*BUSYB
BUSYA
*ABSLD
*ABSLCD
*ARSVD
*BRSVD
*RRSVA
*RRSVB
*DiSCA
*DiSCB
PWRDY
*PWRDY
CACMP
CBCMP
TAG3
BIT9BS
BIT9AS
*DSCA2
*DSCB2
*IMRSV
*CLCK1
TP5
WA5
B17C-0240-0010A01
FUJITSU LIMITED
FDXA-2901-3


TMSS (WA7-4G)
TCK1 (WA7-4F)
TCK2 (WA7-10A)
+5V
C15 10pF 16V
R20 50KΩ
(WA5-5C) *ABSLD
M43*
TP6
R2 100Ω
C7 680pF
M30* LS11
M21* LS02
*IMRSV (WA5-9C) (WA5-3E)
(WA6-6C) TIEUP (WA5-2A)
(WA6-5F) R3TM3
(WA6-5E) *DiSA3
(WA6-5E) *DiSB3
M01* LS08
M45* 43G
(WA5-5A) CA3LD
R13 3.9KΩ
CAENB (WA7-4F) (4E)(6E)
(WA5-5C) CB3LD
R14 3.9KΩ
CBENB (WA2-9A) (WA3-2A) (6C)
(4D) CAENB
M32* LS32
M33* LS37
*U3LTD (WA3-7H) (WA7-4F)
(WA5-10C) *DiSCA
M46* 43G
R15 3.9KΩ
*D3CA2 (WA5-2B) (WA5-7E) (WA7-4E)
(WA5-10F) *DiSCB
M66* 43G
R16 3.9K
*D3CB2 (WA3-2A) (WA3-6B) (WA5-2D) (WA5-7C)
T1
T2
T3
(8C) *3KENA
(6D) *3KEND
(8D X 9A) *3KENB
(6D) *3KEND
*3KENB (WA3-6E) (8A)
M33* LS37
*3KENi (WA7-8B)
(WA6-6C) TIEUP (WA5-2A)
(WA5-3E) CACMP
M30* LS74
(WA5-5D) CBRSV
(4E) CBENB
M31* LS32
*3KENA (6A)
(WA6-6C) TIEUP (WA5-2A)
(WA6-6B) CBCMP
M30* LS74
(WA5-5B) CARSV
(4D) CAENB
M31* LS32
(8D) *iNTR
M01* LS08
(WA7-10C) *3KEND
M26* LS04
3KEND (6B) (8B)
M31* LS32
3KENB (8A) (WA3-6E)
(WA6-6C) TIEUP (WA5-2A)
+5V
R21 88KΩ
C5 560pF
C6 560pF
M43* LS123
TP3
*iNTR (6D)
(WA6-6C) TIEUP (WA5-2A)
M67* 43G
R17 3.9KΩ
*D3CB2 (WA3-2A) (WA3-6B) (WA5-2D) (WA5-7C)
DOCUMENT CONTROL SECTION
DATE
W A 6
B17C-0240-0010A01 6
FUJITSU LIMITED
FDXA-2901-3


CNP55
CNP55
CNP55
GATE
+5V
-5.2V
WA7
FUJITSU LIMITED
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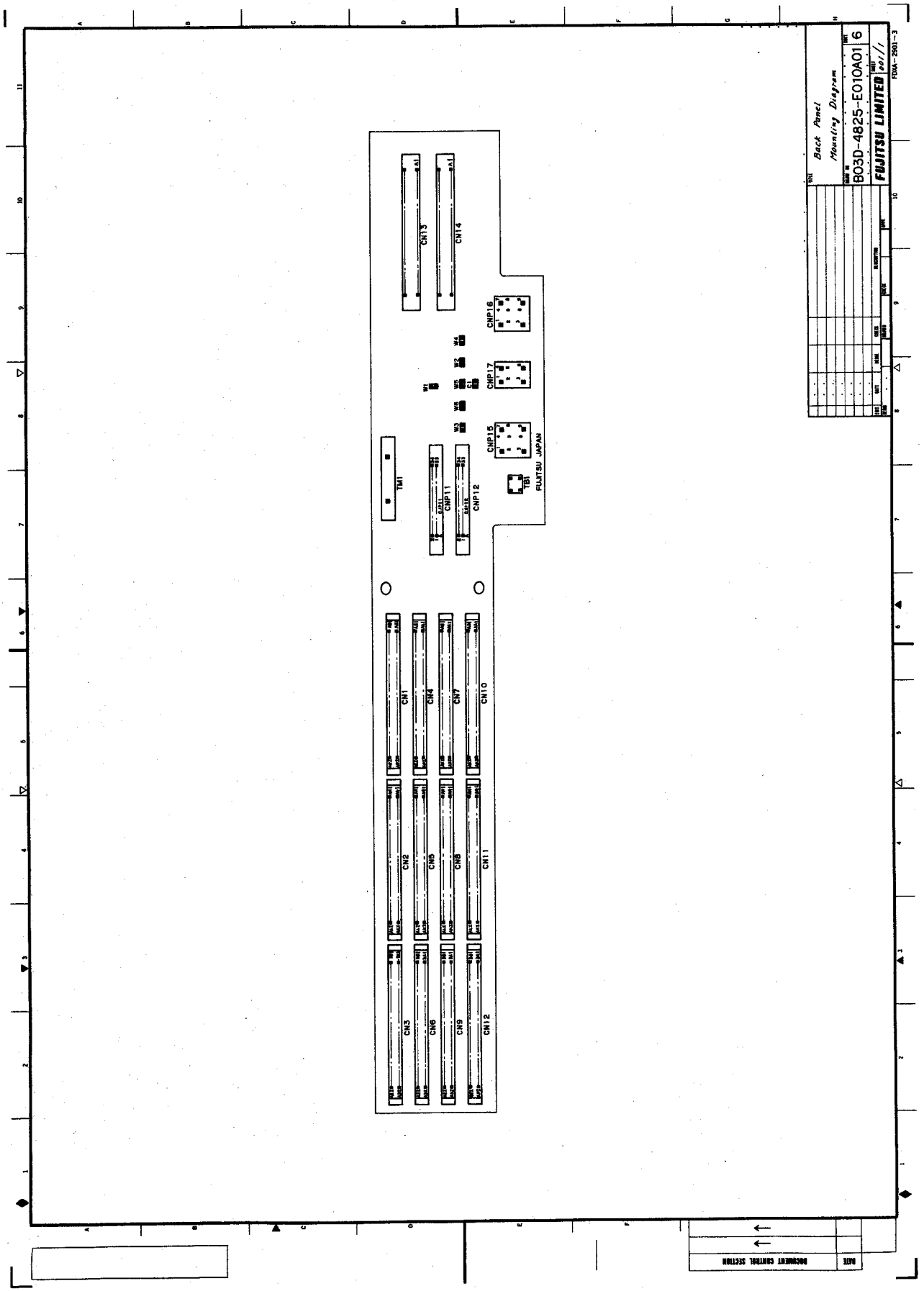
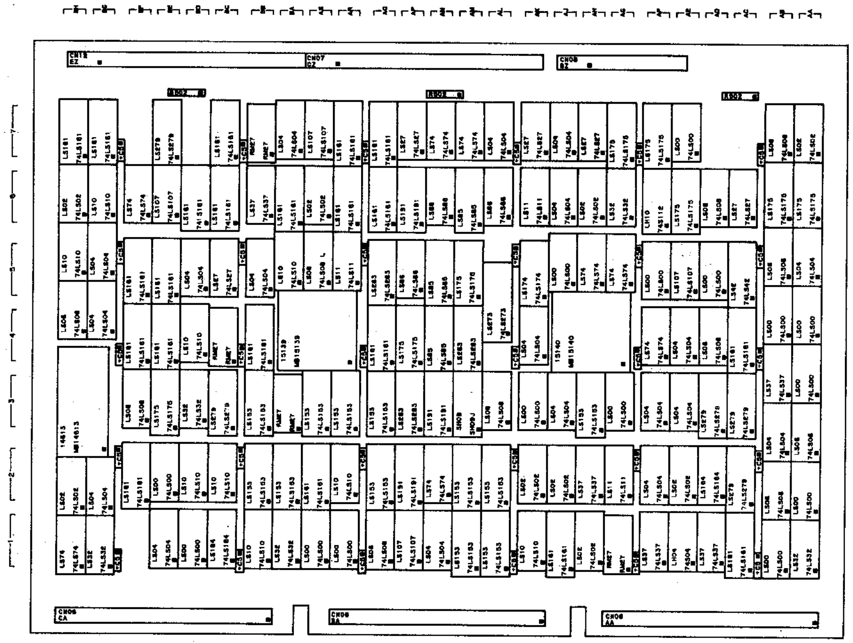

Back Panel
Mounting Diagram
B03D-4825-E010A01
6
FUJITSU LIMITED
FUJITSU JAPAN
CN1
CN2
CN3
CN4
CN5
CN6
CN7
CN8
CN9
CN10
CN11
CN12
CN13
CN14
CNP11
CNP12
CNP15
CNP16
CNP17
TB1
TM1



Logic Circuit Mounting Diagram

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DOCUMENT CONTROL SECTION

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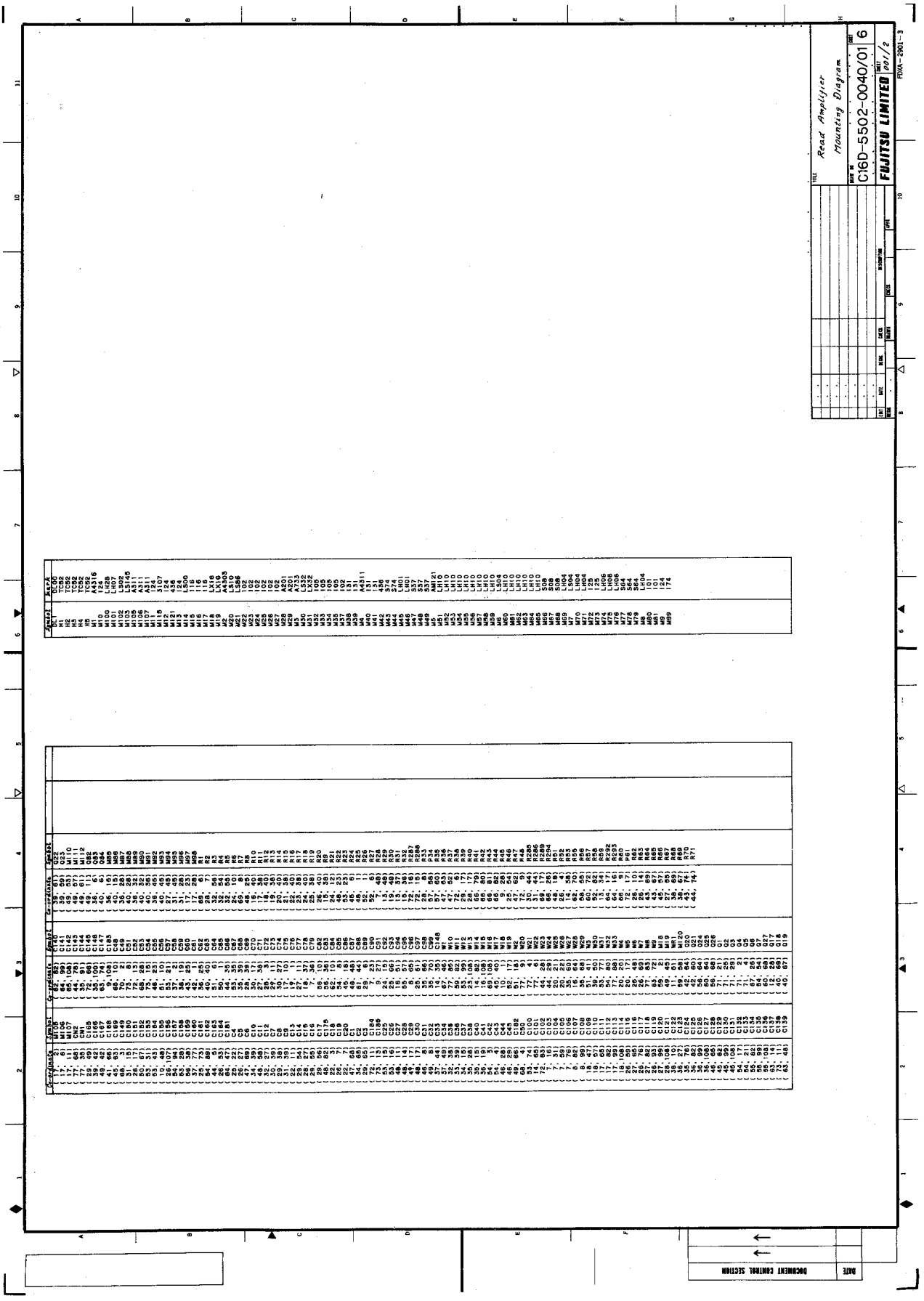
Read Amplifier
Mounting Diagram
C16D-5502-0040/01
FUJITSU LIMITED
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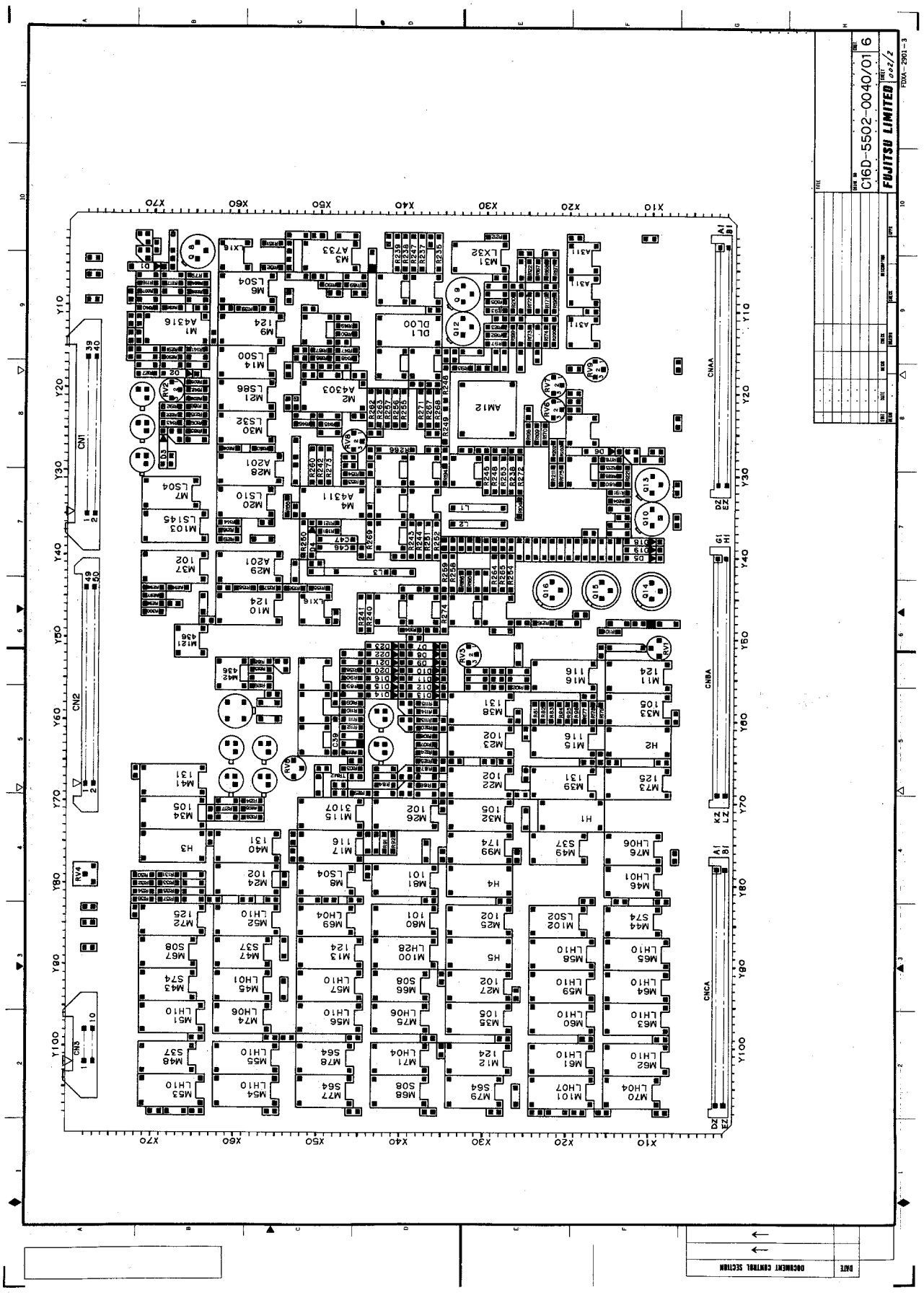
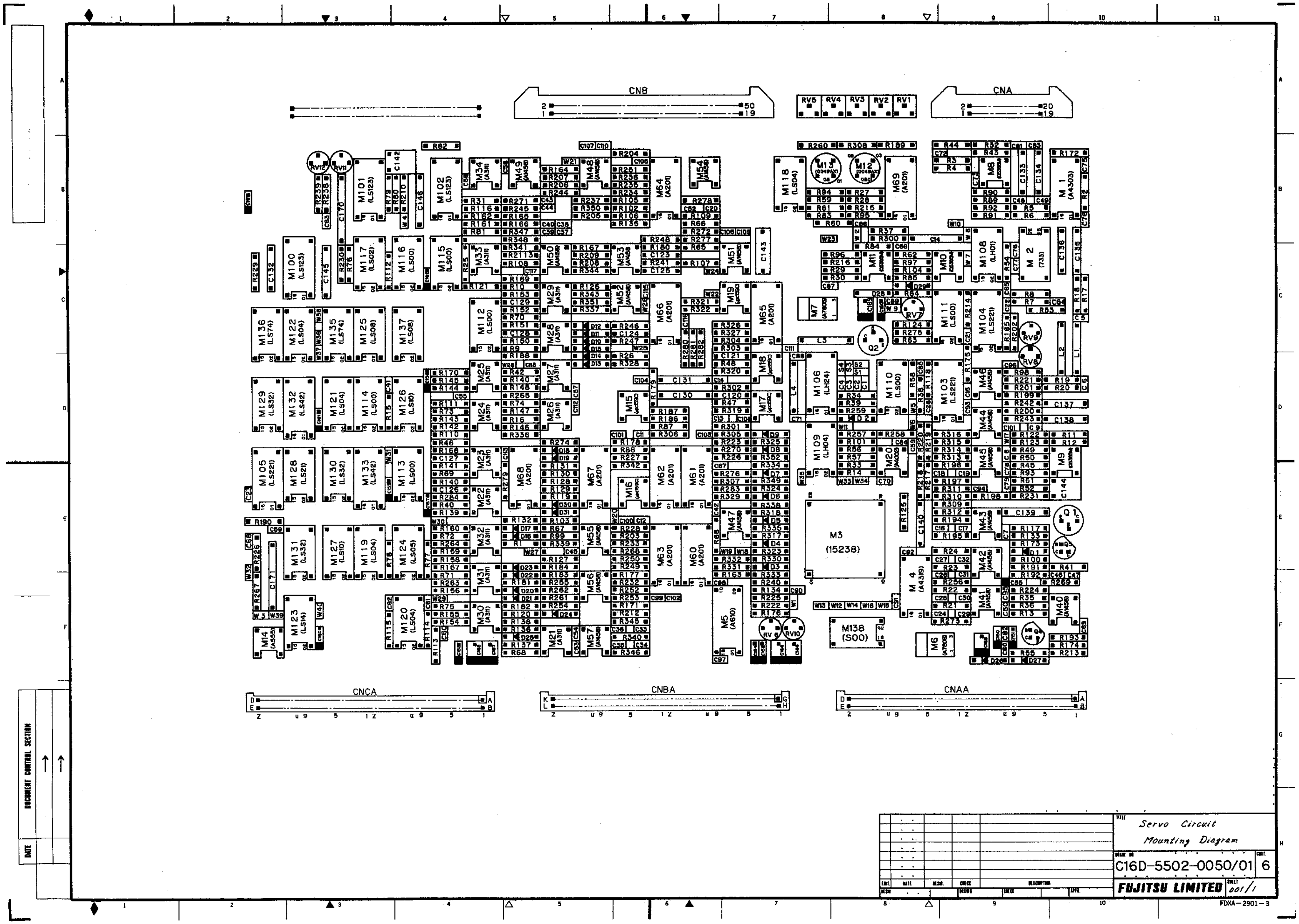
DOCUMENT CONTROL SECTION
DATE


FUJITSU LIMITED
C16D-5502-0040/01
CN1
CN2
CN3
CNAA
CNBA
CNCA
RV1
RV2
RV3
RV4
RV5
RV6


DATE
DOCUMENT CONTROL SECTION
CNB
CNA
CNCA
CNBA
CNAA
Servo Circuit
Mounting Diagram
C16D-5502-0050/01
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FUJITSU LIMITED
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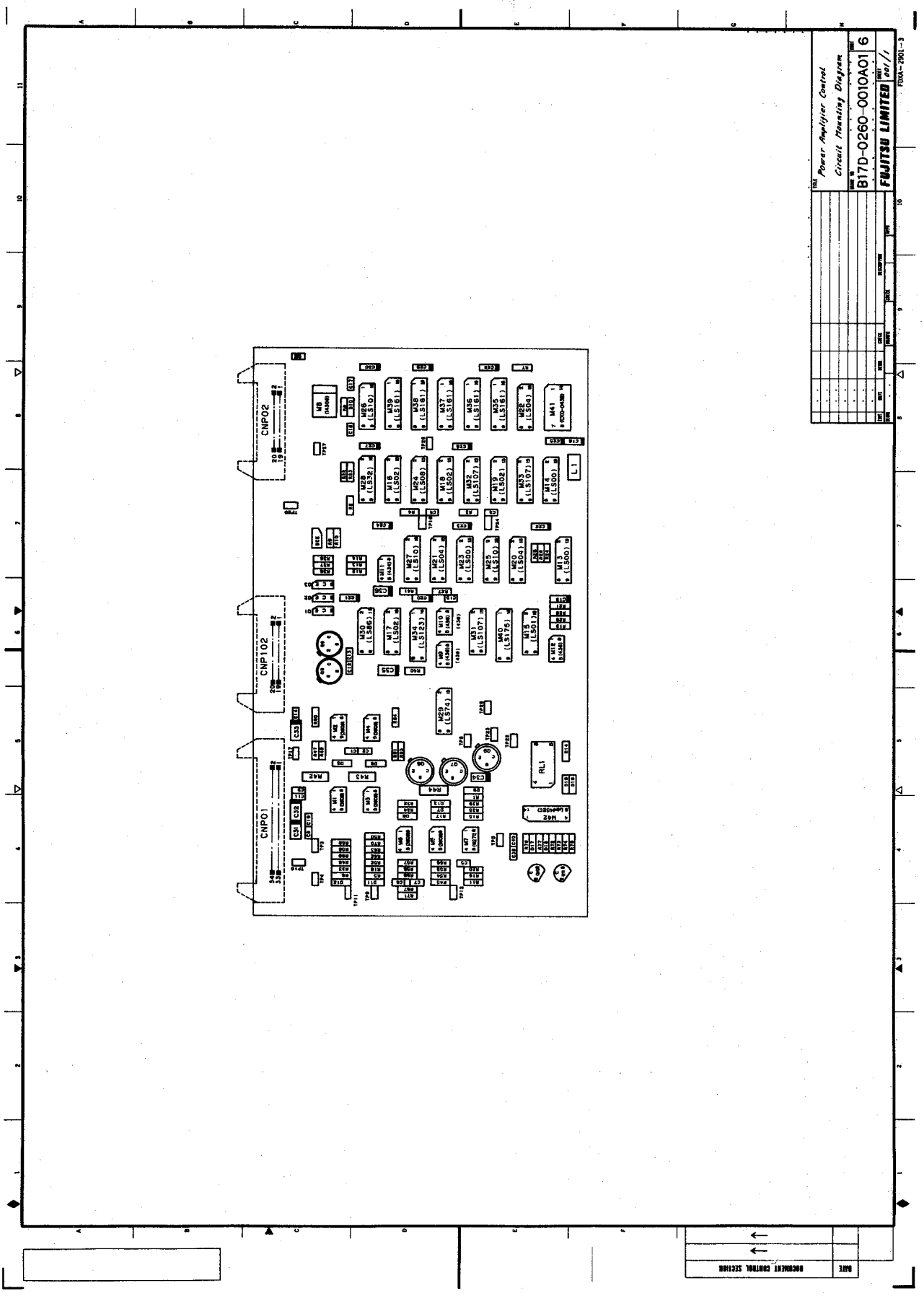
Power Amplifier Control
Circuit Mounting Diagram
B17D-0260-0010A01
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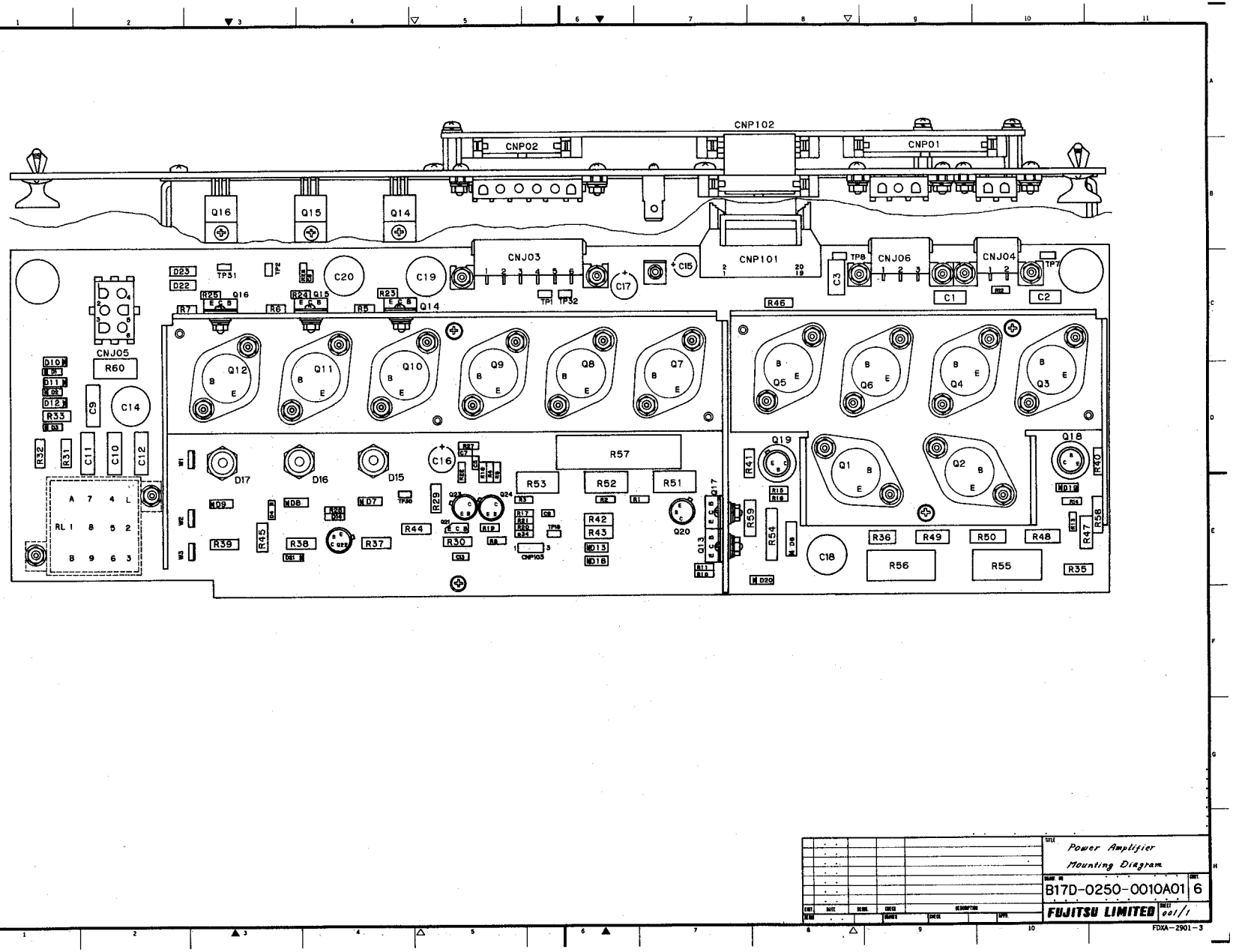
FUJITSU LIMITED
CNP02
CNP102
CNP01
DOCUMENT CONTROL SECTION
DATE


CNP102
CNP02
CNP01
Q16
Q15
Q14
CNJ03
CNP101
CNJ06
CNJ04
CNJ05
R60
C14
C9
C11
C10
C12
C20
C19
C15
C17
C16
C18
C3
C1
C2
R46
R57
R53
R52
R51
R56
R55
R36
R49
R50
R48
R35
Q12
Q11
Q10
Q9
Q8
Q7
Q5
Q6
Q4
Q3
Q19
Q18
Q1
Q2
Q17
Q20
D17
D16
D15
TP31
TP32
TP1
TP2
TP7
TP8
Power Amplifier
Mounting Diagram
B17D-0250-0010A01
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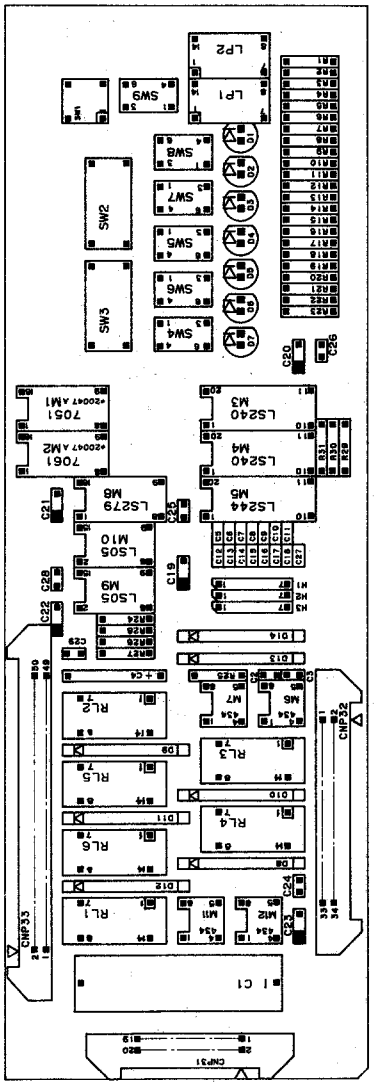
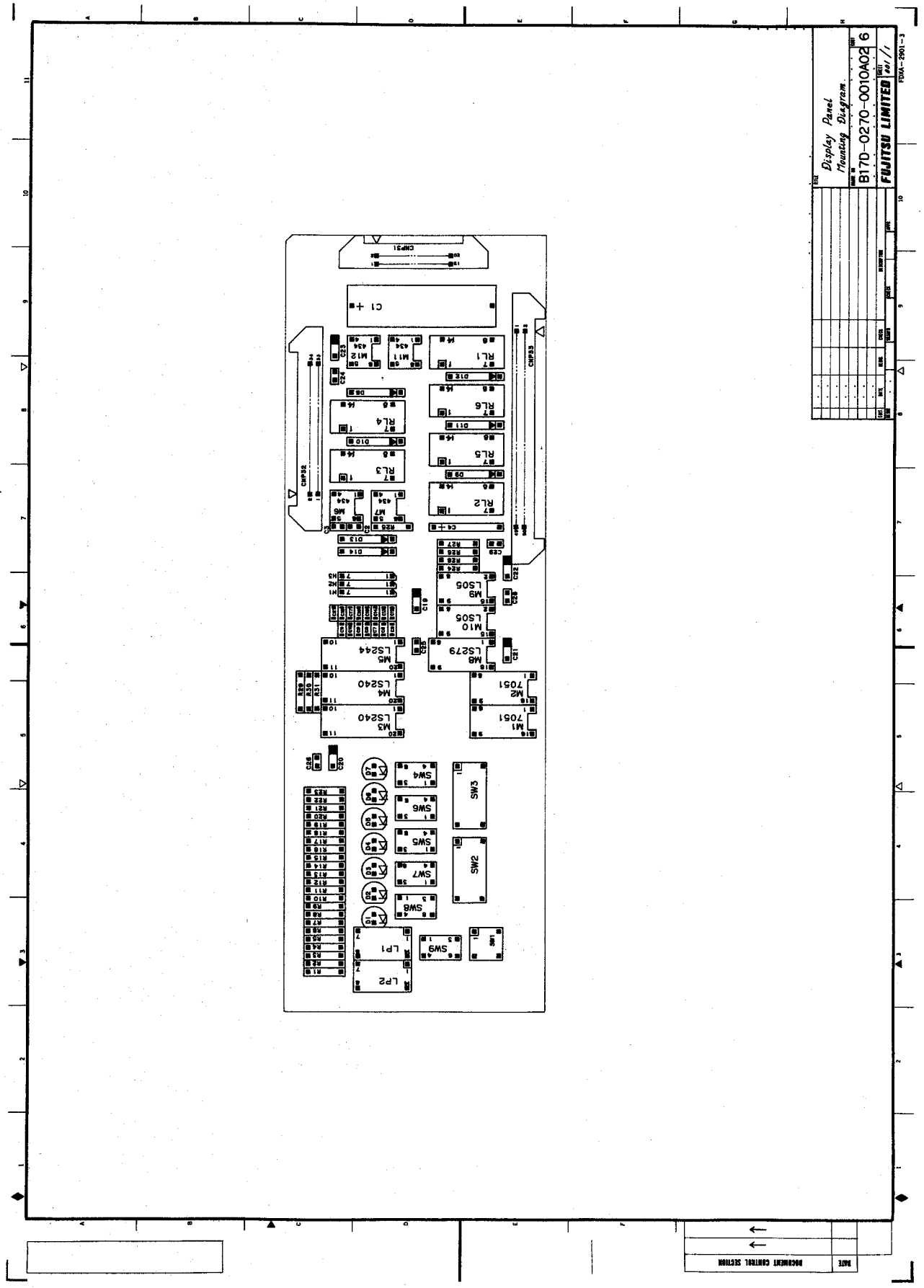
FUJITSU LIMITED
FDXA-2901-3


LP2
LP1
SW9
SW8
SW7
SW5
SW6
SW4
SW2
SW3
C20
C26
7051
7061
LS240
M3
LS240
M4
LS244
M5
LS279
M8
LS05
M10
LS05
M9
C21
C28
C22
C19
RL2
RL3
RL5
RL4
RL6
RL1
M6
M7
M11
M12
C24
C23
CNP32
CNP33
IC1
CNP31


Display Panel Mounting Diagram.
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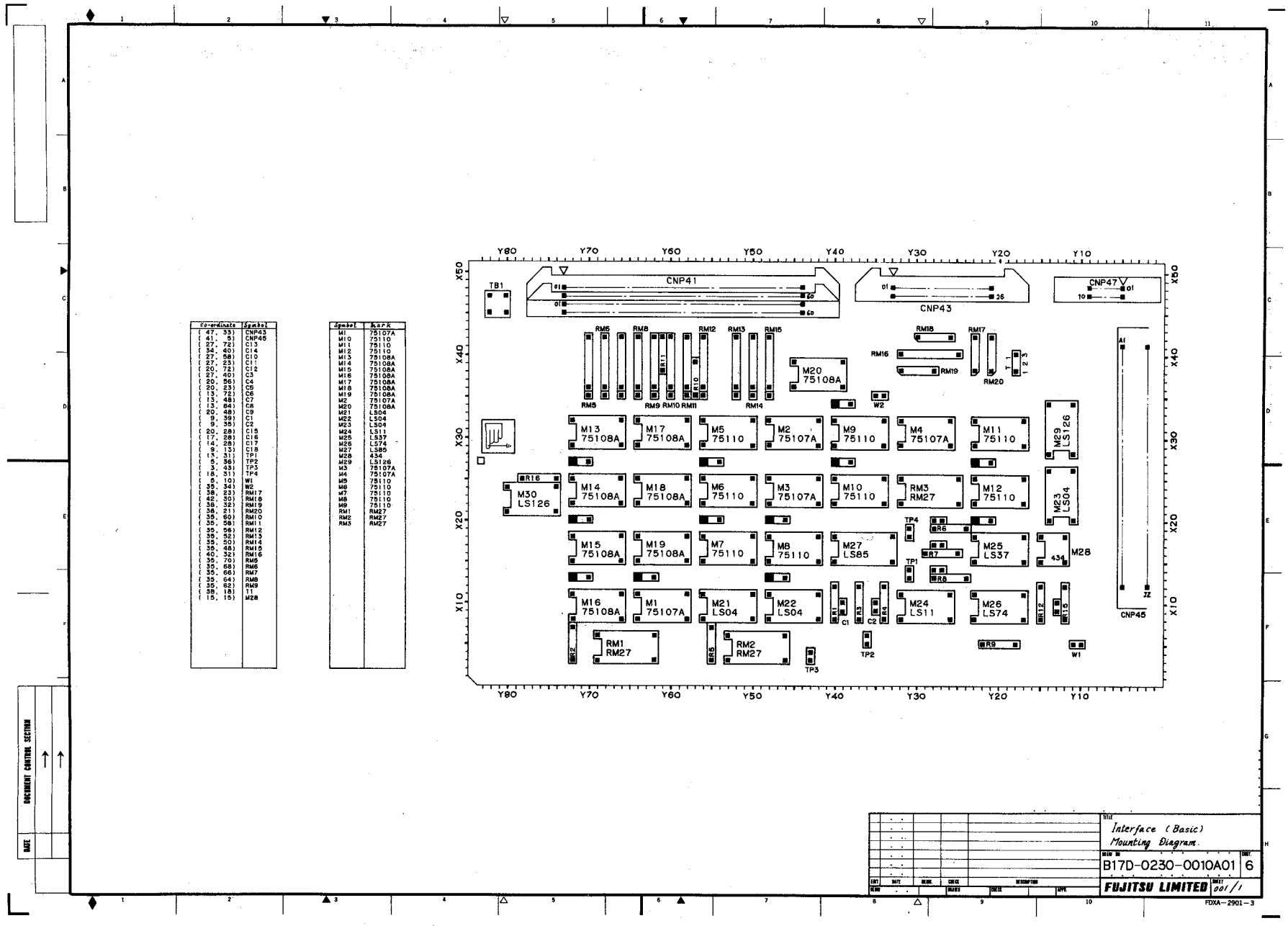

Co-ordinate	Symbol
(47, 35)	CNP43
(41, 5)	CNP45
(27, 72)	C13
(34, 40)	C14
(27, 58)	C10
(27, 23)	C11
(20, 72)	C12
(27, 40)	C3
(20, 56)	C4
(20, 23)	C5
(13, 72)	C6
(13, 48)	C7
(13, 64)	C8
(20, 48)	C9
(9, 39)	C1
(9, 55)	C2
(20, 28)	C15
(17, 28)	C16
(14, 28)	C17
(9, 13)	C18
(1, 31)	TP1
(5, 36)	TP2
(3, 63)	TP3
(18, 21)	TP4
(6, 10)	W1
(39, 34)	W2
(38, 23)	RM17
(42, 30)	RM18
(38, 32)	RM19
(38, 21)	RM20
(39, 60)	RM10
(35, 58)	RM11
(35, 56)	RM12
(39, 52)	RM13
(35, 50)	RM14
(38, 48)	RM15
(40, 52)	RM16
(35, 70)	RM5
(35, 68)	RM6
(35, 66)	RM7
(35, 64)	RM8
(35, 62)	RM9
(38, 18)	11
(15, 15)	M28

Symbol	Mark
M1	75107A
M10	75110
M11	75110
M12	75110
M13	75108A
M14	75108A
M15	75108A
M16	75108A
M17	75108A
M18	75108A
M19	75108A
M2	75107A
M20	75108A
M21	LS04
M22	LS04
M23	LS04
M24	LS11
M25	LS37
M26	LS74
M27	LS85
M28	434
M29	LS126
M3	75107A
M4	75107A
M5	75110
M6	75110
M7	75110
M8	75110
M9	75110
RM1	RM27
RM2	RM27
RM3	RM27

DOCUMENT CONTROL SECTION

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Interface (Basic) Mounting Diagram.

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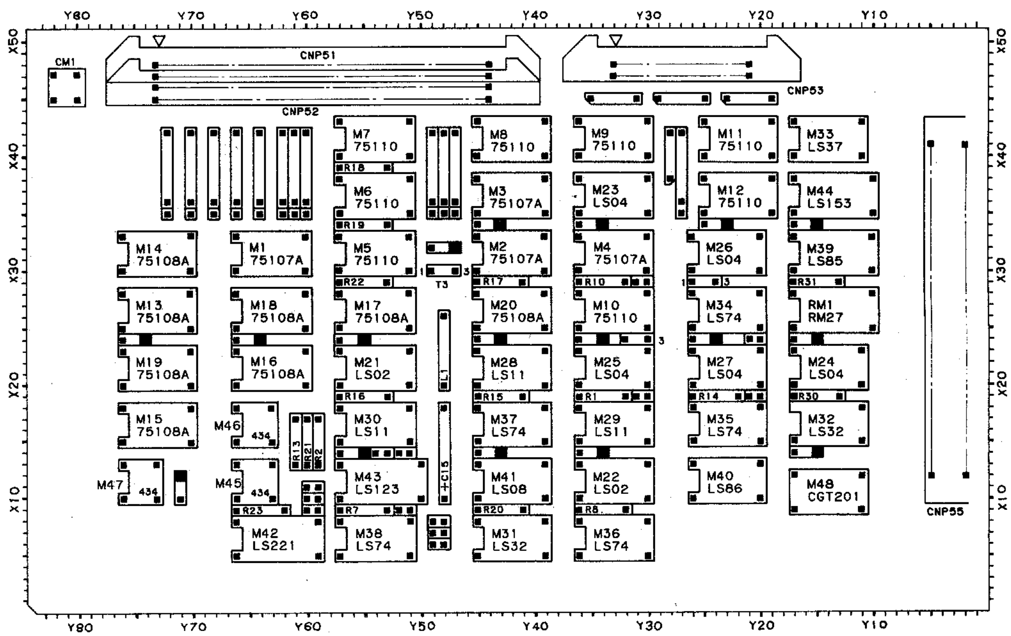

Co-ordinate	Symbol	Co-ordinate	Symbol
(47, 33)	CNP53	(15, 86)	M46
(41, 5)	CNP55	(10, 78)	M47
(10, 71)	C28		
(32, 49)	C29		
(14, 17)	C10		
(27, 17)	C11		
(34, 17)	C12		
(24, 76)	C13		
(24, 28)	C16		
(34, 25)	C17		
(14, 36)	C18		
(14, 45)	C19		
(24, 36)	C20		
(34, 36)	C21		
(24, 45)	C22		
(34, 45)	C23		
(14, 57)	C24		
(24, 57)	C25		
(24, 66)	C26		
(9, 60)	C14		
(19, 31)	C3		
(29, 31)	C4		
(14, 52)	C5		
(14, 54)	C6		
(11, 59)	C7		
(19, 21)	C30		
(24, 21)	C31		
(7, 49)	C50		
(9, 52)	TP3		
(10, 59)	TP4		
(6, 48)	TP5		
(45, 29)	RM16		
(45, 36)	RM17		
(38, 28)	RM18		
(45, 23)	RM19		
(35, 49)	RM10		
(35, 48)	RM11		
(35, 47)	RM12		
(35, 27)	RM13		
(35, 72)	RM2		
(35, 70)	RM3		
(35, 68)	RM4		
(35, 66)	RM5		
(35, 64)	RM6		
(35, 62)	RM7		
(35, 61)	RM8		
(35, 60)	RM9		
(8, 49)	T4		
(29, 26)	T1		
(24, 32)	T2		
(30, 49)	T3		
(10, 66)	M45		

Symbol	Mark
M1	75107A
M10	75110
M11	75110
M12	75110
M13	75108A
M14	75108A
M15	75108A
M16	75108A
M17	75108A
M18	75108A
M19	75108A
M2	75107A
M20	75108A
M21	LS02
M22	LS02
M23	LS04
M24	LS04
M25	LS04
M26	LS04
M27	LS04
M28	LS11
M29	LS11
M3	75107A
M30	LS11
M31	LS32
M32	LS32
M33	LS37
M34	LS74
M35	LS74
M36	LS74
M37	LS74
M38	LS74
M39	LS85
M4	75107A
M40	LS86
M41	LS08
M42	LS221
M43	LS123
M44	LS153
M45	434
M46	434
M47	434
M48	CGT201
M5	75110
M6	75110
M7	75110
M8	75110
M9	75110
RM1	RM27

DOCUMENT CONTROL SECTION

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TITLE: *Interface (Dual Port) Mounting Diagram.*

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