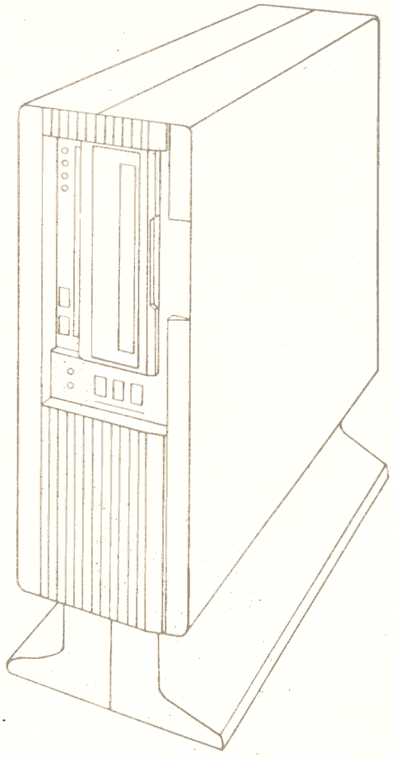
Ford Higgins Ltd.



Reference Manual

PowerFrame

Preliminary Copy

Ford
Higgins Ltd.

Reference Manual

PowerFrame

Microcomputer Systems

Preliminary Copy

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EASYLINK: 62317580

PART NUMBER 202 24500

FCC Compliance

This equipment generates and uses radio frequency energy and if not installed and used properly, i.e., in strict accordance with the operating instructions, reference manuals, and the service manual, may cause interference to radio or television reception. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial installation. If this equipment does cause interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

1) Reorient the receiving antenna.

2) Relocate the equipment with respect to the receiver.

3) Move the equipment away from the receiver.

4) Plug the equipment into a different outlet so that equipment and receiver are on different branch circuits.

If necessary, consult your dealer service representative for additional suggestions.

The manufacturer is not responsible for any radio or TV interference caused by unauthorized modifications to this equipment. It is the responsibility of the user to correct such interference.

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POWERFRAME COMPONENTS

CHAPTER 3

11/23+ MICROCOMPUTER

INTRODUCTION

The compact 11/23+ microcomputer system is designed to increase system performance and provide efficient backplane utilization. This low-cost, 16-bit microcomputer can address up to four full megabytes of parity MOS MSV11-P memory while offering full processor functionality. It is compatible with a wide range of software and hardware design, using the Extended Q-Bus.

The 11/23+ CPU module contains diagnostic and bootstrap ROM, a memory management unit, line-time clock, two asynchronous serial lines, and three sockets for the Commercial Instruction Set (CIS) and Floating Point Instruction Set options. Because of this unique packaging density, most applications will fit in a single PowerFrame unit.

SPECIFICATIONS

Identification	KDF11-B
Size	Quad
Dimensions	CPU chassis is 13.2 cm high x 48.3 cm wide x 68 cm deep (5.2 in x 19 in x 26.8 in)
Power Consumption	+5V 5%, at 6.4 A max. (at 4.5 A typ)
	+12V 5%, at .7 A max. (at .3 A typ)
Bus Loads	2 AC unit loads

	1 DC unit load
Non-operating Environment	-40 C to 66 C (-40 F to 151 F), 10% to 90% relative humidity, non-condensing
Operating Environment	5 C to 50 C (41 F to 122 F), 10% to 95% relative humidity Maximum outlet temperature rise of 5 C (9 F) above 60 C (140 F)
Altitude	To 15.25 km (50,000 feet) for non-operating environment. To 2.44 km (8000 feet) for operating environment.
Instruction Timing	Based on 75 ns intervals (see Appendix J)
Interrupt Latency	5.7 microseconds (typical) 12.6 microseconds, max. (except EIS) 54.225 microseconds, max. (including EIS)
Interrupt Service Time	8.625 microseconds (memory management off) 9.750 microseconds (memory management on)
DMA Latency	1.35 microseconds, max.
	NOTE: Interrupt and DMA latencies assume a KDF11-B with memory management enabled and using MSV11-P Memory.

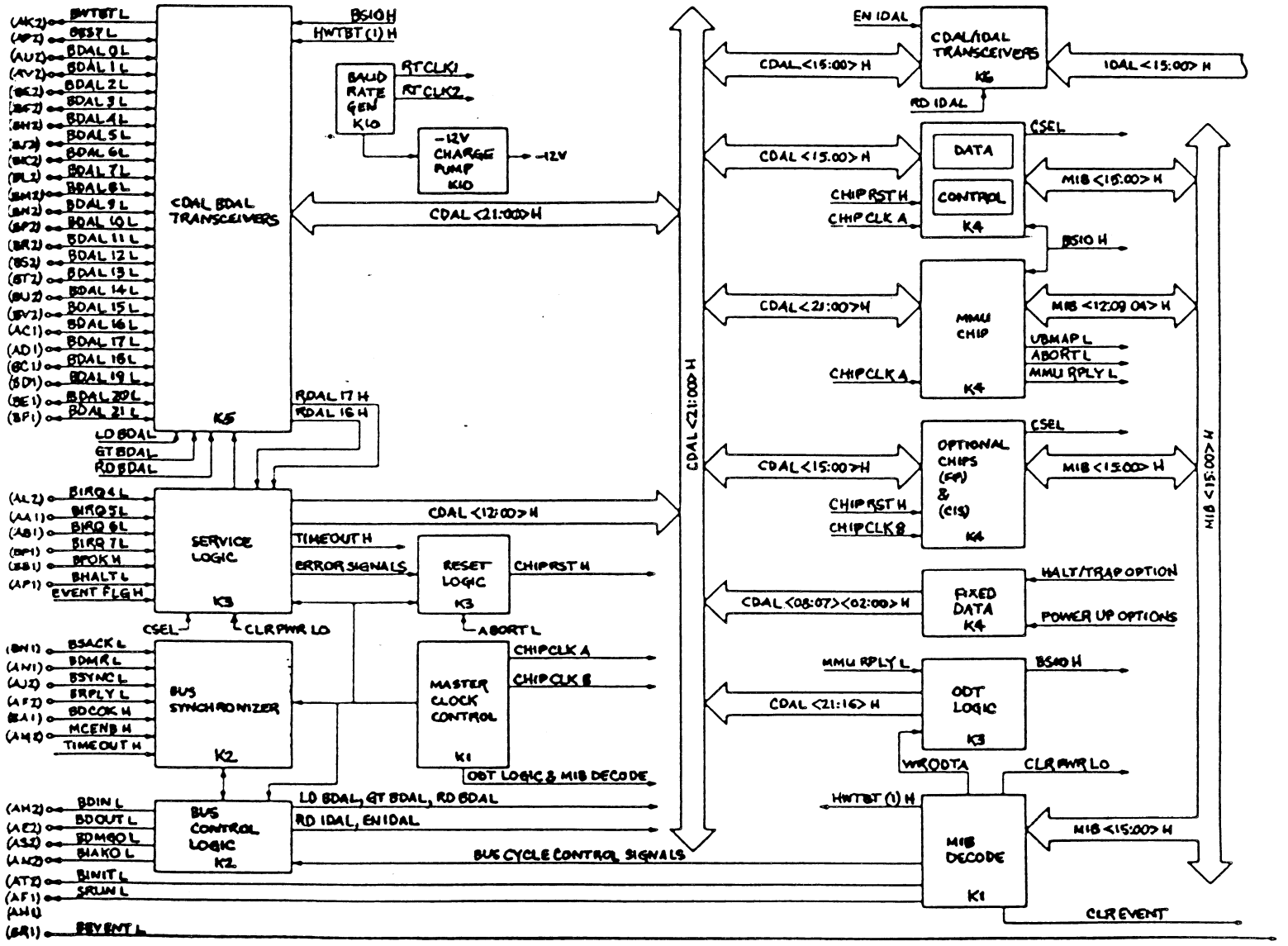
DESCRIPTION Central Processor

The 11/23+ central processing unit is contained on two LSI chips, control and data, which reside on a single 40-pin carrier (a dual in-line package). The standard Memory Management Unit (MMU) is contained on one LSI chip which also resides on a 40-pin carrier. 11/23+ contains sockets for these two carriers, plus three extra sockets which are reserved for the Commercial Instruction Set (CIS) or floating point options.

The architecture of the 11/23+ is highly expandable because of its internal bus structure. The control and data chips communicate with each other, as well as with the external 11/23+ logic, over the Micro Installation Bus (MIB) <15:00> and Chip Data and Address Line (CDAL) <21:00> bus. 11/23+ logic interfaces

these chips to the Internal Data and Address Line (IDAL) <15:00> bus and the external Extended Q-Bus. The IDAL bus provides additional loading capacity on the chip set bus. For an illustration of the positions of these busses, please refer to Figure 3-1, the 11/23+ functional block diagram.

FIGURE 3-1 - Functional Block Diagram



The 11/23+ boot and diagnostic ROMs, line clock, and serial line units reside on the IDAL bus. Memory and additional peripherals interface to the Extended Q-Bus. Bidirectional interfaces (CDAL/IDAL) transceivers and CDAL/BDAL transceivers on the 11/23+ CPU module connect the CDAL <21:00> bus with the IDAL <15:00> bus. 11/23+ logic supporting LSI chip set includes the master clock control logic, MIB decode logic, fixed data logic, service logic, reset logic, and ODT logic. Logic pertaining to the Extended Q-Bus includes the bus control logic, bus synchronizer, and the CDAL/BDAL transceivers. Logic pertaining to the IDAL bus peripherals includes the bus control logic, CDAL/IDAL transceivers, the IDAL address decode, the boot/diagnostic ROMs, the line clock logic, the console and second SLU logic, the baud rate generator, and the -12V charge pump circuits.

Floating Point Option

Forty-six floating point instructions are available as a microcode option (KEF11-A) on the 11/23+ processor to supplement the integer arithmetic instructions in the basic instruction set. The Floating Point Instruction Set executes floating point operations much faster than equivalent software routines. It also provides both single-precision (32-bit) and double-precision (64-bit) operands, and conserves memory space by executing in microcode instead of software. This option implements the same Floating Point Instruction Set available with the 11/34, 11/60, and 11/70 minicomputers.

Commercial Instruction Set

The Commercial Instruction Set (CIS), a microcode option, adds character string instructions to the basic 11/23+ instruction set. These character string operations implement functions of commercial data and text processing applications. CIS microcode resides in six MOS/LSI chips which are mounted on a single double-width 40-pin carrier.

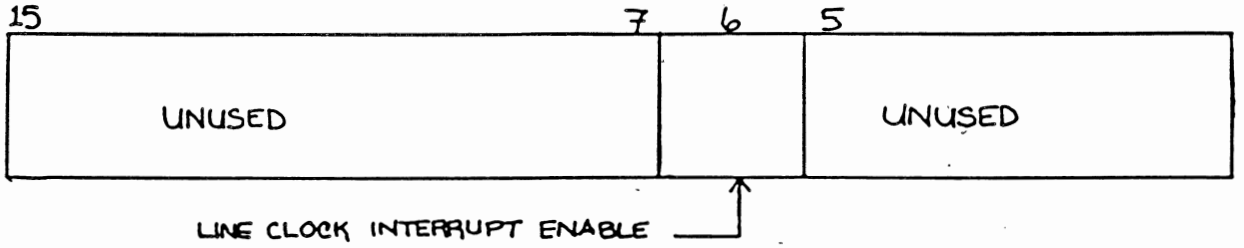
Line Clock

Line frequency clock provides the system with timing information at fixed intervals. The intervals are synchronized with the line frequency of the user's input power. The line clock generates bus request level 6 interrupts to the processor at time intervals determined by the BEVENT L signal. The BEVNT L signal is obtained from the power supply via module pin BR1 at 16 2/3 ms or 20 ms intervals, depending on the line frequency source (60 Hz or 50 Hz, respectively).

Line Clock Status Register

The contents of the line clock status register consist of a single read/write bit. The program communicates with the line clock via a status register at address 777 546. Program recognition of this register, along with the recognition of the boot/diagnostic registers and second wire-wrap (J11) jumper, when installed, forces the line clock interrupt enable bit to the set condition. The line clock status register bit assignment is shown below.

FIGURE 3-2 - Line Clock Status Register (LKS) 777 546



BIT: 15:7 FUNCTION: Unused

BIT: 6 (Read/Write) NAME: LINE CLOCK Interrupt Enable FUNCTION: When Set, this bit allows the BEVENT line to initiate program interrupt requests. When clear, line clock interrupts are disabled. LCIE is cleared by Power-up and BINIT. LCIE is held set when the LTC ENJ L jumper is installed.

BIT: 5:0 FUNCTION: Unused

Bootstrap/Diagnostic ROM

The bootstrap and diagnostic logic features three hardware registers and two ROM sockets for 2K, 4K, or 8K read-only memory. This 16-bit read-only memory

contains diagnostic programs, plus a selection of bootstrap programs. These programs are user-selectable by setting eight switches on a 16-pin Dual In-Line Pack (DIP) switch pack. Programming the bootstrap and diagnostic logic consists of setting the switches for the programs desired. The bootstrap/diagnostic switch configurations and console operator responses are described in the Configuration section of this chapter. The diagnostic programs test the processor, memory, the console terminal, and the device to be bootstrapped.

The user may replace the standard ROMs with 2716-type ROMs containing programs of his/her choice, but the 11/23+ will have the functionality described above only if the standard bootstrap/diagnostic ROMs are installed in the ROM sockets.

Table 3-1 lists the error messages associated with the 11/23+ ROMs.

TABLE 3-1 - LIST OF ERROR HALTS

ADDRESS OF ERROR	DISPLAY (OCTAL)	CAUSE OF ERROR
173036	01	CP1ERR, R0 contains address of error.
0xx173040	05	SLU switch selection incorrect. Error in switches.
173046	05	SLU error, CSR address for selected device in error. Check CSR for selected device in floating CSR address area.
173200	12	ROM Loader error. Check sum on data block.
173232	02	Memory error 2. Write address into itself.
173236	01	CP3ERR, R0 points to cause of error.
173240	01	CP4ERR, R0 points to address of error.
173262	02	Memory error 3. Byte addressing error.
173302	02	Memory error in pre-memory data test. R2 = Failing Data R3 = Expected Data R5 = Failing Address (0-776)
173316	02	Memory error. Bit 15 set in one of the parity CSR's (172100-172136). Failing memory should have the parity light on.

173364	12	ROM Loader error. Checksum on address block.
173376	12	ROM Loader error. Jump address is odd.
173526	05	RL01/RL02 device error.
173652	05	RK05 device error.
173654	01	Switch mode halt. Match was not made with switches.
173660	02	Memory error in 0-2044 KW 22-bit memory test. Common error halt for six different tests. If R3=0, then error in tests 1-5. R4 determines failing test. R4 = Expected data R5 = Failing data

CONTENTS OF R4	TEST	TEST DESCRIPTION
20000-27776	1	Address Test, bit 11 to 0
177777	2	Data Test
000000	3	Data Test
072527	4	Odd Parity Pattern Test
125125	5	Byte Addressing Test

For tests 1-5 (R3 = 0), determine 22-bit failing address as follows:

R1 Bits 11-0 = Failing address bits 11-0.
R2 Bits 15-6 = Failing address bits 21-12.
Errors in address uniqueness test.
Test checks address bits 21-6, Test 6.
If R3 is not equal to 0, then error is in this test.

R4 = Expected data
R5 = Failing data
R2 = 22-bit failing physical address bits 21-6.
Failing address bits 5-0 are always 0.

173664	02	Memory error in pre-memory address test for locations 000-776. R2 = Failing data R5 = Failing address and expected data

173670	01	Error in CPU Test 9. JSR R3 failed.
173700	01	Error CPU Test 9. JSR PC failed.
173704	05	RX01/RX02 device error.
173714	04	A "NO" typed in console terminal test.
173736	02	Memory error 1, data test failed. Test 0-30 Kw with MMU off if present. R1 = Failing address R4 = Expected data (either 0 or 177777) R5 = Failing data
173740	01	Error CPU Test 9. "RTS" return failed.
173742	03/04	Console terminal test. No done flag.
173760	05	TU58 error halt.

Bootstrap and Diagnostic Registers

The bootstrap and diagnostic logic contains three hardware registers that are software-addressable. One of the registers is dual-purpose register which functions as the configuration register when read, and the display register when written. These registers are assigned separate, individual addresses that cannot be changed or modified. The particular designations and addresses of these registers are listed in Table 3-2, below. The registers and associated logic are described in the following paragraphs.

TABLE 3-2 - BOOTSTRAP AND DIAGNOSTIC REGISTER ASSIGNMENTS

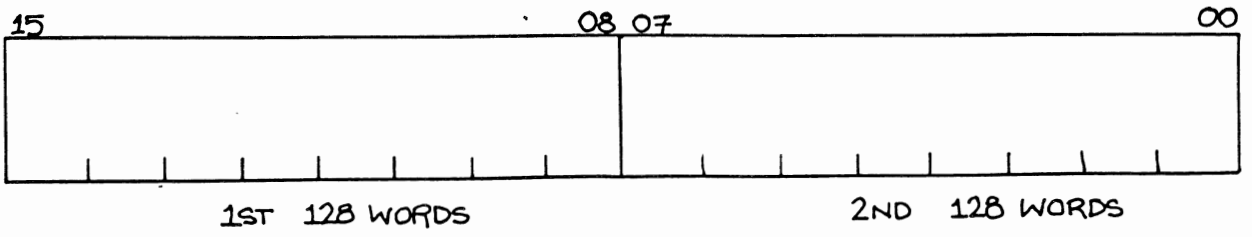
REGISTER	READ/ WRITE	BIT SIZE	ADDRESS
Page Control	W	12	777520
Read/Write Maintenance	R/W	16	777522
Configuration*	R	8	777524
Display*	W	4	777524

* Dual-Purpose Register

Page Control Register (PCR) 777520

The PCR is a write-only register which is both word-addressable and byte-addressable. This register is cleared by Power-up, and when the 'Restart' switch on the CPU mounting box is activated. The PCR, in conjunction with the ROM address multiplexer, permit all 2048 locations in the 2K bootstrap/ diagnostic ROM to be accessed by 256 of the Extended Q-Bus addresses reserved for peripheral device addressing. The 256 addresses cover a byte address range of 773000-773777. Figure 3-3 illustrates the page control register.

FIGURE 3-3 - PAGE CONTROL REGISTER



The contents of the PCR are used to select any one of the 16 pages of ROM. Each page of ROM consists of 128 word locations. Table 3-3, below, describes the relationship between the PCR contents to the PCR page for pages 0-17. If the PCR is loaded with data 000400, the PCR low byte contains data 000, while the high byte contains data 001. The PCR bytes can be loaded separately. To select ROM locations 1600-1777, for example, one need only load the PCR high byte with page 7. In this example, the high byte contains 007, while the low byte is disregarded.

TABLE 3-3 - PCR CONTENTS/PAGE RELATIONSHIP, PAGES 0-17

PCR PAGES (OCTAL)	PCR CONTENTS	PCR HIGH BYTE (BITS 13:08)	PCR LOW BYTE (BITS 05:00)
0/1	000400	001	000
2/3	001402	003	002
4/5	002404	005	004
6/7	003406	007	006
10/11	004410	011	010
12/13	005412	013	012
14/15	006414	015	014
16/17	007416	017	016

Read/Write Maintenance Register 777522

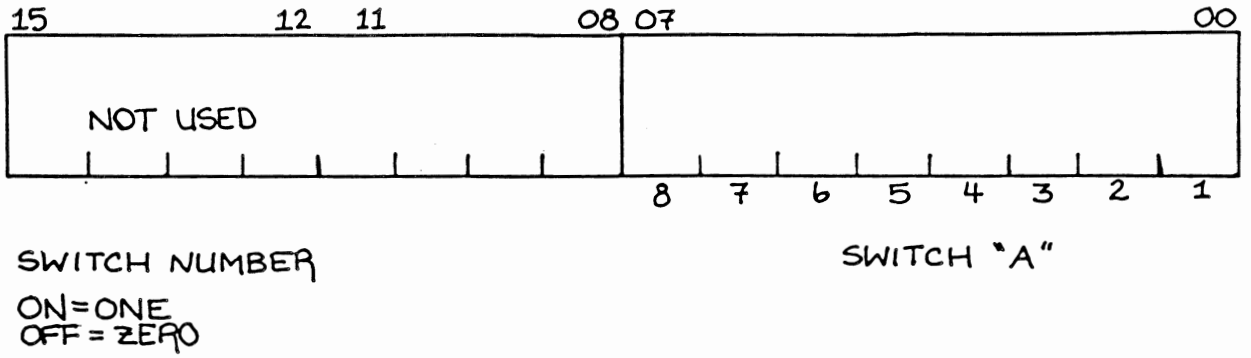
The read/write maintenance register (RWR) is a 16-bit read/write register which is both word- and byte-addressable. It is used by the ROM diagnostics to test various read/write functions before accessing main memory. The register is cleared by Power-up and system reset.

Configuration Register 777524

This 8-bit read-only register is used to select diagnostic programs for maintenance and/or bootstrap programs for system configuration. The boot/diagnostic program selection procedure is described in the Configuration section of this chapter. The interpretation of the switch configuration is determined by the ROM bootstrap and diagnostic programs. The switch register is depicted

below in Figure 3-4.

FIGURE 3-4 - SWITCH REGISTER 777524

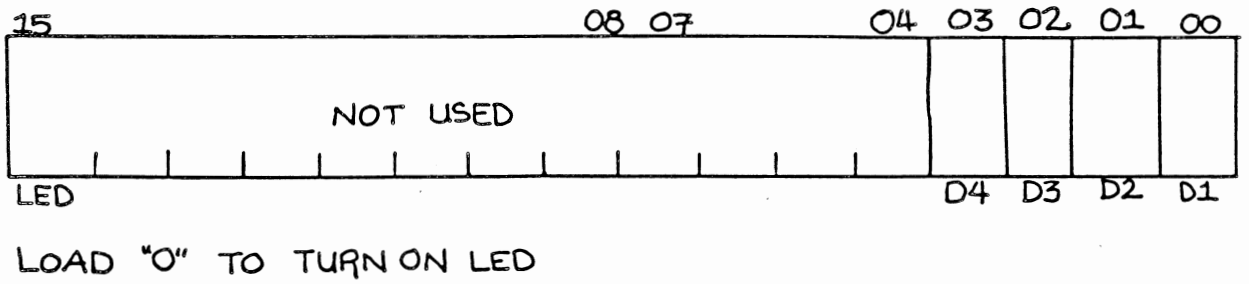


Display Register 777524

This 4-bit write-only register allows the program to control a four LED diagnostic display. Clearing one of the four display register bits lights the corresponding LED. The display register is cleared by Power-up (which turns all red LEDs on) and when the system is rebooted.

The diagnostic LED display is normally used when there is no printout on the terminal after a failure. It indicates the type of error when a failure occurs in a diagnostic test or bootstrap program. The display will indicate the type of errors described in Table 3-4, below. Figure 3-5 depicts the display register.

FIGURE 3-5 - DISPLAY REGISTER 777524



Standard ROMs must be installed in ROM sockets E126 (low byte) and E127 (high byte) respectively to obtain the described errors.

TABLE 3-4 - DIAGNOSTIC LED ERROR DISPLAY*

DISPLAY (OCTAL)	MSD BIT 3	BIT 2	LSD BIT 1	BIT 0	TYPE OF ERROR
01	OFF	OFF	OFF	ON	CPU error
02	OFF	OFF	ON	OFF	Memory
03	OFF	OFF	ON	ON	Console Terminal test display error
04	OFF	ON	OFF	OFF	Console Terminal test keyboard error
05	OFF	ON	OFF	ON	Load device status error
06	OFF	ON	ON	OFF	Bootstrap code incorrect (NOP In-

					struction not in location 000000)
07	OFF	ON	ON	ON	SLU error, no response from host
10	ON	OFF	OFF	OFF	SLU received done flag set
11	ON	OFF	OFF	ON	SLU message received in DDCMP format
12	ON	OFF	ON	OFF	ROM bootstrap error
13	ON	OFF	ON	ON	Attempted access to memory Loc 0-6 failed. This failure will normally occur when the memory does not reply
17	ON	ON	ON	ON	Halt switch on or unable to run

* The light pattern indicates the corresponding test is in progress or failed. Some tests retry (DECnet), and others will halt the CPU (CPU, memory non-DECnet boots).

Serial Line Units

The two full-duplex asynchronous serial line units (console serial line unit and the second serial line unit) provide the 11/23+ (KDF11-B) with an EIA interface which is RS-232-C and RS-423 compatible. The serial line baud rates are determined by a clock signal from an internal baud rate generator or an external clock signal via connector J1 and J2. Jumpers are provided to select either the internal clock or the external clock. If the internal clock is jumper-selected, the serial line baud rates are switch-selectable from 50 to 19.2 baud. The console serial line and the second serial line may operate at different baud rates. However, a split baud rate is not possible. Each serial line must transmit and receive data at the same baud rate. If desired, 20 ma active or passive current loop operation at 110 baud may be obtained with DLV11-KA EIA to 20 ma converter option. The DLV11-KA contains a 110 baud rate clock signal which is supplied to pin 1 or the console serial line J1 and the second serial line J2 connectors.

The console serial line unit may be configured to halt in response to a break signal received from the console terminal. Both serial lines interrupt the

processor at bus interrupt priority request level 4 (BR4).

The character format for each of the serial line units selected by wire-wrap jumpers and may consist of 7 or 8 data bits, 1 or 2 stop bits, parity or no-parity, and even and odd parity.

The console serial line unit is connected to the console terminal via connector J1. The second serial line unit is connected to the line printer, the TU58 cassette tape, or an additional terminal via connector J2.

Serial Line Unit Registers

The program communicates with and transfers data to and from the external peripheral devices via four associated with each serial line. Two of the registers (RCSR and TCSR) contain control/status information for receiver and transmitter operation. The other two registers (RBUF and TBUF) contain data received from, and data to be transmitted to the peripheral device. The addresses assigned to the console and second serial line registers are listed in Table 3-5.

TABLE 3-5 - SERIAL LINE REGISTER VECTORS

CONSOLE SERIAL LINE REGISTER	ADDRESS*	SECOND SERIAL LINE REGISTER	ADDRESS	
RCSR1	777560	RCSR2	776500**	776540***
RUF1	777562	RBUF2	776502	776542
TCSR1	777564	TCSR2	776504	776544
TBUF1	777566	TBUF2	776506	776546

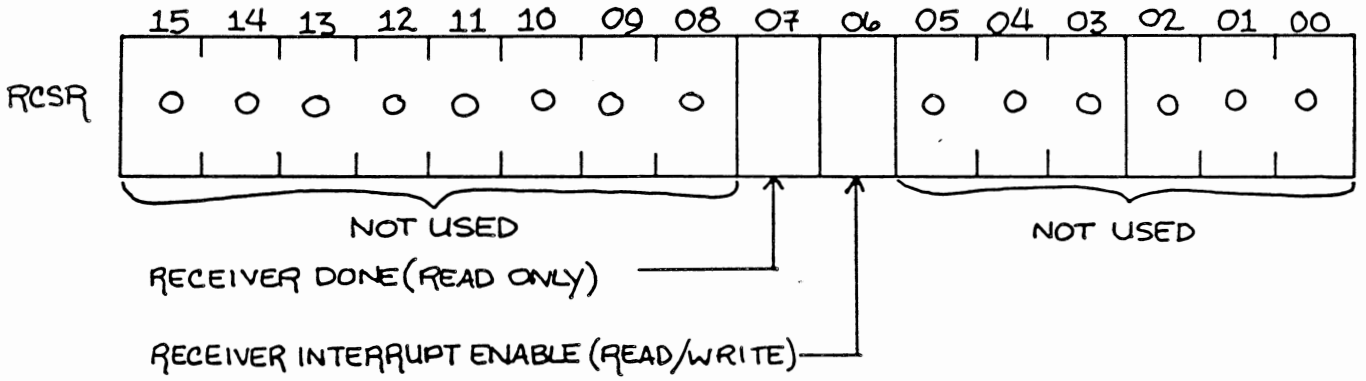
* DL1 DISJ L (J14) must be ungrounded.
** DL2 DISJ L (J13) and DL2 ADRJ L (J12) must be ungrounded.
*** DL2 DISJ L (J13) must be ungrounded and DL2 ADRJ L (J12) must be grounded.

Register Bit Assignments

The console and second serial line registers have the same bit assignments with the exception of bit 0 of the TCSR. Bit 0 is used as a transmit break bit (TX BRK) in the second serial line register (TCSR2), and it is unused in the console serial line register (TCSR 1).

The bit formats for the registers are shown in the Figures below, as are the register bit assignments.

FIGURE 3-6 - RECEIVER STATUS REGISTER (RCSR 1 AND RCSR 2)



BIT: 15:8
FUNCTION: Unused. Read as zeros.

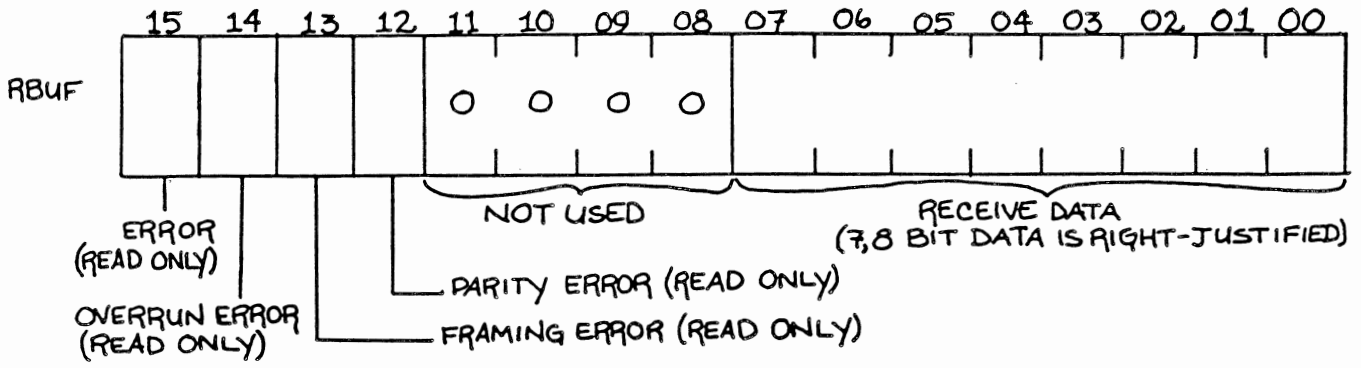
BIT: 7 (read-only)
NAME: Receiver Done (RX DONE)
FUNCTION: Set when an entire character has been received and is ready to be read from the RBUF register. This bit is automatically cleared when RBUF is read. It is also cleared by Power-up and Bus INIT.

BIT: 6 (Read/Write)
NAME: Receiver Interrupt Enable (RX IE)
FUNCTION: Cleared by Power-up and Bus INIT. If both RCVR DONE and RCVR INT ENB are set, a program interrupt is requested.

BIT: 5:0

FUNCTION: Unused. Read as zeros.

FIGURE 3-7 - RECEIVER BUFFER REGISTER (RBUF 1 AND RBUF 2)



BIT: 15 (read-only)
NAME: Error (ERR)
FUNCTION: Set if any RBUF bit 14:12 is set. ERR is clear if all RBUF bits 14:12 are clear. This bit cannot generate a program interrupt.

BIT: 14 (read-only)
NAME: Overrun Error (OVR ERR)
FUNCTION: Set if a previously received character was not read before being overwritten by the present character.

BIT: 13 (read-only)
NAME: Framing Error (FRM ERR)
FUNCTION: Set if the present character had no valid stop bit. Also used to detect a break condition.

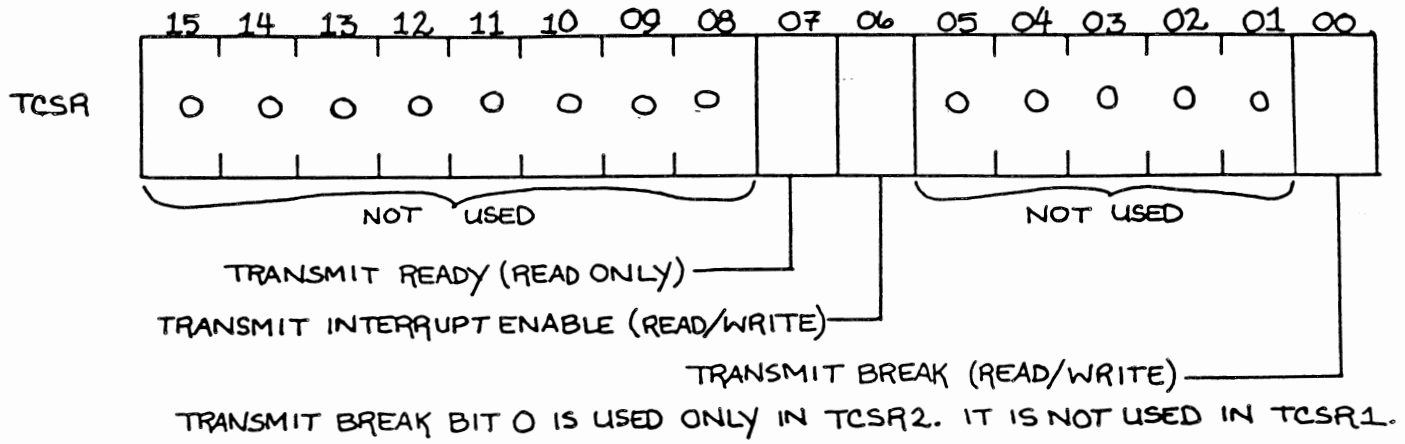
BIT: 12 (read-only)
NAME: Parity Error (PAR ERR)
FUNCTION: Set if received parity does not agree with expected parity. Always 0 if no parity is selected.

NOTE: Error conditions remain present until the next character is received at which point, the error bits are updated. The error bits are cleared by Power-up and Bus INIT.

BIT: 11:8
FUNCTION: Unused. Read as zeros.

BIT: 7:0 (read-only)
NAME: Received Data Bits.
FUNCTION: These bits contained the last received character. If less than eight bits are selected, the character will be right-justified with the most significant bit(s) reading zero.

FIGURE 3-8 - TRANSMITTER/CONTROL STATUS REGISTER (TCSR 1 AND TCSR 2)



BIT: 15:8
FUNCTION: Unused. Read as zeros.

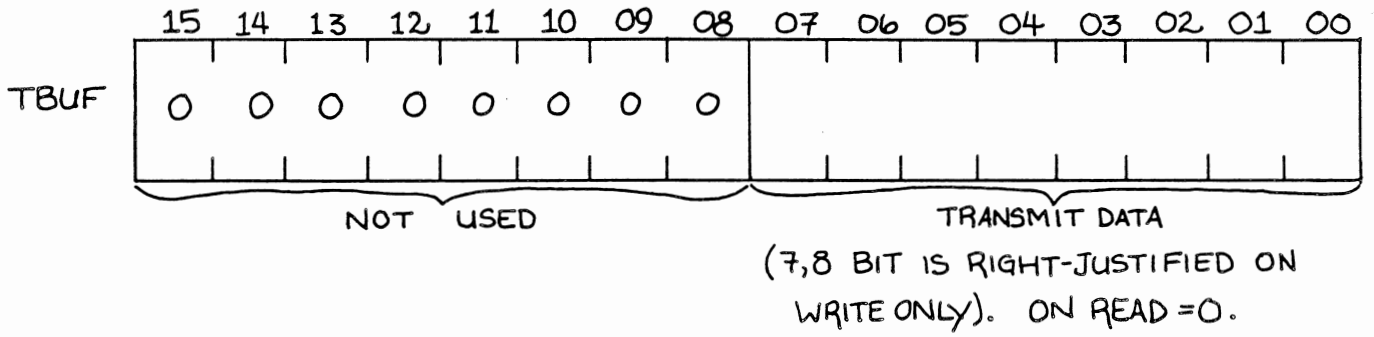
BIT: 7 (read-only)
NAME: Transmitter Ready (TX RDY).
FUNCTION: Cleared when TBUF is loaded and sets when TBUF can receive another character. XMT RDY is set by Power-up and Bus INIT.

BIT: 6 (read/write)
NAME: Transmitter Interrupt Enable (TX IE).
FUNCTION: Cleared by Power-up and Bus INIT. If both XMT RDY and XMT INT ENB are set, a program interrupt is requested.

BIT: 5:1
FUNCTION: Unused. Read as zeros.

BIT: 0 (read/write)
NAME: Break (TX BRK).
FUNCTION: When set, transmits a continuous space. This bit is cleared by Power-up and System INIT. This bit is used only in TCSR2. It is unused in TCSR1.

FIGURE 3-9 - TRANSMITTER BUFFER REGISTER (TBUF 1 AND TBUF 2)



BIT: 15:8
FUNCTION: Unused. Read as zeros.

BIT: 7:0 (write-only)
FUNCTION: TBUF bits 7:0 are write-only bits used to load the transmitted character. If less than eight bits are selected, the character must be right-justified.

CONFIGURATION

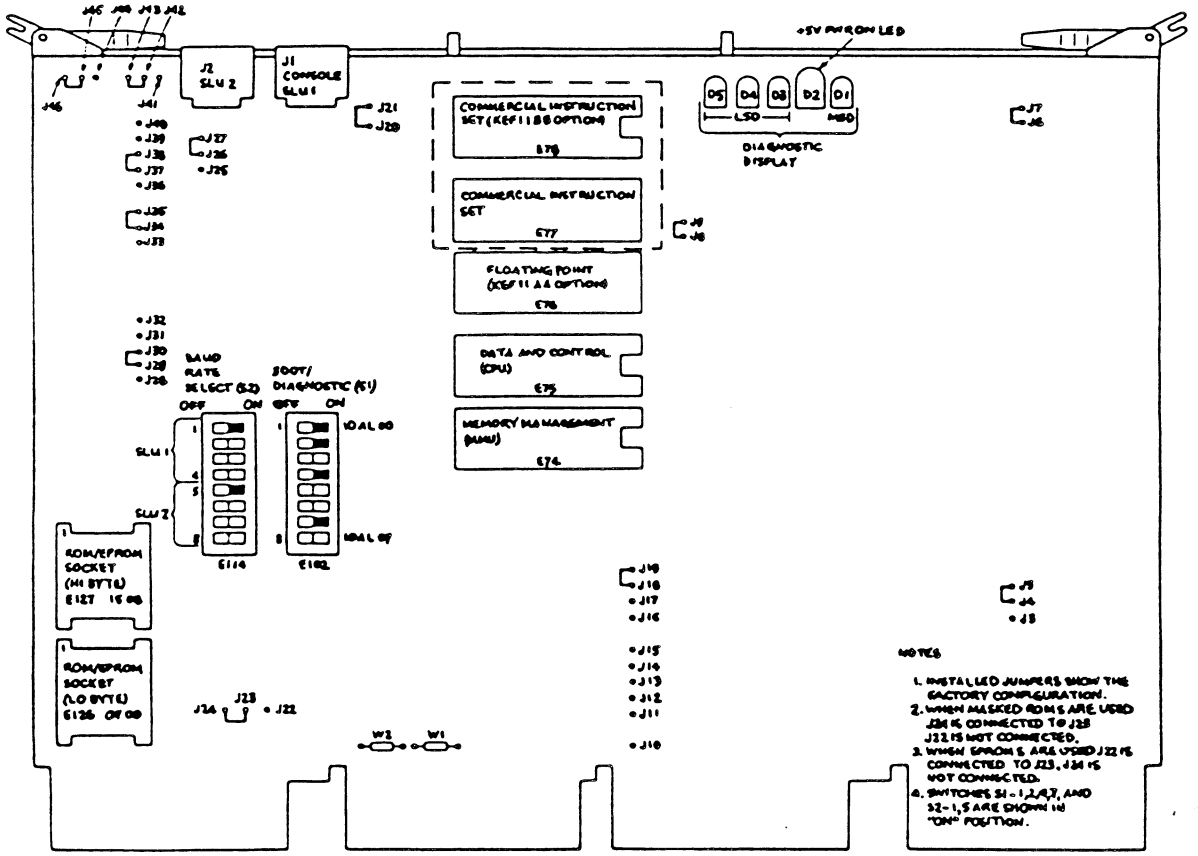
Jumper and Switch Configuration

The 11/23+ contains two Dual In-Line Pack (DIP) switch units (E102 and E114) and several jumpers which allow the user to select the module features desired. The location of the switch units and jumpers is shown in Figure 3-10. The Boot/Diagnostic switch unit (E102) consists of eight switches that let the user select boot and diagnostic programs. The second switch unit (E114) selects the baud rate for the Console SLU and the second SLU. The module contains both wire-wrap jumper stakes and soldered-in jumpers. The jumpers are divided into

the following functional groups:

1. Test Jumpers
2. CPU Option Jumpers
3. Device Selection Jumpers
4. Boot and Diagnostic ROM Jumpers
5. SLU Character Format Jumpers
6. Internal/External SLU Clock Jumpers
7. Q-Bus Backplane Jumpers

FIGURE 3-10 - JUMPER, SWITCH AND DIAGNOSTIC DISPLAY LOCATIONS



Manufacturing Test Jumpers

Five jumpers are provided for manufacturing testing purposes. These jumpers must be configured as follows in Table 3-6 for normal operation.

TABLE 3-6 - MANUFACTURING TEST JUMPERS

JUMPER FROM	TO	STATUS
J6	J7	Installed
J8	J9	Installed
J20	J21	Installed
J35	J34	Installed
J33	J34	Removed
J27	J26	Installed
J25	J26	Removed

CPU Option Jumpers

Four wire-wrap stakes provide user-selectable features associated with the operation of the CPU. The ground stake can be connected to any combination of the other three stakes to select the available features. Two power-up mode stakes select one of three power-up modes. The halt/trap stake selects the halt/trap options.

Power-Up Mode Selection

The three power-up modes are available for user selection. Selection is made by installing or removing wire-wrap jumpers between jumper stakes (J17, J19) and the ground stake (J18) in various combinations. The jumper configuration for the modes are described in the Table 3-7 below.

TABLE 3-7 - POWER-UP MODE JUMPER CONFIGURATION

MODE	NAME	JUMPER J19	J18 TO J17
0	PC@24, PS@26	R*	R
1	Console ODT	R	I
2	Bootstrap	I	R
3	Not Implemented	I	I

* R = Jumper removed; I = Jumper installed

Only the power-up mode is affected, not the power-down sequence. The following paragraphs describe the sequence of events after executing common power-up, when selecting each of the four modes. The state of bus signal BHALT L is significant in power-up mode operation.

Power-Up Mode 0 (PC@24, PS@26)

This mode causes the microcode to fetch the contents of memory locations 24 and 26 and loads their contents into the PC and PS, respectively. The microcode then examines BHALT L. If BHALT L is asserted, the processor enters console ODT mode. If BHALT L is not asserted, the processor begins program execution by fetching an instruction from the location pointed to by the PC. This mode is useful when power-fail/auto restart capability is desired.

Power-Up Mode 1 (Console ODT)

This mode causes the processor to enter console ODT mode immediately after power-up regardless of the state of any service signals. This mode is useful in a program development or hardware debug environment, giving the user immediate control over the system after power-up.

Power-Up Mode 2 - Start at 773000

This mode causes the processor to internally generate a bootstrap starting address of 773000 in 16-bit mode with MMU off. This address is loaded into the PC. The processor sets the PS to 340 (PS<07:05> = 7) to inhibit interrupts before the processor is ready for them. If BHALT L is asserted, the processor enters console ODT mode. If not, the processor begins execution by fetching an instruction from the location pointed to by the PC. This mode is useful for turnkey applications where the system automatically begins operation without operator intervention.

Halt/Trap Option - J16

If the processor is in kernal mode and decodes a HALT instruction, BPOK H is tested. If BPOK H is negated, the processor will continue to test for BPOK H. The processor will perform a normal power-up sequence if BPOK H becomes asserted sometime later. If BPOK H is asserted after the HALT instructon decode, the halt/trap jumper (J16) is tested. If the jumper is removed, the processor enters console ODT mode. If the jumper is connected to J18 (ground), a trap location 10 will occur.

NOTE: In user mode a HALT instruction execution will always result in a trap to location 10 .

This feature is intended for situations, such as unattended operation, where recovery from erroneous HALT instructions is desirable. Table 3-8 describes the halt/trap jumper functions for Kernal and User processor modes.

TABLE 3-8 - HALT/TRAP JUMPER CONFIGURATION

JUMPER J18 to J16	PROCESSOR MODE	FUNCTION
R	Kernal	Processor enters Console ODT microcode when it executes a HALT instruction.
I	Kernal	Processor traps to location 10 when it executes a HALT instruction.
X	User	Halt instruction decode results in a trap to location 10 regardless of the status of the Halt/Trap Jumper.

On-Board Device Selection Jumpers

Six wire-wrap stakes on the 11/23+ module are used to select which on-board peripheral devices are enabled or disabled. The ground stake can be connected to any combination of the other five stakes to obtain the desired configuration. The jumper functions are described in Table 3-9, below.

TABLE 3-9 - ON-BOARD DEVICE SELECTION JUMPERS

STAKE NUMBER	FUNCTION
J10	This wire-wrap stake provides a ground source for the other five wire-wrap stakes in this group.
J11	When grounded, this signal sets the line clock interrupt enable flip-flop and allows the Q-Bus BEVNT signal to request program interrupts.
9J15	When grounded, this signal disables the boot/diagnostic registers, the boot/diagnostic ROMs, and the line clock register.
J12	When J12 is ungrounded, the second SLU device and vector addresses are as follows:

DEVICE	ADDRESSES	INTERRUPT	VECTORS
RCSR	776500	Receiver	300
RBUF	776502	Transmitter	304
XCSR	776504		
XBUF	776506		

When J12 is grounded, the device and vector addresses are as follows:

DEVICE	ADDRESSES	INTERRUPT	VECTORS
RCSR	776540	Receiver	340
RBUF	776542	Transmitter	344
XCSR	776544		
XBUF	776546		

J13	When grounded, this signal disables the second serial line registers. When ungrounded, the device and vector addresses for the second SLU are determined by the status of the J12 jumper.

J14 When grounded, this signal disables the console serial line registers. When ungrounded, the device and vector addresses for the console SLU are the following:

DEVICE	ADDRESSES	INTERRUPT	VECTOR
RCSR	777560	Receiver	060
RBUF	777562	Transmitter	064
XCSR	777564		
XBUF	777566		

SLU CONNECTOR PIN FUNCTIONS

PIN	J1 = CONSOLE SIGNAL	J2 = SECOND SLU FUNCTION
1	EXT CLK	Input for an external SLU clock.*
2	Ground	
3	XMIT+	Transmitter output.
4	Ground	
5	Ground	
6	NC	Key; pin not provided.
7	RCV-	Receiver input (most negative).
8	RCV+	Receiver input (most positive).
9	Ground	
10	+12V	Power for the DLV11-KA option.** Fused at 1A.

* If the DLV11-KA option is installed between the console SLU and the console terminal, jumper J42-J43 must be removed and jumper J42-J41 installed.

** This pin must be unterminated if the DLV11-KA option is not installed.

Console SLU Switch and Jumper Configurations

Four switches of a 16-pin DIP switch pack (E114) and four jumpers provide user-selectable features associated with the operation of the console serial line unit. A jumper is available to disable the console SLU.

Console SLU Baud Rates

Switches 1 through 4 of the S2 switch pack (E114) select 1 of 16 possible SLU baud rates if the internal baud rate generator is used as the clock source. If the module is configured to operate the SLU with an external clock, the positions of these switches are meaningless. The SLU transmits and receives at the selected baud rate. Split baud operation is not provided. The switch configurations to select any one of the available baud rates are listed in Table 3-10 below:

TABLE 3-10 - CONSOLE SLU BAUD RATE SELECTION

SWITCH POSITION S2-4	S2-3	S2-2	S2-1	BAUD RATE
ON	ON	ON	ON	50
ON	ON	ON	OFF	75
ON	ON	OFF	ON	110
ON	ON	OFF	OFF	134.5
ON	OFF	ON	ON	150
ON	OFF	ON	OFF	300
ON	OFF	OFF	ON	600
ON	OFF	OFF	OFF	1200
OFF	ON	ON	ON	1800
OFF	ON	ON	OFF	2000
OFF	ON	OFF	ON	2400
OFF	ON	OFF	OFF	3600
OFF	OFF	ON	ON	4800
OFF	OFF	ON	OFF	7200
OFF	OFF	OFF	ON	9600
OFF	OFF	OFF	OFF	19,200

As stated previously, the UART can be configured to operate at a baud rate that is generated externally. The baud rate is inputted to the module from the external device through connector J1, pin 1. The jumper options are shown below.

JUMPER RATE FROM	TO	FUNCTION	SELECTED BAUD INTERNAL	EXTERNAL
J43	J42	Connects internal baud rate generator to the console SLU UART (Normal configuration)	I	R
J41	J42	Connects external clock to the	R	I

console SLU UART

Console SLU Character Formats

Five wire-wrap stakes select options to establish the console SLU character format. The ground stake can be connected to any combination of the other four stakes to configure the character format options.

The following table, Table 3-11, describes how to configure the character format.

TABLE 3-11 - CONSOLE SLU CHARACTER JUMPER CONFIGURATION

JUMPER FROM	TO J38**	CHARACTER FORMAT OPTION
J39	IN	7-bit characters
	OUT	8-bit characters
J37	OUT	Two stop bits
	IN	One stop bit
J36*	IN	Parity check enabled
	OUT	Parity check disabled
J40	IN	Odd parity if J36 is in
	OUT	Even parity if J36 is in

* If 8-bit characters (J39 OUT) are selected, parity check must be disabled (J36 OUT).

** J38 is the ground source for these functions. "In" means that a jumper connection is to be made to J38.

Break Halt Jumpers

Two jumpers enable and disable the Break Halt feature. If this feature is enabled, the detection of a break condition by the console UART causes the processor to halt and enter the octal debugging technique (ODT) microcode. If this feature is disabled, there is no response to the break condition. Below is Table 3-12, which lists the Break Halt Jumper configurations.

TABLE 3-12 - BREAK HALT JUMPER CONFIGURATION

JUMPER FROM	TO	FUNCTION	BREAK FEATURE ENABLED	BREAK FEATURE DISABLED
J5	J4	Connects ground to RQ HLT H.	R*	I*
J3	J4	Connects DL1 FE H to RQ HLT H.	I	R

* R = removed; I = installed

Second SLU Switch and Jumper Configurations

The second SLU is configured much the same as the console SLU, except that a different set of switches and jumpers are used to select the available SLU features. Also, the Halt/Break jumper is not present. Jumpers are also available to select the second SLU, and to select the range of addresses/vectors to be used. The switch positions for the second SLU baud rates are listed in Table 3-13.

TABLE 3-13 - SECOND SLU BAUD RATE SELECTION

SWITCH POSITION S2-8	S2-7	S2-6	S2-5	BAUD RATE
ON	ON	ON	ON	50
ON	ON	ON	OFF	75
ON	ON	OFF	ON	110
ON	ON	OFF	OFF	134.5
ON	OFF	ON	ON	150
ON	OFF	ON	OFF	300
ON	OFF	OFF	ON	600
ON	OFF	OFF	OFF	1200
OFF	ON	ON	ON	1800
OFF	ON	ON	OFF	2000
OFF	ON	OFF	ON	2400
OFF	ON	OFF	OFF	3600
OFF	OFF	ON	ON	4800
OFF	OFF	ON	OFF	7200
OFF	OFF	OFF	ON	9600
OFF	OFF	OFF	OFF	19,200

The second SLU may be configured to operate at an externally generated baud rate. The baud rate is inputted to the module from the external device through J2, pin 1. The jumper options are:

JUMPER FROM	RATE TO	FUNCTION	SELECTED INTERNAL	BAUD EXTERNAL
J46	J45	Connects internal baud rate generator to the second SLU UART. (Normal configuration)	I	R
J44	J45	Connects external clock to the second SLU UART.	R	I

Second SLU Character Formats

Five wire-wrap stakes select options to establish the second SLU character format. The ground stake can be connected to any combination of the other four stakes to configure the character format options.

The jumper stake functions are:

JUMPER FROM	TO J30	CHARACTER FORMAT OPTION
J31	IN	7-bit characters
	OUT	8-bit characters
J29	OUT	Two stop bits
	IN	One stop it
J28*	IN	Parity check enabled
	OUT	Parity check disabled
J32	IN	Odd parity if J28 is in
	OUT	Even parity if J28 is in

* If 8-bit characters (J31 OUT) are selected, parity check must be disabled (J28 OUT).

** J30 is the ground source for these functions. "IN" means that a jumper connection is to be made to J30.

Boot/Diagnostic Switches and Jumpers

A 16-pin DIP switch pack (E102) and two jumpers on the 11/23+ CPU module

provide switch-selectable bootstrap and diagnostic programs for hard and floppy disks or the customer's own bootstrap program. The 11/23+ will have the functionality as described in the following sections only if 2K x 8-bit Diagnostic/Bootstrap ROMs are installed in sockets E126 and E127.

Bootstrap/Diagnostic Configuration Switches

Switches S1-1 through S1-4 are used to select a diagnostic and/or a bootstrap program. Switches S1-5 through S1-8 are used in conjunction with switches S1-3 and S1-4 to select the specific bootstrap program desired.

S1 SWITCH	CONFIGURATION	FUNCTION
1	ON	When on, execute CPU diagnostic upon power-up or restart
2	ON	When on, execute memory diagnostic upon power-up or restart
3	OFF	When on, select DECnet boot (S1-4 through S1-7 are arguments*)
4	ON	Select console test and dialogue (S1-3 OFF) When off, select turnkey boot dispatched by S1-5 through S1-8 configuration (S1-3 OFF)

* DECnet boot arguments are:

	SWITCH POSITIONS			
BOOT DEVICE**	S1-4	S1-5	S1-6	S1-7
DUV11	ON	X	X	X
DLV11-E	OFF	ON	X	OFF
DLV11-F	OFF	ON	X	ON

** DLV11-E CSR = 775610
DLV11-F CSR = 776500

DUV11 CSR = 760040 if no devices from 760010 to 760036

X = Don't care

All boots other than the above DECnet boots are controlled by the bit patterns in the switches S1-5 through S1-8 or, if the console test is selected, a mnemonic and unit number. The console test prompts with:

TESTING MEMORY
XXXX.KW
START?

Where XXXX is the decimal multiple of 1024 words of RAM found in the system when sized from 0 up in 1024 word increments. The first word of each 1024 word segment is read, then written back into itself. The sizing routine only sizes consecutive memory from location 0 and up.

NOTE: "Testing memory" is only printed if the memory test is selected, Turnkey mode is not selected and memory size is greater than 32 KW with memory management present.

Allowed responses are a two-character mnemonic with a one digit octal unit number (default 0) or one of two special single-character mnemonics. The response must be followed by a return, the special single-character mnemonics are:

'Y' Use switch settings in S1-5 through S1-8 to determine boot device

OR 'N' HALT - Enter Microcode ODT

"TURNKEY" BOOTSTRAP PROGRAM SELECTION

SWITCHES	S1-5	S1-6	S1-7	S1-8	PROGRAM	MNEMONIC
	OFF	OFF	OFF	ON	RK06 Boot	DMn n<8
	OFF	OFF	ON	ON	RL01 or RL02 Boot	DLn n<4
	OFF	OFF	ON	ON	TU58 (SLU at 776500) Boot	DDn n<2
	OFF	ON	OFF	OFF	RX01 Boot	DXn n<2
	OFF	ON	ON	OFF	RX02 Boot	DYn n<2

Boot and Diagnostic ROM Jumpers

Two 24-pin sockets (E126 and E127) are provided for the installation of 2K x 8 ROMs or EPROMs. When EPROMs are inserted in the two ROM sockets, +5 volts must be applied to pin 21 of each socket. For all other ROMs used in this option, ROM address bit 13 (BTRA 13 H) must be applied to pin 21. Note that

supplied devices may be either ROM or EPROM type.

JUMPER FROM	TO	MEMORY TYPE ROM	EPROM
J24	J23	I*	R*
J22	J23	R	I

* I = Installed, R = Removed

Q-Bus Backplane Jumpers

Two soldered jumpers must be installed when the 11/23+ is used in a backplane in which the Q-Bus (or Extended Q-Bus) is connected to both the AB and CD rows. Ford-Higgins supplied backplanes of this type include: H9270, H9275, and the DDV11-B. The jumpers provide continuity for the interrupt acknowledge (BIAK) and direct memory access grant (BDMG) Q-Bus signals.

JUMPER	FUNCTION
W1	Connects backplane pins CM2 and CN2 providing continuity for BIAK L
W2	Connects backplane pins CR2 and CS2 providing continuity for BDMG L

NOTE: If the KDF11-B is installed in a LSI-11/CD Backplane (H9273-A) and the W1 and W2 jumpers are in, pin CM1 is shorted to CN1 and pin CR1 is shorted to CS1 on slot 2. Therefore, do not install peripherals in the slot immediately following the KDF11-B if they use these lines.

TABLE 3-14 - FACTORY JUMPER CONFIGURATION

JUMPER	JUMPER NAME	JUMPER STATE	FUNCTION
W1	BIAK	I	Provides backplane continuity for BIAK signal. Must be installed when a LSI-11/ LSI-11 backplane is used.
W2	BDMG	I	Provides backplane continuity for BDMG signal. Must be installed when a LSI-11/ LSI-11 backplane is used.

JUMPER FROM	JUMPER TO	JUMPER NAME	JUMPER STATE	FUNCTION
J22	J23	+5V	R	When EPROMs are used, jumper J24 to J23 is removed and jumper J22 to J23 is installed.
J24	J23	BTRA 13 H	I	Connects ROM address bit 13 to pin 21 of both ROM sockets (E126 to E127)
J3	J4	DL1 FE H	R	Enables BREAK HALT feature. The detection of a break condition by the console SLU causes the processor to halt and enter ODT.
J5	J4	DL1 FE H	R	No halt on break.
J6	J7	Master Clock	I	Enables internal master clock; do not remove.
J8	J9	PHASE	I	Connects PHASE signal to F11 chip clock drivers; do not remove.
J11	J10	LTC ENBJ L	R	Allows BEVENT signal to request interrupts only if bit 6 in the Line Clock Register (777546) is set.
J12	J10	DL2 ADJR L	R	Selects the following device and vector addresses for the

second SLU.

DEVICE ADDRESSES		VECTOR ADDRESSES	
RCSR	776500	Receiver	300
RBUF	776502	Transmitter	304
XCSR	776504		
XBUF	776506		

J13	J10	DL2 DISJ L	R	Enables the DL2 ADRJ L Jumper to determine the device and vector addresses for the second SLU.
J14	J10	DL1 DISJ L	R	Selects the following device and vector addresses for the console SLU.

DEVICE ADDRESSES		VECTOR ADDRESSES	
RCSR	776560	Receiver	060
RBUF	776562	Transmitter	064
XCSR	776564		
XBUF	776566		

J15	J10	BDK DISJ L	R	Enables boot/diagnostic registers, boot/diagnostic ROMs and the line clk register.
J16	J18	TRAP DPJ L	R	Enter console ODT if the processor is executing a HALT instruction and the processor is in Kernal mode.
J17	J18	PUP CDOJ L	R	Power-up code bit 0 — Bootstrap Power-up
J19	J18	PUP CDIJ L	I	Power-up code bit 1 — Mode 2
J20	J21	XTL H	I	Connects baud rate oscillator to the baud rate generator. Removed for manufacturing test only.
J25	J26	RCV IN	R	Console Loop-back test dis-

				abled.
J27	J26	XMIT OUT	I	Connects console SLU output to the console SLU connector.
J28	J30	DL2 PARJ L	R	Disable second SLU character parity check.
J29	J30	DL2 ST1J L	I	Second SLU character contains one stop-bit.
J31	J30	DL2 CH7J L	R	Second SLU character contains 8 bits.
J32	J30	DL2 ODDJ L	R	Second SLU parity check disabled by DL2 ODDJ L.
J33	J34	DCOKC2B H	R	Installed only during manufacturing testing.
J35	J34	LINITF (1) H	I	BINIT L clears console SLU.
J36	J38	DLI PARJ L	R	Disables console SLU character parity check.
J37	J38	DLI ST1J L	I	Console SLU character contains one stop bit.
J39	J38	DLI CH7J L	R	Console SLU character contains 8 bits.
J40	J38	DLI ODDJ L	R	Console parity check disabled by DLI PARJ L.
J41	J42	EXT CLK 1 H	R	Disconnects EXT CLK 1 input from the console SLU.
J43	J42	INT CLK 1 H	I	Connects baud rate clock to the console SLU.
J44	J45	EXT CLK2 H	R	Disconnects EXT CLK2 input from the second SLU.
J46	J45	INT CLK2 H	I	Connects baud rate clock to the second SLU.

TABLE 3-15 - BOOTSTRAP/DIAGNOSTIC FACTORY SWITCH CONFIGURATION

SWITCH S1 NUMBER	(E102) POSITION	FUNCTION
1	ON	Execute CPU diagnostic upon power-up or restart
2	ON	Execute Memory Diagnostic upon power-up or restart
3	OFF	DECnet boot disabled
4	ON	Console test and dialogue Enabled
5	OFF	
6	OFF	
7	ON	RL01/RL02 Bootstrap Program selected
8	OFF	

NOTE: With the switch configuration shown, the KDF11-B upon Power-Up or restart, will execute the CPU diagnostic, the Memory Diagnostic and then enter the Console test. If the operator wishes to terminate the Memory diagnostic and immediately enter the Console test, the Control/C keys must be depressed on the console terminal. If the memory test is terminated before completion, some memory locations may have wrong parity written into them.

TABLE 3-16 - SLU BAUD RATE FACTORY SWITCH CONFIGURATION

SWITCH S2 NUMBER	(E114) POSITION	FUNCTION
1	ON	
2	OFF	Console SLU set for 9600 baud per Table 3-10
3	OFF	
4	OFF	
5	ON	
6	OFF	
7	OFF	Second SLU set for 9600 baud per Table 3-13
8	OFF	

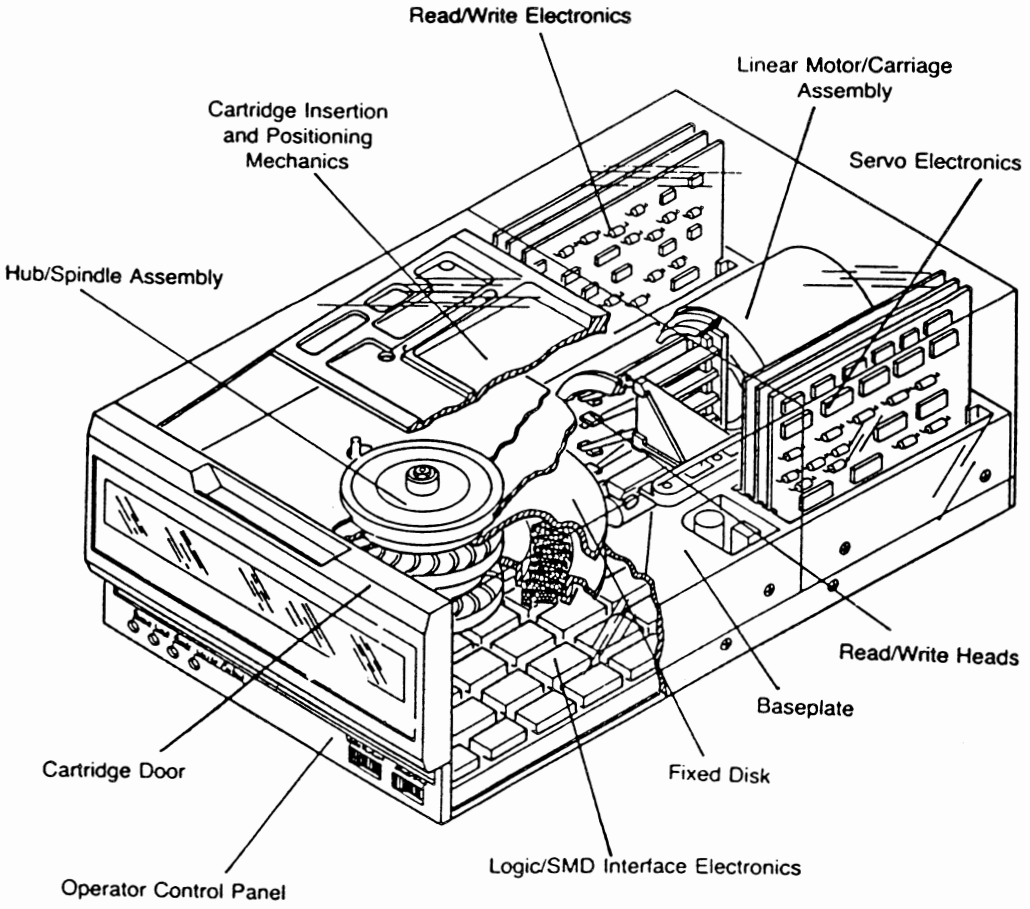
CHAPTER 4

DC40 POWER DRIVE

INTRODUCTION

The DC40 is the first of a family of high performance 8-inch disk drives that incorporate applicable elements of Winchester/Whitney technology. Unformatted storage capacity of the DC40 is 53.2 megabytes, with 26.6 megabytes in an ANSI-standard removable cartridge and 26.6 megabytes on a fixed medium.

FIGURE 4-1 - DC40 BASIC COMPONENTS



BASIC COMPONENTS

Basic components in the drive are shown in Figure 4-1. They consist of:

* Base Plate
* Spindle with integral spindle drive motor and fixed disk
* Cartridge insertion and positioning mechanism
* Linear servo motor and cartridge assembly with read/write heads
* Read/Write electronics
* Servo Drive electronics
* Logic/SMD interface electronics
* Air cooling and filtration components
* Operator control switches and indicators

PERFORMANCE CHARACTERISTICS

The performance characteristics of the DC40 Disk Drive are shown in Table 4-1.

TABLE 4-1 - PERFORMANCE CHARACTERISTICS

	CAPACITY	
	Unformatted	Formatted
Cartridge	26.6 Mbytes	21 Mbytes
Fixed Disk	26.6 Mbytes	21 Mbytes
Total	53.2 Mbytes	42 Mbytes

	CONFIGURATION
Number of Disks	1 Fixed, 1 Removable (Cartridge)
Data Surfaces	2 Fixed, 2 Removable
Data Heads	4 (1 per surface)
Servo	Embedded
Tracks per Surface	644
Track Density	555 Tracks per Inch
Track Capacity	Unformatted: 20,672 Bytes Formatted: 16,384 Bytes

PERFORMANCE

Actuator	Linear Voice-Coil Motor
Access Time (Seek and Latency)	
	Track to Track: 10 msec.
	Average: 35 msec.
	Maximum: 55 msec.
Average Latency	8.45 msec.
Rotation Speed	3545 RPM
Data Transfer Rate	1.229 Mbytes/sec.
Start Time	45 seconds
Stop Time	15 seconds
Stop Time (Power off)	120 seconds

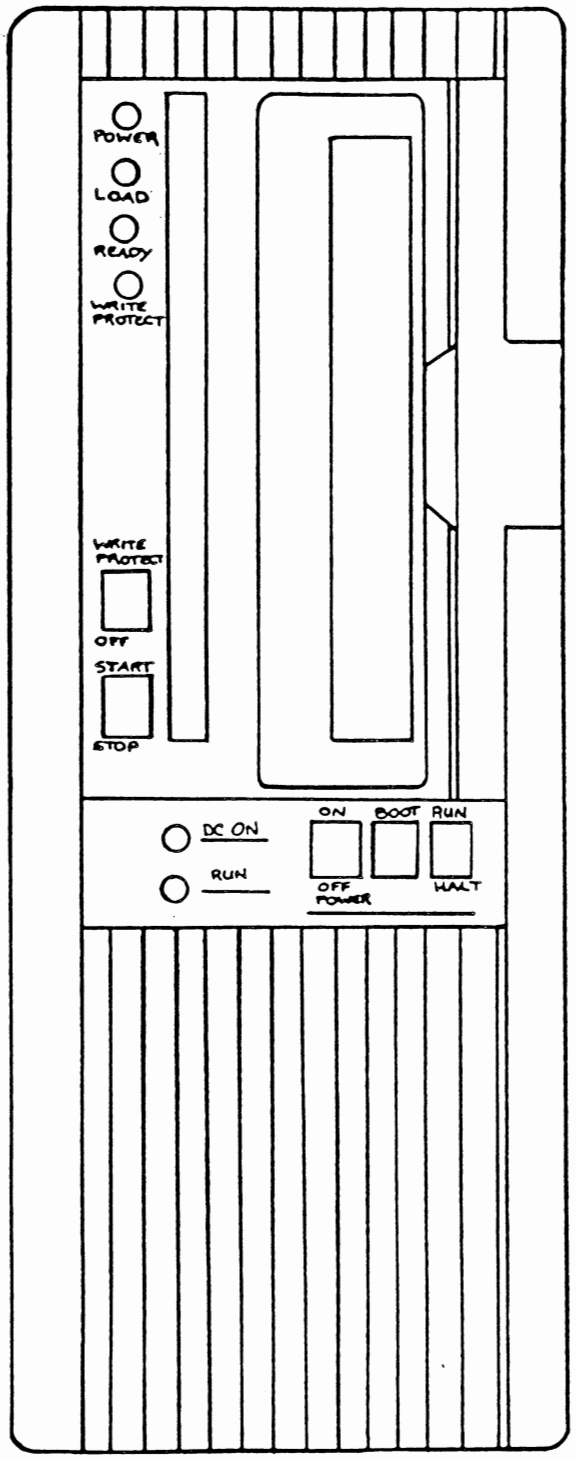
READ/WRITE

Interface	SMD
Recording Method	Whitney, 2-of-7 run length limit code
Recording Density	10,889 bits/inch
Flux Density	7259 flux-reversals/inch

PHYSICAL DIMENSIONS

Drive	Height	4.62 in	(117.4mm)
	Width	8.55 in	(217.1)
	Depth	14.00 in	(355.6mm)
	Weight	26 lbs	(11.8kg)
Cartridge	Height	1.0 in	(25mm)
	Width	8.2 in	(208mm)
	Depth	8.3 in	(211mm)
	Weight	1.5 lbs	(0.7kg)

FIGURE 4-2 - OPERATOR CONTROL PANEL



OPERATION

Operator Controls and Indicators

The locations of the operator controls and indicators are shown in Figure 4-2. All operator controls and indicators are on the front panel. A full operational description of these controls and indicators are given in Table 4-2.

TABLE 4-2 - CONTROLS AND INDICATORS

CONTROL OR INDICATOR	OPERATIONAL DESCRIPTION
START/STOP Rocker Switch	To initiate a spin-up and load heads sequencing of the drive, assuming the following conditions have been met. A. All proper DC power has been provided B. The cartridge is loaded C. The cartridge door is closed and locked D. The head carriage is home, in its unloaded position E. The local mode option is selected (if the remote option is selected, the hold control line should be at a low logic level) Pressing the START switch energizes the spin motor and brings the disks up to normal speed, while a purge period is under way. After the purge period the heads are loaded onto the disks and a seek to cylinder zero is performed. During the start sequence a resident set of diagnostics will have been executed. Drive Ready is achieved in 45 seconds and is indicated when the Ready indicator is lit. Pressing the STOP switch during the spin-up sequencing, or when the drive is Ready initiates head retract to the home position and spindle braking. This requires approximately 15 seconds for the complete spin-down sequence. When the LOAD indicator is lit, the cartridge may be removed. An automatic safety latch secures

the cartridge access door closed any time the LOAD indicator is not lit.

The START/STOP switch will also clear a primary fault and initiate a reset procedure by cycling the switch from its current position and then back again. See "ERROR CONDITIONS AND ACTIONS."

WRITE PROTECT Rocker Switch

Allows the operator to place the drive's fixed media in read-only mode for file protection purposes. Pressing this switch will turn on or off the Write Protect indicator (towards indicators: on; away from indicators: off). When the indicator is lit, writing on the fixed disk is inhibited, and any command to write in the protected file will cause an error. To update fixed volume data the Write Protect indicator must be turned off, allowing both reading and writing.

The Write Protect switch will also clear a secondary type of device fault and initiate a recovery procedure by cycling the switch from its current position and then back again. See "ERROR CONDITIONS AND ACTIONS."

Write Protect status for the removable cartridge is governed by a removable write enable tab on the back of the cartridge. When the tab is removed, writing in the removable volume is inhibited. Any command to write in the protected files will cause an error condition.

POWER LED Indicator

Indicates that DC power is on.

LOAD LED Indicator

Indicates that drive is available for disk cartridge insertion or removal.

READY LED Indicator

Indicates that drive is ready to receive commands for data transfer to/from host.

WRITE PROTECT LED Indicator

Indicates that fixed media has been write protected.

Note: When any of the indicators are flashing on and off, an error condition code is being indicated to the operator. Refer to section on error conditions and actions.

Operating Procedures

The following procedures are for normal day to day use and should only be performed after installation and initial checkout has been performed.

Power Up

Apply power to disk system power supplies or with the optional DC power supply place the ON/OFF switch to ON. Both the POWER and LOAD indicators should now be

Start/Spin-Up

1. Install disk cartridge as per the "CARTRIDGE INSTALLATION" procedure.
2. Place START/STOP switch to start. The LOAD indicator will extinguish as the cartridge door is locked and the spin motor comes up to speed.
3. Within 50 seconds the READY indicator should illuminate. If after 50 seconds the READY indicator is not lit, an error condition may exist; see the procedure on error conditions and actions.

Write Protect

1. Remove write tab from disk cartridge as shown in Figure 4-3.
2. Perform Start/Spin-Up procedure.
3. Place drive in Write Protect mode by depressing the WRITE PROTECT switch. The WRITE PROTECT indicator should now be lit.

Stop/Spin-Down

1. Depress the START/STOP switch to STOP. The READY indicator will

extinguish as the spin motor spins down. After 10 seconds the spin motor should have stopped and the LOAD indicator illuminated.

2. Remove the disk cartridge, if desired, as per the "Normal Cartridge Removal" procedure. Remember the cartridge door does not unlock until the LOAD indicator is lit.

Power Down

Remove power to the disk system power supplies or with optional DC power supply place the ON/OFF switch to OFF. All indicators should now be off. With no power present it is impossible to open the cartridge normally. See the "Emergency Cartridge Removal" procedure.

Cartridge Handling and Storage

When handling or storing the removable disk cartridge, shown in Figure 4-3, the following practices should be observed.

1. Never manually try to open the door to the air inlet and head port openings.

2. Store the disk cartridge in its protective jacket when not inserted in the drive.

3. Avoid stacking the disk cartridges on one another. Cartridges can be stored on edge or flat.

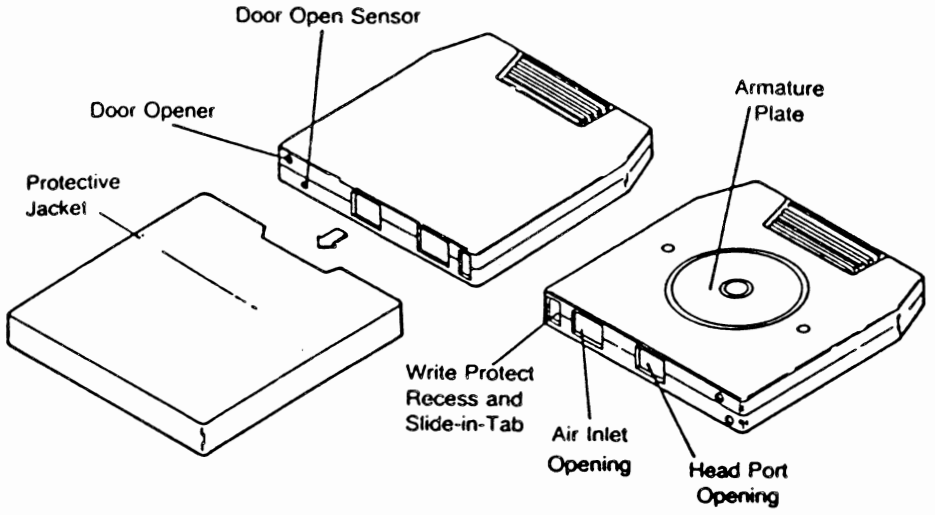
4. When the cartridge is removed from its protective jacket, store the jacket in such a way as to prevent dust from collecting inside.

5. Disk cartridges should be stored in a cool, dry place and kept free of dust accumulations. Preferably stored in the same computer room or office as the drive or in an equally clean and temperate environment.

6. Cartridges should be kept away from magnetic sources. Do not place cartridges on top of drive enclosure or near CRT displays.

7. Keep cartridges out of direct sunlight and away from sources of heat.

FIGURE 4-3 - REMOVABLE DISK CARTRIDGE



Cartridge Stabilization

The removable disk cartridge must be allowed to stabilize to the same temperature as the drive at least one hour prior to installation and use. In the event a cartridge is brought in from a temperature environment significantly colder than the operating temperature, below 60 degrees F (16 C), the possibility of condensation in the cartridge exists. If condensation occurs, disk cartridges should not be used for at least 24 hours after all condensation disappears from the exterior surfaces.

Error Condition Codes

When any of the LED indicators are flashing on and off, an error condition or fault has occurred. The indicators will be flashing repetitively a three digit hexadecimal code in the form FXX, where the hexadecimal digit F indicates the start of the string and XX are the actual two digit hexadecimal error code. Table 4-3 contains all error codes and a description of each.

Operator Actions

There are two types of error conditions: primary device faults and secondary device faults. The following are a list of the required actions.

1. To clear a secondary device fault and initiate a recovery, cycle

the WRITE PROTECT switch from its current position for one complete cycle of the flashing lights, and then back again. These faults can also be cleared and recovered by issuing a fault clear command from the Controller.

2. To clear a primary device fault and initiate a recovery, cycle the START/STOP switch from its current position and back again.

3. If neither procedure seems successful or the problem persists, contact your service representative.

A list of all error codes and required operator actions are contained in Table 4-3.

TABLE 4-3 - ERROR CONDITION CODES AND OPERATOR ACTIONS

ERROR CODE	ERROR DESCRIPTIONS	FAULT TYPE P/S	OPERATOR ACTIONS
	HARDWARE - Basic		
11	No carriage return from terminal	P	2,3
12	Deadman timer too short	P	2,3
13	Deadman timer too long		
14	Write current unsafe	P	2,3
15	Power unsafe test failed	P	2,3
16	Not Used		
17	Not Used		
18	Not Used		
19	Not Used		
1A	Not Used		
1B	Not Used		
1C	Download checksum error	P	2,3
1D	Not Used		
1E	Not Used		
	HARDWARE - Control		
21	Not Used		
22	Cannot find sync	P	2,3
23	Servo field error	S	1,2,3
24	Not Used		
25	No index	S	1,2,3
26	Write gate fault 2	S	1,2,3
27	Write gate fault 1	S	1,2,3
28	Actuator current detected	P	2,3
29	Hardware fault	P	2,3
2A	Actuator command with no command in	S	1,2,3
2B	No offset directed, but have	S	1,2,3

	command		
2C	Have detected fault, but no fault	S	2,3
2D	Not Used		
2E	Not Used		

Operator Actions to be taken in order one at a time:

1. Toggle WRITE PROTECT switch
2. Toggle START/STOP switch
3. Contact Service Representative

SPIN

31	Will not spin up	P	2,3
32	Spinning in wrong direction	P	2,3
33	Spin up too slow	P	2,3
34	Not Used		
35	Not Used		
36	Trying to spin-up when not stopped	P	2,3
37	Not Used		
38	Not Used		
39	Not Used		
3A	Not Used		
3B	Spin down too slow	P	2,3
3C	Not spinning for Hall test	P	2,3
3D	Spin too slow	P	2,3
3E	Spin too fast	P	2,3

ACTUATOR

41	Heads not unloaded	P	2,3
42	Heads retracted during normal operation	P	2,3
43	Heads did not load	P	2,3
44	No spin for loading Heads	P	2,3
45	Heads did not load - emergency retract	P	2,3
46	Heads not loaded	P	2,3
47	Not Used		
48	Not Used		
49	Not Used		
4A	Not Used		
4B	Not Used		
4C	Not Used		
4D	Not Used		
4E	Not Used		

Operator Actions to be taken in order one at a time.

1. Toggle WRITE PROTECT switch
2. Toggle START/STOP switch
3. Contact Service Representative

SERVO

51	No end conversion ADC	P	2,3
52	A/D out of tolerance	P	2,3
53	D/A out of tolerance	P	2,3
54	Off track-position	S	1,2,3
55	Off track-address	S	1,2,3
56	Not Used		
57	Not Used		
58	Not Used		
59	Not Used		
5A	Not Used		
5B	D/A to A/D disagree	P	2,3
5C	Seek error - did not arrive at target	S	1,2,3
5D	Seek duration too long	S	1,2,3
5E	Seek retry - too many	S	1,2,3

MISCELLANEOUS

61	Software interrupt	P	2,3
62	Power unsafe interrupt	P	2,3
63	ICF interrupt	P	2,3
64	OCF interrupt	P	2,3
65	TOF interrupt	P	2,3
66	Terminal interrupt	P	2,3
67	NMI interrupt	P	2,3
68	Door switch closed when solenoid energized	P	2,3
69	Door opened during normal operation	P	2,3
6A	Not enough cylinders in inner guard band	P	2,3
6B	Not enough cylinders in outer guard band	P	2,3
6C	Not Used		
6D	Not Used		
6E	Not Used		

Operator Actions to be taken in order one at a time.

1. Toggle WRITE PROTECT switch
2. Toggle START/STOP switch
3. Contact Service Representative

OPERATOR and SMD INTERFACE

71	Data parameter entry error (keybd)	S	1,2,3

72	Cartridge not in place	P	2,3
73	Door not closed properly	P	2,3
74	Cylinder request over range	S	1,2,3
75	Not Used		
76	Seek attempted when not ready, not on cylinder, seek error or fault	S	1,2,3
77	Both rev. and fwd. offset received	S	1,2,3
78	Invalid user command	S	1,2,3
79	Tag-2 received when not ready	S	1,2,3
7A	Not Used		
7B	Not Used		
7C	Not Used		
7D	Not Used		
7E	Not Used		

Operator Actions to be taken in order one at a time.

1. Toggle WRITE PROTECT switch
2. Toggle START/STOP switch
3. Contact Service Representative

Environmental Considerations

Both the Model DC40 and Cartridge have been designed to operate in a computer room or typical office environment. Table 4-4 summarizes the required environmental conditions.

TABLE 4-4 - ENVIRONMENTAL CONSIDERATIONS

	TEMPERATURE
Operating Drive:	50 to 104 F (10 to 40 C) with maximum gradient of less than 2 F (1 C) per minute, not to exceed 18 F (1 C) per hour.
Non-Operating Drive:	-40 to 140 F (-40 to 60 C)
Cartridge Storage:	0 to 115 F (-18 to 46 C) Note: Cartridges must be allowed to stabilize to the same temperature environment as the drive for at least one hour prior to installation and use.
	RELATIVE HUMIDITY

Operating Drive:	20 to 80%, non-condensing
Non-Operating Drive:	5 to 95%, non-condensing
Cartridge Storage:	5 to 95%, non-condensing

ALTITUDE

Operating Drive:	1,000 feet (300 m) below sea level to 10,000 feet (3 km) above sea level
Non-Operating Drive:	1,000 feet (300 m) below sea level to 40,000 feet (12.2 km) above sea level
Cartridge Storage:	Same as Non-Operating Drive.

Power Requirements

The DC power supply used must be capable of delivering the following DC voltages, Table 4-5, within the specifications provided for each at the J10 drive connector.

TABLE 4-5 - DC POWER REQUIREMENTS

VOLTAGE INPUT	TOLERANCE @ 25 C	REGULATION OVERLOAD RANGE	LOAD CURRENTS MAX	MIN
+5 V	+/- 4%	+/- 0.8%	4A	3A
-5.2 V	+/- 4%	+/- 2%	2A	1.5A
-12 V	+/- 5%	+/- 2%	2.5A	0.3A
+24V	+/- 8%	-	4.5A	0.15A

Interface Cables and Connectors

The DC40 uses an industry standard SMD interface, consisting of two flat ribbon cables. The "A" cable, 60 lines, contains all the control signals and the "B" cable, 26 lines, contains all the read/write signals. The pin assignments for each cable are listed in Table 4-6 and the general characteristics are given in Table 4-7.

TABLE 4-6 - SMD INTERFACE CABLE PIN ASSIGNMENTS, A CABLE

SIGNAL NAME	DIRECTION OF SIGNAL CONTROLLER DRIVE	BALANCED SIGNAL PINS (-,+)	NOTES
Tag 1	----------	1,31	
Tag 2	----------	2,32	
Tag 3	----------	3,33	
Bit 0	----------	4,34	
Bit 1	----------	5,35	
Bit 2	----------	6,36	
Bit 3	----------	7,37	
Bit 4	----------	8,38	
Bit 5	----------	9,39	
Bit 6	----------	10,40	
Bit 7	----------	11,41	
Bit 8	----------	12,42	
Bit 9	----------	13,43	
Open Cable Detect	----------	14,44	
Fault	----------	15,45	
Seek Error	----------	16,46	
On Cylinder	----------	17,47	
Index	----------	18,48	
Unit Ready	----------	19,49	
Address Mark Found	----------	20,50	1
Busy	----------	21,51	2
Unit Select Tag	----------	22,52	
Unit Select 2	----------	23,53	
Unit Select 2	----------	24,54	
Sector	----------	25,55	
Unit Select 2	----------	26,56	
Unit Select 2	----------	27,57	
Write Protected	----------	28,58	
Pick	----------	29	3
Hold	----------	59	4
Not Used	----------	30,60	

NOTES:
1. Always logic zero if unit selected
2. Daisy chained signal, not generated
3. Not balanced signal, daisy chained not interpreted
4. Not balanced signal

Ground	----------	1	
Servo Clock	----------	2,14	
Ground	----------	15	
Read Data	----------	3,16	
Ground	----------	4	
Read Clock	----------	5,17	

Ground	----------	18
Write Clock	----------	6,19
Ground	----------	7
Write Data	----------	8,20
Ground	----------	21
Unit Select	----------	22,9
Seek End	----------	10,23
Ground	----------	11
Index	----------	12,14
Ground	----------	25
Sector	----------	13,26

TABLE 4-7 - SMD CABLE CHARACTERISTICS

A CABLE
Type: 30 Pair, Flat Cable
Twists Per Inch: 2
Impedance: 100+/-10 Ohms
Wire Size: 28 AWG, 7 Strands
Propagation Time: 1.6 to 1.8 nsec./ft.
Maximum Cable Length: 100 ft. cumulative
Voltage Rating: 300 V rms

B CABLE
Type: 26 Conductor, Flat Cable with Ground Plane and Drain Wire
Impedance: 65 Ohms
Wire Size: 28 AWG, 7 Strands
Propagation Time: 1.5 to 1.8 nsec./ft.
Maximum Cable Length: 50 ft.
Voltage Rating: 300 V rms

Configurations

When using the Daisy-Chained disk system only one drive in the chain (usually the last drive) is allowed to have A cable signal terminators. This requires that four 16 pin DIP resistor packs be removed from their sockets on the base PC board of each drive in the chain except for one. If external terminators are to be used the internal resistor packs must be removed.

The following procedure lists the steps necessary to remove the terminator resistor packs (refer to Figure 4-6).

CAUTION: This procedure should only be performed by trained service personnel.

1. Disconnect all power and interface cables from the drive.

2. Remove the six screws (three on a side) along the bottom of the unit that secures the base PC board to the drive.

3. Lower the PC board from the drive disconnecting the inter-board ribbon cable and ground wire. Caution must be used since components can be damaged by electrostatic discharge.

4. Remove the four 16-pin resistor packs, shown in Figure 4-6, from their DIP sockets. Use an IC extractor if available. Save resistor packs for possible future use.

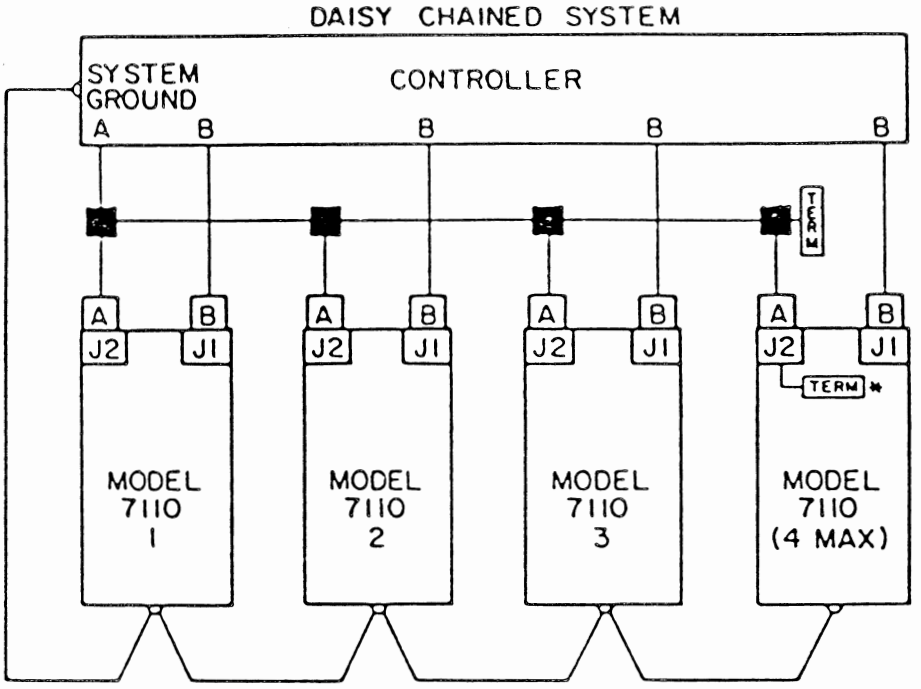
NOTE: The internal jumper options should be set at this time.

5. Replace inter-board ribbon cable and ground wire.

6. Secure the base PC board back on the bottom of the drive using the six removed screws.

Repeat procedure for all required drives.

FIGURE 4-4 - DAISY CHAINED INTERFACE CONFIGURATION



Unit Address Selection

The logical unit address is set for each disk drive by selecting the proper switch setting for the DIP switch block that resides behind the operator control panel on the base PC board. See Figure 4-5. To gain access to these switches, just flip the control panel up. A list of possible addresses and their settings are given in Table 4-8.

TABLE 4-8 - UNIT ADDRESS SWITCH SETTINGS

LOGICAL UNIT ADDRESS	ADDRESS BITS 2	2	2	2	SWITCHES 1	2	3	4
0	0	0	0	0	ON	ON	ON	ON
1	0	0	0	1	ON	ON	ON	OFF
2	0	0	1	0	ON	ON	OFF	ON
3	0	0	1	1	ON	ON	OFF	OFF
4	0	1	0	0	ON	OFF	ON	ON
5	0	1	0	1	ON	OFF	ON	OFF
6	0	1	1	0	ON	OFF	OFF	ON
7	0	1	1	1	ON	OFF	OFF	OFF
8	1	0	0	0	OFF	ON	ON	ON
9	1	0	0	1	OFF	ON	ON	OFF
10	1	0	1	0	OFF	ON	OFF	ON
11	1	0	1	1	OFF	ON	OFF	OFF
12	1	1	0	0	OFF	OFF	ON	ON
13	1	1	0	1	OFF	OFF	ON	OFF
14	1	1	1	0	OFF	OFF	OFF	ON
15	1	1	1	1	OFF	OFF	OFF	OFF

Of the two other switches, switch 6 is not used and switch 5 is for the remote spin-up option. See Table 4-9.

Internal Jumper Option Selection

Several user selectable jumper options exist on the base PC board. A list of the Internal Jumpers is contained in Table 4-9.

The following procedure lists the required steps to select the appropriate jumper options.

CAUTION: This procedure should only be performed by trained service personnel.

1. Disconnect all power and interface cables from the drive.
2. Remove the six screws (three on a side) along the bottom of the unit that secures the base PC board to the drive.
3. Lower the PC board from the drive, disconnecting the inter-board ribbon cable and ground wire. Caution must be used since components can be damaged by electostatic discharge.
4. Select proper jumper options by referring to Table 4-9.
5. Replace inter-board ribbon cable and ground wire.
6. Secure base PC board back to bottom of drive using the six removed screws.

TABLE 4-9 - INTERNAL JUMPER OPTIONS

DESCRIPTION	BOARD LOCATIONS	SETTINGS	FACTORY DEFAULT
S5 Remote Spin-Up	Switch Block	Up: Local Spin-Up Down: Remote Spin-Up	X
Z1 Read Driver Enable	A7	For Maintenance Only	
Z2 Read Clock Polarity	A7	1,2: Normal 2,3: Inverse	X
Z6 Seek On Head Change	E11	G: Automatic Seek On Head Change S: Seek Command Required After Head Change	X
Z7 Interface Servo Clock Source	J5	1,2: Frequency Locked Clock 2,3: Servo Field Clock	X
Z9 External ROM Emulator	M10	For Maintenance Only	

DC Power Cable and Connector

If the optional DC power supply is not being used, make sure the DC supply cable consists of eight single wires, 18 AWG, and the cable connector is a Molex 2139 Series or equivalent female connector. See Table 4-10 for the J10 DC power pin assignments.

FIGURE 4-5 - BASE PCB, INTERNAL JUMPER LOCATIONS

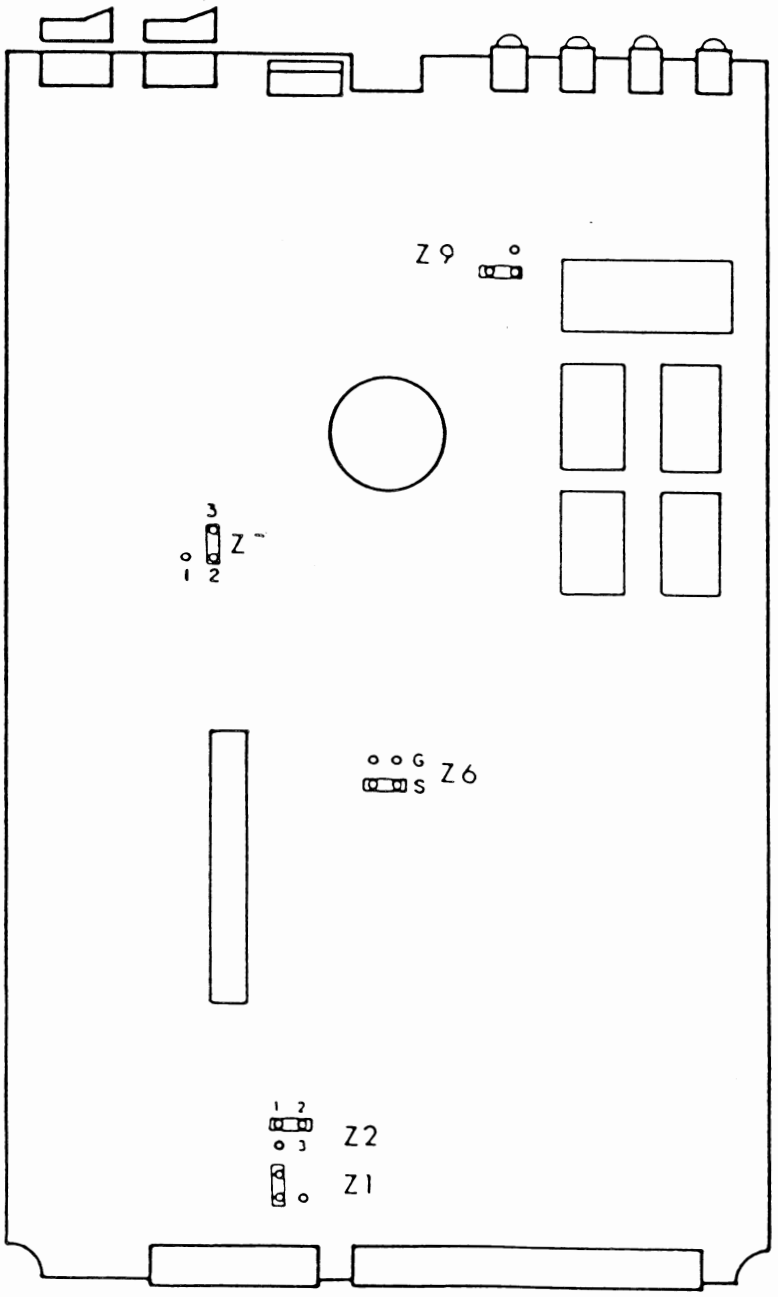


TABLE 4-10 - J10 POWER PIN ASSIGNMENTS

PIN NUMBER	USAGE
1	+24 V
2	Ground
3	Ground
4	-12 V
5	Ground
6	-5 V
7	Ground
8	+5 V

GROUNDING

To ensure reliable operation, a good DC ground should exist between all drives and the controller or computer system. Using a low impedance braided cable, connect all the drives in the disk system together with the system ground. If optional DC power supplies are being used, they too should be connected to this ground.

INITIAL CHECKOUT AND START UP

The following procedure is used to make the initial power application to the DC40 Power Drive. This procedure assumes that the preceding procedures and requirements of this section have been performed.

1. Ensure the system AC power circuit breaker is off.

2. Verify the START/STOP rocker switch is in the off position.

3. Install the DC power cable from the DC power supply to the J10 connector at rear of drive (connector not keyed).

4. Connect the A and B interface cables according to the disk system configuration.

5. Turn on the subsystem AC power circuit breaker.

6. Turn on system power switch. The POWER and LOAD indicators should be illuminated. The WRITE PROTECT indicator may be on, depending on the position of the WRITE PROTECT rocker switch.

7. Insert a disk cartridge into the disk drive. As the cartridge door closes, an audible "clunk" should be heard when the cartridge seats on the spindle.

8. Position the START/STOP switch to START. The spin-up sequence is initiated: the spindle should begin to rotate, the load indicator extinguishes and the cartridge door locks.

9. Ensure that disk is operating normally, and no error messages occur.

OPTIONS

The items in Table 4-11 are accessories to the DC40 Power Drive.

TABLE 4-11 - OPTIONS

DESCRIPTION	PART NUMBER
Removable Cartridge	082-00775-001
DC40 Power Supply, 120 VAC	101-00150-001
DC40 Power Supply, 220 VAC	107-01074-001
Cable, Power Supply to Drive	102-00498-001
Cooling Fan Assembly, 120 VAC	107-01067-007
Cooling Fan Assembly, 220 VAC	107-01067-008
SMD Control "A" Cable	102-00147-0XX*
SMD R/W "B" Cable	102-00148-0XX*

*Last two digits denote cable length

CABLE LENGTH (in feet)	2	4	6	8	10	15	20	25	30	35	40	50
"A" Cable (Radial) 102-00147-0XX	01	02	03	04	05	06	07	08	09	10	11	12
"A" Cable (w/Daisy Chain Connector) 102-00147-0XX	31	32	33	34	35	36	37	38	39	40	41	42
"B" Cable 102-00148-0XX	01	02	03	04	05	06	07	08	09	10	11	12

CHAPTER 5

CQ06 DISK CONTROLLER

INTRODUCTION

Described in this manual is the installation, operation, programming, troubleshooting, and theory of operation for the Ford-Higgins Ltd. CQ06 Disk Controller. The controller interfaces the 11/23+ computer to one or two SMD I/O disk drives, including 8- and 14-inch Winchester, SMD pack and CMD cartridge type drives. The entire contoller occupies one quad module in the backplane. Full sector buffering in the contoller matches the transfer rate of the disk drive and the CPU. The controller is compatible with RK06/RK07 software drivers in RT-11, RSX-11, and RSTS/E.

CONTROLLER CHARACTERISTICS

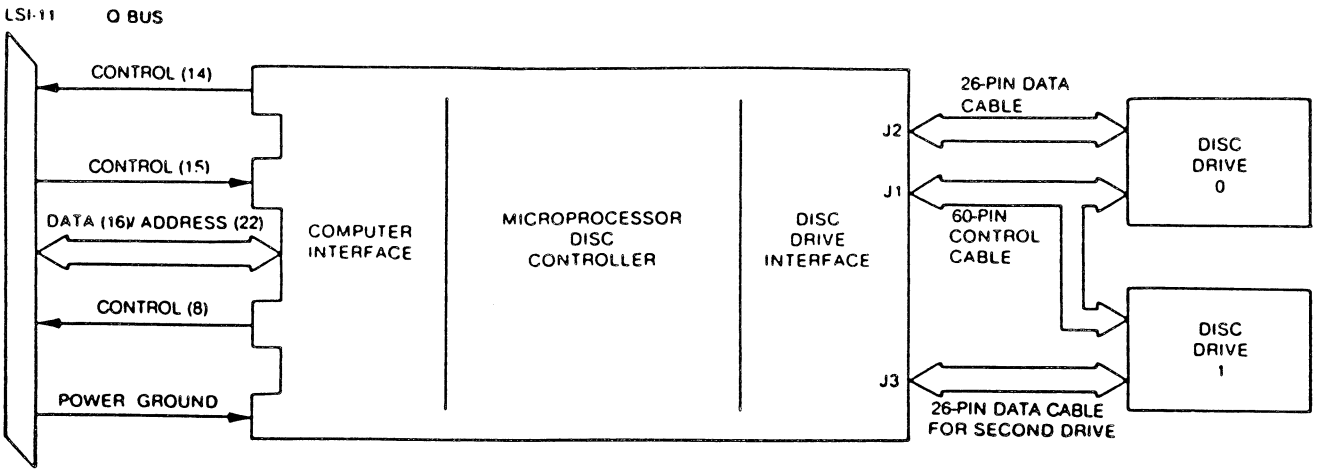
The CQ06 Disk Controller links the 11/23+ computer to one or two disk storage units. The controller receives and interprets commands from the computer and translates them into a form compatible with the disk. Buffering and signal timing for data transfers between the computer and the disks are also handled by the controller.

The sequence and timing of the controller is a microprocessor. The control information is stored as firmware instructions in read-only-memory (ROM) on the controller board. A diagnostic program contained in the ROM tests the functional operation of the controller. This self-test is performed automatically each time power is applied. A green light on the control board indicates if the self-test is successful.

Data is transferred directly to and from the computer memory using the DMA facility of the 11/23+ Q-Bus. The controller monitors the status of the disk units and the data being transferred and supplies this information to the computer upon request. An error correction code with a 56-bit checkword corrects error bursts up to 11-bits. To compensate for media errors, bad sectors are skipped and alternates assigned. There is also an automatic retry

feature for read errors. The controller is capable of addressing up to four megabytes and controlling up to two disk drives in various configurations up to a total on-line formatted capacity of 220.32 megabytes. Figure 5-1 is a simplified diagram of a disk system.

FIGURE 5-1 - DISK CONTROLLER SYSTEM DIAGRAM



11/23+ Q-Bus Interface

Commands, data and status transfers between the controller and the computer are executed via the parallel I/O bus (Q-bus) of the computer. Data transfers are direct to memory via the DMA facility of the Q-bus; commands and status are under programmed I/O. Controller/Q-bus interface lines are listed in Table 5-1.

TABLE 5-1 - CONTROLLER/Q-BUS INTERFACE LINES

BUS PIN	MNEMONIC	CONTROLLER INPUT/ OUTPUT	DESCRIPTION
AC2, AJ1, AM1, AT1, BJ1, BM1, BT1, BC2, CC2, CJ1, CM1, CT1, DC2, DJ1, DM1, DT1	GND	O	Signal Ground and DC return.
AN1	BDMR L	O	Direct Memory Access (DMA) request from controller: active low.
AP1	BHALT L	N/A	Stops program execution. Refresh and DMA is enabled. Console operation is enabled.
AR1	BREF L	N/A	Memory Refresh.

BA1	BDCOK H	I	DC power ok. All DC voltages are normal.
BB1	BPOK H	N/A	Primary power ok. When low activates power fail trap sequence.
BN1	BSACK L	O	Select Acknowledge. Interlocked with BDMGO indicating controller is bus master in a DMA sequence.
BR1	BEVNT L	O	External Event Interrupt Request. Real Time Clock Control.
AA2,BA2,BV1,CA2, DA2	+5	I	+5 volt system power.
AD2,BD2	+12	N/A	+12 volt system power.
AE2	BDOUT L	I/O	Data Out. Valid data from bus master is on the bus. Interlocked with BRPLY.
AF2	BRPLY L	I/O	Reply from slave to BDOUT or BDIN and during IAK.
AH2	BDIN L	I/O	Data Input. Input transfer to master (states master is ready for data). Interlocked with BRPLY.
AJ2	BSYNC L	I/O	Synchronize: becomes active when master places address on bus; stays active during transfer.
AK2	BWTBT L	I/O	Write Byte: indicates output sequence to follow (DATO or DATOB) or marks byte address time during a DATOB.
AA1,AB1,AL2,BP1	BIRQ4L,5, 6,7	O	Interrupt Request.
AM2 AN2 CM2	BIAK1I L BIAK1O L BIAK2I L	I O I	Serial Interrupt Acknowledge input and output lines routed from Q-Bus, through devices, and

CN2	BIAK20 L	O	back to processor to establish and interrupt priority chain.
AT2	BINIT L	I	Initialize. Clears devices on I/O bus.
AU2,AV2,BE2,BF2, BH2,BH2,BK2,BL2, BM2,BN2,BP2,BR2, BS2,BT2,BU2,BV2	BDAL0 L through BDAL15 L	I/O	Data/address lines, 0-15
AR2 AS2 CR2 CS2	BDMG1I L BDMG1O L BDMG2I L BDMG2O L	I O I	DMA Grant Input and Output. Serial DMA priority line from computer, through devices and back to computer.
AP2	BBS7 L	I	Bank 7 Select. Asserted by bus master when address in upper 4K bank is placed on the bus.
AC1,AD1,BC1,BD1, BE1,BF1	BDAL 16 L -BDAL 21 L	O	Extended Address Bits 16-21.

Interrupt

The interrupt vector address is factory-set to address 210 (or 254). The vector address is programmed in a PROM on the controller, allowing user selection. Interrupt requests are generated under the following conditions:

1. When the Controller Ready bit is set upon completion of a command.

2. When any drive sets an associated Attention Flag in the Attention Register and the Controller Ready bit is set.

3. When the controller or any drive indicates the presence of an error by setting the combined Error/Reset bit in the Control and Status Register.

4. When the Controller Ready bit is set by conventional initialization upon completion of a controller command or when an error condition is detected. A forced interrupt may be generated by the Controller Ready and Interrupt Enable bits for test purposes.

Disk Interface

The controller interfaces one or two disk drives through 60- and 26-pin cables. If two drives are used, the 60-pin control cable ("A" cable) is daisy-chained to drive 0 and 1. The 26-pin cables ("B" cable) are connected separately from the controller to each drive. The maximum length of the 60-pin cable is 100 feet. The maximum length of the 26-pin cable is 50 feet. Table 5-2 lists the 60-pin interface signals, and Table 5-3 lists the 26-pin interface signals.

TABLE 5-2 - CONTROLLER TO DRIVE I/O INTERFACE: "A" CABLE

SIGNAL NAME (FHL TERM)	PIN POLARITY (ACTIVE) −	+	SOURCE
Device Select 0 (USEL0)	23	53	Controller
Device Select 1 (USEL1)	24	54	Controller
Device Select 2 (USEL2)	26	56	Controller
Device Select 3 (USEL3)	27	57	Controller
Select Enable (USTAG)	22	52	Controller
Set Cylinder Tag (TAG1)	1	31	Controller
Set Head Tag (TAG2)	2	32	Controller
Control Select (TAG3)	3	33	Controller
Bus Out 0 (BIT0)	4	34	Controller
Bus Out 1 (BIT1)	5	35	Controller
Bus Out 2 (BIT2)	6	36	Controller
Bus Out 3 (BIT3)	7	37	Controller
Bus Out 4 (BIT4)	8	38	Controller
Bus Out 5 (BIT5)	9	39	Controller
Bus Out 6 (BIT6)	10	40	Controller
Bus Out 7 (BIT7)	11	41	Controller
Bus Out 8 (BIT8)	12	42	Controller
Bus Out 9 (BIT9)	13	43	Controller
Bus Out 10 (BIT10)	30	60	Controller
Device Enable (OCD)	14	44	Controller
Index (INDEX)	18	48	Drive
Sector Mark (SEC)	25	55	Drive
Fault (FAULT)	15	45	Drive
Seek Error (SERR)	16	46	Drive
On Cylinder (ONCYL)	17	47	Drive
Unit Ready (UNRDY)	19	49	Drive
Write Protected (WPRT)	28	58	Drive
Address Mark (AMF)	20	50	Drive
Bus-Dual-Port Only	21	51	Drive
Sequence In (PICK)	29		Controller
Hold (HOLD)	59		Controller

TABLE 5-3 - CONTROLLER TO DRIVE I/O INTERFACE: "B" CABLE

SIGNAL (FHL TERM)	PIN POLARITY (ACTIVE) -	+	GROUND	SOURCE
Ground			1	
Servo Clock (SCLOCK)	2	14		Drive
Ground			15	
Read Data (RDATA)	3	16		Drive
Ground			4	
Read Clock (RCLOCK)	5	17		Drive
Ground			18	
Write Clock (WCLOCK)	6	19		Controller
Ground			7	
Write Data (WDATA)	8	20		Controller
Ground			21	
Unit Selected (USEL)	22	9		Drive
Seek End (SEEK)	10	23		Drive
Ground			11	
Reserved for Index	12	24		
Ground			25	
Reserved for Sector	13	26		

Operating System Compatibility

RT-11: The emulation is transparent to the RT-11 version 4.0 operating system, using the standard device handler supplied by FHL.

RSX-11: The emulation is transparent to the RSX-11M and RSX-11M-PLUS version 4.0 operating systems, using the standard device handler supplied by FHL.

RSTS/E: The emulation is transparent to the RSTS/E version 7.2 operating system, using the standard device handler supplied by FHL.

Controller Specifications

(Controller specifications are subject to change without notice.)

MECHANICAL: The Model CQ06 is entirely contained on one quad module measuring 10.44 inches wide by 8.88 inches deep, and plugs into and requires one slot in the 11/23+ based backplane.

Computer I/O

Register Addresses (PROM selectable):

* Control/Status Register 1 (RKCS1) 777 440
* Word Count Register (RKWC) 777 442
* Bus Address Register (RKBA) 777 444
* Disk Address Register (RKDA) 777 446
* Control/Status Register 2 (RKCS2) 777 450
* Drive Status Register (RKDS) 777 452
* Error Register (RKER) 777 454
* Attention Summary/Offset Register (RKAS/OF) 777 456
* Desired Cylinder Register (RKDC) 777 460
* Extended Memory Address Register (RKXMA) 777 462
* Data Buffer Register (RKDB) 777 464
* Maintenance Register 1 (RKMR1) 777 466
* ECC Position Register (RKECPS) 777 470
* ECC Pattern Register (RKECPT) 777 472
* Maintenance Register 2 (RKMR2) 777 474
* Maintenance Register 3 (RKMR3) 777 476
* Enable Real Time Clock Control (RKERTC) 777 546

Data Transfer

* Method: DMA
* Maximum block size transferred in a single operation is 64K words.

Bus Load

* 1 std unit load

Address Ranges

* Disk drive: up to 220.32 megabytes
* Computer memory: up to 2 megawords

Interrupt Vector Addresses

* PROM selectable, factory set at 210 (or 254) priority level BR5

Disk Drive I/O

CONNECTOR - one 60-pin type "A" flat ribbon cable mounted on outer edge of controller module. Two 26-pin type "B" ribbon cables (1 for each drive interfaced with).

SIGNAL - SMD A/B flat cable compatible

POWER - +5 volts at 3.5 amps, +12 volts at 300 milliamps from computer power supply.

ENVIRONMENT - operating temperature 40 degrees F. to 140 degrees F., humidity 10 to 95% non-condensing.

SHIPPING WEIGHT - 5 pounds, includes documentation and cables.

INSTALLATION

Installation instructions for the disk drive are contained in the disk drive manual. Before installing any components of the disk system, read the manual. Figure 5-2 illustrates the configuration of the controller. Tables 5-4 and 5-5 describe switch and jumper settings.

FIGURE 5-2 - CONTROLLER CONFIGURATION

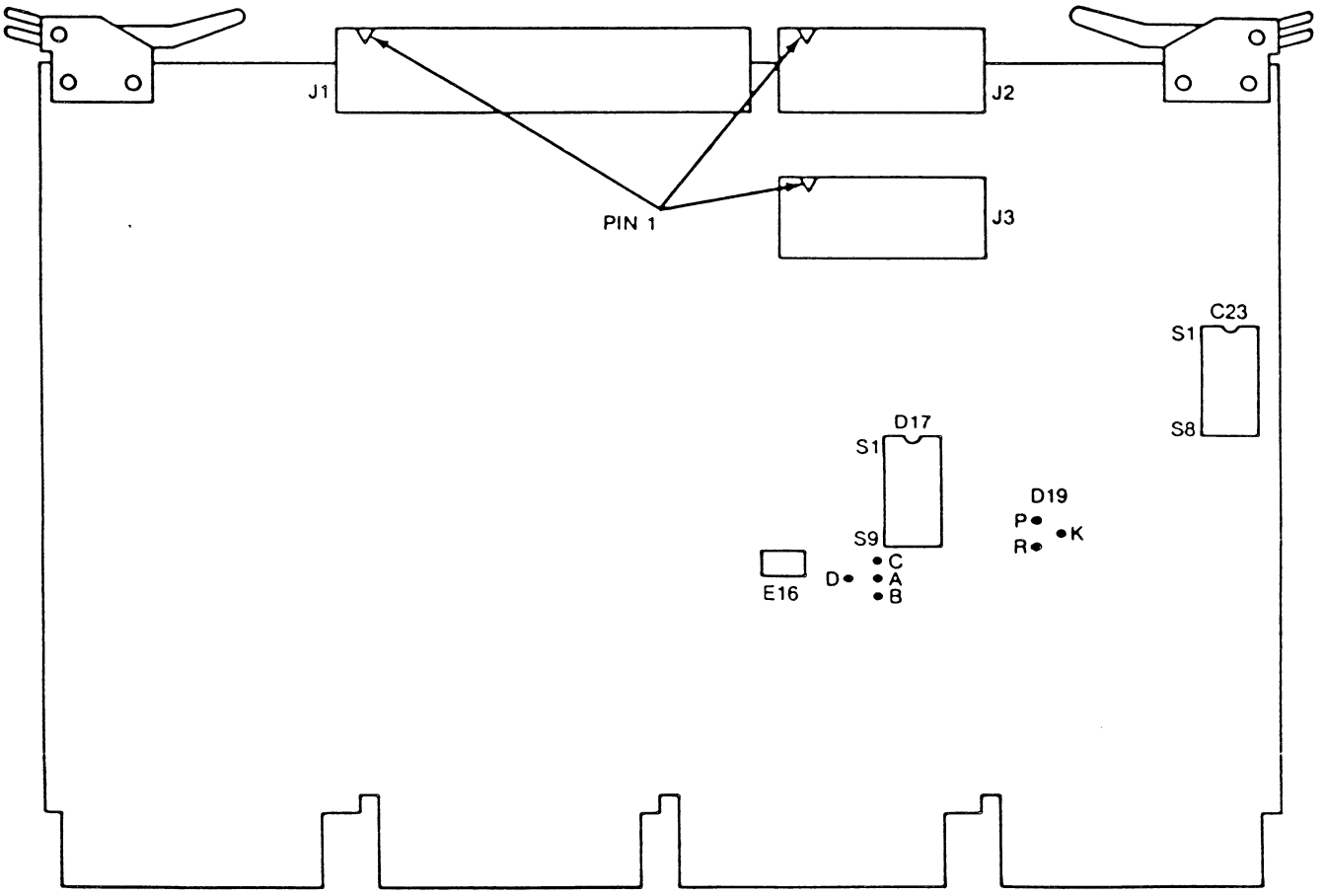
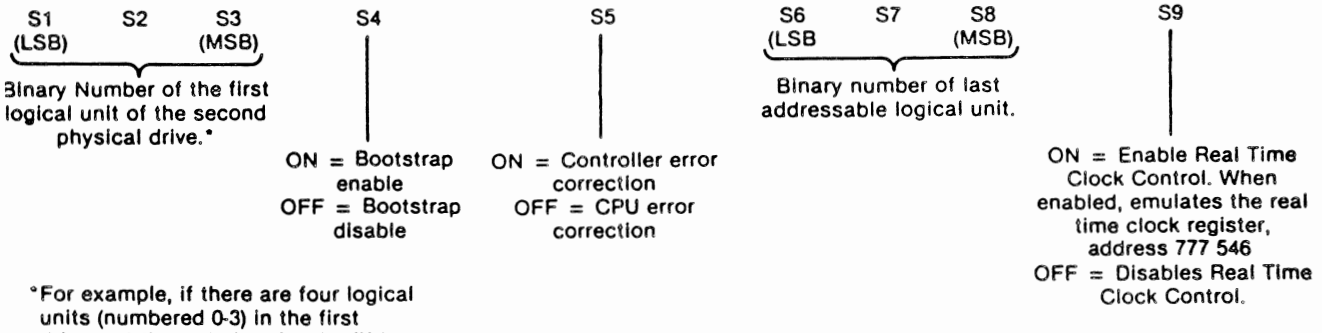


TABLE 5-4 - CONFIGURATION SWITCHES

LOCATION D17 SWITCHES



*For example, if there are four logical units (numbered 0-3) in the first drive, set the switches for the fifth logical unit (number 4) as follows:

(LSB) S1	S2	(MSB) S3
0	0	1

Note

If S1, S2, and S3 are off (000), the controller will default to all logical units on the first physical drive (drive 0). Because of the characteristics of some operating systems, the switches should be set for two drives even if only one drive is present.

LOCATION C23 SWITCHES

Switch	Position	Logical Unit and Emulation
S1	ON	LU0 = RK07
	OFF	LU0 = RK06
S2	ON	LU1 = RK07
	OFF	LU1 = RK06
S3	ON	LU2 = RK07
	OFF	LU2 = RK06
S4	ON	LU3 = RK07
	OFF	LU3 = RK06
S5	ON	LU4 = RK07
	OFF	LU4 = RK06
S6	ON	LU5 = RK07
	OFF	LU5 = RK06
S7	ON	LU6 = RK07
	OFF	LU6 = RK06
S8	ON	LU7 = RK07
	OFF	LU7 = RK06

TABLE 5-5 - JUMPER INSTALLATION

BOOTSTRAP
ADDRESS JUMPERS E16

	.C	*A to B (standard)	773 000
D.	.A		
	.B	A to C (alternate)	775 000

DEVICE
ADDRESS JUMPERS D19

R to K (standard)	777 440
Interrupt Vector = 210	
R to P (alternate)	776 700
Interrupt Vector = 254	

* On the 11/23+ computer, bootstrap address 775 000 must be used.

Installation

To install the controller module, proceed as follows:

CAUTION: Remove DC power from mounting assembly before inserting or removing the controller module. Damage to the backplane assembly may occur if the controller module is plugged in backwards.

1. Select the backplane location into which the controller is to be inserted. Be sure that the disk controller is the lowest priority DMA device in the computer except if the DMA refresh/bootstrap ROM option module is installed in the system. The lowest priority device is the farthest from the processor module. Note that the controller contains a bootstrap ROM.

   Figure 5-3 shows typical backplane configurations. Note that the processor module is always installed in the first location of the backplane or in the first location in the first backplane of multiple backplane systems.

   It is important that all option slots between the processor and the disk controller be filled to ensure that the daisy-chained interrupt (BIAK) and DMA (BDMG) signal be complete to the controller slots. If there must be empty slots between the controller and any option board, the following backplane jumpers must be

installed:

FROM	TO	SIGNAL
CO x NS	CO x M2	BIAK1/LO
CO x S2	CO x R2	BDMG1/LO
(last full option slot)	(controller slot)	

2. Insert the controller into the selected backplane position. Be sure the controller is installed with the components facing row one, the processor.

   The controller module is equipped with handles on the side opposite the slot connectors. Gently position the module slot connectors in to the backplane, then press until the module connectors are firmly seated into the backplane. Both handles must be pressed simultaneously. When removing the module, apply equal pulling pressure to both handles.

3. Feed the module connector end of the disk I/O cables into the controller module connectors. Make sure that pin 1 is matched with the triangle on the connector as shown in Figure 5-4. Install the cable connectors into the module connectors. Verify that the connectors are firmly seated.

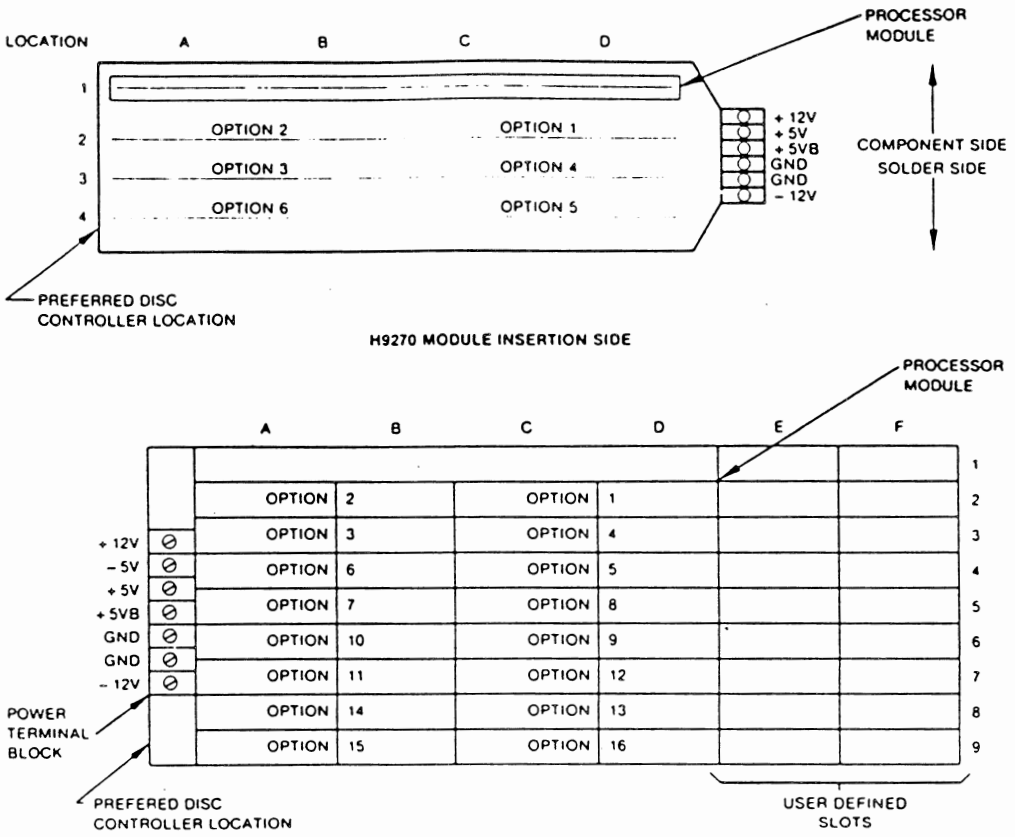
4. Connect the disk-end of the I/O cables to the disk I/O connectors. Be sure that the bus terminator is installed at the last disk in the system.

5. Refer to the disk manual for operating instructions and apply power to the disk and computer.

6. Observe that the green diagnostic LED on the controller board is lit.

7. The system is now ready to operate.

FIGURE 5-3 - TYPICAL BACKPLANE CONFIGURATION



Grounding

To prevent grounding problems, a standard ground braid should be installed from the computer DC ground point to the disk drive DC ground point and also between disk drives at the DC ground points.

OPERATION

Introduction

This section contains procedures for operating the computer system with the controller and a disk drive or drives. An understanding of DEC operating procedures is assumed. The material here is provided for "first time users" of disk subsystems and describes procedures for bootstrapping, formatting, and diagnostic testing.

Precautions and Pre-operational Checks

The following precautions should be observed while operating the system. Failure to observe these precautions could damage the controller, the disk cartridge, the computer, or could erase a portion or all of the stored hardware.

1. If the controller bootstrap is to be used, set controller switch S4 on, and disable other bootstraps that reside at that address.

2. See Figure 5-2 for proper positions of the switches and jumpers. See Tables 5-4 and 5-5 for switch and jumper settings.

3. Do not remove or replace the controller board with power applied to the computer.

Before operation the following checks should be made:

1. Verify that the controller board is firmly seated in backplane connector.

2. Verify that the cables between the controller and the disk drive are installed.

3. Be sure the disk drive cartridge is installed (if it is to be used).

4. Apply power to the computer and the console device.

5. Verify that the green diagnostic light on the controller board lights.

6. Be sure power is applied to disk drive and READY light is on.

Bootstrap Procedure

THESE PAGES OMITTED INTENTIONALLY

PROGRAMMING

Programming Definitions

FUNCTION - The expected activity of the disk system (write, seek, read, etc.)

COMMAND - To initiate a function (halt, clear, go, etc.)

INSTRUCTION - One or more orders executed in a prescribed sequence that causes a function to be performed.

ADDRESS - The binary code placed in the BDAL015 lines by the bus master to select a register in a slave device. NOTE: for memory other than computer internal memory, i.e., peripheral device registers, the upper 4K (28-32K) address space is used.

REGISTER - An associated group of memory elements that react to a single address and store information (status, control, data) for use by other assemblies of the total computer system. Classically, registers have been made up of groups of flip-flops. More and more often, registers are the contents of addressed locations in solid-state or core memory.

Disk Controller Functions

The disk controller performs 14 functions. A function is initiated by a GO command after the processor has issued a series of instructions that store function-control information into controller registers. To accept a command and perform a function, the controller must be properly addressed and the disk drive(s) must be powered up, be at operational speed, and be ready.

The functions performed by the controller are established by bits 01, 02, 03, and 04 of the control status register (RKCS1). The function and bit codings are given in Table 4-1. Descriptions of the functions are given in the following paragraphs.

Note that the controller automatically performs certain functions during each commmand. For example, the controller always performs the following steps:

1. Decodes instruction
2. Selects drive
3. Acknowledges pack (tests for RK06/RK07 drive type)
4. Executes one of the following remaining nine functions

TABLE 5-6 - FUNCTION CODES

BIT 4321	COMMAND
0000	Select Drive
0001	Pack Acknowledge
0010	Drive Clear (Reset Attention Status)
0011	Unload (No Op)
0100	Start Spindle (No Op)
0101	Recalibrate (Restore Drive and Reset Fault)
0110	Offset
0111	Seek
1000	Read Data
1001	Write Data
1010	Read Headers (1 Track of Headers)
1011	Write Headers (Format Track)
1100	Write Check

Select Drive

Performed automatically as part of all functions related to drive selection (connects drive).

Pack Acknowledge

Performed automatically to verify emulation (RK06/RK07) as part of all functions related to drive selection. Controls bit 08 in RKDS.

Drive Clear

Resets attention status in RKAS/0F.

Recalibrate

Relocates the heads to cylinder zero and clears the cylinder address register. Also resets all fault conditions. Sets attention bit in RKAS/OF.

Offset

Sets drive attention bit in RKAS/OF.

Seek

Performed automatically as part of all functions related to drive selection. Sets attention bit in RKAS/OF. During Overlapped Seeks, loads cylinder address into RKMR3 (Maintenance Register 3).

Read Data

Causes the following sequence to be executed: A Seek to the cylinder in RKDC is performed. Headers are read and compared with the desired disk address until the correct sector is found. Transfer of data through the data buffer to memory is initiated. When the sector data transfer is complete, the ECC logic is checked to ensure that the data read from the disk was error-free. If a data error occurred, the ECC correction logic is initiated to determine whether the error is correctable; when finished, the command is terminated to allow software or hardware (as selected) to apply the correction information. Assuming no data errors, the word count in RKWC is checked; if non-zero, the data transfer operation is repeated into the next sector. The word count is checked at the end of each sector until it reaches zero, at which time the command is terminated by setting the Ready bit.

Write Data

Causes the following sequence to be executed: A Seek to the cylinder in RKDC is performed. Transfer of data from memory to the data buffer is begun, and headers are read and compared with the desired disk address until the correct sector is found. Preamble, Data (256 words), and ECC bits (56) are written on the disk. If the word count in RKWC goes to zero during the sector, the rest of the sector is zero-filled. After the sector transfer, the word count is RKWC, is checked, and if non-zero, the data transfer operation is continued into the next sector. The word count in RKWC is checked at the end of each sector and, when it equals zero, the command is terminated by setting the Ready Bit.

Read Headers

A Seek to the cylinder in RKDC is performed. This function causes the controller to read all headers starting at the Index mark. Each 5-word header is read in the order in which it appears on the disk. If an ECC error is detected in the header, the HRE bit of RKER is set.

Write Headers

A Seek to the cylinder in RKDC is performed. The controller then waits until Index is detected. When detected, zeros are written until Index is again detected. This "cleans" the track of potential spurious signals. After Index is detected a second time, 5 header words and a 32-bit ECC are written after each sector pulse. When Index is next detected, the command is terminated and the Ready bit is set.

NOTE: All five words and the ECC code are prepared by the format routine (software) and treated as data by the controller. Only one complete track can be formatted at a time.

Write Check

Causes the following sequence to be executed: A Seek to the cylinder in RKDC is performed. The selected drive provides data as in a Read command, and data is obtained from memory as in a Write command. The data are compared on a word-for-word basis until the word count reaches zero or until a failure to compare occurs. If the data fails to compare, the command is terminated immediately.

Mapping and Map Override

In a typical FHL disk subsystem, the method by which the disk drive finds the proper location to read data from or write data to is as follows:

1. The application software program running under the operating system sends a record number to the disk device driver software.

2. The device driver converts this record number into head, sector, and cylinder numbers.

3. The driver then sends this information to dedicated hardware registers on the disk controller.

4. The controller in turn passes these parameters on to the disk drive over I/O interface cables.

5. The drive interprets these signals and activates electronics and electromechanics enabling it to seek to the exact physical location where information will be recorded or retrieved.

In an FHL subsystem which includes the CQ-06 controller, the above procedure is the same up to step 4. But instead of passing on the head, sector and cylinder information to the drive, the controller first takes that information sent by the device driver software and reconverts it to the original record number. Then by invoking a special algorithm, the controller develops a new head, sector and cy- linder number. This is called "mapping" and it is a necessary procedure whenever the disk drive that is attached to the CPU does not contain the same specifications as the drive supplied by the CPU manufacturer.

Map Override is nothing more than a special operating mode of the disk controller which allows it to transfer the disk address to the drive as described in steps 1-5, bypassing the mapping procedure. Typically, this feature is only used in an environment in which the user requires the entire disk drive to be formatted as one large logical unit. In other words, one logical unit would equal one physical unit.

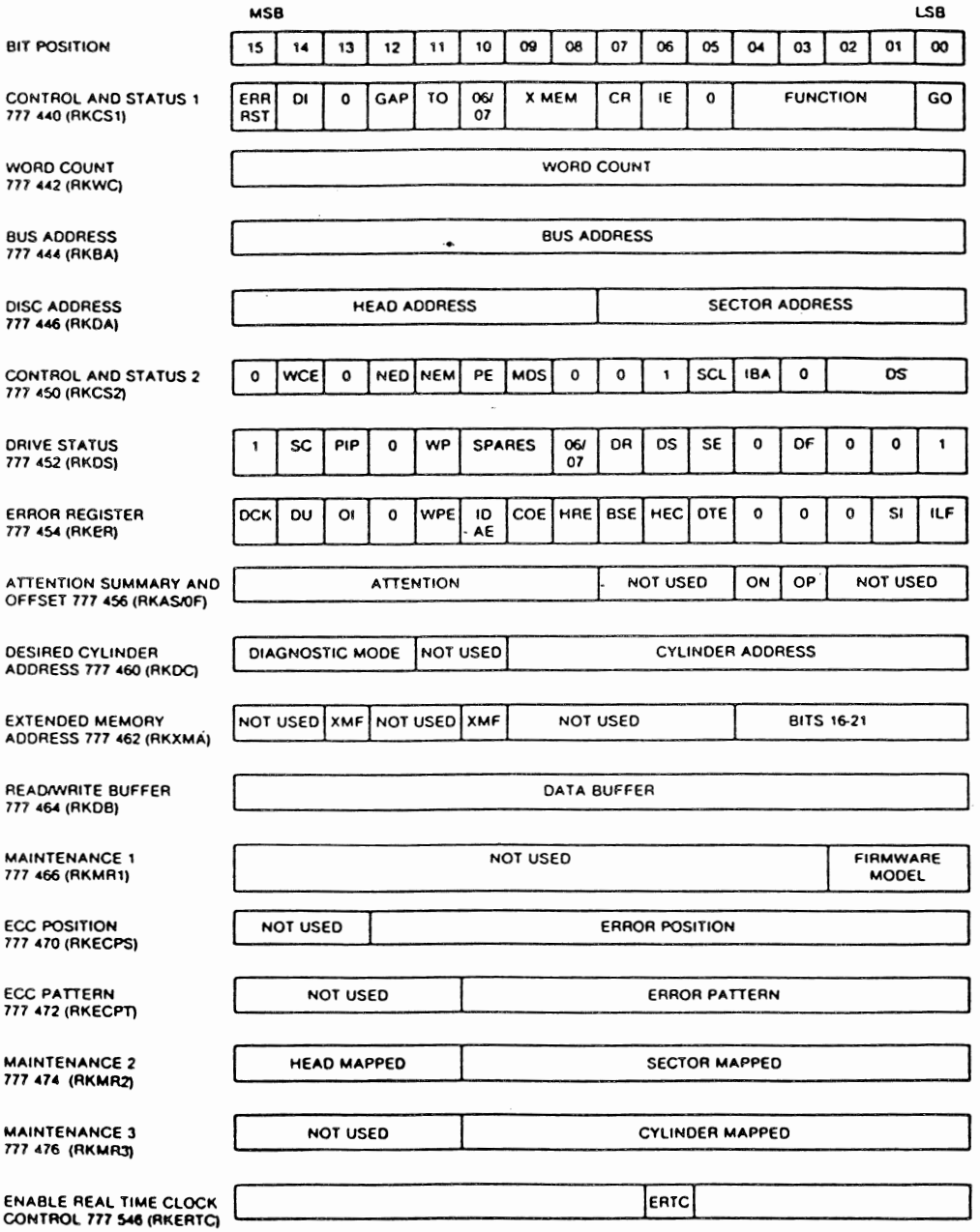
Enable Real Time Clock Control

The real time clock line is from the 60-cycle power supply in the LSI. The Operating System uses the clock for time and date. The line on the Q-Bus, BEVNT, can be disabled by a switch on the controller, which when ON enables real time clock control, or when OFF disables control. The register, address 777 546, is shown at the end of this section.

REGISTERS

A summary of the registers is shown in Figure 5-5, followed by a description of each register.

FIGURE 5-5 - CONTROLLER REGISTER CONFIGURATION



CONTROL & STATUS REGISTER 1 777 44Ø (RKCS1)

BIT(S) DEFINITION

00 GO - When set, this bit causes programmed commands (function codes) to be executed. When set, only two other bits can be set (except in the diagnostic mode); they are: Bit 15, CCLR, in RKCS1, and Bit 05, SCLR, in RKCS2.

01-04 FUNCTION CODE--

BIT 4321	0(GO)	OCTAL	COMMAND
0000	1	01	Select Drive
0001	1	03	Pack Acknowledge
0010	1	05	Drive Clear (Reset Drive Fault)
0011	1	07	Unload (No Operation)
0100	1	11	Start Spindle
0101	1	13	Recalibrate (Restore Drive Reset Fault)
0110	1	15	Offset
0111	1	17	Seek (No Operation)
1000	1	21	Read Data
1001	1	23	Write Data
1010	1	25	Read Headers (1 Track of Headers)
1011	1	27	Write Headers (Format Track)
1100	1	31	Write Check

05 SPARE - ALWAYS 0

06 INTERRUPT ENABLE - When this bit is set, the controller is allowed to interrupt the processor under any of the following conditions:

* When the Controller Ready bit (bit 07 in RKCS1) is set upon completion of a command.
* When any drive sets an associated Attention flag (ATN7-ATN0) in RKAS/0F, and the Controller Ready bit is set.
* When the controller or any drive indicates the presence of an error by setting the ERR/RST bit in RKCS1.

In addition, via program control, an interrupt can be forced by the simultaneous setting of the IE and RDY bits in RKCS1. The IE bit can be reset via program control as well as by conventional initialization (INIT, CCLR, SCLR).

07 CONTROLLER READY - This is a read-only bit. It is set via conventional initialization (INIT, CCLR, SCLR) upon completion of a controller command, or when an error condition is de-

tected. The RDY bit is reset when the GO bit (bit 00 in RKCS1) is set.

08-09 EXTENDED BUS ADDRESS - These bits constitute an extension of the 16-bit Bus Address register (RKBA), which contains the memory address for the current data transfer.

10 RK06/RK07 SELECT - When set, this bit selects RK07. When reset, RK06 is selected.

11 OPERATION TIME OUT - When set, this read-only bit indicates that the GO bit has been set for a specified time period and the current command has not been executed within that time period.

12 GAP CONTROL - In the Write Header command (or write format) bit 12 will direct the controller to generate a long gap (24 bytes) or a short gap (16 bytes) between sector and header. NOTE: When bit 12 is set, the Word Count Register should be set for 520 bytes.

Bit 12 1 = Short Gap

2 = Long Gap

In the Write Data or Read Data command, bit 12 will direct the controller to Write or Read a sector data field (512 bytes) with or without ECC (7 bytes) to or from memory.

Bit 12 1 = 512 Bytes + 7 Bytes
(DATA) (ECC)

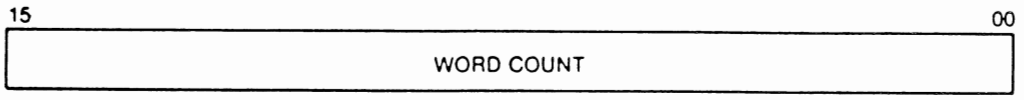
0 = 512 Bytes

13 SPARE - ALWAYS 0

14 DRIVE INTERRUPT ENABLE (SEEK OR RESTORE) - This bit is set during a Seek or Restore operation or when any attention bit is set in the RKAS/0F register. The bit is reset by Bus Initialize (INIT), Subsystem Clear (SCLR) or by Drive Clear commands asserting attention.

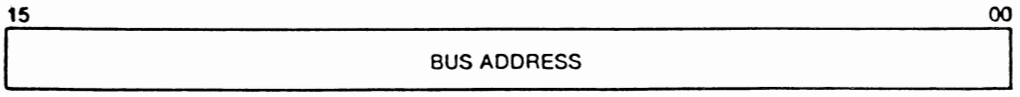
15 COMBINED ERROR/RESET - When reading bit 15 via programmed control, a zero indicates an operation complete with good status; a one indicates an operation complete with an error.

WORD COUNT REGISTER 777 442 (RKWC)



This is a Read/Write register. The bits of this register contain the 2's complement of the total number of words to be transferred during a Read, Write, or Write Check operation. The register is incremented by one after each transfer. When the register overflows (all WC bits go to zero), the transfer is complete and controller action is terminated at end of the present disk sector. Only the number of words specified in the RKWC are transferred. It is cleared by INIT or RESET functions.

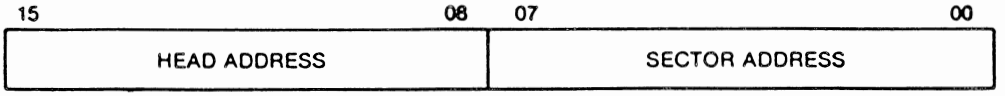
BUS ADDRESS REGISTER 777 444 (RKBA)



The Bus Address Register is initially loaded with the low-order sixteen bits of the bus address that reflects the main memory start location for a data transfer. With the low-order bit (bit 00) always forced to zero, the Bus Address Register bits are combined with bits 09 and 08 of the RKSC1 register (BA17, BA16) to form a complete even-numbered, 18-bit memory address. Following

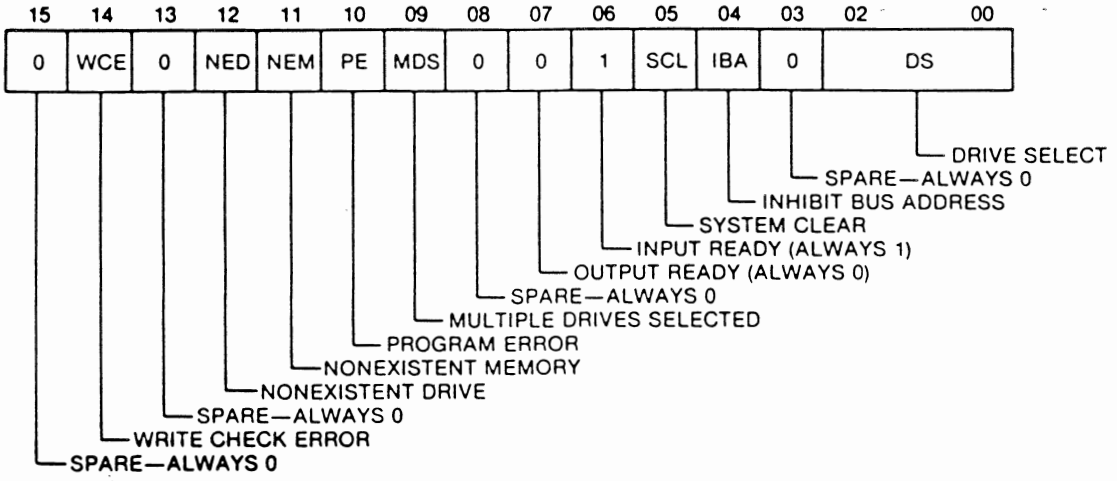
each data transfer bus cycle, the Bus Address Register is incremented to select the next even-numbered location.

DISK ADDRESS (TRACK AND SECTOR) REGISTER 777 446 (RKDA)



BIT(S)	DEFINITION
00-04 (00-07)	SECTOR ADDRESS - In the emulation mode, bits 00-04 select up to 20 sectors of 16-bit words. In the map override mode, bits 15, 14, 13, 12 in the Desired Cylinder Register 777 460, are set to 1, 0, 0, 0, respectively. The Sector Address then uses bits 00-07.
08-10 (08-15)	HEAD (TRACK) ADDRESS - In the emulator mode, bits 08-10 select heads 0, 1, 2. In the map override mode, bits 15, 14, 13, 12 and in the Desired Cylinder Address Register 777 460, are set to 1, 0, 0 and 0, respectively. The Head (TRACK) Address then uses bits 08-15.

CONTROL AND STATUS REGISTER 2 777 450 (RKCS2)



BIT(S)	DEFINITION
00-02	DRIVE SELECT - These bits specify the drive to be selected.
03	SPARE - ALWAYS 0
04	INHIBIT BUS ADDRESS INCREMENT - When this bit is set, the Bus Address register is prevented from incrementing during data transfers.
05	SYSTEM CLEAR - When this bit is set, the controller and drive are reset.
06	INPUT READY - ALWAYS 1
07	OUTPUT READY - ALWAYS 0
08	SPARE - ALWAYS 0
09*	MULTIPLE DRIVES SELECTED - This bit is set when more than one drive has been selected at the same time. This bit can only be cleared by INIT or SCLR.
10*	PROGRAM ERROR - This read-only error bit is set if any controller register is written (CCLR and SCLR excluded) while the GO bit in RKCS1 is set.
11*	NONEXISTENT MEMORY - This read-only error bit is set when the controller attempts to execute a bus cycle and SSYN is not returned within the specified time period.
12*	NONEXISTENT DRIVE - When set, this read-only error bit indi-

cates that Select Acknowledge (SACK) has not been asserted by the selected drive in response to a Select Enable sent to the drive.

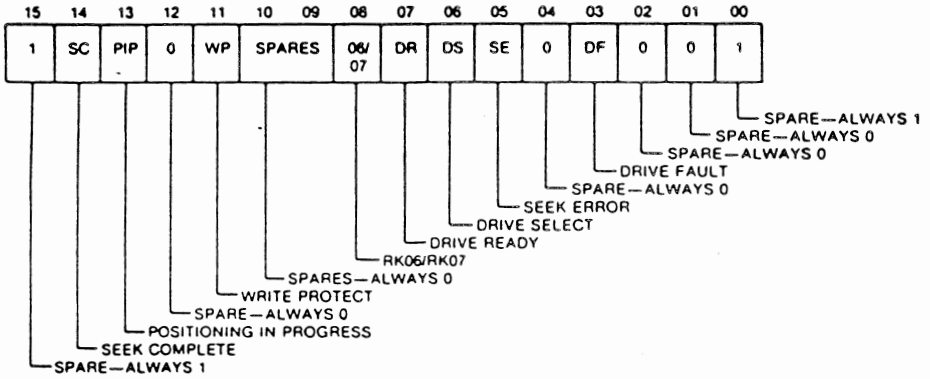
13* SPARE - ALWAYS 0

14* WRITE CHECK ERROR - When set, this read-only bit indicates that a data word read from the disk (during a Write Check command) did not compare with the data word in main memory. If a Write Check error is detected and the IBA bit (bit 04 of RKCS2) is cleared, Bus Address register will contain the memory address of the mis-matched word plus two or plus four.

15 SPARE - ALWAYS 0

*Causes bit 15 in RKCS1 to set.

DRIVE STATUS REGISTER 777 452 (RKDS) READ ONLY REGISTER



BIT(S) DESCRIPTION

00 SPARE - ALWAYS 1

01 SPARE - ALWAYS 0

02 SPARE - ALWAYS 0

03 DRIVE FAULT - When set, indicates an error condition is detected within the drive and is prohibiting all operations. This bit is reset manually by clearing the fault condition within the drive.

04 SPARE - ALWAYS 0

05 SEEK ERROR - When set, indicates a seek was not completed within a specified time period after it was initiated.

06 DRIVE SELECTED - When set, the drive is selected and on-line.

07 DRIVE READY - Drive Ready is a read-only bit which when set indicates the selected drive is up to speed, the heads are on cylinder and the drive is ready to accept commands. It is reset when these conditions are not met or when drive is seeking.

08 RK06/RK07 - When set indicates RK07; when reset indicates RK06.

09-10 SPARES - ALWAYS 0

11 WRITE PROTECT - When set, the selected disk is write protected.

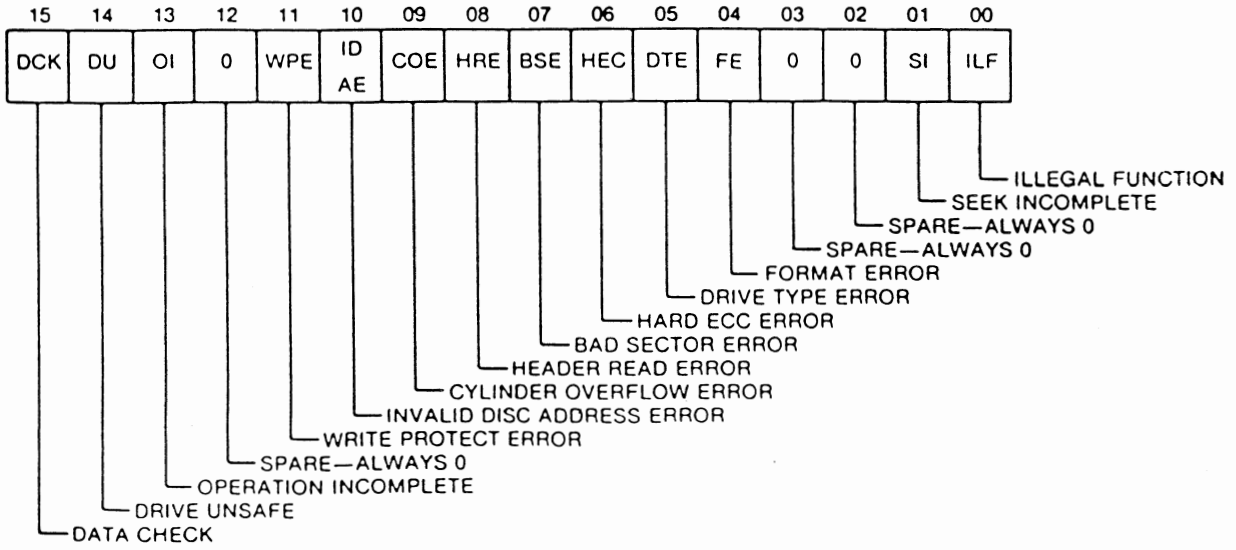
12 SPARE - ALWAYS 0

13 POSITIONING IN PROGRESS - When set, the selected disk is write protected.

14 SEEK INCOMPLETE - This read-only bit sets when the drive is ON CYLINDER. SEEK or RESTORE is completed.

15 ALWAYS 1

ERROR REGISTER 777 454 (RKER)



BIT(S)	DEFINITION
00	ILLEGAL FUNCTION - When set, this read-only bit indicates that an illegal command has been loaded into the RKCS1 register.
01	SEEK INCOMPLETE - When set, this read-only bit indicates that a seek operation has not been completed by the selected drive.
02	SPARE - ALWAYS 0
03	SPARE - ALWAYS 0
04	FORMAT ERROR - When set in conjunction with bit 09, indicates that the sector pulses are too close together. Diagnostic message is "SECTOR SIZE TOO SMALL."
05	DRIVE TYPE ERROR - This read-only bit is set when the drive type status does not compare with Control Drive Type bit (RKCS1, bit 10), i.e., RK06 instead of RK07 or vice-versa.
06	HARD ECC ERROR - When set, this read-only bit indicates that a data error detected by the ECC logic cannot be corrected using ECC.
07	BAD SECTOR ERROR - When set, this read-only bit indicates that a data transfer was attempted to or from a sector and the sector is bad.
08	HEADER READ ERROR - When set, this read-only bit indicates that an uncorrectable ECC error was detected on a sector header during a data transfer. If bit 13 is also set, the error indication is "HEADER NOT FOUND."
09	CYLINDER OVERFLOW ERROR - When set, the word count is not equal to zero and the operation is programmed to continue beyond the last logical sector on the disk. This will occur on a Read or Write data operation.
10	INVALID DISK ADDRESS ERROR - When set, this bit indicates that an invalid cylinder address or an invalid head address has been detected during a Seek command or Write/Read data command.
11	WRITE PROTECT ERROR - When set, this read-only bit indicates that the drive received assertion of Write Gate while in the write protect mode.
12	SPARE - ALWAYS 0

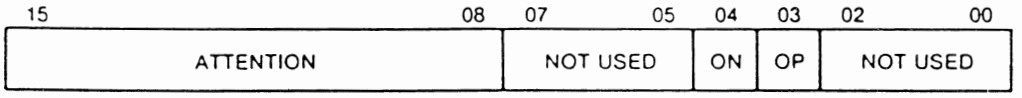
13 OPERATION INCOMPLETE - When set, this read-only bit indicates that during a data transfer, the desired header could not be found. This error can result from any one of the following:

* Head Mis-position
* Incorrect Head Selection
* Read Channel Failure
* Improper Pack Formatting

14 DRIVE UNSAFE - When set, this read-only bit indicates that a Read/Write Unsafe condition has been detected.

15 DATA CHECK - When set, this read-only bit indicates that a data error was detected when the current sector was read.

ATTENTION SUMMARY AND OFFSET REGISTER 777 456 (RKAS/OF)

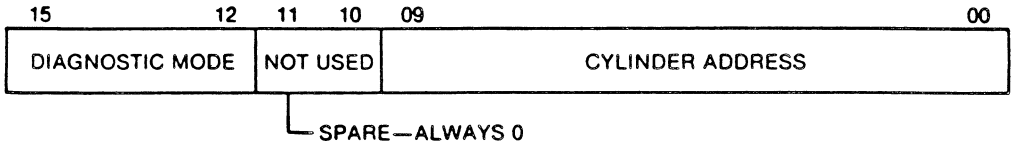


BIT(S)	DEFINITION
00-02	SPARE - ALWAYS 0
03	OFFSET POSITIVE - Offsets the head in the positive direction from the centerline of the track (positive is from the lower cylinder number toward the higher cylinder number).
04	OFFSET NEGATIVE - Offsets the head in the negative direction from the centerline of the track (negative is from the higher cylinder number toward the lower cylinder number).

05-07 SPARE - ALWAYS 0

08-15 ATTENTION - The eight Attention bits, one for each drive, correspond to the logical unit number of each drive. Each bit indicates the state of the Drive Status Change flip-flop in the corresponding drive. All of the ATN bits are continuously scanned and updated (polled).

DESIRED CYLINDER ADDRESS REGISTER 777 460 (RKDC)



BIT(S) DEFINITION

00-09 CYLINDER ADDRESS - The cylinder address in RKDC is the emulated address. The actual mapped address is contained in RKMR2. The cylinder number is written in octal in the register.

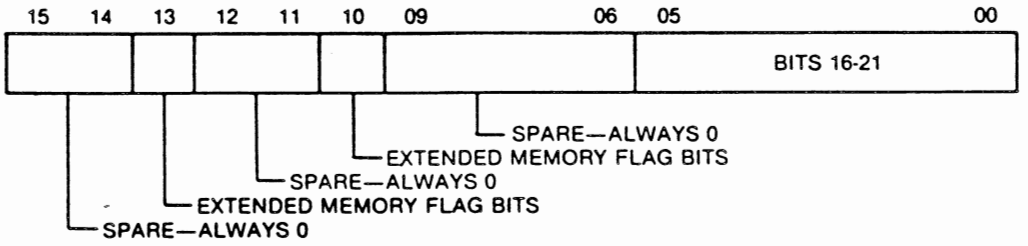
10-11 SPARE - ALWAYS 0

12-15 DIAGNOSTIC MODE - These bits are as follows:

15	14	13	12	
0	0	0	0	RK06/RK07 Emulation Mode
1	0	0	0	MAP OVERRIDE MODE - These bits can be set by the programmer to override the mapping algorithm. When set, the head, cylinder, and sector addresses supplied to the controller specify absolute address to the disk. Could be typically used to permit the device handler to be modified to take advantage of the head per track options available in some disk drives.

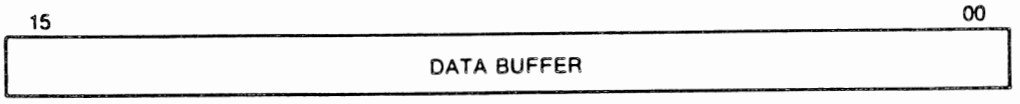
1	1	0	0	DMA BUFFER TEST MODE - Allows Reading/Writing of the controller data buffer using the computer DMA interface. The controller word count and memory address registers are used to set up the DMA transfer with a maximum transfer of 1024 bytes starting with location 0 of the data buffer. The write command, 23 , will write from the buffer. The read command, 21 , will read from the data buffer.
1	1	1	0	ECC TEST MODE
1	1	0	1	I/O BUS INTERFACE TEST MODE
1	1	1	1	I/O W/R INTERFACE TEST MODE

EXTENDED MEMORY ADDRESS REGISTER (22-bit) 777 462 (RKXMA)



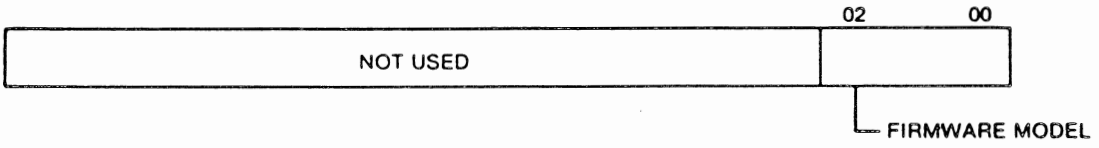
BIT(S)	DEFINITION
00-05	BITS 16-21 - These bits, when set, define bits 16-21 of the 22-bit extended memory.
06-09	SPARE - ALWAYS 0
10,13	EXTENDED MEMORY - When bits 10 and 13 are set, the 22-bit address is used.
11-12, 14-15	SPARE - ALWAYS 0

READ/WRITE BUFFER REGISTER 777 464 (RKDB)



BIT(S)	DEFINITION
00-15	The Data Buffer Register is a Read/Write register. Writing into the register loads data into the controller data buffer, one word at a time. Reading the register reads data from the controller data buffer. The commands INIT, CLL, and SRC clears the Data Buffer address allowing writing or reading of the Data Buffer starting at location 0. Reading from or writing into the buffer will increment the address register.

MAINTENANCE REGISTER 1 776 466

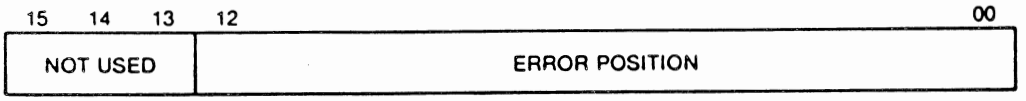


BIT(S)	DEFINITION
00-02	FIRMWARE MODEL - These three bits define the model number of

the firmware used in the controller.

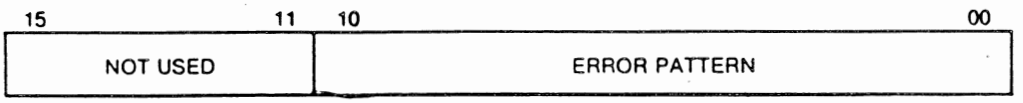
03-15 SPARE - ALWAYS 0

ECC POSITION REGISTER 777 470 (RKECPS)



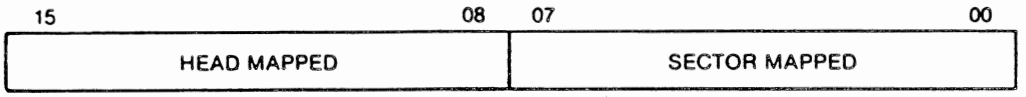
BIT(S)	DEFINITION
00-12	ERROR POSITION - These read-only bits define the start location of an error burst (containing from one to eleven error bits) within a 256-word data field, sequence. The position is valid if the error is ECC correctable.
13-15	SPARE - ALWAYS 0

ECC PATTERN REGISTER 777 472 (RKECPT)



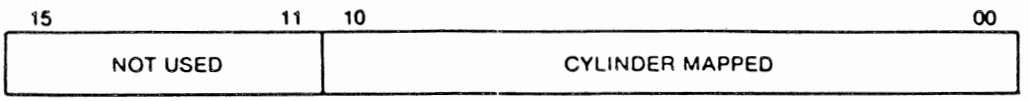
BIT(S)	DEFINITION
00-10	ERROR PATTERN - These are read-only bits that provide an 11-bit correction pattern for an error burst that does not exceed 11 error bits in length and is therefore ECC correctable.
11-15	SPARE - ALWAYS 0

MAINTENANCE REGISTER 2 777 474 (RKMR2)



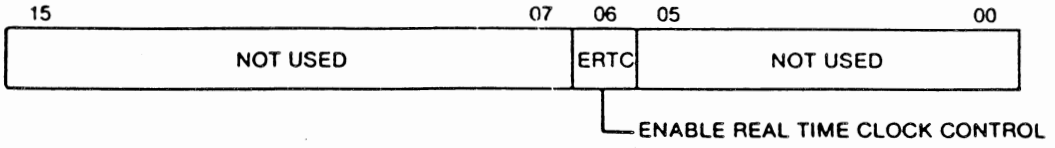
BIT(S)	DEFINITION
00-07	SECTOR MAPPED - These bits define the actual mapped sector address in the disk as opposed to the emulated address.
08-15	HEAD MAPPED - These bits define the actual mapped head address on the disk as opposed to the emulated address.

MAINTENANCE REGISTER 3 777 476



BIT(S)	DEFINITION
00-10	CYLINDER MAPPED - These bits define the actual mapped cylinder address on the disk as opposed to the emulated address.
11-15	SPARE - ALWAYS 0

ENABLE REAL TIME CLOCK CONTROL REGISTER 777 546



The Enable Real Time Clock Control register performs a separate function from the other registers. During a read operation, bit 06 is always reset. During a write operation bit 06 is set, giving the real time clock control. Switch S9 must be ON to enable this function.

TROUBLESHOOTING AND THEORY

This section describes troubleshooting procedures at three levels of complexity: basic system, controller symptoms and detailed analysis. Basic system troubleshooting procedures are visual checks not requiring test equipment and may be performed by the operator. Controller symptom procedures may require a scope, meter, extender board or diagnostics, and should be performed by a technician. Detailed analysis is troubleshooting at the IC level, and is presented for engineers or system analysts for controller evaluation. The latter method may require the use of test equipment and the material presented here: board layout, term listing, theory of operation and logic diagrams.

CAUTION: Make sure the power is off when connecting or disconnecting board or plugs.

Basic System Troubleshooting

The following should be checked before power is applied:

1. Verify that all signal and power cables are properly connected. Ribbon cable connectors are not keyed. The arrows on the connectors should be properly aligned.

2. Verify that all switches are properly set.

3. Verify that all modules are properly seated in the computer and properly oriented.

The following should be checked during or after application of power:

1. Verify that the computer and disk drive generate the proper responses when the system is powered up.

2. Verify that the computer panel switches are set correctly.

3. Verify that the console can be operated in the local mode. If not, the console may be defective.

4. With the drive power switch on, verify that the drive READY light is on.

5. Verify that the green diagnostic light on the controller is on.

Controller Symptoms

Controller symptoms, possible causes and checks/corrective action are described in Table 5-8. Voltage checks should be performed before trouble-shooting more complex problems. The +5V source may be checked from any component shown on the logic diagrams.

Physical Layout

The physical layout of the board is shown in Figure 5-6.

TERM TESTING

The input and output terms for each logic diagram are described in Table 5-7.

TABLE 5-7 - TERM LISTING

Term	Origin	Description
LXRF –	11	Load External Register RAM Destination
MRQB +	3	Memory Request Q Bus
OCD + / –	16	Open Cable Detect
ONCYL + / –	17	On Cylinder From Drive
PICK	16	Power Pick
QBUSA	2	Q Bus Access
Q3	10	Q Register Shift Line
RAM3 +	10	Shift Output of ALU RAM
RCLOCKA/B + / –	18	Read Clock From Drives A or B
RDATAA/B + / –	18	Read Data From Drives A or B
RDATA +	18	Read Data
REP	19	Read Error Pattern
RESET	4	Reset Signal to Controller
RMCLK	3	RAM Clock
RSYNC –	13	Read Synchronize
R/WCK –	18	Read/Write Clock
R/WSRE +	3	Read/Write Shift Register Enable
SELA/B	18	Drives A or B Selected
SENDA/B	18	Drives A or B Seek End
SCLK	3	System Clock
SCLOCKA/B	18	Servo Clock From Drives
SDB08 +	2	Slave Data Bus Bit 8
SEEKA/B	18	Seek End From Drives
SEC + / –	17	Sector Pulse From Drive
SERR + / –	17	Seek Error From Drives
SL/IN +	2	Slave Interrupt Acknowledge Request
TAG1/2/3	16	Tag Lines To Drives
TDIN +	3	Transmit Data In
TDOUT +	3	Transmit Data Out
TDMG +	2	Transmit Direct Memory Grant
TDMR +	2	Transmit Direct Memory Request
TIAK +	2	Transmit Interrupt Acknowledge
TIRQ +	3	Transmit Interrupt Request
TRPLY	3	Transmit Reply
TSACK	2	Transmit Select Acknowledge

Term	Origin	Description
TSYNC	3	Transmit Synchronize
TWTBT	3	Transmit Write Byte
UNRDY	17	Drive Unit Ready
USEL0/1/2/3	16	Drive Unit Select Bits 0, 1, 2, 3
USELA/B	18	Drive Unit Select A, B
USTAG	16	Drive Unit Select Tag
VEC –	8	Vector Address Register Select
WDATA +	14	Write Data Bit Stream
WCLOCKA/B + / –	18	Write Clock To Drives A or B
WDATAA/B + / –	18	Write Data To Drives A or B
WPRT	17	Drive Write Protect
WREN –	3	Write Enable
XSD0	11	External Source Decode Slave Address
XSD1	11	External Source Decode Data Input MSB
XSD2	11	External Source Decode Data Input LSB
XSD3	11	External Source Decode CPU Bus Status
XSD4	11	External Source Decode Data Buffer
XSD5	11	External Source Decode Disc Drive Status
XSD6	11	External Source Decode Seek End Status
XSD7	11	External Source Decode Error Status Register
XSD8	11	External Source Decode Bootstrap PROM
XSD9	11	External Source Decode Configuration Switches
XSDA	11	External Source Decode Literal PROM
XSDB	11	External Source Decode RK06 Switches
XSDF	11	External Source Decode RAM
Y00/Y07	10	Y-Bus Bits 0-7
ZERO +	10	Zero Output of 2901
1K0V +	15	1024 Address Counter Overflow

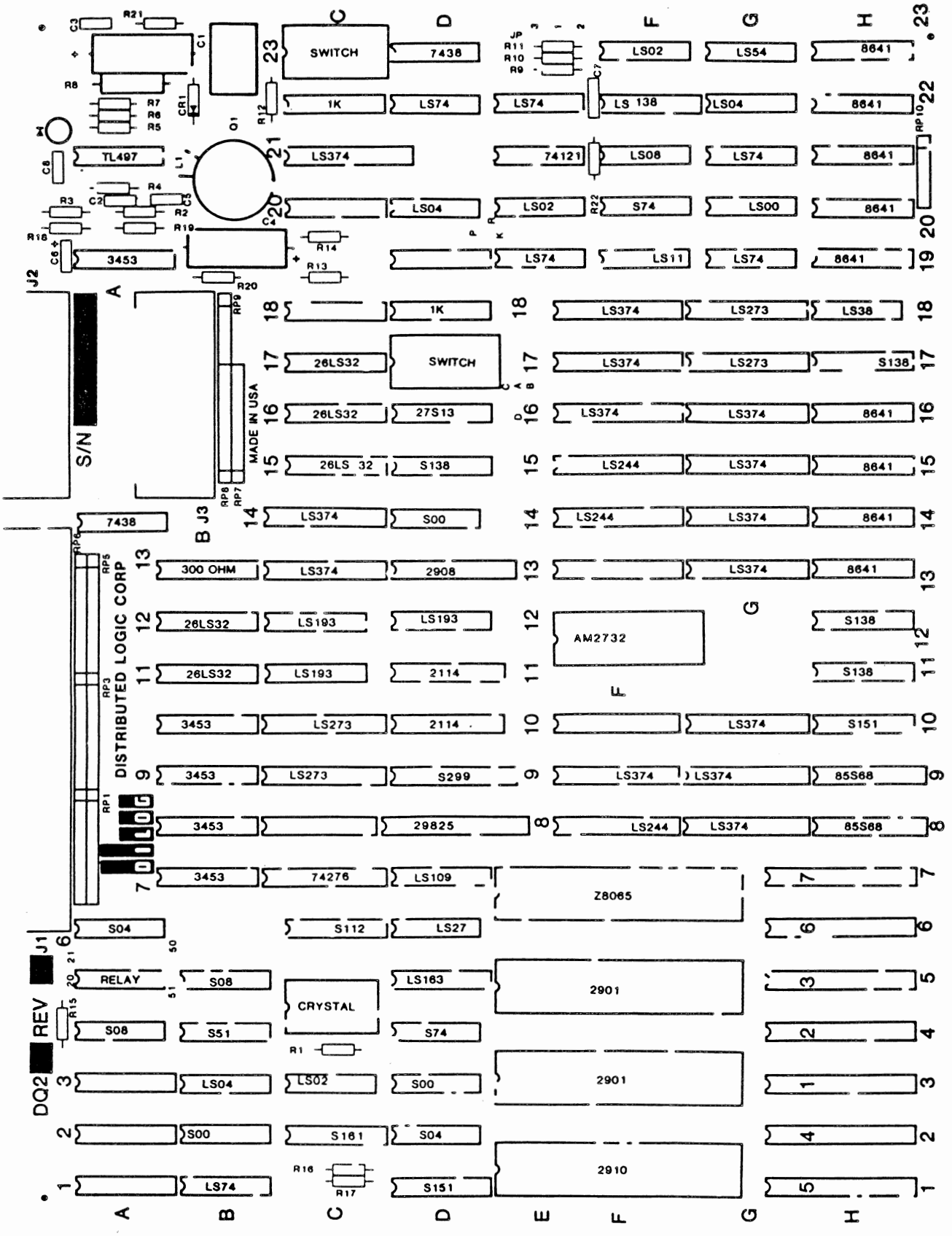
(TABLE 5-7 CONTINUED)

Term	Origin	Description
AMF	17	Address Mark Found From Disc
BA00-BA09 +	15	Buffer Address Counter Bits 00-09
BBS7L	BUS (AP2)	Bus Peripheral Address Select
BBS7 +	4	Peripheral Address Select
BC4 +	13	Bit Count 4 From Bit Counter
BDAL00L	BUS (AW2)	Bus Data/Address Line 00
BDAL01L	BUS (AV2)	Bus Data/Address Line 01
BDAL02L	BUS (BE2)	Bus Data/Address Line 02
BDAL03L	BUS (BF2)	Bus Data/Address Line 03
BDAL04L	BUS (BH2)	Bus Data/Address Line 04
BDAL05L	BUS (BI2)	Bus Data/Address Line 05
BDAL06L	BUS (BK2)	Bus Data/Address Line 06
BDAL07L	BUS (BL2)	Bus Data/Address Line 07
BDAL08L	BUS (BM2)	Bus Data/Address Line 08
BDAL09L	BUS (BN2)	Bus Data/Address Line 09
BDAL10L	BUS (BP2)	Bus Data/Address Line 10
BDAL11L	BUS (BR2)	Bus Data/Address Line 11
BDAL12L	BUS (BS2)	Bus Data/Address Line 12
BDAL13L	BUS (BT2)	Bus Data/Address Line 13
BDAL14L	BUS (BU2)	Bus Data/Address Line 14
BDAL15L	BUS (BY2)	Bus Data/Address Line 15
BDAL16L	BUS (AC1)	Bus Address Extension Line 16
BDAL17L	BUS (AD1)	Bus Address Extension Line 17
BDAL18L	BUS (BC1)	Bus Address Extension Line 18
BDAL19L	BUS (BD1)	Bus Address Extension Line 19
BDAL20L	BUS (BE1)	Bus Address Extension Line 20
BDAL21L	BUS (BF1)	Bus Address Extension Line 21
BDINL	BUS (AH2)	Bus Data In
BDIN +	4	Data In
BDMGIL	BUS (AR2)	Bus DMA Grant In
BDGOL	BUS (AS2)	Bus DMA Grant Out
BDMRL	BUS (AN1)	Bus DMA Request
BDOUTL	BUS (AE2)	Bus Data Out
BDOUT +	4	Data Out
BEVENT	BUS (BR1)	Real Time Clock Control
BFULE +	3	Enable Buffer Full
BFULL –	15	Buffer Full
BIAKIL	BUS (AM2)	Bus Interrupt Acknowledge In
BIAKOL	BUS (AN2)	Bus Interrupt Acknowledge Out
BINITL	BUS (AT2)	Bus Initialize—Clear
BIRQ4L	BUS (AL2)	Bus Interrupt Request Level 4
BIRQ5L	BUS (AA1)	Bus Interrupt Request Level 5
BIRQ6L	BUS (AB1)	Bus Interrupt Request Level 6
BIRQ7L	BUS (BP1)	Bus Interrupt Request Level 7
BIT0-BIT10	16	Control Bits to Disc Drives
BIT7 + , –	13	"Complete Byte" Output of Bit Counter
BPOK-H	BUS (BB1)	Primary Power O.K.
BPOK –	4	Primary Power O.K.
BRPLYL	BUS (AF2)	Q Bus Reply
BRPLY +	4	Q Bus Reply
BSACKL	BUS (BN1)	DMA Select Acknowledge
BSYNCL	BUS (AJ2)	Bus Synchronize I/O
BTSPF +	2	Bootstrap Flag
BWTBTL	BUS (AK2)	Bus Write Byte
BWTBT +	4	Bus Write Byte
BYTCK +	13	Byte Clock
COUT +	10	Carry Out
CP1	12	Control Pulse 1
CP2	12	Control Pulse 2
CP3	12	Control Pulse 3
CP4	12	Control Pulse 4
CP5	12	Control Pulse 5
CP6	12	Control Pulse 6
CP7	12	Control Pulse 7
CRCER +	13	Cyclic Redundancy Check Error
CR1-0/7	9	Control Register One Bits 0-7
CR2-0/7	9	Control Register Two Bits 0-7
CR3-0/7	9	Control Register Three Bits 0-7
CR4-0/7	9	Control Register Four Bits 0-7
CR5-0/7	9	Control Register Five Bits 0-7
CR6-0/7	9	Control Register Six Bits 0-7
CSA0 + /CSA9 +	8	Control Store Address Bits 0-9
DA16 +	3	Extended Data/Address Bit 16
DA17 +	3	Extended Data/Address Bit 17
DAT0 + /DAT7 +	14,15	Data Buffer Bits 0-7
DBWC1 +	13	Data Buffer Write Control In
DBWS –	13	Data Buffer Write Strobe
DBWS1 –	13	Data Buffer Write Strobe In
DB00 + /DB07 +	6	Data Bus Bits 0-7
DB08 + /DB15 +	7	Data Bus Bits 8-15
DEN –	6	Data Enable
DMGI +	4	DMA Grant In
D00 + /D07 +	2,3,4,9,11, 12,14,17, 18,19	D-Bus Bits 0-7
EADD +	3	Enable Address
EADD –	6	Enable Address
EBITC +	3	Enable Bit Count
ECCO +	19	Error Correction Code Out
EDATA +	3	Enable Data
ENRD –	13	Enable Read Data Register
ENWD –	13	Enable Write Data To Buffer
FAULT	17	Drive Fault
GDATA +	13	Gated Read Data
GSCLK –	3	Gated System Clock
GTIRQ +	5	Gated Transmit Interrupt Request
IAKI +	4	Interrupt Acknowledge In
IAKIG –	2	Interrupt Acknowledge In Grant
INDEX	17	Index Pulse From Drive
INIT +	4	Initialize
LXR0 –	11	Load External Register Data Out MSB
LXR1 –	11	Load External Register Data Out LSB
LXR2 –	11	Load External Register DMA Address MSB
LXR3 –	11	Load External Register DMA Address LSB
LXR4 –	11	Load External Register Data Buffer LSB
LXR5 –	11	Load External Register Data Buffer MSB
LXR6 –	11	Load External Register Data Buffer
LXR7 –	11	Load External Register Extended Address
LXR9 –	11	Load External Register Drive Control Tags
LXRA –	11	Load External Register Drive Control Bus Bits
LXRB –	11	Load External Register Vector Address
LXRC –	11	Load External Register System Control
LXRD –	11	Load External Register Bootstrap Address
LXRE –	11	Load External Register CPU Bus Control

TABLE 5-8 – CONTROLLER SYMPTOMS

Symptom	Possible Causes	Check/Corrective Action
1. Green DIAG light on the controller is OFF.	1. Microprocessor section of controller inoperative: a. Bad oscillator b. Short or open on board c. Bad IC d. PROMs not properly seated	1. Controller/Place controller on extender board. With a scope, check the pins on the 2901. All pins except power and ground should be switching. Check for "stuck high" or "stuck low," or half-amplitude pulses. Check + 12V and – 5V power and + 5V at various IC's. Check PROMs A1 through A7 for proper seating. Check oscillator.
2. No communication between console and computer.	2. I/O section of controller "hanging" Q Bus: a. $\overline{DEN}$ always low b. Shorted bus transceiver IC. c. Bad CPU board.	2. Computer interface logic of controller/ a. Check signal $\overline{DEN}$ for constant assertion. b. Check I/O IC's. Remove controller board to see if trouble goes away. (Ensure slot is filled or jumpered.) c. Run CPU diagnostics.
3. No data transfers to/from disc.	3. Disc not ready, bad connection, or bad IC in register section of the controller.	3. Disc/Consult the disc manufacturer's manual for proper setting of disc switches, or READY, NO FAULT, or UNSAFE lights. Check cable connections. Controller Registers/Using ODT, examine the Drive Status Register. The DISC READY and SELECTED must be "one's." Using ODT, deposit "ones" and "zeros" in the remaining disc registers and verify proper register data.
4. Data transferred to/from from disc incorrect.	4. Multiple Causes: a. Bad memory in backplane b. Noise or intermittent source of DC power in computer. c. Bad IC in disc I/O section of controller. d. Bad area on disc. e. Disc heads not properly aligned.	4. Computer-controller-disc/ a. Run memory diagnostics. b. Check AC and DC power. c. While operating, check lines from controller to disc with a scope for short or open. d. Run the Format and Diagnostic Test program (Section 3). If errors occur at the same place on the disc, it is probably a bad area on the disc. Assign alternate tracks as specified in Section 3. e. Consult disc drive manufacturer's manual and align heads.
5. Intermittent failure—Controller runs for a short time after power is applied and then fails.	5. Failure of heat sense component on controller.	5. Isolate the bad component by using heat and cooling methods (heat gun, freon spray) and replace the bad component.

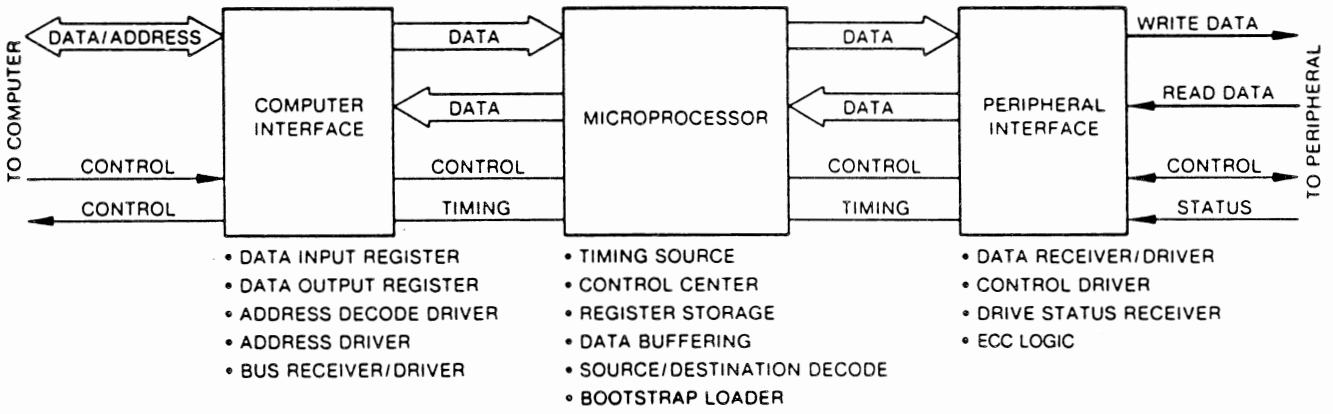
FIGURE 5-6 - BOARD LAYOUT



THEORY

The controller may be examined as three parts: computer interface, disk interface and controller internal functions. Signals from and to the computer are described in Table 5-1. Signals from and to the disk drive are described in Tables 5-2 and 5-3. Figure 5-7 is a simplified block diagram illustrating the interfaces and some of the functonal components. Single lines in the illustration represent serial data and the wider lines represent parallel data.

FIGURE 5-7 - SIMPLIFIED BLOCK DIAGRAM



Computer Interface

The purpose of the computer interface is to (1) buffer lines between the Q-Bus of the 11/23+ computer and the controller, and (2) to synchronize information transfers. The controller is a slave device during initialization and status-transfer sequences. The controller is selected by base address 777 440 . The controller is bus master during data transfers and either receives data from or outputs data to the computer memory via the 11/23+ DMA facility.

The control lines request information transfers, select the type and direction of transfers, and synchronize the transfers. The control lines are uni-directional and used for "bus arbitration." Bus synchronization is fully

controlled by the controller microprocessor. This allows the computer bus to be used by other devices when the disk controller is busy with internal functions and controller/disk data transfers.

Data bus driver/receiver registers 13H through 16H buffer the input data and distribute it as DB 00-15 in the controller. The DB signals are routed to a data input MUX and address decode registers.

Output data and addresses from the microprocessor Y-Bus (Y00-Y07) is latched by registers 13G through 16G, and transferred to the Q-Bus via bus driver/receivers 13H through 16H.

Note that the Device Enable signal (DEN-) is active when either Address Enable (EADD) or Data Enable (EDATA) signal is active. DEN controls the operating mode of all data and address driver/receivers, under control of the firmware, via the Y-Bus.

Disk Interface

The disk is connected to the controller by separate data and control cables. A common control cable is daisy-chained to both drives in a multiple-drive configuration, while separate data cables are always used.

Serial read data is received by receivers 16C or 15C and then converted to parallel data by the read/write shift register 9D In the reverse direction, parallel data from the data buffer is converted to serial data by the shift register, then sent to data cable drivers.

The Control Cable drivers 7B, 8B, 9B, and 10B are always enabled and are driven by the output of registers 9C and 10C, which act as latches to capture the Y-Bus data from the microprocessor.

Control Cable receivers 11B and 12B supply data to the disk status register/multiplexer 13C at all times. The data is available to the microprocessor via the D-Bus when signal XSD5- is active.

CONTROLLER INTERNAL FUNCTIONS

The microprocessor is the timing and control center of the controller. The microprocessor is controlled by instructions stored in programmable read-only

memory (PROM). The instructions, called "firmware," cause the microprocessor to operate in a prescribed manner during each of the computer-selected functions. The functions are established by a series of instructions issued by the 11/23+.

Because the disk and computer transfer data at different rates, it is necessary to buffer data going to and from the disk. High-speed RAM allows a full sector of data to be buffered during read and write operations.

All data transfer and computer/disk protocol is under microprocessor control. This feature allows modification of controller operating characteristics by making only changes to the firmware. Input/output logic remains essentially unchanged.

The output from the microprocessor is the "Y-Bus." Y-Bus instructions govern all controller operations by acting as the controller source for all receivers and drivers either directly or through the source/destination decode IC's.

The "D-Bus" is the data input to the microprocessor. Tri-state drivers allow many signal sources to be connected to the bus while only one at a time is enabled by the source/destination decode logic. The following list describes D-Bus enabling signals:

FUNCTION	TERM	ENABLED
Slave Address	XSD0	16F
Data Input (MSB)	XSD1	14F
Data Input (LSB)	XSD2	15F
Q-Bus Status	XSD3	18F
Data Buffer	XSD4	8F
Disk Status	XSD5	13C
Seek End/Unit Select	XSD6	14C
Error Status	XSD7	9F
Boot PROM	XSD8	12F
Switches	XSD9	17F
Literal	XSDA	7H
RK06 Switches	XSDB	21C
Scratch RAM Enable	XSDF	8H,9H

All data on the D-Bus is under control of the firmware as decoded by source PROMs 11H, 15D. The microprocessor selects the proper input data by enabling one of the above lines.

The Y-Bus is the microprocessor output. Output of the microcode PROM 5H is decoded by 12H and 17H to select the destination of the data on the Y-Bus. The following list describes Y-Bus enabling signals:

FUNCTION	TERM	ENABLED
Data Out Register (MSB)	LXR0	13G
Data Out Register (LSB)	LXR1	15G
DMA Address (MSB)	LXR2	14G
DMA Address (LSB)	LXR3	16G
Data Buffer Address (LSB)	LXR4	11C,12D
Data Buffer Address (MSB)	LXR5	12C
Data Buffer Load	LXR6	7C,8G
Load Extended Address	LXR7	13D
Drive Control (Tags)	LXR9	10C
Drive Control (Bus 0-7)	LXRA	9C
Load Vector Address	LXRB	10G
System Control	LRXC	18G
External Event	LRXD	22D
Q-Bus Control	LRXE	17G
RAM Destination	LRXF	8H,9H

With the single exception of bus reply detector 21E, all Y-Bus data and address activity is controlled by the 15 signals shown above.

Each LXR (Load External Register) signal activates a register, which, in conjunction with Y-Bus data, latches the appropriate data word.

Control Registers CR1 through CR6 are the outputs of the microcode PROMs. These signals control the microprocessor functions and provide the data to the source/destination decode logic.

Data Buffer

Data Transfers to and from the buffer are both two-step operations. First, an entire sector of data is loaded into the buffer during either a read or write operation. Once loaded, the buffer contents are then transferred to disk or 11/23+ memory in a completely separate operation. Figure 5-8 illustrates read and write operations to and from the RAM data buffer.

During a write operation, parallel data (Y00-Y07) is transferred from 11/23+ memory via microprocessor to the write data register 8G. The data (DAT0-DAT7) is then transferred to the buffer 10D and 11D Parallel data (DAT0-DAT7) from the buffer is then transferred to shift register 9D, converted to serial data (W DATA), and transferred to the data cable driver 19A.

During a read operation, serial read data (R DATA) from the data cable receivers is ANDED with Enable Bit Count (E BIT C) resulting in the signal G DATA. This signal enters the shift register F7 and is transferred as parallel data to the Read Data register 8D, for transfer to the data buffer while the next byte is being shifted through shift register 9D. The read data from the buffer (DAT0-DAT7) is transferred to driver 8F to the microprocessor for transfer to 11/23+ memory.

The counter located at 11C, 12C and 12D is used to address the location in the buffer into which data can be written or read from. The counter has the capability of being preset to a specific starting address via the Y-Bus of the microprocessor.

ERROR CORRECTION CODE (ECC) LOGIC

Functional Operation

The ECC Generator does not correct errors; it generates codes during write and read operations and during reading generates a syndrome. A syndrome is the result of merging check characters being read with check characters generated. A zero syndrome indicates no error; a non-zero syndrome indicates an error. This syndrome contains all the information necessary to find the error location and the error pattern, i.e., to allow error correction.

The error location is found by counting the number of clock pulses required to make the EP output go high. The error pattern is then available on the LP0-LP3 and Q0-Q7 outputs and can be used to exclusive OR with data. Depending upon the position of switch S5 (location D17), either the computer or the controller corrects the error. Note that some error patterns cannot be corrected. These are flagged to the computer.

Component Description

During a write operation, a 32-bit ECC is appended to the header record and a 56-bit ECC is appended to the data record of each sector of information on the disk. ECC's are also generated while information is being read from the disk.

The codes generated during the read operation are compared with the equivalent codes previously written. Discrepancies detected (errors) are signalled to the microprocessor and corrected if possible.

The ECC Generator (7E), also referred to as the Burst Error processor, is used in three different types of operations: write, read, and correct. Detailed information about the ECC generator is given by an AMD, AM9520/Z8065 product specification.

During writing or reading, information is connected to the D0 through D7 inputs of the ECC Generator. Select inputs S0 and S1 determine whether a 32- or 56-bit polynomial is being used. The 32-bit polynomial is used for ECC header checks, and the 56-bit polynomial is used for data record check. The Data Buffer Write Strobe (DBWS) is the source of Clock Pulses (CP) to the ECC Generator.

Control information for the ECC Generator from the Y-Bus is stored by LXR5 into ECC Control Register 9G.

When MF- is asserted, the logic is initialized. Asserting REP (Read Error Pattern) makes outputs LP0-LP3 and Q0-Q7 active. Control inputs P0-P3 are not used. The ECC Generator functions selected by the C0-C2 inputs are as follows:

C2	C1	C0	FUNCTION
L	L	L	Compute Check Bits
L	L	H	Write Check Bits
L	H	L	Read Normal
H	L	L	Load
H	H	L	Correct Normal

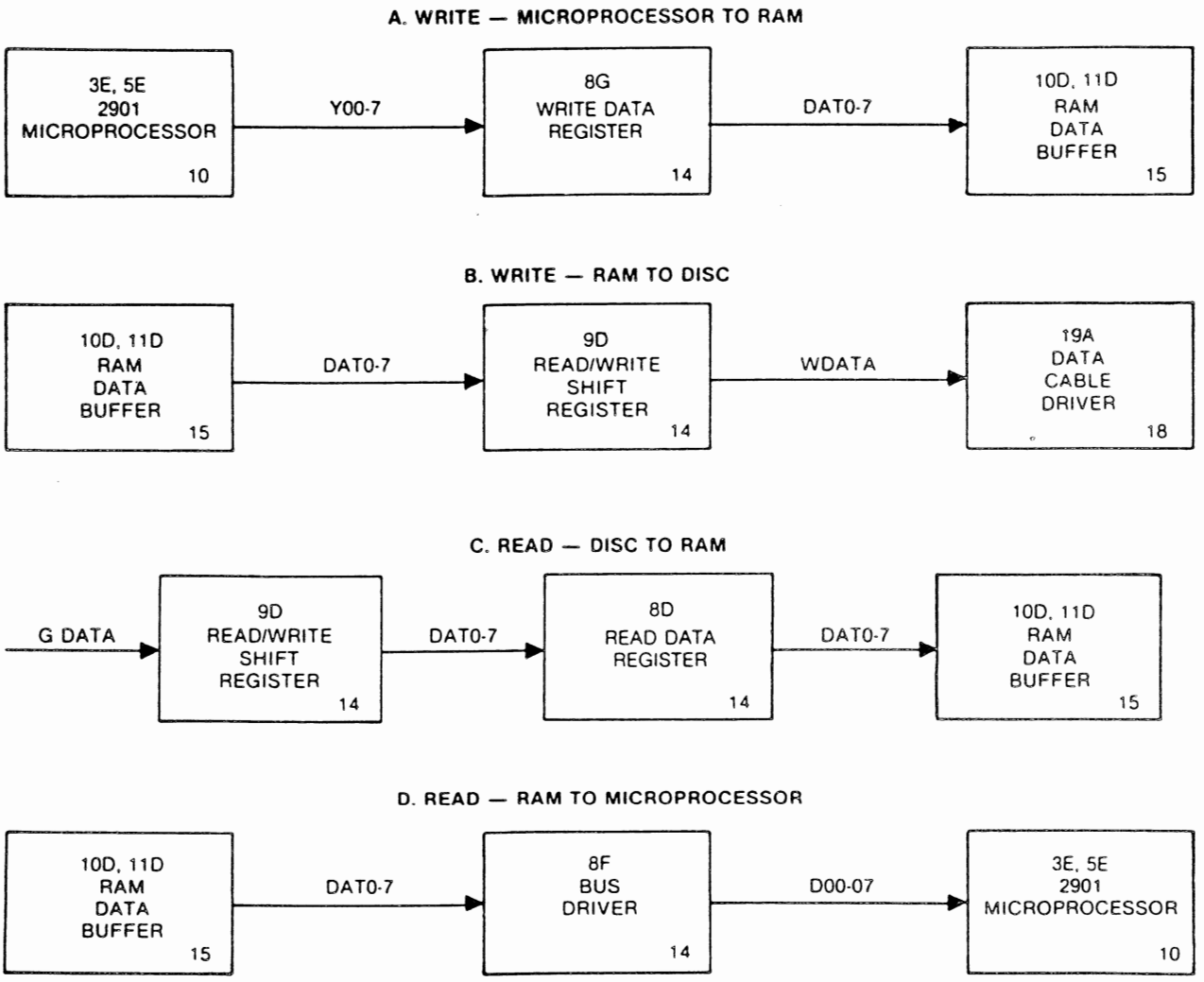
Check bit outputs Q0-Q7 are connected to the DAT0-DAT7 lines one byte at a time under control of REP and C0-C2. The remaining outputs of the ECC Generator are stored in ECC Status Register 9F by clock GSCLK. The microprocessor monitors ECC status on the D-Bus during XSD7 time.

Outputs LP0-LP3 (Located Error Pattern), together with outputs Q0-Q7, provide the 12-bit error pattern. Q7 is the MSB and LP0 is LSB of the pattern. Outputs LP0-LP3 are active only when REP is asserted. Output AE (Alignment Exception) is asserted if the error pattern will not line up automatically during a correction sequence. This can occur because of the method of polynomial

division implemented in the ECC generator.

Output EP (Error Pattern) is asserted when the error pattern has been located during the correction sequence. Output ER is asserted if an error was detected after the last check byte had been read during a read function.

FIGURE 5-8 - DATA PATHS



+12 VOLT TO -5 VOLT POWER SUPPLY

The +12 to -5 volt power supply is a dc-to-dc converter that produces the -5 volts required for the current mode line driver to the disk(s).

Input power is obtained from the +12 volts on the backplane. Oscillator R19, C6, 14A provides rectangular pulse that drives current switch Q1. When the oscillator turns Q1 on, +12V is applied to L1 and an increasing current is produced. When the oscillator turns off Q1, the energy stored in L1 produces a negative voltage (at the top of L1), charging diodes C4 and C5 through diode CR1. Successive oscillator pulses cause the voltage across G5, G4 to build up to approximately -5 volts. Circuit 21A is a zener-referenced regulator that produces a threshold control voltage that regulates the duty cycle of the oscillator drive voltage applied to Q1 (increasing or decreasing "ON" time). Circuit 21A thus controls the energy stored in L1 to maintain and regulate the voltage on G5, G4 at -5 volts under normal load conditions.

CHAPTER 6

MQ SEMICONDUCTOR MEMORY

INTRODUCTION

The MQ memory card is an add-in memory for the FHL PowerFrame system. The standard memory capacity of the MQ memory module is 512K words by 18 bits (529,288 words x 18 bits). Optional memory capacity is available upon request. See Table 6-1.

TABLE 6-1 - MEMORY CAPACITY

MEMORY SIZE	NO. OF DATA BITS	CSR
64K Words	16 Bits	No
64K Words	18 Bits	Yes
128K Words	16 Bits	No
128K Words	18 Bits	Yes
256K Words	16 Bits	No
256K Words	18 Bits	Yes
512K Words	16 Bits	No
512K Words	18 Bits	Yes

Options

Battery backup can be utilized on this module. The +5 battery backup voltage pins are compatible with those that FHL provides on the MSV11-L MOS memory card. Table 6-2 gives jumper requirements.

TABLE 6-2 - BATTERY BACKUP

	W1	W3	W4
For +5 battery backup	I	I	R
For non-battery backup	R	R	R

* I = Install
R = Remove

This module has the capability for address decoding, up to 2 megawords (4MB). Table 6-3 gives jumper settings for this option.

TABLE 6-3 - ADDRESS RANGE

	J23	J24
For 128KW Address Range	R	I
For 2MW Address Range	I	R

* I = Install
R = Remove

The CSR can be enabled or disabled by installing and removing the proper jumpers. Table 6-4 shows the selections.

TABLE 6-4 - CSR OPTION

	J31	J32
For CSR Enabled	I	R
For CSR Disabled	R	I

* I = Install
R = Remove

The MQ256 has on-board parity generation and checking. The I/O page is factory set for 4KW.

Modes of Operation

The MQ256 memory module is capable of operating in the three modes required by the 11/23+ system.

1. DATI (Read)
2. DATO, DATOB (Write)
3. DATIO, DATIOB (Read-Modify-Write)

The read modes operate on the full 16-bit memory word. The write modes operate either on the full word or a byte basis. The memory provides its own refresh timing and addressing.

Timing

The MQ256 performance for access and cycle time is listed in Table 6-5. Up to 500ns may be added to the cycle times if the memory is doing a refresh operation when a memory cycle is requested. Cycle time is defined as SYNC H to SYNC H negated at maximum allowable 11/23+ bus speed. DATI cycle access time is defined as internal SYNC H to RPLY H with 25ns from SYNC to DIN H. DATO (B) cycle access time is defined as internal SYNC H to RPLY H with 50ns from the SYNC H to DOUT H.

TABLE 6-5 - ACCESS AND CYCLE TIMING

MEMORY FUNCTION	BUS CYCLE TYPE	ACCESS TIME (MAX)	CYCLE TIME (MAX)
Read	DATI	190ns	490ns
Write	DATO (B)	90ns	390ns
Read-Modify-Write	DATIO (B)	700ns	1000ns

* Timing values given are referenced to 1.5V level.

Power Requirements

Table 6-6 is a list of power requirements needed for the MQ256 memory module.

TABLE 6-6 - POWER REQUIREMENTS

SUPPLY VOLTAGE	OPERATIONAL	CURRENT REQUIREMENTS	
		STANDBY	OPERATING
+5V	5V +/- 5%	2.8 A	4.0 A max
+5VBB	5V +/- 5%	1.5 A 1.6 max	

Environmental Specifications

The MQ256 is designed to operate in a variety of environmental conditions, including:

* Temperature - Ambient air temperature range of 0 C to +50 C

* Thermal Shock - The memory can withstand a thermal shock with a maximum rate of change of 30 C per hour during operation.

* Humidity - The MQ256 can operate from 10% to 90% relative humidity (without condensation).

Shipping and Storage

* Temperature - During shipment or storage, a temperature range of -40 C to +85 C can be withstood by the memory.

* Thermal Shock - A thermal rate of change as high as 10 C per minute can be tolerated by the memory.

* Altitude - A shipping altitude of 40,000 feet can be withstood.

Dimensions

Table 6-7 gives dimensions on the MQ256 memory module.

TABLE 6-7 - DIMENSIONS

PCB Thickness	.056	inches
Width	10.457	inches quad module
Length	8.930	inches (includes handles)
Max component height	.375	inches
Total thickness max	.490	inches

THEORY AND OPERATION

Interface Specification

Bus Receivers

Input Low Voltage	1.3V maximum
Input High Voltage	1.7V minimum

Maximum input current when connected to 3.8V is 80uA even with no power applied.

Bus Drivers

Output low voltage when sinking 70uA is .7V. Maximum output high leakage current when connected to 3.8V is 25uA even if no power is applied.

Interface Signals

Table 6-8 gives a list of input control signals to the memory. The memory module presents one standard bus load to the 11/23+ system bus for each of the following signals:

TABLE 6-8 - CONTROL SIGNALS

SIGNAL NAME	CONNECTOR PIN
BDOUT L	AE2
BDIN L	AH2
BSYNC L	AJ2
BWTBT L	AK2
BBS7 L	AP2
BDCOKH	BA1
BINIT L	AT2

Description of Control Signals

* BDOUT L - When this signal is asserted it indicates that a write cycle (DATO), or the write portion of a Read-Modify-Write cycle (DATIO) is to be performed by the memory.

* BDIN L - When this signal is asserted it indicates that a read cycle (DATI) or the read portion of a Read-Modify-Write is to be performed by memory.

* BSYNC L - When this signal is asserted, it indicates that a valid address is on the bus. When the address is in the operating range of memory, BSYNC will also initiate a memory cycle. The type of memory cycle will be determined by BDIN, BDOUT, or BWTBT.

* BWTBT L - When this signal is asserted during a leading edge of a BSYNC signal, it indicates a write cycle is to be performed (DATO, DATOB). If asserted during the duration of a BDOUT, a byte write (DATOB, DATIOB) will take place. The byte to be written is determined by the state of BDAIO during the leading edge of BSYNC. BDAIO = 0 indicates Byte 0; BDAIO = 1 indicates Byte 1.

* BBS7L - When this signal is asserted, it indicates an I/O operation. If address bits 1-12 match the CSR address, then a CSR Write or Read will occur.

* BDCOK H - This signal goes active high for 3ms minimum, after DC power is applied. It falls low 5u minimum before DC voltages are out of tolerance. It is used to prevent the memory module from being selected or power up or power down.

* BINIT L - The MQ256 uses this signal to reset the Control and Status Register (CSR).

Description of Output Signals

Table 6-9 gives a list of output signals.

TABLE 6-9 - OUTPUT SIGNALS

SIGNAL NAME	CONNECTOR PIN
PARERR	AC1 (BDAL 16)
	AD1 (BDAL 17)
BRPLY	AD2

* PARERR

  BDAL 16 is used to indicate memory parity error.

  BDAL 17 is the memory enable line.

* BRPLY

  This signal is generated by the memory module to indicate that it has placed its data on the BDAL bus, or that it has accepted output data from the bus.

I/O Connector Pin List

The I/O Connector Pin List for the memory card is shown in Table 6-10.

TABLE 6-10 - I/O CONNECTOR PIN LIST

COMPONENT SIDE	PIN	PIN	SOLDER SIDE
A Connector			
	A1	A2	+5 Volts
	B1	B2	
BDAL16 L	C1	C2	Ground
BDAL17 L	D1	D2	
+5V BATT (option)	E1	E2	BDOUT L
	F1	F2	BRPLY L
	H1	H2	BDIN L
Ground	J1	J2	BSYNC L
	K1	K2	BWTBT L
	L1	L2	
Ground	M1	M2	BIAKI L
	N1	N2	BIAKO L
	P1	P2	BBS7 L
	R1	R2	BDMGI L
Ground	T1	T2	BINIT L
	U1	U2	BDAL00 L
+5V BATT (option)	V1	V2	BDAL01 L
B Connector			
BDCOK H	A1	A2	+5 Volts
	B1	B2	
BDAL 16L	C1	C2	Ground
BDAL 19L	D1	D2	
BDAL 20L	E1	E2	BDAL02 L
BDAL 21L	F1	F2	BDAL03 L
	H1	H2	BDAL04 L
Ground	J1	J2	BDAL05 L
	K1	K2	BDAL06 L

	L1	L2	BDAL07 L
Ground	M1	M2	BDAL08 L
	N1	N2	BDAL09 L
	P1	P2	BDAL10 L
	R1	R2	BDAL11 L
	S1	S2	BDAL12 L
Ground	T1	T2	BDAL13 L
	U1	U2	BDAL14 L
+5 Volts	V1	V2	BDAL15 L

	A1	A2	+5 Volts
	B1	B2	
	C1	C2	Ground
	D1	D2	
	E1	E2	
	F1	F2	
	H1	H2	
	J1	J2	
	K1	K2	
	L1	L2	
	M1	M2	BIAKI L
	N1	N2	BIAKO L
	P1	P2	
	R1	R2	BDMGI L
	S1	S2	BDMGO L
Ground	T1	T2	
	U1	U2	
	V1	V2	

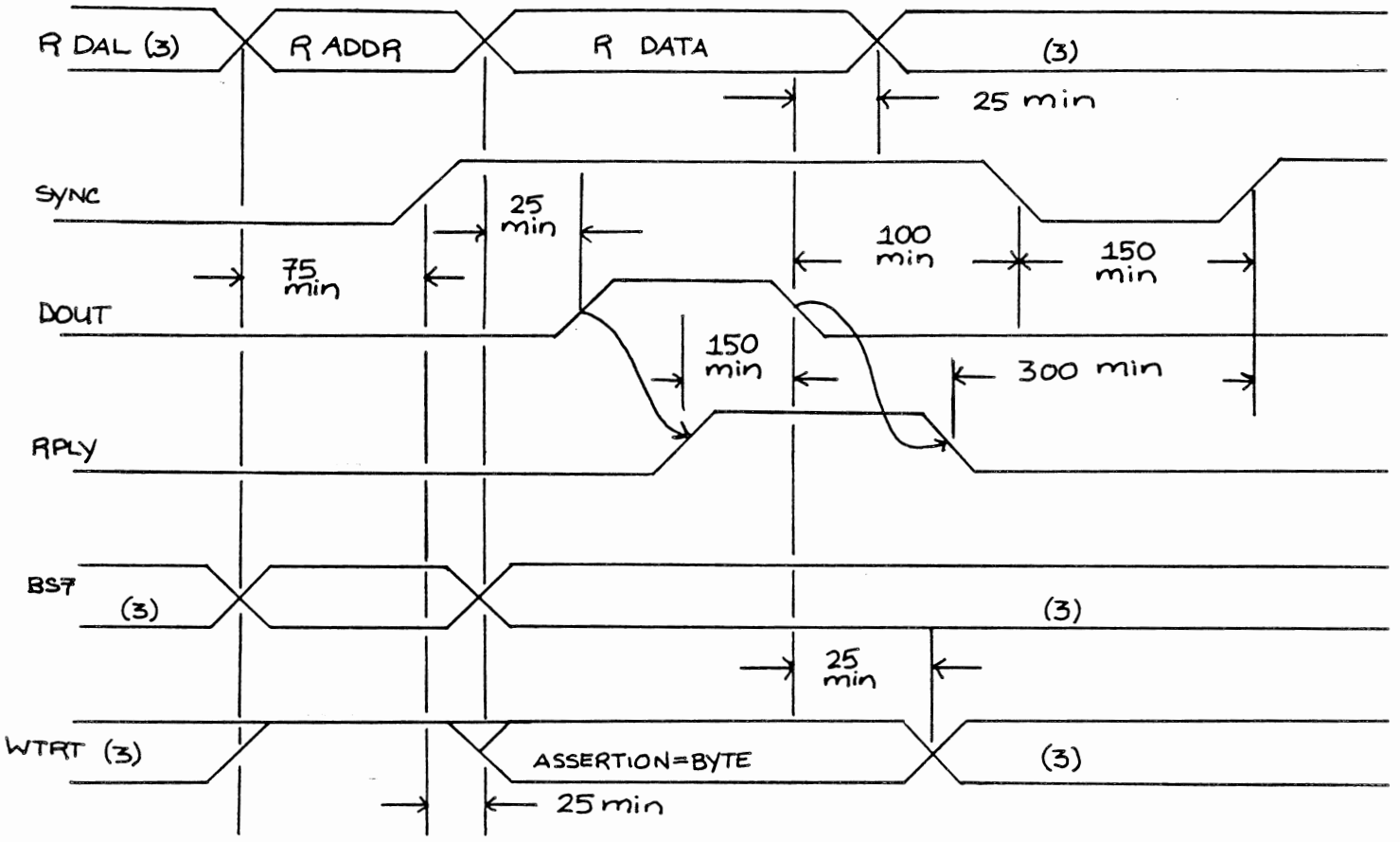
	A1	A2	+5 Volts
	B1	B2	
	C1	C2	Ground
	D1	D2	
	E1	E2	
	F1	F2	
	H1	H2	
	J1	J2	
	K1	K2	
	L1	L2	
	M1	M2	
	N1	N2	
	P1	P2	
	R1	R2	
	S1	S2	
Ground	T1	T2	
	U1	U2	
	V1	V2	

Timing

Timing is done by using a 200ns delay line fed by the Read/Write flip flop and the refresh grant flip flop. Appropriate taps are selected for enable RAS and CAS latches. CAS is disabled during a refresh cycle; therefore only a RAS refresh cycle is performed.

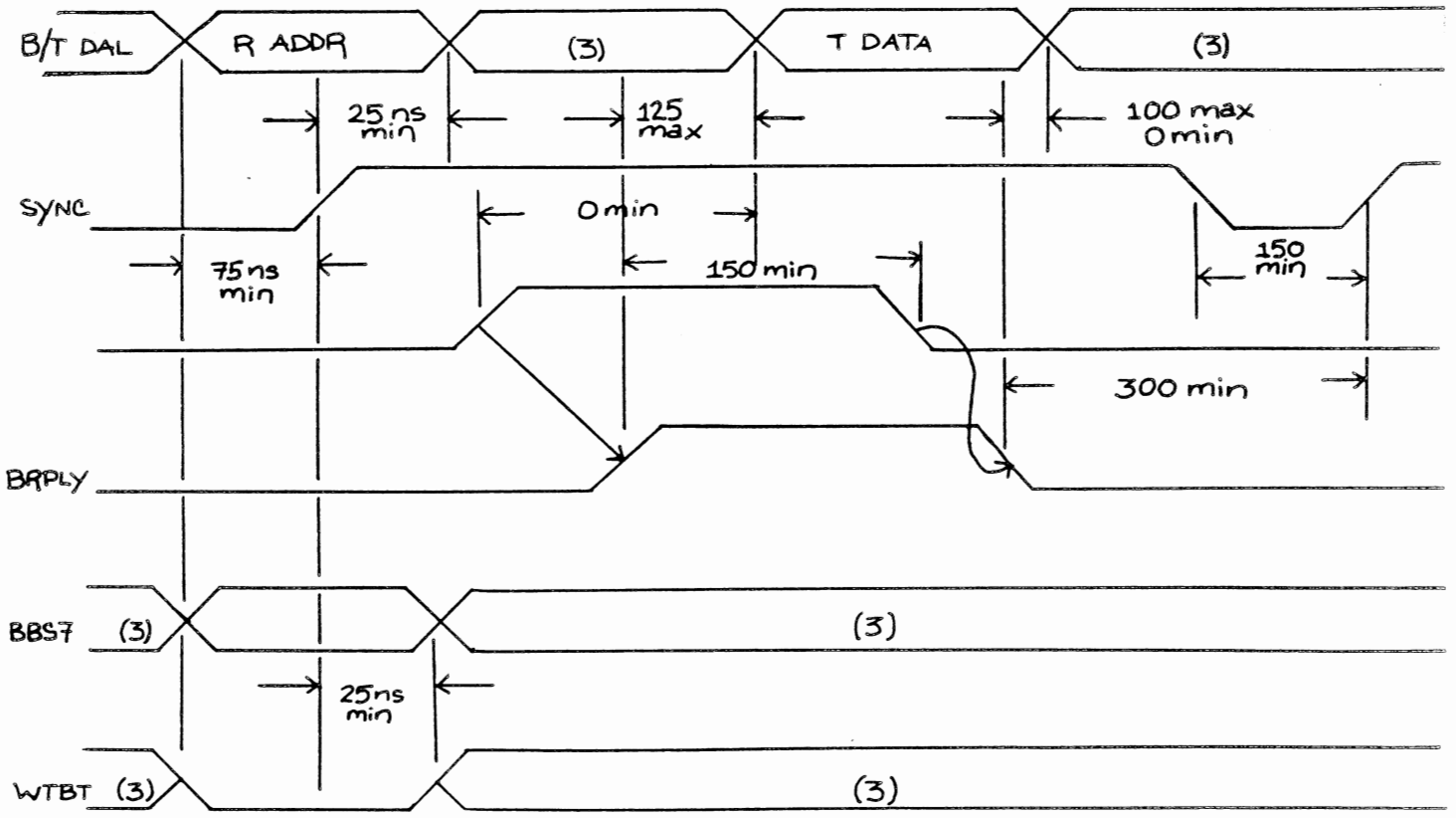
The following figures are the timing charts of DATO, DATOB (Figure 6-1); DATI (Figure 6-2) and DATIO, DATIOB (Figure 6-3).

FIGURE 6-1 - DATO or DATOB



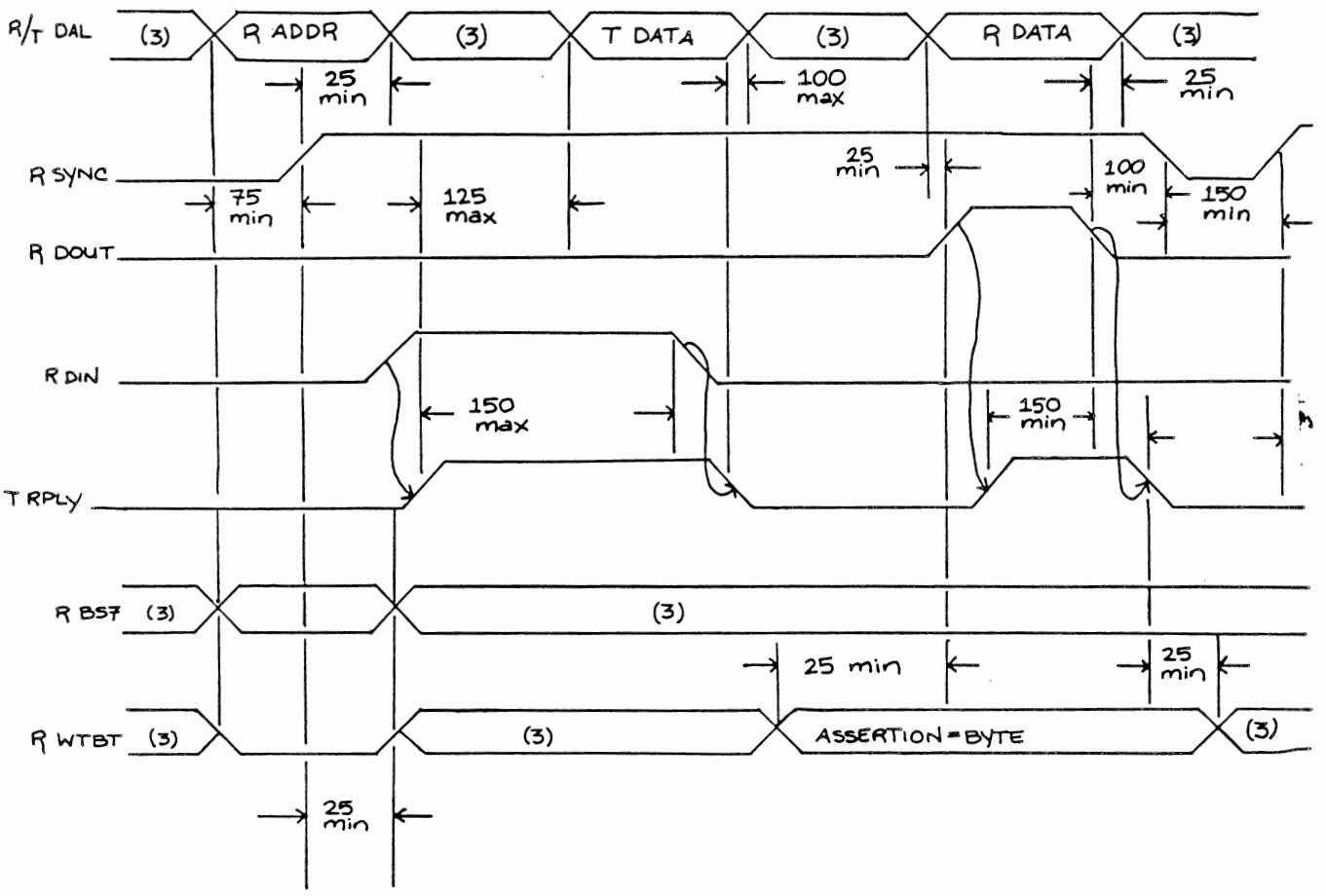
1. Timing shown at Bus Driver Inputs and Bus Receiver Outputs.
2. Signal name prefixes are defined below:
   T. Bus Driver Input
   R. Bus Receiver Output
3. Don't care condition

FIGURE 6-2 - DATI Bus Cycle Timing (Read Memory)



1. Timing shown at Bus Driver Inputs and Bus Receiver Outputs
2. Signal name prefixes are defined below:
   T. Bus Driver Input
   R. Bus Receiver Output
3. Don't care condition
4. All timing given in nanoseconds

FIGURE 6-3 - DATIO or DATIOB Bus Cycle Timing

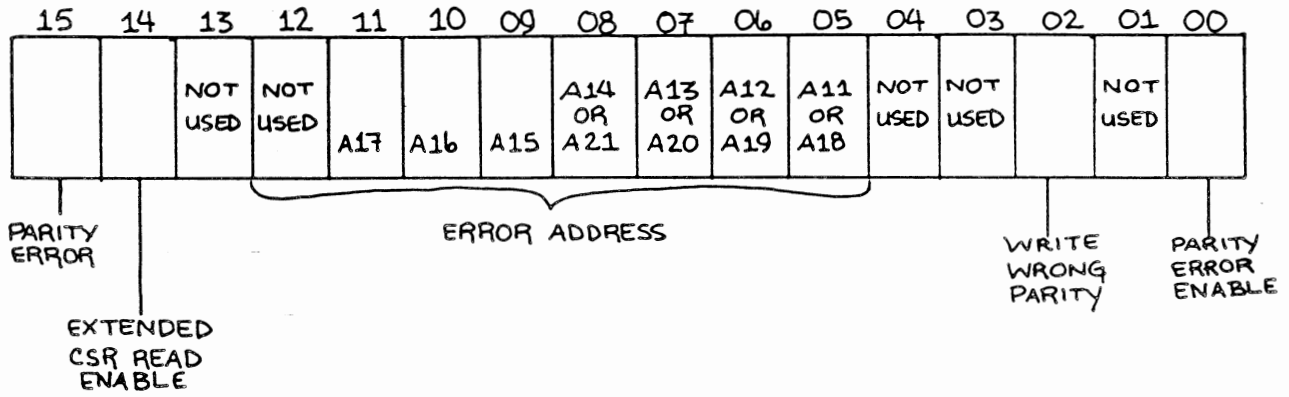


1. Timing shown at Bus Driver Inputs and Bus Receiver Outputs
2. Signal name prefixes are defined below:
   T. Bus Driver Input
   R. Bus Receiver Output
3. Don't care condition
4. All timings are given in nanoseconds

Control and Status Register

The MQ256 uses the Control and Status Register (CSR) for program control of certain parity functions and contains diagnostic information, should a parity error occur. The CSR has a Q-Bus Address. Therefore, it can be accessed by a bus master. Bus INIT (L) will clear some of the CSR bits (see Signal Description for an itemized list). Bus INIT is asserted on system Power Up or by a reset instruction. Refer to Table 6-14 for CSR Address selection, and Table 6-11 for CSR Bit allocation.

TABLE 6-11 - CSR ALLOCATION



NOTE: CSR Bits 01, 03, 04, 12, 13 are not used by the CSR. These bits will always be read as 1's. Writing into these bits will have no effect on the CSR.

* CSR Bit 0: Parity Error Enable: This bit is a Read/Write bit and is set to a 0 on a Bus INIT or a Power Up. If a parity error should ever occur on either a DATI or DATO(B) cycle to memory and CSR Bit 0 = 1, then BDAL 16 and BDAL 17 will be asserted (L) on the bus simultaneously with data.

* CSR Bit 1: Not Used.

* CSR Bit 2: Write Wrong Parity: When this bit is set to a 1 and a DATO(B) cycle to memory occurs, the parity

RAMs will receive wrong parity data. The bit is a maintenance bit used to check parity error logic and CSR failed address information. The bit is a Read/Write bit - Power Up or Bus INIT sets this bit to a 0.

* CSR Bit 3: Not Used.

* CSR Bit 4: Not Used.

* CSR Bits 5-11: These are Read/Write bits, and are not cleared by Bus INIT or Power Up. If a parity error occurs on a DATI or DATO(B) memory cycle, then address bits A11-A17 are stored in CSR bits 5-11 and address bits A18-A21 are latched. Only one read is required on the CSR for 128KW systems (18 bit address). For systems larger than 128KW (22 bit address) a second read of the CSR must be done. The use of CSR bit 14 is required to do this. The parity error address will be narrowed to a 1K segment of memory.

* CSR Bit 12: Not Used.

* CSR Bit 13: Not Used.

* CSR Bit 14: Extended CSR Read Enable: This bit is not used on a 128KW system and is read as a 0. Systems with more than 128KW use this bit to read address bits A18-A21 which are stored in CSR bits 5 through 8, respectively. When reading a parity error address larger than 128KW, the first step is to set CSR bit 14 to a 0, then read the CSR. Bits 5-11 of the CSR will contain address bits A11-A17. The second step is to set CSR bit 14 to a 1, then read the CSR. Bits 5-8 will contain address bits A18-A21. The CSR will isolate the failing address to a 1K segment of memory. This bit will be set to a 0 on a Bus INIT or a Power Up, and is a Read/Write bit.

* CSR Bit 15: Parity Error: This bit will be set to a 1 if a parity error should occur. This is a Read/Write bit and a Power Up or Bus INIT will set this bit to a 0.

Parity Generation and Checking

The MQ256 has the provision on board for parity generation and checking. A parity generator and checker is done on a per byte basis. On all write cycles (DATO) parity is generated per byte. On all read cycles (DATI) parity is checked per byte.

If a parity error should occur on either byte, a parity error signal is gated onto the BDAL 16 and BDAL 17 Q-Bus lines. These signals are checked by the processor during the memory read DATI cycle.

The parity circuitry can be functionally checked by writing a 1 into CSR Bit 2, which causes bad parity to be written during a DATO cycle. By doing a DATI at the same address the parity ERROR signal will be set to BDAL 16, BDAL 17.

Reserved I/O Space

When Bank Select Seven (BBS7 L) is asserted, the memory is deselected during I/O operations. BBS7 L is also used to determine if CSR address selection occurs. The MQ256 is factory set for a 4KW I/O space.

Mechanical Description

The MQ256 is completely contained on one multi-layer printed circuit module. This memory module is designed to plug directly into the standard H9270 ("quad"), the H9273A LSI-11 backplane/card guide, the H9275 11/23+, and the FHL expansion unit.

INSTALLATION

Introduction

This section contains basic information for installation of the MQ256 memory module. The MQ256 can be installed in and is electrically compatible with the 11/23+ system. No special tools are required for installation of the MQ256.

Preliminary Procedure

Run all system exercisers on the system prior to installation, to insure system integrity. If a problem is found it should be noted and fixed before proceeding with the installation of the memory card.

Starting Address Selection

Jumpers J4-J12 provide the starting address selection. Tables 6-12 and 6-13 give a detailed list for starting address selection. Starting address selection is done in 4K increments. For addresses larger than 128KW, J23 must be installed. Tables 6-12 and 6-13 are used together for starting address. Refer to Figures 6-4 and 6-5 for proper orientation of jumper locations.

CSR Address Selection

The MQ256 contains an on board Control and Status Register (CSR) which contains error information in the event of a parity error. There are eight possible CSR addresses which are listed on Table 6-14. Refer to Figures 6-4 and 6-5 for proper orientation of jumper locations.

Memory Size Selection

The MQ256 may be set from a minimum of 64KW to a maximum of 512KW. Table 6-15 lists jumper settings for selecting memory size.

FIGURE 6-4 - ASSEMBLY DRAWING

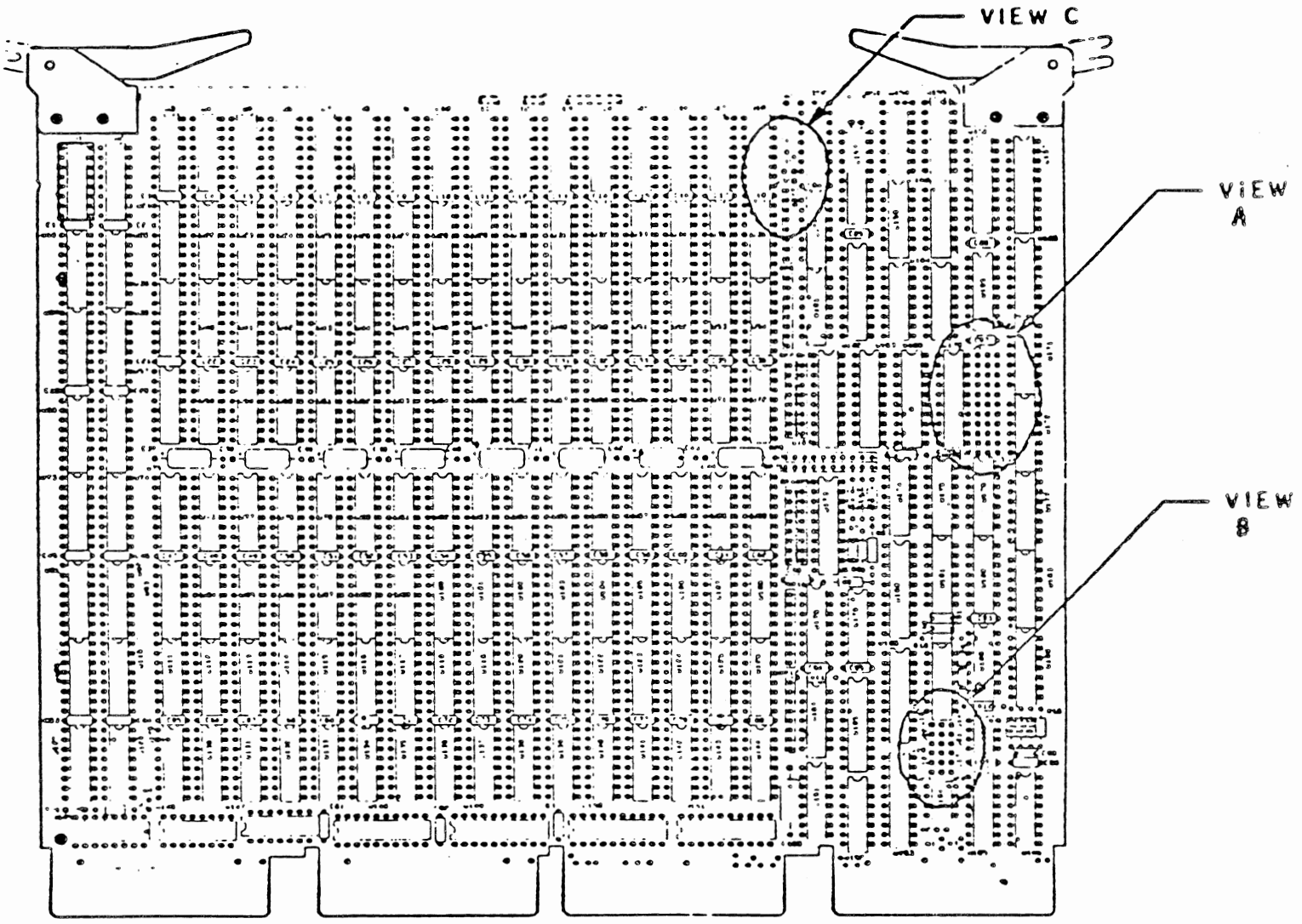


FIGURE 6-5 - JUMPER LOCATIONS

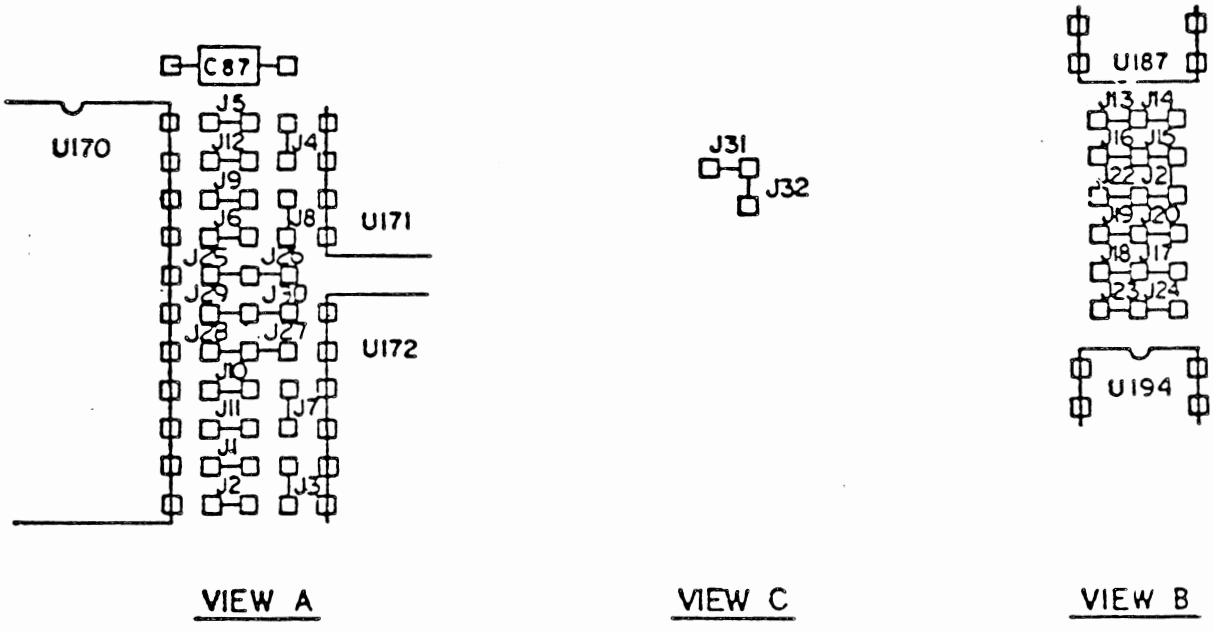


TABLE 6-12 - ADDRESS SELECTION

STARTING ADDRESS*	JUMPERS** J4	J5	J6	J7	J8
0K	0	0	0	0	0
4K	I	0	0	0	0
8K	0	I	0	0	0
12K	I	I	0	0	0
16K	0	0	I	0	0
20K	I	0	I	0	0
24K	0	I	I	0	0
28K	I	I	I	0	0
32K	0	0	0	I	0
36K	I	0	0	I	0
40K	0	I	0	I	0
44K	I	I	0	I	0
48K	0	0	I	I	0
52K	I	0	I	I	0
56K	0	I	I	I	0
60K	I	I	I	I	0
64K	0	0	0	0	I
68K	I	0	0	0	I
72K	0	I	0	0	I
76K	I	I	0	0	I
80K	0	C	I	0	I
84K	I	0	I	0	I
88K	0	I	I	0	I
92K	I	I	I	0	I
96K	0	0	0	I	I
100K	I	0	0	I	I
104K	0	I	0	I	I
108K	I	I	0	I	I
112K	0	0	I	I	I
116K	I	0	I	I	I
120K	0	I	I	I	I
124K	1	I	I	I	I

Note: 0 = Removed

I = Installed

** Standard configuration

External address option
Jumper 24 installed
J23 removed

TABLE 6-13 - JUMPER 23 INSTALLED

ADDRESS RANGE	JUMPERS** J9	J10	11	J12
0K-128K*	0	0	0	0
0K-128K**	0	0	0	0
128K-256K	I	0	0	0
256K-384K	0	I	0	0
384K-512K	I	I	0	0
512K-640K	0	0	I	0
640K-768K	I	0	I	0
768K-896K	0	I	I	0
896K-1024K	I	I	I	0
1024K-1152K	0	0	0	I
1152K-1280K	I	0	0	I
1280K-1408K	0	I	0	I
1408K-1536K	I	I	0	I
1536K-1664K	0	0	I	I
1664K-1792K	I	0	I	I
1792K-1920K	0	I	I	I
1920K-2048K	I	I	I	I

Address Range Selection

Note:

0 = Removed

I = Installed

* Non Extended Address

** Extended Address Option
J24 removed
J23 installed

	J23	J24
Extended Address	I	R
Non Extended Address	R	I

TABLE 6-14 - CSR ADDRESS SELECTION

22 Bit CSR Address	18 Bit CSR Address	JUMPERS J1	J2	J3
17772100	772100	I	I	I
17772101	772102	O	I	I
17772104	772104	I	O	I
17772106	772106	O	O	I
17772110	772110	I	I	O
17772112	772112	O	I	O
17772114	772114	I	O	O
17772116	772116	O	O	O

O = Remove
I = Install

TABLE 6-15 - MEMORY SIZE SELECTION

MEMORY SIZE	JUMPERS J27	J28	J29	J30	J25	J26
65KW	O	I	I	O	I	O
128KW	I	O	I	O	I	O
256KW	I	O	O	I	I	O
512KW	I	O	O	I	O	I

O = Remove
I = Install

TABLE 6-16 - JUMPER DEFINITIONS

JUMPER	PURPOSE		CONFIGURATION
J22, J15, J14 J18, J19	Factory Test Aid	*	Standard Configuration R = Factory Test Only
J21, J16, J13 J17, J20	Factory Test Aid		I = Factory Test Only * R = Standard Configuration
J24	Extended Address Option	**	I = 128K Word Address Range R = 2 Mega Word Address Range
J23	Extended Address Option	**	I = 2 Mega Word Address Range R = 128K Address Range
W1, W2, W3	+5 Battery Supply	*	I = Battery Back-up option R = Non Battery Back-up
W4	+5V Supply =	*	I = Non Battery Back-up R = Battery Back-up option
J31	CSR Enable	*	I = Standard Configuration R = Eliminate CSR
J32	CSR Disable	*	I = Eliminate CSR R = Standard Configuration

I = Install
R = Remove

* Standard Configuration

** Jumpers will be factory set to customers configuration

Add on Installation

A. Set all peripherals to "unload" condition.

B. Turn system power off at this time.

CAUTION: DO NOT INSTALL the memory module with power to the backplane. Damage to memory may occur.

C. Verify jumper configuration for starting address, CSR Address, and memory size.

D. Install memory module carefully into the selected slot. Insure that the component side faces the correct direction and the module is aligned in the card guides. Caution should be taken not to allow components to rub adjacent modules. Press FIRMLY when module engages backplane connectors making sure module is seated properly.

E. Turn system power "ON".

F. Run memory diagnostics. (See following section)

TROUBLESHOOTING

Introduction

This section describes how to use the memory diagnostics to troubleshoot and isolate a failure in memory to a faulty RAM. Standard XXDP loading and starting procedures are used on processors with no hardware switch registers; the software switch register will be in Location 176.

ZKMA: This diagnostic will test 0-256KB of memory on the 11/23+ computer.

Switch Setting Summary:

BIT	15(100000);	SW15=1	Halt on Error
BIT	14(040000);	SW14=1	Loop on Test
BIT	13(020000);	SW13=1	Inhibit Error Printouts
BIT	12(010000);	SW12=1	Enable Testing Above 28K
BIT	11(004000);	SW11=1	Enable Parity Testing
BIT	10(002000);	SW10=1	Halt After Each Test
BIT	09(001000);	SW09=1	Inhibit Program Relocation
BIT	08(000400);	SW08=1	Type First Failure in 4K Bank
BIT	07(000200);	SW07=1	Long Galloe Test *
BIT	06(000100);	SW06=1	Inhibit Memory Sizing
BIT	05(000040);	SW05=1	Inhibit End Pass Printouts
BIT	04(000020);	SW04=1	Inhibit Printouts
BITS	3-0	SW3-0	Beginning Test Number

* CAUTION: The long Galloe Test will increase test times by a factor of 25.

Running ZKMA

1. Load program ZKMA?? into memory (L ZKMA?? <CR>).

2. Select options by setting bits into the switch register. Refer to the above switch settings. NOTE: Normal switch settings would be bits 11 and 12 set (014000).

3. Start program testing (S <CR>).

4. A pass with no errors detected will appear similar to the following sample printout:

```
000000-757777
PARITY
```

```
TST13 BNK  0
TST13 BNK  1
TST13 BNK  2
TST13 BNK  3
TST13 BNK  4
TST13 BNK  5
TST13 BNK  6
RELOC
TST13 BNK  0
END PASS 1
```

5. The following is an example of a typical error message printout:

LOCATION	GOOD	BAD	PC	ERROR	PASFLG
177210	177777	177776	1625	10	[TST0]

LOCATION = FAILING MEMORY LOCATION
GOOD = GOOD DATA (DATA THAT WAS EXPECTED)
BAD = BAD DATA (DATA THAT WAS FOUND)
PC = PROGRAM COUNTER AT ERROR CALL
ERROR = FAILING ERROR NUMBER
PASFLG = CONTENTS OF ERROR PASFLG (THIS MAY NOT BE RELEVANT)

Using the above printout as an example, the failure would be found in the address range 0-128KB (177210 is between 0 and 00377776). The failing bit would be zero; this is determined by comparing good data with bad data (177777-177776 = 000001). Using Figure 4-1, the failing RAM is found to be in the first row of RAMs (U1-U18). Since it is known that bit 0 is bad, the faulty RAM must therefore be U1. The PC, ERROR and PASFLG information are not normally needed to determine the failing RAM and are not needed in this example. If they are needed, refer to the diagnostic listing for ZKMA.

ZQMC: This program has the ability to test memory from address 000000 to 757777, (0-248KB of memory), on the 11/23+ processor.

Switch Setting Summary

BIT 15(100000);	SW15=1	Halt on Error
BIT 14(040000);	SW14=1	Loop on Test
BIT 13(020000);	SW13=1	Inhibit Error Printouts
BIT 12(010000);	SW12=1	Inhibit Memory Management
BIT 11(004000);	SW11=1	Inhibit Subtest Iteration
BIT 10(002000);	SW10=1	Ring Bell on Error
BIT 09(001000);	SW09=1	Loop on Error
BIT 08(000400);	SW08=1	Loop on Test in SWR<4:0>
BIT 07(000200);	SW07=1	Inhibit Program Relocation
BIT 06(000100);	SW06=1	Inhibit Parity Error Detection *

BIT 05(000040);	SW05=1	Inhibit Exercising Vector Area
BITS 4-0	SW4-0	Beginning Test Number

* With parity error detection enabled, a memory failure can cause a parity error. The error printout on a parity error does not type the good data. Thus, a bit dropped or picked up will not be typed as such. Therefore, it is best to run the program for 1 pass with parity disabled, then restart the program with parity enabled.

Running ZQMC

1. Load program ZQMC?? into memory, (L ZQMC?? <CR>).

2. Select options by setting bits into the switch register. Refer to the above switch settings. NOTE: Normal switch settings would be bit 6 set for the first pass (000100), and no bits set for the second pass (000000).

3. Start program testing, (S <CR>).

4. If there are no errors detected the printout will appear similar to the following format:

```
KT11 (MEMORY MANAGEMENT) AVAILABLE
MEMORY MAP:
FROM 000000 TO 757777
PARITY MEMORY MAP:
REGISTER AT 172100 CONTROLS
FROM 000000 TO 757777
PROGRAM RELOCATED TO 720000
PROGRAM RELOCATED TO 000000
END PASS  1
```

5. There is a total of 31 types of error reports generated by this program. Some of the key column heading mnemonics are described below for clarity:

PC	= PROGRAM COUNTER OFF ERROR DETECTION CODE.
V/PC	= VIRTUAL PROGRAM COUNTER. THIS IS WHERE THE ERROR DETECTION CODE CAN BE FOUND IN THE PROGRAM LISTING.
P/PC	= PHYSICAL PROGRAM COUNTER. THIS IS WHERE THE ERROR DETECTION CODE IS ACTUALLY LOCATED IN MEMORY.
TRP/PC	= PHYSICAL PROGRAM COUNTER OF THE CODE WHICH CAUSED A TRAP.
MA	= MEMORY ADDRESS

REG = PARITY REGISTER ADDRESS
PS = PROCESSOR STATUS WORD
IUT = INSTRUCTIONS UNDER TEST
S/B = WHAT CONTENTS SHOULD BE (GOOD DATA)
WAS = WHAT CONTENTS WAS (BAD DATA)

The following is an example of a typical error message printout:

V/PC	P/PC	MA	S/B	WAS
006300	006300	473732	133732	173732

Using the above printout as an example, the failure would be found in the address range 128KB-256KB, (473732 is between 004000000 and 00777776). The failing bit would be bit "14"; this is determined by comparing good data with bad data, (S/B with WAS), and doing an EXCLUSIVE OR of the two (133732-173732 = 040000), and locating the bad octal bit, bit "14". Using Figure 6-6, the failing RAM is found to be in the second row of RAMs, (U19-U36).

Since it is known that bit "14" is bad, the faulty RAM must therefore be U35. For error messages that do not display the failing address and good and bad data, refer to the diagnostic listing for Z@MC.

In the 11/23+ system, a diagnostic/bootstrap ROM provides the necessary test functions. Table 6-17 lists the memory error messages.

TABLE 6-17 - MEMORY ERROR MESSAGES

ADDRESS OF ERROR	DISPLAY (OCTAL)	CAUSE OF ERROR / COMMENT
173232	02	Memory Error 2. Write address to itself.
173262	02	Memory Error 3. Byte addressing error.
173302	02	Memory error in pre-memory test. R2=failing data R3=expected data R5=failing address
173316	02	Memory error. Bit 15 set in one of the parity CSRs (172100-172136). Failing memory should have the parity LED on.
173660	02	Memory error in 0-2044KW. 22 bit memory test. Common error halt for six different tests. If R3=0, then error in Test 1-5. Then R4 determines failing test. R4 = expected data R5 = failing data

CONTENTS OF F4	TEST	TEST DESCRIPTION
20000-27776	1	Address Test, bit 11-0
177777	2	Data Test
000000	3	Data Test
072524	4	Odd Parity Pattern Test
125125	5	Byte Addressing Test

FIGURE 6-4 - RAM/ROM CHART

Row A	U1	U2	U3	U4	U5	U6	U7	U8	U9	U10	U11	U12	U23	U14	U15	U16	U17	U18
Row B	U19	U20	U21	U22	U23	U24	U25	U26	U27	U28	U29	U30	U31	U32	U33	U34	U35	U36
Row C	U37	U38	U39	U40	U41	U42	U43	U44	U45	U46	U47	U48	U49	U50	U51	U52	U53	U54
Row D	U55	U56	U57	U58	U59	U60	U61	U62	U63	U64	U65	U66	U67	U68	U69	U70	U71	U72
Row E	U73	U74	U75	U76	U77	U78	U79	U80	U81	U82	U843	U84	U85	U86	U87	U88	U89	U90
Row F	U91	U92	U93	U94	U95	U96	U97	U98	U99	U100	U101	U102	U103	U104	U105	U106	U107	U108
Row G	U109	U110	U111	U112	U113	U114	U115	U116	U117	U118	U119	U120	U121	U122	U123	U124	U125	U126
Row H	U127	U128	U129	U130	U131	U132	U133	U134	U135	U136	U137	U138	U139	U140	U141	U142	U143	U144
Data Bit	0	1	2	3	4	5	6	7	P0	P1	8	9	10	11	12	13	14	15

Row A = 0-64Kw (0-00377776)
Row B = 64Kw-128Kw (00400000-00777776)
Row C = 128Kw-192Kw (01000000-01377776)
Row D = 192Kw-256Kw (01400000-01777776)

Row E = 256Kw-320Kw (02000000-02377776)
Row F = 320Kw-384Kw (02400000-02777776)
Row G = 384Kw-448Kw (03000000-03377776)
Row H = 498Kw-512Kw (03400000-03777776)

For Test 1-5 (R3=0) determine 22 bit failing address as follows:

R1 bits 11-0 failing address bits 11-0
R2 bits 15-6 failing address bits 22-12

Errors in address uniqueness test. Test checks address bits 21-6 Test 6. If R3 is not equal to 0 then error is in this test.

R4 = expected data
R5 = failing data
R2 = 22-bit failing address bits 21-6 failing address
Bits 5-0 are always 0.

173664	02	Memory error in pre-memory address test for locations 0-776. R2 = failing data R5 = failing address and expected data
173736	02	Memory error 1, data test failed. Test 0-30 with MMU off if present. R1 = failing address R4 = expected data (either 000000 or 177777) R5 = failing data

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